Analysis of working of CMOS transistors in three input NOR gate

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2023102012

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Introduction:

Logic gates are one of the most important element of digital electronics engineering. It works on the concept of boolean function. their are several gates in digital electronics, NOR Gate is one of them, which is also lies under Universal Gate because it can be used to implement other basic logic gates like AND, OR and NOT gate by connecting NOR gates together in specific configurations.

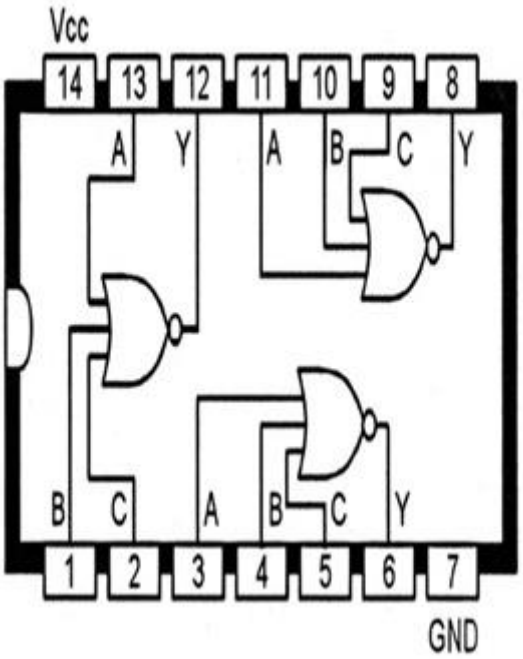
NOR gate is a digital logic gate that performs NOR operation between two or more binary inputs and output binary signal. This is basically a combination of OR gate and NOT gate.Here, in this context we are discussing about a three input NOR gate.

About CMOS:

CMOS (Complementary Metal-Oxide-Semiconductor) transistors serve as fundamental components in digital circuits due to their attributes like low power consumption and high-speed operations. However, implementing a triple input NOR gate using CMOS transistors poses challenges primarily related to increased transistor count, layout complexity, and area consumption. Typically, constructing this gate demands six transistors - three PMOS and three NMOS - escalating concerns about circuit complexity and spatial requirements.

3 – Input NOR Gate:

From the name itself suggest that, its takes three inputs, so n = 3. The truth table will have $2^n = 8$ combinations of possible outcomes.



Functionality and Application of a 3-Input NOR Gate in CMOS Technology:

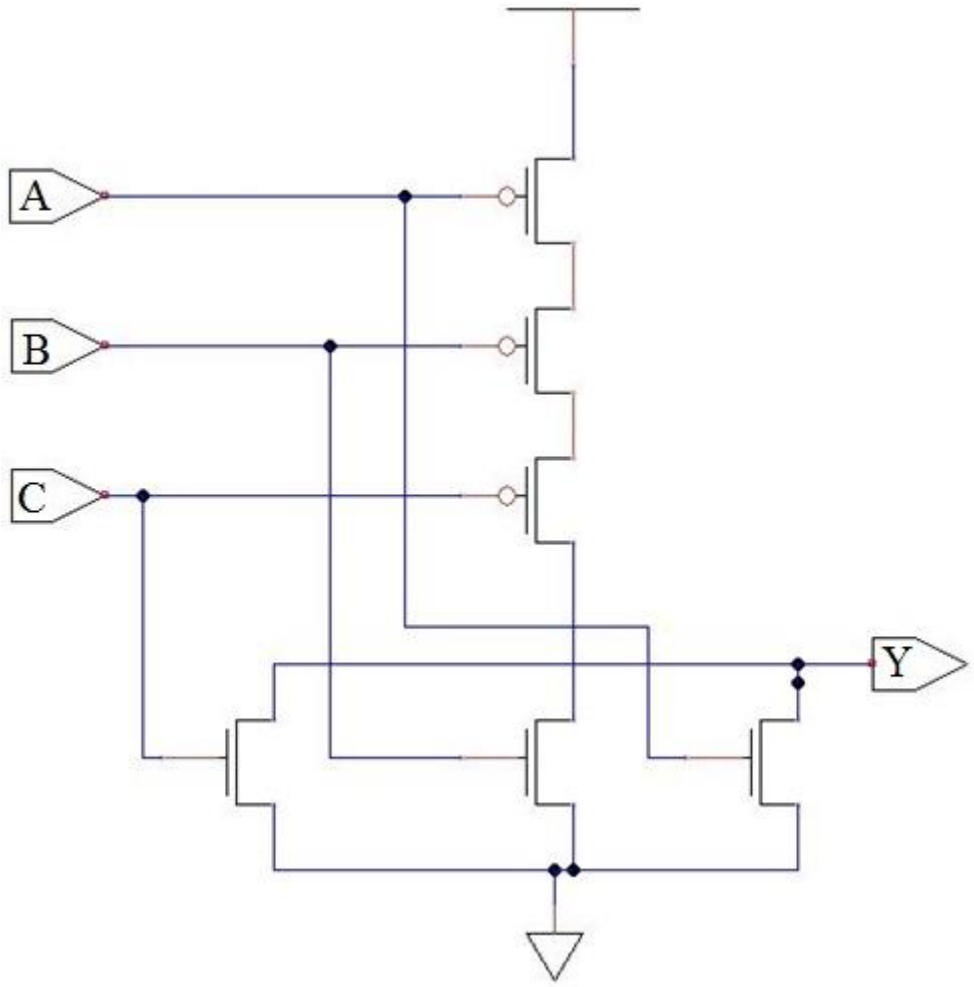
The main function of a 3 Input Nor Gate Cmos is to compare the three inputs and determine an appropriate output. It does this by evaluating the logic levels of each input. If all three inputs are low then the output will be high. If any of the three inputs are high then the output will be low. This type of device is used in many digital systems where it allows for the comparison of several inputs to arrive at a single output.

A 3-input NOR gate implemented using CMOS (Complementary Metal-Oxide-Semiconductor) technology involves combining multiple transistors to create the logic function. In CMOS technology, both NMOS (N-channel Metal-Oxide-Semiconductor) and PMOS (P-channel Metal-Oxide-Semiconductor) transistors are used to construct logic gates

To create a 3-input NOR gate in CMOS, you'll utilize a combination of PMOS and NMOS transistors arranged in a specific configuration.

Consider the logic expression for a 3-input NOR gate:

Output = NOT (Input1 OR Input2 OR Input3)



ANALYSIS ON HOW CMOS WORKS IN 3-INPUT NOR GATE:

There would be three PMOS (P-channel Metal-Oxide-Semiconductor) transistors in the pull-up network, with each PMOS transistor connected to one input. These PMOS transistors form the parallel configuration in the pull-up network, enabling the gate to output a high signal when all inputs are low.

There would also be three NMOS (N-channel Metal-Oxide-Semiconductor) transistors in the pull-down network, with each NMOS transistor connected to one input. These NMOS transistors are connected in series, forming the series configuration in the pull-down network, ensuring that the gate output is pulled low when any input is high.

Therefore, a 3-input NOR gate in CMOS technology consists of three PMOS transistors in series in the pull-up network and three NMOS transistors in parallel in the pull-down network. This configuration allows the gate to function according to the NOR logic behavior, producing the correct output based on the inputs.

The following steps describe a basic implementation of a 3-input NOR gate using CMOS technology:

Pull-Up Network (PMOS Transistors):

Connect multiple PMOS transistors in series between the output and the power supply (VDD).

Each PMOS transistor's gate is connected to an input, and its source is connected to VDD.

Pull-Down Network (NMOS Transistors):

Connect multiple NMOS transistors in parellel between the output and ground (GND).

Each NMOS transistor's gate is connected to an input, and they are all connected in parallel.

The sources of these NMOS transistors are connected to GND.

If any input is HIGH, it creates a path to ground, pulling the output down to GND.

Logic Function Realization:

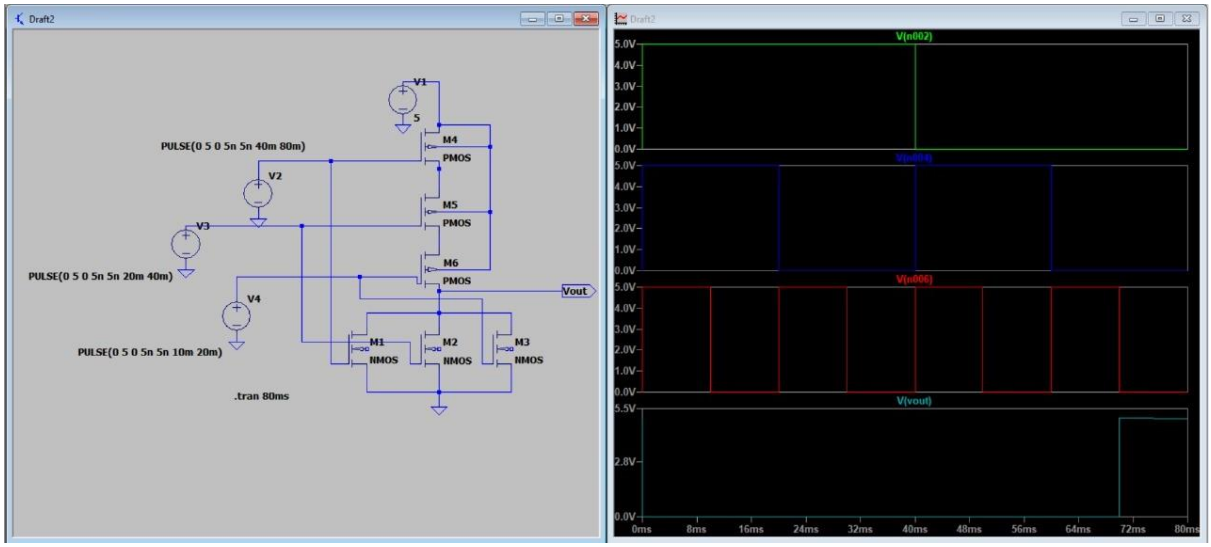
When any input is high (1), its corresponding PMOS transistor turns off, while the NMOS transistor connected to that input turns on.

If any input is high (1), the voltage at the output node is pulled to GND, making the output low (0). This aligns with the behavior of a NOR gate.

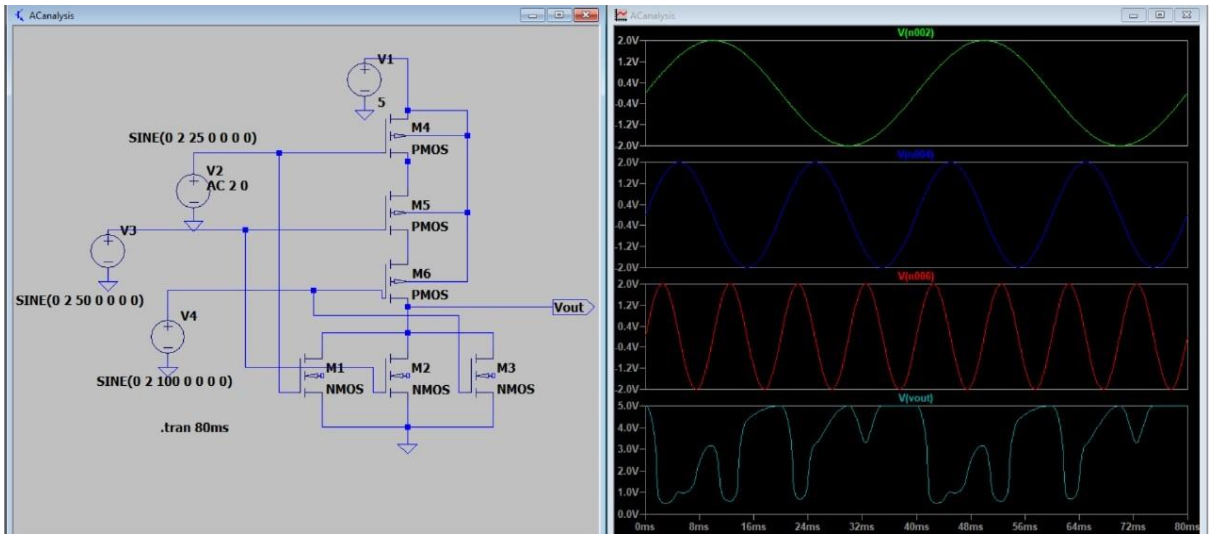
Only when all inputs are low (0), all PMOS transistors are on, and all NMOS transistors are off. This situation pulls the output to VDD, resulting in a high output (1), indicating a true NOR gate output.

The combination of these Series PMOS transistors and parallel NMOS transistors forms a 3-input NOR gate in CMOS technology, allowing for efficient logic operations based on the inputs' logic levels.

Analysis of CMOS in 3 - input NOR Gate with DC input:



Analysis of CMOS in 3 - input NOR Gate with AC input:



From the above graph we can come to the conclusion:

Truth table:

Input (**A**)	Input (**B**)	Input (**C**)	Output $Y=\overline{A+B+C}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0