ECE 524 Synthesis & Verification of Digital Circuits - Fall 2017

Project-1 **Due Date: 10/17/17**

1) Form the bdds for each node in the circuit, where variable ordering is assigned according to the ascending order of the index of primary inputs. Find the maximum number of nodes in the manager for the generated circuit.

2) Identify the function equivalence and containment for each primary output pair.
Equivalence: Given functions F1 and F2, the equivalence check is defined as

$F1 \Leftrightarrow F2 \rightarrow (F1'.F2 = \emptyset)\ \&\&\ (F1.F2' = \emptyset)$

Where:

- '.' is the Boolean AND operator.
- F' is the complement of F.
- && is the C logical AND operator.

To determine if a function F is constant zero (F = Ø) you can use the CUDD operations Cudd_IsConstant(F) && Cudd_IsComplement(F).
Containment: Given functions F1 and F2, F1 is contained in F2 but is not equivalent to F2 is defined as

$$F1 \subset F2 \Leftrightarrow (F1.F2' = \emptyset)\ \&\&\ (F1'.F2 \neq \emptyset)$$

Similarly, F2 is contained in F1 but is not equivalent to F1 is defined as

$$F1 \supset F2 \Leftrightarrow (F1'.F2 = \emptyset)\ \&\&\ (F1.F2' \neq \emptyset)$$

3) Implement and compare different reordering techniques for the given ISCAS' 85 benchmarks. Report the maximum number of the nodes in the manager and the CPU time for each of the reordering techniques.

Reordering techniques:

- CUDD_REORDER_RANDOM
- CUDD_REORDER_SIFT
- CUDD_REORDER_GROUP_SIFT
- CUDD_REORDER_SYMM_SIFT
- CUDD_REORDER_GROUP_SIFT_CONV
- CUDD_REORDER_WINDOW2
- CUDD_REORDER_ANNEALING

NOTE: Enable the reordering technique ONLY when the number of nodes in the manager is more than half the maximum number of the nodes reported in Q.1.

No Late Submission