Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2019

EC3EV03 / EI3EV03 Low Power VLSI Design

Programme: B.Tech. Branch/Specialisation: EC/EI

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The junction parasitic capacitance are produced due to: **1**

(a) Source diffusion regions (b) Drain diffusion regions

(c) Both (a) and (b) (d) None of these

ii. nMOS devices are formed in **1**

(a) p-type substrate of high doping level

(b) n-type substrate of low doping level

(c) p-type substrate of moderate doping level

(d) n-type substrate of high doping level

iii. The power consumption of static CMOS gates varies with the _____ of power supply voltage. **1**

(a) Square (b) Cube

(c) Fourth power (d) $1/8^{th}$ power

iv. In DIBL, which among the following is/are regarded as the source/s of leakage? **1**

(a) Subthreshold conduction (b) Gate leakage

(c) Junction leakage (d) All of these

v. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? **1**

(a) Static dissipation (b) Dynamic dissipation

(c) Both (a) and (b) (d) None of these

P.T.O.

vi. In accordance to the scaling technology, the total delay of the logic circuit depends on _____ **1**
(a) The capacitor to be charged
(b) The voltage through which capacitance must be charged
(c) Available current
(d) All of these

vii. Which clock is preferred in storage devices? **1**
(a) Single phase overlapping clock signal
(b) Single phase non overlapping clock signal
(c) Two phase overlapping clock signal
(d) Two phase non overlapping clock signal

viii. Which is comparatively slower device? **1**
(a) ROM (b) RAM
(c) Flash memory (d) SRAM

ix. In VLSI design, which process deals with the determination of resistance & capacitance of interconnections? **1**
(a) Floor planning (b) Placement & Routing
(c) Testing (d) Extraction

x. Which type of simulation mode is used to check the timing performance of a design? **1**
(a) Behavioural (b) Switch-level
(c) Transistor-level (d) Gate-level

Q.2 i. Give capacitive model of MOS transistor. **3**

ii. Implement functions X=A+B+C and Y=A+B+C+D in dynamic CMOS logic. **7**

OR iii. Explain voltage transfer characteristics of CMOS Inverter. Show effect of β-ratio on it. **7**

Q.3 i. What do you mean by short channel effects? Enlist them. **3**

ii. Explain how transistor staking can be used to reduce leakage power dissipation. **7**

OR iii. Explain limitations of SiO_2 as gate oxide. How can we overcome these limitations? **7**

Q.4 i. Explain the mechanism behind short circuit power dissipation in VLSI circuits. Why runtime leakage power is becoming important in the present day context? **2**

ii. What are the techniques to reduce dynamic power dissipation? Explain clock gating technique in brief. **8**

OR iii. What is run time leakage power in low power VLSI. Why leakage current is a major problem at low voltages? **8**

Q.5 Attempt any two:

i. Compare SRAM and DRAM memories. **5**

ii. Give and explain block diagram structure of the 4-bit Braun algorithm for the unsigned binary multiplication. **5**

iii. Explain how read and write operations are performed in a SRAM. **5**

Q.6 Attempt any two:

i. What are probabilistic techniques for power estimation? Explain any one approach in brief. **5**

ii. Explain Gate – Level power estimation technique with one example. **5**

iii. What do you mean by low level and high level power estimation techniques? Explain with suitable example. **5**

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Marking Scheme
EC3EV03 / EI3EV03 Low Power VLSI Design

Q.1	i.	The junction parasitic capacitance are produced due to: (c) Both (a) and (b)	**1**
	ii.	nMOS devices are formed in (c) p-type substrate of moderate doping level	**1**
	iii.	The power consumption of static CMOS gates varies with the _____ of power supply voltage. (a) Square	**1**
	iv.	In DIBL, which among the following is/are regarded as the source/s of leakage? (d) All of these	**1**
	v.	In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? (b) Dynamic dissipation	**1**
	vi.	In accordance to the scaling technology, the total delay of the logic circuit depends on _____ (d) All of these	**1**
	vii.	Which clock is preferred in storage devices? (d) Two phase non overlapping clock signal	**1**
	viii.	Which is comparatively slower device? (c) Flash memory	**1**
	ix.	In VLSI design, which process deals with the determination of resistance & capacitance of interconnections? (d) Extraction	**1**
	x.	Which type of simulation mode is used to check the timing performance of a design? (d) Gate-level	**1**
Q.2	i.	Capacitive model of MOS transistor.	**3**
	ii.	Implement functions X=A+B+C and Y=A+B+C+D in dynamic CMOS logic.	**7**
OR	iii.	Voltage transfer characteristics of CMOS Inverter 5 marks Effect of β-ratio on it. 2 marks	**7**
Q.3	i.	Short channel effects 2 marks Enlist them. 1 mark	**3**
	ii.	Transistor staking can be used to reduce leakage power dissipation	**7**
OR	iii.	Limitations of SiO_2 as gate oxide 4 marks Overcome these limitations 3 marks	**7**
Q.4	i.	Mechanism behind short circuit power dissipation in VLSI circuits 1 mark Runtime leakage power is becoming important in the present day context 1 mark	**2**
	ii.	Techniques to reduce dynamic power dissipation 5 marks Clock gating technique 3 marks	**8**
OR	iii.	Run time leakage power in low power VLSI 4 marks Leakage current is a major problem at low voltages 4 marks	**8**
Q.5		Attempt any two:	
	i.	Comparison SRAM and DRAM memories.	**5**
	ii.	Block diagram structure of the 4-bit Braun algorithm for the unsigned binary multiplication.	**5**
	iii.	Read and write operations are performed in a SRAM.	**5**
Q.6		Attempt any two:	
	i.	Probabilistic techniques for power estimation 3 marks Any one approach 2 marks	**5**
	ii.	Gate – Level power estimation technique with one example.	**5**
	iii.	Low level and high level power estimation techniques 3 marks Example 2 marks	**5**

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