Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2019

EC3EV05 / EI3EV05

VLSI for Wireless Communication

Programme: B.Tech. Branch/Specialisation: EC/EI

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Communication happens only in one direction **1**

(a) Simplex (b) Duplex

(c) Half Duplex (d) None of these

ii. In enhancement MOSFET the magnitude of output current _____ due to increase in magnitude of gate potential **1**

(a) Increase (b) Remain constant

(c) Decrease (d) None of these

iii. Which of the following is not a reason for distortion in amplifier output? **1**

(a) Incorrect biasing level (b) Sinusoidal input

(c) Nonlinear amplification (d) Large input signal

iv. _____ is defined as the ratio of input signal to noise ratio of output signal to noise ratio **1**

(a) Noise figure (b) Noise temperature

(c) SNR (d) None of these

v. The power consumption of static CMOS gates varies with the ____ of power supply voltage. **1**

(a) Square (b) Cube

(c) Fourth power (d) 1/8 th power

vi. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? **1**

(a) Static dissipation (b) Dynamic dissipation

(c) Both (a) and (b) (d) None of these

P.T.O.

vii. An ideal op-amp has _____ **1**
(a) Infinite input resistance
(b) Zero output voltage
(c) Infinite differential voltage gain
(c) All of these

viii. In two stage op-amp, what is the purpose of compensation circuit? **1**
(a) To provide high gain
(b) To lower output resistance & maintain large signal swing
(c) To establish proper operating point for each transistor in its Q state
(d) To achieve stable closed-loop performance

ix. The PLL device is: **1**
(a) Feedback system that compares output frequency and input frequency
(b) Feedback system that compares output phase and input phase
(c) Linear system that compares output resistance and input resistance
(d) Non-Linear system that compares output current and input current

x. The Logic gate that works similar to phase detector is **1**
(a) AND gate (b) OR gate (c) XOR gate (d) NOT gate

Q.2 i. What is the need of communication engineering for IC engineers? **2**
ii. Define envelope fading? **3**
iii. Develop the points to explain about the Binary Phase shift keying. **5**
OR iv. Explain the different types of Optical fibers with suitable diagram. **5**

Q.3 i. Name the various applications of LNA circuit. **2**
ii. Discuss trade -off between noise figure and power. **3**
iii. Summarize the distortion due to non linearites. **5**
OR iv. Demonstrate the various Non linearites that arise in design of receiver front end. **5**

Q.4 i. Why double balanced mixer is commonly used? Justify? **2**
ii. Discuss about the mixer topology. **3**
iii. Write a note on passive CMOS mixer. **5**

OR iv. Point out the detailed analysis of Gilbert mixer for the following **5**
(a) Distortion (b) Low frequency case

Q.5 i. What is mean by Quantization noise. **2**
ii. Discuss in detail various types of DAC used in communication system. **3**
iii. Explain architecture of Analog to Digital Convertor. **5**
OR iv. Explain the operation of sample and hold circuit. **5**

Q.6 Attempt any two:
i. Write the design and function of PLL based frequency synthesizer. **5**
ii. Analyse the operation of a Ring oscillator with a neat diagram. **5**
iii. Explain positive feedback theory of VCO with the required expressions. **5**

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Marking Scheme

EC3EV05 / EI3EV05 VLSI for Wireless Communication

Q.1	i.	Communication happens only in one direction (a) Simplex	**1**
	ii.	In enhancement MOSFET the magnitude of output current _____ due to increase in magnitude of gate potential (a) Increase	**1**
	iii.	Which of the following is not a reason for distortion in amplifier output? (d) Large input signal	**1**
	iv.	_____ is defined as the ratio of input signal to noise ratio of output signal to noise ratio (a) Noise figure	**1**
	v.	The power consumption of static CMOS gates varies with the ____ of power supply voltage. (a) Square	**1**
	vi.	In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? (b) Dynamic dissipation	**1**
	vii.	An ideal op-amp has _____ (c) All of these	**1**
	viii.	In two stage op-amp, what is the purpose of compensation circuit? (d) To achieve stable closed-loop performance	**1**
	ix.	The PLL device is: (b) Feedback system that compares output phase and input phase	**1**
	x.	The Logic gate that works similar to phase detector is (c) XOR gate	**1**
Q.2	i.	Need of communication engineering for IC engineers	**2**
	ii.	Definition of envelope fading	**3**
	iii.	Develop at least five points about the Binary Phase shift keying 1 mark for each point (1 mark * 5)	**5**
OR	iv.	Types of Optical fibers 3 marks Diagram 2 marks	**5**
Q.3	i.	Naming the applications of LNA circuit.	**2**
	ii.	Trade -off between noise figure and power 3 differences 1 mark for each (1 mark * 3)	**3**
	iii.	Distortion due to non linearites Stepwise marking	**5**
OR	iv.	Non linearites that arise in design of receiver front end At least three issues	**5**
Q.4	i.	Reason for using double balanced mixer commonly	**2**
	ii.	Mixer topology.	**3**
	iii.	Passive CMOS mixer Diagram 2 marks Functionality 3 marks	**5**
OR	iv.	(a) Distortion 2.5 marks (b) Low frequency case 2.5 marks	**5**
Q.5	i.	Quantization noise.	**2**
	ii.	Types of DAC used in communication system.	**3**
	iii.	Architecture of Analog to Digital Convertor 3 marks Explanation 2 marks	**5**
OR	iv.	Operation of sample and hold circuit 3 marks Diagram 2 marks	**5**
Q.6		Attempt any two:	
	i.	PLL based frequency synthesizer Design 2.5 marks Function 2.5 marks	**5**
	ii.	Operation of a Ring oscillator 2.5 marks Diagram 2.5 marks	**5**
	iii.	Positive feedback theory of VCO 3 marks Expressions 2 marks	**5**

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