Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2022

EC3EL08 Computer Organization & Architecture

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. ENIAC Computer belongs to _____. **1**
(a) First generation (b) Second generation
(c) Third generation (d) Fourth generation

ii. Which electronic components are used in first generation computers? **1**
(a) Vacuum tube (b) IC's
(c) Transistors (d) All of these

iii. ADD R1, R2, R3 is- **1**
(a) Three operand instruction
(b) RISC instruction
(c) One word instruction
(d) All of these

iv. Round off 13.5 to two digits using IEEE754 is- **1**
(a) 13 (b) 14 (c) 13.5 (d) None of these

v. In the pipelining the stages are interleaved by- **1**
(a) Special unit (b) Control unit
(c) Clock (d) All of these

vi. The duration of time when unit is idle known as- **1**
(a) Bubbles (b) Hazards (c) Holes (d) None of these

vii. a + b* c % d is example of- **1**
(a) SISD (b) SIMD (c) MISD (d) MIMD

viii. PCB stands for- **1**
(a) Process control block (b) Procedure control block
(c) Process computer batch (d) Procedure computer batch

P.T.O.

ix. Write through procedure is- **1**
(a) Write on memory permanently
(b) To write directly on the memory and cache simultaneously
(c) To write and read from memory permanently
(d) None of these

x. The value of cache memory is based on the property of- **1**
(a) Memory size (b) Memory localization
(c) Locality of reference (d) All of these

Q.2 i. What do you mean by MIPS? **2**
ii. Write short note on computer and its classification. **3**
iii. Explain hardwired control unit. **5**
OR iv. Write steps to execute instruction Add (R1), R2. **5**

Q.3 Attempt any two:
i. Represent 7.25 to floating point single precision method. Also write the significance of bias and 1. M. **5**
ii. Define addressing mode and give their any four classifications with an example. **5**
iii. Compare RISC and CISC characteristics in tabular format. **5**

Q.4 i. Describe pipelining with diagram and discuss the role of cache in pipelining. **4**
ii. What is data hazard and how it is handled in software and hardware? **6**
OR iii. Explain control hazard and its removal with sketch. **6**

Q.5 i. What do you mean by program, process and thread? **4**
ii. Describe the vector processor with diagram. **6**
OR iii. Describe multicore architecture with characteristics. **6**

Q.6 i. Define Hit rate and Miss rate and average access time. **3**
ii. Explain memory hierarchy with neat sketch and characteristics. **7**
OR iii. What do you mean by memory mapping of cache? Discuss any two methods in detail. **7**

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Marking Scheme
EC3EL08 Computer Organization & Architecture

Q.1	i.	ENIAC Computer belongs to _____.		**1**
		(a) First generation		
	ii.	Which electronic components are used in first generation computers?		**1**
		(a) Vacuum tube		
	iii.	ADD R1, R2, R3 is-		**1**
		(d) All of these.		
	iv.	Round off 13.5 to two digits using IEEE754 is-		**1**
		(b) 14		
	v.	In the pipelining the stages are interleaved by-		**1**
		(c) Clock		
	vi.	The duration of time when unit is idle known as-		**1**
		(a) Bubbles		
	vii.	a + b* c % d is example of-		**1**
		(d) MIMD		
	viii.	PCB stands for-		**1**
		(a) Process control block		
	ix.	Write through procedure is-		**1**
		(b) To write directly on the memory and cache simultaneously		
	x.	The value of cache memory is based on the property of-		**1**
		(c) Locality of reference		
Q.2	i.	Define MIPS	1 Marks	**2**
		Expression	1 Marks	
	ii.	Computer	1 Marks	**3**
		Its classification.	2 Marks	
	iii.	Explain hardwired control unit.	3 Marks	**5**
		Diagram	2 Marks	
OR	iv.	Instruction Add (R1), R2.	(2.5 Marks*2)	**5**
Q.3		Attempt any two:		
	i.	Represent 7.25 to floating point single precision method . Also write the significance of bias and 1. M.	3 Marks (1 Mark+1 Mark)	**5**
	ii.	Define addressing mode	1 Mark	**5**
		Give their any four classifications with an example.	4 Marks	
	iii.	Compare RISC and CISC characteristics in tabular format.	(As per explanation)	**5**
Q.4	i.	Describe pipelining with diagram	3 Marks	**4**
		Discuss the role of cache in pipelining.	1 Mark	
	ii.	Data hazard	2 Marks	**6**
		Software	2 Marks	
		Hardware	2 Marks	
OR	iii.	Explain control hazard	3 Marks	**6**
		its removal with sketch.	3 Marks	
Q.5	i.	Program	1.5 Marks	**4**
		Process	1.5 Marks	
		Thread	1 Mark	
	ii.	vector processor explanation	4 Marks	**6**
		Diagram.	2 Marks	
OR	iii.	Multicore architecture	1 Mark	**6**
		Characteristics.	1 Mark	
		Diagram	4 Mark	
Q.6	i.	Hit rate and Miss rate and average access time	(1 Mark *3)	**3**
	ii.	Explain memory hierarchy	3 Marks	**7**
		Neat sketch	2 Marks	
		Characteristics.	2 Marks	
OR	iii.	What do you mean by memory mapping of cache	1 Mark	**7**
		Two methods in detail.	(3 Mark*2)	

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