Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Science

End Sem (Odd) Examination Dec-2017

CA3C002 Digital Electronics

Programme: BCA Branch/Specialisation: Computer Application

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The binary equivalent of $(436)_8$ is **1**

(a) 100100110 (b) 100011110

(c) 10011110 (d) 10000110110

ii. The range for 2's complement representation is: **1**

(a) $-(2^{n-1})$ to $+(2^{n+1})$ (b) $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

(c) $-(2^{n-1}-1)$ to $+(2^{n-1})$ (d) $-(2^{n-1})$ to $+(2^{n-1}-1)$

iii. The code used in k-map is **1**

(a) BCD Code (b) Gray Code

(c) Excess 3 Code (d) None of these

iv. Which of the following is universal gate: **1**

(a) AND (b) OR (c) NAND (d) NOT

v. A multiplexer is also known as **1**

(a) Data divider (b) Data distributer

(c) Data selector (d) None of these

vi. The T flip-flop is mainly designed for **1**

(a) Counters (b) Registers (c) Delay device (d) Latches

vii. The slowest shift register is **1**

(a) Parallel in parallel out shift register

(b) Parallel in serial out shift register

(c) Serial in parallel out shift register

(d) Serial in serial out shift register

P.T.O.

viii. The fastest logic family is **1**
(a) TTL (b) CMOS (c) ECL (d) RTL

ix. The slowest memory is **1**
(a) RAM (b) ROM (c) Cache (d) Flash memory

x. CD-ROM is a **1**
(a) Semiconductor memory (b) Memory register
(c) Magnetic memory (d) Optical Disk

Q.2 Attempt any two:

i. Perform following conversions: **5**
(a) $(10110111)_2$ to($)_{10}$
(b) (10010101)2 to ($)_8$
(c) $(1000)_{BCD}$ to excess three code
(d) $(675)_{10}$ to ($)_{BCD}$
(e) $(10001100)_{BCD}$ to ($)_{10}$

ii. Design a binary full adder and explain its working. **5**

iii. (a) Perform addition of following binary numbers: **2**
101011010 + 1011010 + 1011001

(b) Perform subtraction of following numbers using two's complement representation: 4 - 5 **3**

Q.3 i. How can we design AND and OR gate with the help of NAND gate? Explain with the help of diagram **4**

ii. Minimize following Boolean function and implement it through minimum numbers of two inputs NAND gate only **6**
F(A,B,C,D) = A'B'C'D'+A'B'C'+ABC'D+AB'C'D

OR iii. (a) Write and prove De-morgan theorem **2**

(b) Simplify the following Boolean function in Product of Sum (POS) form: **4**
F(A,B,C,D) = A'B'C+ABCD'+AB'+AB'C'+BCD+CD'+C'D'

Q.4 i. Design a 4×16 decoder using two 3×8 decoders. **3**

ii. Design a 16×1 multiplexer and explain it's working **7**

OR iii. Make the diagram for J-K flip flop and write its characteristics table. Explain master slave J-K flip-flop also in brief. **7**

Q.5 i. Write various characteristics of TTL logic family **4**

ii. Design a 3 bit asynchronous down counter **6**

OR iii. Make the diagram for R - 2R Ladder D to A converter and explain it's working with the help of an example. **6**

Q.6 Attempt any two:

i. Write comparison between SRAM and DRAM **5**

ii. What is cache? Why it is the fastest memory? Explain. **5**

iii. Write various types of ROM and explain them in brief. **5**

******

CA3C002 Digital Electronics
Marking Scheme

Q.1	i.	The binary equivalent of $(436)_8$ is (b) 100011110	b
	ii.	The range for 2's complement representation is: (d) $-(2^{n-1})$ to $+(2^{n-1}-1)$	d
	iii.	The code used in k-map is (b) Gray Code	b
	iv.	Which of the following is universal gate: (a) AND (b) OR (c) NAND (d) NOT	**1**
	v.	A multiplexer is also known as (c) Data selector	**1**
	vi.	The T flip-flop is mainly designed for (a) Counters	**1**
	vii.	The slowest shift register is (d) Serial in serial out shift register	**1**
	viii.	The fastest logic family is (c) ECL	**1**
	ix.	The slowest memory is (d) Flash memory	**1**
	x.	CD-ROM is a (d) Optical Disk	**1**
Q.2		Attempt any two:	
	i.	Perform following conversions: (a) $(10110111)_2$ to $(\ )_{10}$ (b) (10010101)2 to $(\ )_8$ (c) $(1000)_{BCD}$ to excess three code (d) $(675)_{10}$ to $(\ )_{BCD}$ (e) $(10001100)_{BCD}$ to $(\ )_{10}$ 1 mark for each part (1 mark * 5 = 5 marks)	**5**
	ii.	Design a binary full adder and explain its working. 2 marks for truth table, 2 marks for simplification of expression 1 mark for diagram	**5**
	iii.	(a) Perform addition of following binary numbers: 101011010 + 1011010 + 1011001 (b) 1 mark for two's complement representation	**2** **3**
		1 mark for operation, 1 mark for result interpretation	
Q.3	i.	2 marks for Designing and explaining AND gate, 2 marks for designing and explaining OR gate	**4**
	ii.	2 marks for minimization of function, 1 mark for AND-OR implementation, 2 marks for NAND implementation, 1 mark for minimizing number of NAND gates.	**6**
OR	iii.	(a) De-morgan theorem (b) 2 marks for making k-map and filling it 1 mark for grouping of squares 1 mark for writing simplified expression.	**2** **4**
Q.4	i.	2 marks for diagram 1 mark for explanation	**3**
	ii.	3 marks for truth table 1 mark for expressions 2 marks for diagram 1 mark for explanation.	**7**
OR	iii.	2 marks for table 2 marks for diagram 3 marks for explanation about master slave JK flip-flop	**7**
Q.5	i.	1 mark for each characteristics (1 mark * 4 = 4 marks)	**4**
	ii.	1 mark for truth table 3 marks explanation regarding selection of appropriate flip-flop 2 marks for diagram	**6**
OR	iii.	2 marks for diagram 2 marks for explanation 2 marks for example.	**6**
Q.6		Attempt any two:	
	i.	1 mark for each comparison (1 mark * 5 = 5 marks)	**5**
	ii.	2 marks for definition of cache 3 marks for explanation about its fastest speed.	**5**
	iii.	0.5 mark for ROM and 1.5 marks for each type.	**5**

****