*Total No. of Questions: 6* *Total No. of Printed Pages:3*

**Enrollment No.....**

# Faculty of Engineering / Science

## End Sem (Odd) Examination Dec-2022

## CS3CO29 / CS3CO33 / EC3CO07 / IT3CO26 / BC3CO38

## Digital Electronics

Programme: B.Tech./ B.Sc.(CS) Branch/Specialisation: CS/EC/IT/ Computes Science

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. In Boolean algebra, the OR operation is performed by which properties? **1**

(a) Associative properties (b) Commutative properties

(c) Distributive properties (d) All of these

ii. Binary number 1001 is equal to octal number- **1**

(a) 13 (b) 9 (c) 10 (d) 11

iii. Decimal number 7 in Gray code is- **1**

(a) 1100 (b) 0101 (c) 0100 (d) 0111

iv. Half-adders have a major limitation in that they cannot- **1**

(a) Accept a carry bit from a present stage

(b) Accept a carry bit from a next stage

(c) Accept a carry bit from a previous stage

(d) Accept a carry bit from the following stages

v. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature? **1**

(a) Low input voltages (b) Gate impedance

(c) Synchronous operation (d) Cross coupling

vi. In T flip flop, when T = 1, the flip-flop will be in the _____. **1**

(a) Set mode (b) Complement mode

(c) Reset mode (d) Store mode

vii. The total capacity of a memory that has 1024 addresses and can store 8 bits at each address is- **1**

(a) 2048 (b) 16384 (c) 128 (d) 8192

viii. How many address lines required for a 8K memory system? **1**

(a) 13 (b) 11 (c) 12 (d) 8

P.T.O.

ix. Which logic has higher speed among all the logic families? **1**
(a) DTL (b) RTL (c) TTL (d) ECL

x. A TTL circuit acts as a current sink in the- **1**
(a) High state (b) Low state (c) High impedance state (d) Ideal state

Q.2 i. Convert the decimal number 250.5 to Base 7. **2**

ii. Convert the following in other canonical form: **3**
(a) F(A,B,C)= ∑(0,2,6,7) (b) F(W,X,Y,Z)= Π(0,1,2,3,4,6,12)

iii. Reduce the following function using K-map technique- **5**
F (A, B, C, D) = Π (0, 3, 4, 7, 8, 10, 12, 14) + d (2, 6).

OR iv. Reduce the following using tabulation method- **5**
F=m2+m3+m4+m6+m7+m9+m11+m13.

Q.3 i. Show that a positive logic AND gate is a negative-logic OR gate and vice versa. **3**

ii. Design full adder circuit on the basis of following- **7**
(a) Circuit diagram (b) Truth table
(c) Characteristic equation

OR iii. Define multiplexer. Implement the Boolean function using 8:1 mux. **7**
F (A, B, C, D) =A'BD'+ACD+B'CD+A'C'D.

Q.4 i. Define flip-flop. Write down its applications. **2**

ii. Explain race around condition with neat diagram. **3**

iii. Draw the circuit diagram of JK flip flop and explain its operation using truth table. **5**

OR iv. Design an asynchronous MOD 10 up counter with neat diagram & truth table. **5**

Q.5 i. State the classification of memories. Write down differences between RAM & ROM. **3**

ii. Write notes on any two of the following: **7**
(a) EPROM (b) PAL (c) SRAM

OR iii. A combinational circuit is defined by the functions. **7**
F1 (a, b, c) = m (3, 5, 6, 7)
F2 (a, b, c) = m (0, 2, 4, 7) implement the circuit with a PLA.



Q.6 Attempt any two:

i. Write down following specification for logic families **5**
(a) Propagation delay (b) Figure of merit (c) Fan out

ii. State five characteristic of TTL logic. **5**

iii. Write note on CMOS, NMOS, PMOS. **5**

******

## Marking Scheme
## CS3CO29 - CS3CO33 -EC3CO07 - IT3CO26 -BC3CO38
## Digital Electronics

| | | | |
|---|---|---|---|
| Q.1 | i) | d) All of the Mentioned | **1** |
| | ii) | (d) 11 | **1** |
| | iii) | (c) 0100 | **1** |
| | iv) | (c) Accept a carry bit from a previous stage | **1** |
| | v) | (d) Cross coupling | **1** |
| | vi) | (b) complement mode | **1** |
| | vii) | (d) 8192 | **1** |
| | viii) | (a) 13 | **1** |
| | ix) | (d) ECL | **1** |
| | x) | (b) low state | **1** |
| | | | |
| Q.2 | i. | $(505.333)_7$ | **2** |
| | ii. | As Per the solution | **3** |
| | iii. | Give proper solution | **5** |
| OR | iv. | Step by step solution. marks as per step | **5** |
| | | | |
| Q.3 | i. | Give proper reason | **3** |
| | ii. | (a) circuit diagram<br>(b) truth table<br>(c) characteristic equation | **2.5**<br>**2.5**<br>**2** |
| OR | iii. | Give proper solution | **7** |
| | | | |
| Q.4 | i. | definition<br>applications | **1**<br>**1** |
| | ii. | Explanation & diagram | **2,1** |
| OR | iii. | circuit diagram<br>operation<br>truth table | **2**<br>**2**<br>**1** |
| | iv. | Diagram<br>Operation<br>Truth table | **2**<br>**2**<br>**1** |
| | | | |

| | | | |
|---|---|---|---|
| Q.5 | i. | Classification<br>Difference | **1.5**<br>**1.5** |
| | ii. | Explanation for each | **3.5+3.5** |
| OR | iii. | Implementation & diagram | **7** |
| | | | |
| Q.6 | i. | (a) Propagation delay (b) figure of merit (c) fan out | **1.5+1.5 +2** |
| | ii. | five characteristic | **5** |
| | iii. | CMOS, NMOS, PMOS | **2+1.5+ 1.5** |
| | | | |

******