

Total No. of Questions: 6

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Enrollment No.....



Faculty of Science  
End Sem (Even) Examination May-2019  
CA3CO06 Computer Architecture  
Programme: BCA Branch/Specialisation: Computer Application

Duration: 3 Hrs.

Maximum Marks: 60

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

- |     |      |   |   |
|-----|------|---|---|
| Q.1 | i.   | The brain of any computer system is   | 1 |
|     |      | (a) ALU (b) Memory (c) CPU (d) Control Unit                                       |   |
|     | ii.  | The basic operations performed by a computer are                                  | 1 |
|     |      | (a) Arithmetic operation (b) Logical operation                                    |   |
|     |      | (c) Storage and relative (d) All of these   |   |
|     | iii. | Booth's algorithm is used for multiplying   | 1 |
|     |      | (a) Only positive operands  |   |
|     |      | (b) Both positive and negative operands   |   |
|     |      | (c) Only when the multiplier is positive  |   |
|     |      | (d) None of these   |   |
|     | iv.  | The signed magnitude representation for -6 is                                     | 1 |
|     |      | (a) 1110 (b) 0110 (c) 0001 (d) 1001   |   |
|     | v.   | How many types of micro-operations  | 1 |
|     |      | (a) 2 (b) 4 (c) 6 (d) 8   |   |
|     | vi.  | Which language is termed as the symbolic depiction used for indicating the series | 1 |
|     |      | (a) Random transfer language  |   |
|     |      | (b) Register transfer language  |   |
|     |      | (c) Arithmetic transfer language  |   |
|     |      | (d) All of these  |   |
|     | vii. | Which is not part of the execution unit (EU)                                      | 1 |
|     |      | (a) Arithmetic logic unit (b) Clock   |   |
|     |      | (c) General registers (d) Flags   |   |

P.T.O.

[2]

- viii. The intel 8086 microprocessor is a \_\_\_\_\_ processor. **1**  
 (a) 8 bit (b) 16 bit (c) 32 bit (d) 4 bit
- ix. In the memory hierarchy the fastest memory is **1**  
 (a) SRAM (b) Cache (c) Registers (d) DRAM
- x. Type of memory which is used to read data but not to write on it is classified as **1**  
 (a) Random only memory (b) Read access memory  
 (c) Read only memory (d) Random access memory
- Q.2 Attempt any two:
- i. Define computer. Classify computer according to the Flynn's. **5**  
 ii. Explain any five addressing modes of computer with example. **5**  
 iii. Discuss in brief about generation of computers. **5**
- Q.3 i. Perform the following **4**  
 (a)  $(+25) + (30)$   
 (b)  $(-18) - (+12)$   
 (c)  $1101 * 101$   
 (d)  $(0.7462 * 10^{-3}) + (0.5641 * 10^{-2})$
- ii. Multiply  $(+12)$  and  $(-8)$  using Booth's algorithm. **6**
- OR iii. Perform  $12/3$  using restoring division algorithm. **6**
- Q.4 Attempt any two:
- i. Define: - **5**  
 (a) Micro-Operation (b) Register Transfer Language
- ii. Design a 4-bit combinational circuit incrementor using four Half adder circuits. **5**
- iii. Define Arithmetic Logic Unit (ALU). Explain the hardware implementation of it along with function table. **5**
- Q.5 i. Explain the physical address formation in 8086. **2**  
 ii. Draw and discuss the internal block diagram of 8086. **8**
- OR iii. Explain the function of the following signals of 8086 **8**  
 (a) ALE (b) READY (c) HOLD (d) (BHE)'

[3]

- Q.6 i. What is the objective of paging? **2**  
 ii. What are the differences among EPROM, EEPROM and Flash memory. Write any 3 differences. **3**  
 iii. Consider the following page address trace generated by a two-level (M1-M2) memory scheme using page system. The M1 has the capacity of four page:  
                                 6  4  5  1  4  3  2  1  2  1  4  6  7  4  
 Assuming the M1 has pages 1,2,3, and 4 initially. Show the trace using  
 (a) LRO (b) FIFO
- OR iv. (a) State why cache memory is always be smaller than main memory. **5**  
 (b) Explain access time, memory cycle time and data transfer rate of memory system.

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## Marking Scheme

# CA3C006 Computer Architecture

Q.1	i.	The brain of any computer system is	1
		(c) CPU	
	ii.	The basic operations performed by a computer are	1
		(d) All of these	
	iii.	Booth's algorithm is used for multiplying	1
		(b) Both positive and negative operands	
	iv.	The signed magnitude representation for -6 is	1
		(a) 1110	
	v.	How many types of micro-operations	1
		(b) 4	
	vi.	Which language is termed as the symbolic depiction used for indicating the series	1
		(b) Register transfer language	
	vii.	Which is not part of the execution unit (EU)	1
		(b) Clock	
	viii.	The intel 8086 microprocessor is a _____ processor.	1
		(b) 16 bit	
	ix.	In the memory hierarchy the fastest memory is	1
		(c) Registers	
	x.	Type of memory which is used to read data but not to write on it is classified as	1
		(c) Read only memory	
Q.2		Attempt any two:	
	i.	Definition of computer	1 mark
		Classification computer according to the Flynn's.	
		1 mark for each (1 mark * 4)	4 marks
	ii.	Any five addressing modes of computer	5
		0.5 mark for each (0.5 mark * 5)	2.5 marks
		Example.	
		0.5 mark for each (0.5 mark * 5)	2.5 marks
	iii.	Generation of computers.	5
		1 mark for each	(1 mark * 5)

Q.3	i.	Perform the following 1 mark for each	(1 mark * 5)	4
	ii.	Booth's algorithm.		6
OR	iii.	Restoring division algorithm.		6
Q.4	Attempt any two:			
	i.	Define 2.5 marks for each	(2.5 marks * 2)	5
	ii.	Design a 4-bit combinational circuit	3 marks	5
		Explanation	2 marks	
	iii.	Define Arithmetic Logic Unit (ALU)	1 mark	5
		Hardware implementation	1 mark	
		Functional table.	2 marks	
		Description	1 mark	
Q.5	i.	Physical address formation in 8086.		2
	ii.	Internal block diagram of 8086.	3 marks	8
		Description of blocks	5 marks	
OR	iii.	Function of signals of 8086		8
		2 marks for each	(2 marks * 4)	
Q.6	i.	Objective of paging		2
	ii.	Differences among EPROM, EEPROM and Flash memory.		3
		1 mark for each difference	(1 mark * 3)	
	iii.	(a) LRO	2.5 marks	5
		(b) FIFO	2.5 marks	
OR	iv.	(a) State why cache memory is always be smaller than main memory.	2 marks	5
		(b) Access time,	1 mark	
		Memory cycle time	1 mark	
		Data transfer rate of memory system.	1 mark	

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