Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2019

EC3CO12 / EI3CO12 VLSI Design

Programme: B.Tech. Branch/Specialisation: EC/EI

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Due to body effect in MOS transistors **1**

(a) Channel length decreases (b) Drain current increases

(c) Channel width increases (d) Threshold voltage gets affected

ii. Which of these is one of the states of tristate inverter **1**

(a) Short circuit (b) High impedance

(c) Unknown (d) Closed

iii. Minimum _____ transistors will be required to implement 3 input NAND gate by using static CMOS logic. **1**

(a) 3 (b) 4 (c) 6 (d) 10

iv. Propagation delay of any static CMOS logic circuit can be reduced by **1**

(a) Decreasing load capacitance

(b) Decreasing the size of transistors

(c) Increasing no. of series connected transistors

(d) Increasing fan out

v. If in a state machine state, A is k-distinguishable to state B, and N is the total number of states than which of the following is true **1**

(a) k>N (b) k>2N (c) k = N (d) k< N

vi. J, K excitations required for state transition 1→0 in JK flip flop are **1**

(a) 0, X (b) 1, X (c) X, 1 (d) X, 0

vii. When a circuit goes through a unique sequence of unstable states then it is called as **1**

(a) Race (b) Cycle (c) Hazard (d) Glitch

viii. Which of these is a type of asynchronous sequential circuits **1**

(a) Cut-off mode (b) Linear mode

(c) Saturation mode (d) Pulse mode

P.T.O.

ix. In IC fabrication, diffusion is primarily used for formation of **1**
(a) Doped regions (b) Oxide layer
(c) Metal contacts (d) Epitaxial layer

x. Full form of PLA is **1**
(a) Programmable linear array
(b) Programmable logic array
(c) Propagation line array
(c) Propagation logic array

Q.2 i. Draw neat and detailed Y-chart regarding VLSI design flow **2**

ii. Explain various operating regions of enhancement type n-channel MOSFET with proper diagrams. **3**

iii. What do you mean by pass transistors (PT) and transmission gate (TG)? Draw TG schematic diagram of positive edge triggered D-flip flop and explain its working. **5**

OR iv. Discuss following effects in detail **5**
(a) Body effect (b) Channel length modulation

Q.3 i. Realize following functions with static CMOS **4**
(a) Y= (AB)' (b) Y= (A+B)'
(c) Y= [A(B+C)+DE]' (d) Y=(A+B)(C+D)

ii. Draw schematic and explain the working of static CMOS inverter with the help of VTC. Also derive mathematical expressions of V_{IL}, V_{IH} and V_{TH} for same circuit. **6**

OR iii. Draw neat schematic diagram of 28-transistor CMOS full adder circuit. **6**

Q.4 i. Give at least four differences between Mealy and Moore state machines. **2**

ii. Minimize following state machine by using partition method. **3**

	NS, z	
PS	$x=0$	$x=1$
A	$E,0$	$C,0$
B	$C,0$	$A,0$
C	$B,0$	$G,0$
D	$G,0$	$A,0$
E	$F,1$	$B,0$
F	$E,0$	$D,0$
G	$D,0$	$G,0$

iii. Design a '011' sequence detector by using JK flip flops. **5**

OR iv Derive minimal form of state machine given below. **5**

	NS, z			
PS	I_1	I_2	I_3	I_4
A	—	$C,1$	$E,1$	$B,1$
B	$E,0$	—	—	—
C	$F,0$	$F,1$	—	—
D	—	—	$B,1$	—
E	—	$F,0$	$A,0$	$D,1$
F	$C,0$	—	$B,0$	$C,1$

Q.5 Attempt any two:

i. Design a fundamental mode asynchronous sequential circuit having two inputs (x_1 and x_2) and one output (z). Z=1 if both inputs are equal to 1, but only if x_1 becomes 1 before x_2. **5**

ii. Find all the races in the flow table given below and indicate those that are critical and those that are not. Find another assignment and draw table which contains no critical races. **5**

	State			
	x_1x_2			
y_1y_2	00	01	11	10
00	(00)	11	(00)	11
01	11	(01)	11	11
10	00	(10)	11	11
11	(11)	(11)	00	(11)

iii. Draw the logic diagram of POS **5**
$Y= (x_1+x_2')(x_2+x_3)$
Show the presence of hazard, its type and a way of removal.

Q.6 i. Realize the following functions by using PAL with four inputs and 3-wide AND-OR structure: **4**
(a) $F_1= \Sigma_m (0,2,12,13)$ (b) $F_2= \Sigma_m (0,2,3,4,5,6,7,8,10,11,15)$

ii. Discuss CMOS n-well fabrication process step by step with the help of appropriate diagrams. **6**

OR iii. Write detailed note on: **6**
(a) CPLD (b) FPGA

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Marking Scheme
EC3CO12 / EI3CO12 VLSI Design

Q.1	i.	Due to body effect in MOS transistors (d) Threshold voltage gets affected		**1**
	ii.	Which of these is one of the states of tristate inverter (b) High impedance		**1**
	iii.	Minimum _____ transistors will be required to implement 3 input NAND gate by using static CMOS logic. (c) 6		**1**
	iv.	Propagation delay of any static CMOS logic circuit can be reduced by (a) Decreasing load capacitance		**1**
	v.	If in a state machine state, A is k-distinguishable to state B, and N is the total number of states than which of the following is true (d) k< N		**1**
	vi.	J, K excitations required for state transition 1→0 in JK flip flop are (a) 0, X (b) 1, X (c) X, 1 (d) X, 0		**1**
	vii.	When a circuit goes through a unique sequence of unstable states then it is called as (b) Cycle		**1**
	viii.	Which of these is a type of asynchronous sequential circuits (d) Pulse mode		**1**
	ix.	In IC fabrication, diffusion is primarily used for formation of (a) Doped regions		**1**
	x.	Full form of PLA is (b) Programmable logic array		**1**
Q.2	i.	Y-chart regarding VLSI design flow		**2**
	ii.	Operating regions of enhancement type n-channel MOSFET 1 mark for each (Diagram + explanation)	(1 mark * 3)	**3**
	iii.	Pass transistors (PT) Transmission gate (TG) D-flip flop diagram Working	1 mark 1 mark 2 marks 1 mark	**5**
OR	iv.	(a) Body effect (b) Channel length modulation	2.5 marks 2.5 marks	**5**
Q.3	i.	1 mark for each functions with static CMOS	(1 mark * 4)	**4**
	ii.	Schematic VTC Working	1 mark 1 mark 1 mark	**6**
		Derivation 1 mark for each (1 mark * 3)	3 marks	
OR	iii.	Schematic diagram of 28-transistor CMOS full adder circuit. For carry part For sum part	3 marks 3 marks	**6**
Q.4	i.	At least four differences between Mealy and Moore state machines 0.5 mark for each difference	(0.5 mark * 4)	**2**
	ii.	Minimal partition method. Reduced table	2 marks 1 mark	**3**
	iii.	'011' sequence detector by using JK flip flops. For state diagram State table Transition table Excitation table Logic table	1 mark 1 mark 1 mark 1 mark 1 mark	**5**
OR	iv	Minimal form of state machine Merger graph/table Determination of minimal set of compatibles Reduced Table	2 marks 2 marks 1 mark	**5**
Q.5		Attempt any two:		
	i.	Wave form Flow table Reduced flow table Transition table Logic circuit	1 mark 1 mark 1 mark 1 mark 1 mark	**5**
	ii.	Race identification State assignment Table	3 mark 1 mark 1 mark	**5**
	iii.	Logic diagram of POS Hazard Identification Way of removal	1 mark 2 marks 2 marks	**5**
Q.6	i.	2 marks for each function by using PAL with four inputs and 3-wide AND-OR structure	(2 marks * 2)	**4**
	ii.	CMOS n-well fabrication process step 1 mark for each step	(1 mark * 6)	**6**
OR	iii.	(a) CPLD (b) FPGA	3 marks 3 marks	**6**

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