Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2022

EC3EV05 VLSI for Wireless Communication

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. What is the output of a balanced modulator? **1**
(a) AM (b) DSB (c) SSB (d) ISB

ii. The technique that may be used to reduce the side band power is- **1**
(a) MSK (b) BPSK (c) GMSK (d) BFSK

iii. The frequency of local oscillator in a superheterodyne receiver is- **1**
(a) Equal to incoming signal
(b) Higher than incoming signal
(c) Less than incoming signal
(d) Half that of incoming signal

iv. Neutralization is used in RF amplifiers to- **1**
(a) Stop oscillation (b) Increase bandwidth
(c) Improve selectivity (d) All of these

v. What is the purpose of the tuned circuit? **1**
(a) Local oscillator
(b) Amplify RF signals
(c) Mix oscillator and input signals
(d) Select desired signal and reject all

vi. Which of the following signals do not appear at the output of the mixer? **1**
(a) Input signal
(b) Audio signal
(c) Local oscillator signal
(d) Local oscillator signal plus input signal

vii. Which of the following is an indication by settling time? **1**
(a) Accuracy of conversion (b) Speed of conversion
(c) Precision in conversion (d) All of these

P.T.O.

viii. An ADC works by sampling value of input at- **1**
(a) Discrete intervals (b) Continuous intervals
(c) Exponential intervals (d) Determinant intervals

ix. In a PLL circuit the phase comparator is used to provide- **1**
(a) Dc control voltage
(b) Double crystal oscillator signal
(c) RF output with audio modulation
(d) One- half the crystal oscillator frequency

x. In a voltage-controlled oscillator, the varacter needs- **1**
(a) Audio signal below 1000 Hz
(b) Forward bias
(c) Parallel capacitance more than 5 μF
(d) Reverse dc control voltage

Q.2 i. What is path loss? **2**
ii. Why CMOS used for RF design? **3**
iii. Illustrate multi path Fading in wireless communication. **5**
OR iv. Explain QPSK modulator and demodulator. **5**

Q.3 i. Elaborate designing concept of image rejection filter. **3**
ii. Describe receiver front end using heterodyne architecture. **7**
OR iii. What are LNA topologies? Discuss anyone. **7**

Q.4 i. Define mixer with block diagram. **2**
ii. Explain passive mixer with its properties. **8**
OR iii. Describe operation of Gilbert Mixer. **8**

Q.5 i. Explain operation of sample & hold circuit. **4**
ii. Elaborate sigma delta ADC. **6**
OR iii. Describe binary weighted DAC. **6**

Q.6 Attempt any two:
i. Phase Detector **5**
ii. Voltage controlled Oscillator **5**
iii. Ring Oscillator **5**

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Marking Scheme
EC3EV05 VLSI for Wireless Communication

Q.1	i.	What is the output of a balanced modulator? B. DSB	**1**
	ii.	The technique that may be used to reduce the side band power is c. GMSK	**1**
	iii.	The frequency of local oscillator in a superheterodyne receiver is (B) Higher than incoming signal	**1**
	iv.	Neutralization is used in RF amplifiers to A. stop oscillation	**1**
	v.	What is the purpose of the tuned circuit? D) select desired signal and reject all	**1**
	vi.	Which of the following signals do not appear at the output of the mixer? B) audio signal	**1**
	vii.	Which of the following is an indication by settling time? b) Speed of conversion	**1**
	viii.	An ADC works by sampling value of input at A) discrete intervals	**1**
	ix.	In a PLL circuit the phase comparator is used to provide (A) Dc control voltage	**1**
	x.	In a voltage controlled oscillator, the varacter needs (D) Reverse dc control voltage	**1**
Q.2	i.	Define dynamic range.	**2**
	ii.	Why CMOS used for RF design?	**3**
	iii.	Illustrate multi path Fading in wireless communication?	**5**
OR	iv.	Explain QPSK modulator demodulator.	**2.5** **2.5**
Q.3	i.	Elaborate designing concept of image rejection filter.	**3**
	ii.	Describe receiver front end using heterodyne architecture.	**7**
OR	iii.	What are LNA topologies? Discuss any one.	**7**
Q.4	i.	Define harmonic distortion & IIP3.	**2**
	ii.	Explain SSB DSB Noise figure.	**4** **4**
OR	iii.	diagram of Gilbert Mixer. operation of Gilbert Mixer.	**2** **6**
Q.5	i.	Diagram Operation of sample & hold circuit.	**2** **2**
	ii.	Diagram Operation of sigma delta ADC.	**2** **4**
OR	iii.	Diagram Operation of binary weighted DAC.	**2** **4**
Q.6		Attempt any two:	
	i.	Diagram Operation of Phase Detector	**2** **3**
	ii.	Diagram Function of Voltage controlled Oscillator	**2** **3**
OR	iii.	Diagram Operation of Ring Oscillator	**2** **3**

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