Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem Examination Dec 2024

RA3CO51 Digital Electronics

Programme: B.Tech. Branch/Specialisation: RA

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

				Marks	BL	PO	CO	PSO
Q.1	i.	$(120)_{10} = (?)_2$		**1**	1	1	1	
		(a) 1110000	(b) 1111000					
		(c) 1100110	(d) 1110010					
	ii.	$(10010)_2 = (?)_{Gray}$		**1**	1	1	1	
		(a) 11000	(b) 11100					
		(c) 11011	(d) 11001					
	iii.	Which logic families consumes the least power?		**1**	1	1	2	
		(a) TTL	(b) Schottkey TTL					
		(c) ECL	(d) CMOS					
	iv.	Propagation delay of logic gate:		**1**	1	1	2	
		(a) Increases the power dissipation						
		(b) Limit the maximum speed at which circuit can operate						
		(c) Increases the logic level for high state						
		(d) All of these						
	v.	Number of Input and output in full subtractor:		**1**	1	1	3	
		(a) Input-3, Output-2						
		(b) Input-2, Output-2						
		(c) Input-2, Output-1						
		(d) Input-2, Output-3						
	vi.	In 8 to 1 multiplexer, if the value of the select line is 010 then which input is selected:		**1**	1	1	3	
		(a) I_6	(b) I_4					
		(c) I_2	(d) I_0					

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vii.	Which of the following is not a sequential circuit? (a) Flip flop (b) Decoder (c) Register (d) Counter	**1**	1	1	4		
viii.	Ring and Johnson counters are _____. (a) Synchronous counters (b) Asynchronous counters (c) Ripple counters (d) Serial counter	**1**	1	1	4		
ix.	Which of the following is the correct statement regarding memory? (a) RAM and ROM are volatile memory (b) RAM and ROM are non-volatile memory (c) RAM is volatile while ROM is non-volatile memory (d) RAM is non-volatile while ROM is volatile memory	**1**	1	1	5		
x.	In which Programmable Logic Device (PLD), both AND and OR gates are programmable: (a) Programmable Read-Only Memory (b) Programmable Array Logic (c) Programmable Logic Array (d) None of these	**1**	1	1	5		
Q.2 i.	Convert $(1110110)_2$ into octal and hexadecimal number.	**2**	1	1	1		
ii.	Define non-weighted code with examples.	**2**	1	1	1		
iii.	Subtract 25 from 45 using: (a) 1's complement method (b) 2's complement method	**6**	2	1	1		
OR iv.	For the following function- $F(A, B, C, D) = \sum m(0,1,2,5,8,9,10)$ Obtain SOP and POS expression using K-Map.	**6**	3	1	1		

Q.3 i.	Define the parameters used to characterise logic families.	**4**	1	1	2		
ii.	Describe Metal oxide semiconductor (MOS) logic families with switching properties of NMOS and PMOS.	**6**	1	1	2		
OR iii.	Write short note on TTL and Schottky TTL logic families.	**6**	1	1	2		
Q.4 i.	Write short note on magnitude comparator and parity generator.	**4**	1	1	3		
ii.	Define De-multiplexer. Describe 1 to 8 de—multiplexer and design its logic diagram using basic logic gates.	**6**	1	1	3		
OR iii.	Explain full adder with its truth table. Design 4 bit parallel adder by using full adder.	**6**	2	1	3		
Q.5 i.	Write difference between asynchronous and synchronous counter.	**3**	1	1	4		
ii.	Explain SISO, SIPO and PISO shift register with its logic diagram.	**7**	1	1	4		
OR iii.	Discuss the limitation of the JK flip-flop and how it is resolved in the Master-Slave JK flip-flop. Explain with its logic diagram.	**7**	3	1	4		
Q.6	Attempt any two:						
i.	Describe how static RAM and dynamic RAM work with suitable diagrams.	**5**	2	1	5		
ii.	Discuss ROM organization with its types.	**5**	1	1	5		
iii.	Implement the given Boolean function through PLA and PAL- $X = AB + AC'$ $Y = AB' + BC'$	**5**	3	1	5		

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Marking Scheme

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Q.1	i)	(b) 1111000		**1**
	ii)	(c) 11011		**1**
	iii)	(d) CMOS		**1**
	iv)	(b) Limit the maximum speed at which circuit can operate		**1**
	v)	(a) Input-3, Output-2		**1**
	vi)	(c) I_2		**1**
	vii)	(b) Decoder		**1**
	viii)	(a) Synchronous counters		**1**
	ix)	(c) RAM is volatile while ROM is non-volatile memory		**1**
	x)	(c) Programmable Logic Array		**1**
Q.2	i.	$(1110110)_2 = 001\ 110\ 110 = (166)_8$	-1 mark	**2**
		$(1110110)_2 = 0111\ 0110 = (76)_{16}$	-1 mark	
	ii.	Non-weighted code Definition -1M, examples (any two)- 1M		**2**
	iii.	1) 1's complement Method.		**6**
		1's complement of 25 (100110)	-1 mark	
		101101 + 100110 = 010100	-2 marks	
		2) 2's complement Method.		
		2's complement of 25 (100111)	- 1 mark	
		101101 + 100111 = 010100	- 2 marks	
OR	iv.	Plotting K-Map and placing correct value	-2 marks	**6**
		Pairing of 1 and finding SOP expression	-2 marks	
		Pairing of 0 and finding POS expression	-2 marks	
Q.3	i.	Definition of any four parameters	-1 marks (for each)	**4**
	ii.	Describe Metal oxide semiconductor logic families	- 2 marks	**6**
		switching properties of NMOS	- 2 marks	
		switching properties of PMOS	- 2 marks	
OR	iii.	TTL	- 3 marks	**6**
		Schottkey TTL	- 3 marks	
Q.4	i.	magnitude comparator	- 2 marks	**4**
		parity generator	-2 marks	
	ii.	Define De-multiplexer	-1 mark	**6**
		1 to 8 demultiplexer description	-1 marks	
		truth table	- 1 mark	
		logic diagram using basic logic gates	- 3 marks	
OR	iii.	full adder explanation	-2 marks	**6**
		truth table	-1 mark	
		Design 4-bit parallel adder by using full adder	- 3 marks	
Q.5	i.	asynchronous and synchronous counter – 1 mark for each difference		**3**
	ii.	SISO shift register with its logic diagram	- 2 marks	**7**
		SIPO shift register with its logic diagram	- 2 marks	
		PISO shift register with its logic diagram	-3 marks	
OR	iii.	limitation of JK flip-flop (Race around condition	- 2 mark	**7**
		working of Master-Slave JK flip-flop.	– 3 marks	
		logic diagram	- 2 marks	
Q.6				
	i.	static RAM working-	- 1.5 marks	**5**
		dynamic RAM working	- 1.5 marks	
		diagrams for static RAM	- 1mark	
		diagram for dynamic RAM	- 1 mark	
	ii.	ROM organization	-3 marks	**5**
		Types of ROM	-2 marks	

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iii. Implementation of Boolean function through PLA 2.5 marks **5**

Implementation of Boolean function PAL - 2.5 marks

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