*Total No. of Questions: 6* *Total No. of Printed Pages:3*

**Enrollment No.....**

# Faculty of Engineering

## End Sem (Odd) Examination Dec-2019

## CA5CO03 Computer Organization & Architecture

Programme: MCA Branch/Specialisation: Computer Application

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Binary equivalent of hexadecimal number $A85_{16}$ is: **1**

(a) 2687 (b) 2767 (c) 2693 (d) 1085

ii. In terms of Boolean laws, $A+\overline{A}B=$ **1**

(a) B (b) A (c) A+B (d) AB

iii. A microoperation is an elementary operation performed on the information stored in: **1**

(a) Registers (b) RAM

(c) Secondary memory (d) Cache

iv. In high impedance state, output is **1**

(a) Connected (b) Disconnected

(c) High (d) Low

v. In relative address mode, effective address is equal to **1**

(a) Address part of the instruction

(b) Address part of instruction + content of program counter

(c) Address part of instruction + content of index register

(d) Address part of the instruction +contents of base register

vi. Choose the correct sequence of phases in instruction cycle: **1**

(a) Fetch instruction → Decode instruction → Calculate effective address → Fetch operands → Execute instruction

(b) Fetch instruction→ Calculate effective address →Decode instruction → Fetch operands → Execute instruction

(c) Fetch instruction → Decode instruction →Fetch operands → Execute instruction

(d) Fetch instruction → Decode instruction → Fetch operands → Calculate effective address→ Execute instruction

P.T.O.

vii. Which of the following is not a data register in 8086?
(a) DX (b) BX (c) EX (d) CX

viii. Which is a flag manipulation instruction in 8086. **1**
(a) JLE (b) CLD (c) JS (d) LOOP

ix. A memory unit accessed by data content rather than by specific address is called: **1**
(a) Primary memory (b) Secondary memory
(c) Associative memory (d) Extended memory

x. Full form of EEPROM is: **1**
(a) Electrically erasable programmable ROM
(b) Electrically extendable programmable ROM
(c) Electively erasable programmable ROM
(d) Electrically erasable primary ROM

Q.2 i. Briefly specify real life applications of multiplexers. **2**

ii. Prove the following Boolean expression **3**
$(A + B)(\overline{A}\,\overline{C} + C)(\overline{B} + A\,C) = \overline{A}\,B$

iii. Determine the single error-correcting code for information code 1001 using even parity. **5**

OR iv. Why NAND and NOR gates are called universal logic gates? **5**

Q.3 i. Briefly explain register transfer language. **3**

ii. Implement 4-bit arithmetic circuit which can perform various arithmetic microoperations. **7**

OR iii. Explain the concept of common bus system in a typical digital computer. **7**

Q.4 i. Differentiate between synchronous and asynchronous data transfer. **3**

ii. Explain how an interrupt is handled by the computer. **7**

OR iii. Explain direct memory access (DMA) mode of data transfer. **7**

Q.5 i. Discuss the advantages of segmented memory in 8086. **3**

ii. Explain pin configuration of 8086. **7**

OR iii. Discuss the addressing modes of 8086. **7**



Q.6 Attempt any two:

i. Briefly explain significance of memory hierarchy. **5**

ii. Write a short note on set-associative mapping for cache memory. **5**

iii. How many 128 * 8 RAM chips are needed to provide a memory capacity of 2048 bytes? How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? How many lines must be decoded for chip select? Specify the size of the decoders. **5**

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# Marking Scheme

## CA5CO03 Computer Organization & Architecture

| | | | | |
|---|---|---|---|---|
| Q.1 | i. | Binary equivalent of hexadecimal number $A85_{16}$ is: | | **1** |
| | ii. | In terms of Boolean laws, $A+\overline{A}B=$ | | **1** |
| | | (c) A+B | | |
| | iii. | A microoperation is an elementary operation performed on the information stored in: | | **1** |
| | | (a) Registers | | |
| | iv. | In high impedance state, output is | | **1** |
| | | (b) Disconnected | | |
| | v. | In relative address mode, effective address is equal to | | **1** |
| | | Address part of instruction + content of program counter | | |
| | vi. | Choose the correct sequence of phases in instruction cycle: | | **1** |
| | | (a) Fetch instruction → Decode instruction → Calculate effective address → Fetch operands → Execute instruction | | |
| | vii. | Which of the following is not a data register in 8086? | | |
| | | (c) EX | | |
| | viii. | Which is a flag manipulation instruction in 8086. | | **1** |
| | | (b) CLD | | |
| | ix. | A memory unit accessed by data content rather than by specific address is called: | | **1** |
| | | (c) Associative memory | | |
| | x. | Full form of EEPROM is: | | **1** |
| | | (a) Electrically erasable programmable ROM | | |
| Q.2 | i. | Real life applications of multiplexers | | **2** |
| | | Any 4 points 0.5 mark for each | (0.5 mark * 4) | |
| | ii. | Prove the expression | | **3** |
| | iii. | Determination of number of parity bits | 1 mark | **5** |
| | | Proper placing of parity bits | 1 mark | |
| | | Determining the value of all three parity bits and creating code | | |
| | | 1 mark for each (1 mark * 3) | 3 marks | |
| OR | iv. | NAND gates | 2.5 marks | **5** |
| | | NOR gates | 2.5 marks | |
| Q.3 | i. | Register transfer language. | | **3** |
| | | Any 6 points 0.5 mark for each | (0.5 mark * 6) | |
| | ii. | Implement 4-bit arithmetic circuit | | **7** |
| | | Specifying all arithmetic microoperations | 1 mark | |
| | | Diagram | 2 marks | |
| | | Function table | 1 mark | |
| | | Explanation | 3 marks | |
| OR | iii. | Definition of common bus system | 1 mark | **7** |
| | | Diagram | 2 marks | |
| | | Function table | 1 mark | |
| | | Explanation | 3 marks | |
| Q.4 | i. | Difference b/w synchronous and asynchronous data transfer | | **3** |
| | | Any 6 points 0.5 mark for each | (0.5 mark * 6) | |
| | ii. | Interrupt is handled by the computer. | | **7** |
| | | Diagram of interrupt cycle | 2 marks | |
| | | Explanation | 3 marks | |
| | | Example | 2 marks | |
| OR | iii. | Direct memory access (DMA) mode of data transfer | | **7** |
| | | Diagram | 3 marks | |
| | | Explanation | 4 marks | |
| Q.5 | i. | Advantages of segmented memory in 8086. | | **3** |
| | | Any 4 points 0.5 mark for each (0.5 mark * 4) | 2 marks | |
| | | Diagram | 1 mark | |
| | ii. | Pin configuration of 8086. | | **7** |
| | | Diagram | 2 marks | |
| | | Description of pins | 5 marks | |
| OR | iii. | Any seven addressing modes of 8086. | | **7** |
| | | Any 7 points 1 mark for each | (1 mark * 7) | |
| Q.6 | | Attempt any two: | | |
| | i. | Significance of memory hierarchy. | | **5** |
| | | Diagram | 1 mark | |
| | | Explanation | 4 marks | |
| | ii. | Set-associative mapping for cache memory. | | **5** |
| | | Diagram | 1 mark | |
| | | Explanation | 4 marks | |
| | iii. | How many 128 * 8 RAM chips are needed to provide a memory | | **5** |

capacity of 2048 bytes? 1 mark

How many lines of the address bus must be used to access 2048 bytes of memory? 1 mark

How many of these lines will be common to all chips? 1 mark

How many lines must be decoded for chip select? 1 mark

Specify the size of the decoders. 1 mark

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