Total No. of Questions: 21

Enrollment No : _____

MEDICAPS UNIVERSITY

Faculty of Engineering / Science

End Semester Examination May 2025

CS3CO35 / BC3CO61 Microprocessor & Interfacing

Programme	:	B.Tech. / B. Sc.	**Branch/Specialisation**	:	CSE All / CS
Duration	:	3 hours	**Maximum Marks**	:	60

Note: *All questions are compulsory. Internal choices, if any, are indicated. Assume suitable data if necessary. Notations and symbols have their usual meaning.*

Section 1 (Answer all question(s))

		Marks	CO	BL
Q1.	Which of the following is not a valid register pair in 8085 µP? (•) AB ( ) BC ( ) DE ( ) HL	1	1	1
Q2.	Which of the following are temporary registers? ( ) BC ( ) DE ( ) HL (•) WZ	1	1	1
Q3.	Which of the following is a 2-byte instruction in 8085 µP? ( ) LDA 2500H ( ) MOV A, B (•) IN 01H ( ) JMP 2085H	1	2	2
Q4.	Which of the following is a register-indirect addressing mode instruction set? ( ) LDA 2700H ( ) ADI 36H ( ) DAA (•) LDAX B	1	2	2
Q5.	How many address lines are required to connect a 4 KB RAM to 8085 µP? ( ) 10 (•) 12 ( ) 16 ( ) 20	1	3	3
Q6.	How many I/O lines are present in 8255 PPI. ( ) 10 ( ) 12 ( ) 20 (•) 24	1	1	1
Q7.	Which of the following interrupt has lowest priority in 8085? ( ) RST 7.5 ( ) RST 6.5 ( ) RST 5.5 (•) INTR	1	2	2
Q8.	Operation performed in one clock period is known as- ( ) Instruction cycle ( ) Machine cycle (•) T-State ( ) Execution time	1	2	2
Q9.	The computer architecture aimed at reducing the time of execution of instructions is- ( ) CISC (•) RISC ( ) ANNA ( ) ISA	1	2	2
Q10.	What is the primary purpose of pipelining in computer architecture? ( ) To increase clock frequency (•) To decrease instruction latency ( ) To reduce power consumption ( ) To simplify instruction set architecture	1	2	2

Section 2 (Answer all question(s))

Marks CO BL

Q11. Differentiate between terms microcomputer and microprocessor. **3 2 2**

Rubric	Marks
Differences at least 3	3

Q12. (a) Draw and explain the internal architecture block diagram of 8085 μP. **7 2 2**

Rubric	Marks
Block diagram-3 Explanation-4	7

(OR)

(b) Draw pin diagram of 8085 μP and explain their functions.

Rubric	Marks
8085 μP Pin diagram-3 Explanation of Pin functions-4	7

Section 3 (Answer all question(s))

Marks CO BL

Q13. What is meant by stack and subroutines? Explain the terms with suitable example. **4 2 2**

Rubric	Marks
Explanation of stack-2 Explanation of subroutines.-2	4

Q14. (a) What are different type of addressing modes in 8085? Explain with suitable example. **6 3 3**

Rubric	Marks
1 mark for each addressing mode with example.	6

(OR)

(b) Write an 8085-assembly language program for generating a delay routine with explanation.

Rubric	Marks
Assembly program-4 Explanation-2	6

Section 4 (Answer all question(s))

Marks CO BL

Q15. Differentiate between I/O mapped I/O, and memory mapped I/O techniques. **4 2 2**

Rubric	Marks
1 mark for each valid point.	4

Q16. (a) Draw & explain the functional block diagram of programmable peripheral interface (Intel 8255). **6 2 2**

Rubric	Marks
Functional block diagram of 8255- 3 Explanation-3	6

(OR)

(b) Draw & explain the functional block diagram of Programmable timer interface (Intel 8253/ 54).

Rubric	Marks
Functional block diagram of 8253- 3 Explanation -3	6

Section 5 (Answer all question(s))

Marks CO BL

Q17. Differentiate between hardware and software interrupts of 8085 µP. **4 2 2**

Rubric	Marks
valid Differences at least 4	4

Q18. (a) Draw and explain the timing diagram of the instruction: MVI A, 45H. **6 3 3**

Rubric	Marks
Timing diagram-3 Explanation -3	6

(OR)

(b) Draw and explain the timing diagram of the instruction: MOV A, B.

Rubric	Marks
Timing diagram-3 Explanation-3	6

Section 6 (Answer any 2 question(s))

Marks CO BL

Q19. How an intel architecture system works? Explain. **5 2 2**

Rubric	Marks
Intel Architecture System Diagram-2 Intel Architecture System Working-3	5

Q20. What are the basic components of the Intel Core 2 Duo Processor? Explain. **5 2 2**

Rubric	Marks
Basic Components of the Intel Core 2 Duo Processor-2 Explain Basic Components of the Intel Core 2 Duo Processor-3	5

Q21. Explain the system with Intel atom processor in detail. **5 2 2**

Rubric	Marks
Diagram with explanation-5	5

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