*Total No. of Questions: 6* *Total No. of Printed Pages:3*

**Enrollment No.....**

Faculty of Engineering

End Sem Examination May-2023

IT3CO31 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: IT

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. What is computer organization? **1**

(a) Structure and behaviour of a computer system as observed by the user

(b) Structure of a computer system as observed by the developer

(c) Structure and behaviour of a computer system as observed by the developer

(d) All of these

ii. Which of the architecture is power efficient? **1**

(a) RISC (b) ISA (c) IANA (d) CISC

iii. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____. **1**

(a) EA = 5+R1 (b) EA = R1

(c) EA = [R1] (d) EA = 5+[R1]

iv. In the case of, Zero-address instruction method the operands are stored in _____. **1**

(a) Registers (b) Accumulators

(c) Push down stack (d) Cache

v. The drawback of building a large memory with DRAM is _____. **1**

(a) The large cost factor

(b) The inefficient memory organisation

(c) The Slow speed of operation

(d) All of these

P.T.O.

vi. The algorithm to remove and place new contents into the cache is called _____. **1**
(a) Replacement algorithm (b) Renewal algorithm
(c) Updation (d) None of these

vii. The DMA transfers are performed by a control circuit called as- **1**
(a) Device interface (b) DMA controller
(c) Data controller (d) Overlooker

viii. The technique where the controller is given complete access to main memory is _____. **1**
(a) Cycle stealing (b) Memory stealing
(c) Memory Con (d) Burst mode

ix. The computer architecture aimed at reducing the time of execution of instructions is _____. **1**
(a) CISC (b) RISC (c) ISA (d) ANNA

x. Any condition that causes a processor to stall is called as _____. **1**
(a) Hazard (b) Page fault
(c) System error (d) None of these

Q.2 i. Explain working of the system bus in a computer system. **2**
ii. Explain Von Newman model with the help of labelled diagram. Explain Von Newman bottleneck. **3**
iii. Define Instruction cycle. Explain working of Instruction cycle in detail. **5**
OR iv. What is register transfer language? Explain different types of RTL. **5**

Q.3 i. Draw & explain typical hardwired control unit. **3**
ii. Explain working principal of micro program sequencer with the help of diagram. **7**
OR iii. What do you understand by addressing mode? Explain different types of addressing modes used in basic computer system. **7**

Q.4 i. Draw & explain memory hierarchy. **3**
ii. What is content addressable memory? What are its advantages? How it is different from set associative memory? **7**
OR iii. What is cache memory? Write about different characteristics of cache memory & types of cache memory in computer system. **7**



Q.5 i. Describe input-output interface with the help of diagram. **4**
ii. Define & differentiate between programmed I/O and Interrupt-initiated I/O. **6**
OR iii. What is DMA? How does DMA controller work? Explain with suitable block diagram. **6**

Q.6 Attempt any two:
i. Explain parallel processing with the help of example. Also differentiate parallel processing & vector processing. **5**
ii. Explain arithmetic pipeline with the help of example. **5**
iii. Explain instruction pipeline with the help of example. **5**

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# Marking Scheme

## IT3CO31 [T] -Computer System Architecture

| | | | |
|---|---|---|---|
| Q.1 | i) | a) structure and behaviour of a computer system as observed by the user | **1** |
| | ii) | a) RISC | **1** |
| | iii) | d) EA = 5+[R1] | **1** |
| | iv) | c) Push down stack | **1** |
| | v) | c) The Slow speed of operation | **1** |
| | vi) | a) Replacement algorithm | **1** |
| | vii) | b) DMA controller | **1** |
| | viii) | d) Burst mode | **1** |
| | ix) | b) RISC | **1** |
| | x) | a) Hazard | **1** |
| Q.2 | i. | Explanation of system bus with Diagram. | **2** |
| | ii. | Explanation with diagram von Newman model. | **2** |
| | | von Newman bottleneck. | **1** |
| | iii. | Definition of Instruction cycle | **1** |
| | | working of Instruction cycle | **4** |
| OR | iv. | Explanation of Register transfer language | **1** |
| | | Types of Register transfer language | **4** |
| Q.3 | i. | Diagram of Hardwired Control Unit | **1** |
| | | Explanation of typical Hardwired Control Unit | **2** |
| | ii. | working principal of Micro Program Sequencer | **3** |
| | | Diagram of Micro Program Sequencer | **4** |
| OR | iii. | Explanation of addressing modes | **2** |
| | | Types of addressing modes | **5** |
| Q.4 | i. | Diagram of memory hierarchy | **1** |
| | | Explanation of memory hierarchy | **2** |
| | ii. | Explanation of Content Addressable Memory | **3** |
| | | Advantage of Content Addressable Memory | **2** |
| | | difference from set associative memory | **2** |
| OR | iii. | Explanation of Cache Memory | **3** |



| | | | |
|---|---|---|---|
| | | different characteristics of Cache Memory | **2** |
| | | Types of cache memory in computer system | **2** |
| Q.5 | i. | Describe Input-Output Interface | **2** |
| | | diagram of Input-Output Interface | **2** |
| | ii. | Definition of programmed I/O and Interrupt-initiated I/O? | **3** |
| | | Differentiate between programmed I/O and Interrupt-initiated I/O? | **3** |
| OR | iii. | Explanation of DMA | **2** |
| | | DMA controller working | **2** |
| | | Block Diagram of DMA | **2** |
| Q.6 | | | |
| | i. | Explanation of parallel Processing & example | **2** |
| | | Difference of Parallel Processing & Vector Processing | **3** |
| | ii. | Explanation of Arithmetic Pipeline | **2** |
| | | Example of Arithmetic Pipeline | **3** |
| | iii. | Explanation of Instruction Pipeline | **2** |
| | | Example of Instruction Pipeline | **3** |

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