Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination May-2024
EC3EL08 / EI3EL08
Computer Organization & Architecture

Programme: B.Tech. Branch/Specialisation: EC/EI

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. MFC stands for _____. **1**
(a) Memory Format Caches (b) Memory Function Complete
(c) Memory Find Command (d) Mass Format Command

ii. In multiple bus organisation, the registers are collectively placed and referred as: **1**
(a) Set registers (b) Register file
(c) Register Block (d) Map registers

iii. In IEEE double precision floating point format, the size of the mantissa part is: **1**
(a) 32 bit (b) 64 bit (c) 72 bit (d) 52 bit

iv. In order to implement complex instructions, CISC architectures use: **1**
(a) Macro-programming (b) Hardwired logic
(c) Micro-programming (d) None of these

v. An instruction pipeline can be implemented by means of: **1**
(a) LIFO buffer (b) FIFO buffer
(c) Stack (d) None of these

vi. The contention for the usage of a hardware device is called: **1**
(a) Structural hazard (b) Stall
(c) Deadlock (d) None of these

vii. Which of the following architecture is/are not suitable for realizing SIMD model? **1**
(a) Vector processor (b) Array processor
(c) Von Neumann (d) All of these

P.T.O.

viii. The throughput of a superscalar processor is: **1**
(a) Less than 1 (b) 1 (c) More than 1 (d) Not known

ix. The slowest data access is provided using: **1**
(a) Caches (b) DRAM's (c) SRAM's (d) CPU Registers

x. The method of mapping the consecutive main memory blocks to consecutive cache blocks is called _____. **1**
(a) Associative (b) Set associative
(c) Direct (d) Indirect

Q.2 i. What is Von-Neumann Architecture? **2**

ii. Explain three factors that influence computer performance using its basic performance equation. **3**

iii. Compare and contrast between the first and second generation of electronic computers. **5**

OR iv. Explain the micro programmed CPU control unit with its block diagram. **5**

Q.3 i. Convert the decimal number (-85.25) into IEEE 754 single precision floating point format. **3**

ii. What do you mean by a floating point number? Compare RISC & CISC architecture with their five characteristics. **7**

OR iii. What is an addressing mode? Explain any five types of addressing modes with example of each. **7**

Q.4 i. How does an instruction pipeline improves the speed of execution of a program? **3**

ii. What do you mean by pipeline hazards? Explain instruction hazard with a relevant diagram. **7**

OR iii. Describe the operation of four stage instruction pipelining with diagram. **7**

Q.5 i. Differentiate between a process and thread. **3**

ii. What do you mean by an array processor? Explain its operation with a diagram. **7**

OR iii. What is Flynn's taxonomy for parallel processing? Explain any two type of its computer structures with diagram. **7**

Q.6 Explain any two with the help of relevant diagram:

i. Computer memory hierarchy **5**

ii. Cache memories **5**

iii. Shared memory systems **5**

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Marking Scheme

EC3EL08 / EI3EL08 Computer Organization and Architecture

Q.1	i.	MFC stands for _____. b) Memory Function Complete	**1**
	ii.	In multiple bus organisation, the registers are collectively placed and referred as: b) Register file	**1**
	iii.	In IEEE double precision floating point format, the size of the mantissa part is: d) 52 bit	**1**
	iv.	In order to implement complex instructions, CISC architectures use: c) Micro-programming	**1**
	v.	An instruction pipeline can be implemented by means of: b) FIFO buffer	**1**
	vi.	The contention for the usage of a hardware device is called: a) Structural hazard	**1**
	vii.	The throughput of a superscalar processor is: c) More than 1	**1**
	viii.	Which of the following architecture is/are not suitable for realizing SIMD model? c) Von Neumann	**1**
	ix.	The slowest data access is provided using: b) DRAM's	**1**
	x.	The method of mapping the consecutive main memory blocks to consecutive cache blocks is called : c) Direct	**1**
Q.2	i.	What is Von-Neumann Architecture? Explanation – 2 Marks	**2**
	ii.	For best performance, the following factors must be considered: 1. Compiler 2. Instruction set 3. Hardware design, etc. (1x3 Marks) Basic performance equation T=(N x S)/R	**3**
	iii.	Comparison: First and Second generation based on: Vacuum tubes, Transistors 1x5 Marks	**5**
OR	iv.	Explain the Micro programmed CPU control unit with its block diagram. Block diagram - 2 Marks, Description – 3 Marks	**5**
Q.3	i.	Convert the decimal number (-85.25) into IEEE 754 single precision floating point format. Mantissa = 01010101 1 Mark E' = 10000101 1 Mark Ans. 1 10000101 01010101000000000000000 1 Mark	**3**
	ii.	Floating point number description – 2 Marks Comparison b/w RISC & CISC architecture – 5 Marks	**7**
OR	iii.	Definition of addressing mode 2 Marks Five types of addressing modes with example 1x5 Marks	**7**
Q.4	i.	How does an instruction pipeline improves the speed of execution of a program? Justify reason – 3 Marks	**3**
	ii.	Pipeline hazards - 2 Marks Diagram - 2 Marks Instruction hazards description with example – 3 Marks	**7**
OR	iii.	Four stage instruction pipelining Block diagram – 2 Marks Explanation – 5 Marks	**7**
Q.5	i.	Difference between process and thread – 3 Marks	**3**
	ii.	Array processor description– 2 Marks Diagram – 2 Marks, Operation – 3 Marks	**7**
OR	iii.	Flynn's taxonomy – 2 Marks Computer structures – 2.5x2	**7**
Q.6		Explain any **two** with the help of relevant diagram: Diagram – 2 Marks, Description – 3 Marks	
	i.	Computer Memory hierarchy	**5**
	ii.	Cache memories	**5**
	iii.	Shared Memory Systems	**5**

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