Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2022

RA3CO26 Digital Electronics

Programme: B.Tech. Branch/Specialisation: RA

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Reflected binary code is also known as- 1

(a) BCD code (b) Binary code

(c) ASCII code (d) Gray code

ii. According to DeMorgan's theorem- 1

(a) NAND= Bubbled OR (b) NAND= Bubbled AND

(c) NOR= Bubbled OR (d) None of these

iii. What are the basic gates in MOS logic family? 1

(a) NAND and NOR (b) AND and OR

(c) NAND and OR (d) AND and NOR

iv. In DTL logic gating function is performed by- 1

(a) Diode (b) Transistor (c) Inductor (d) Capacitor

v. In a multiplexer, the selection of a particular input line is controlled by- 1

(a) Data controller (b) Selected lines

(c) Logic gates (d) Both (a) & (b)

vi. The purpose of a Digital Comparator is- 1

(a) To convert analog input into digital

(b) To create different outputs

(c) To add a set of different numbers

(d) To compare a set of variables or unknown numbers

vii. The D flip-flop has _____ input. 1

(a) 1 (b) 2 (c) 3 (d) 4

viii. The basic latch consists of - 1

(a) Two inverters (b) Two comparators

(c) Two amplifiers (d) Two adders

P.T.O.

ix. ROMs retain data when- 1

(a) Power is on (b) Power is off

(c) System is down (d) All of these

x. The full form of PLD is- 1

(a) Programmable Load Devices (b) Programmable Logic Data

(c) Programmable Logic Devices (d) Programmable Loaded Devices

Q.2 i. Convert $(11011.101)_2$ to decimal. 2

ii. Implement Ex-OR using NOR gate only. 3

iii. Reduce the logical expression using K map 5

Y (A, B, C, D) = minterm (1,5,7,9,11,13,15) and realize the minimized expression using basic gates.

OR iv. Reduce the expression A[B+C'(AB+AC')']. 5

Q.3 i. What is propagation delay? 2

ii. Explain the different characteristic of logic families. 8

OR iii. Explain TTL logic in detail with suitable diagram. 8

Q.4 i. Draw the circuit of one bit magnitude comparator. 3

ii. Draw circuit diagram of full adder and write its truth table. 7

OR iii. Explain in detail the working of 8*1 multiplexer with circuit diagram. 7

Q.5 i. Draw the SR flip flop with characteristic table. 4

ii. Draw and explain the working of master slave JK flip flop. 6

OR iii. Explain ripple counter with suitable timing diagram. 6

Q.6 Attempt any two:

i. Explain Random Access Memory in detail. 5

ii. Explain Read Only Memory in detail. 5

iii. Explain Programmable logic array in detail. 5

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Marking Scheme
Digital Electronics RA3CO26

Q.1	i)	(d) Gray code	1
	ii)	(a) NAND= Bubbled OR	1
	iii)	(a) NAND and NOR	1
	iv)	(a) Diode	1
	v)	(b) Selected lines	1
	vi)	(d) To compare a set of variables or unknown numbers	1
	vii)	(b) 2	1
	viii)	(a) Two inverters	1
	ix)	(d) All of the Mentioned	1
	x)	(c) Programmable Logic Devices	1

Q.2	i.	Conversion 2 marks
	ii.	Implement -3 marks
	iii.	Complete solution 5 marks
OR	iv.	Complete solution 5 marks

Q.3	i.	2 marks
	ii.	Four characteristic with description- 8 marks
OR	iii.	TTL logic in detail-5 diagram- 3 marks

Q.4	i.	Draw circuit – 3 marks
	ii.	circuit diagram 4 marks, truth table- 3 marks
OR	iii.	circuit diagram 3 marks, working – 4 marks

Q.5	i.	Draw SR flip flop -2marks, characteristic table- 2marks
	ii.	master slave JK flip flop -3 marks, working- 3 marks
OR	iii.	Explain ripple counter - 3 marks, timing diagram- 3 marks

Q.6

	i.	Description 5 marks
	ii.	Description 5 marks
	iii.	Description 5 marks

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