Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2022

EN3ES14 Computer Organization and Architecture

Programme: B.Tech. Branch/Specialisation: CSBS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Convert the following binary number to decimal. 01011- **1**
(a) 15 (b) 18 (c) 14 (d) 11

ii. A micro-operation is an elementary operation performed on the information stored in- **1**
(a) Registers (b) RAM
(c) Secondary memory (d) Cache

iii. In Booth's multiplication algorithm where $Q_{n-1}Q_0$ bit is equal to 00 or 11 then what operation is performed? **1**
(a) A – M (b) A +M (c) Ashr (d) Shr

iv. When we perform subtraction on -7 and -5 the answer in 2's complement form is- **1**
(a) 11110 (b) 1110 (c) 1010 (d) 0011

v. The DMA controller has _____ registers. **1**
(a) 4 (b) 2 (c) 3 (d) 1

vi. The software mechanism that allows a device to notify the CPU is called- **1**
(a) Polling (b) Interrupt (c) Driver (d) Controlling

vii. Which is used to speed-up the processing? **1**
(a) Pipeline (b) Vector processing
(c) Both (a) and (b) (d) None of these

viii. Data hazards occur when _____. **1**
(a) Greater performance loss
(b) Pipeline changes the order of read/write access to operands
(c) Some functional unit is not fully pipelined
(d) Machine size is limited

P.T.O.

ix. Whenever the data is found in the cache memory it is called as- **1**
(a) Hit (b) Miss (c) Found (d) True

x. Which of the following is true for a memory hierarchy? **1**
(a) It tries to bridge the processor memory speed gap.
(b) The speed of the memory level closest to the processor has the highest speed.
(c) It is based on the principle of locality of reference.
(d) All of these

Q.2 i. What is RTL? Explain with example. **3**

ii. What do you mean by the term addressing modes? List any six addressing modes with one example for each. **7**

OR iii. What are the different fields of an instruction? Explain instruction cycle with the help of flowchart. **7**

Q.3 i. What is ripple carry adder? **2**

ii. Explain Booth's algorithm for multiplication of two fixed point numbers. Take two numbers of your choice for explaining the multiplication process. **8**

OR iii. Draw flowchart to explain division algorithm for signed magnitude data. What is divide overflow condition? **8**

Q.4 i. What is I/O interface in computer architecture? **3**

ii. Define interrupt. Explain any six different types of interrupts. **7**

OR iii. Explain hardwired implementation of control unit. **7**

Q.5 i. What is pipelining and what are the advantages of it? **4**

ii. What is pipeline hazard? Explain its types. **6**

OR iii. What is cache coherence and how is it eliminated? **6**

Q.6 Attempt any two:

i. Write a short note on set-associative mapping for cache memory. **5**

ii. Explain contemporary memory hierarchy structure. **5**

iii. What is cache memory and why is it important? **5**

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Marking Scheme
EN3ES14 Computer Organization and Architecture

Q.1	i)	Convert the following binary number to decimal. 01011 (d) 11	**1**
	ii)	A micro-operation is an elementary operation performed on the information stored in: (a) Registers	**1**
	iii)	In Booth's multiplication algorithm where $Q_{n-1}Q_0$ bit is equal to 00 or 11 then what operation is performed? (c) Ashr	**1**
	iv)	When we perform subtraction on -7 and -5 the answer in 2's complement form is (b) 1110	**1**
	v)	The DMA controller has _____ registers (c) 3	**1**
	vi)	The software mechanism that allows a device to notify the CPU is called- (a) Polling	**1**
	vii)	Which is used to speed-up the processing: (c) Both (a) & (b)	**1**
	viii)	Data hazards occur when..... (b) Pipeline changes the order of read/write access to operands	**1**
	ix)	Whenever the data is found in the cache memory it is called as (a) Hit	**1**
	x)	Which of the following is true for a memory hierarchy? (d) All of these	**1**
Q.2	i.	What is RTL? -1.5 marks Explain with example. -1.5 marks	**3**
	ii.	Addressing mode definition -1 mark 6-types with example -1 mark of each (6 marks)	**7**
OR	iii.	What are the different fields of an instruction? -3 marks Explain instruction cycle with the help of flowchart. -4Marks	**7**
Q.3	i.	ripple carry adder definition -2 marks	**2**
	ii.	Booth's Algorithm+ Flow chart -4 marks Example for explaining the multiplication process -4 marks	**8**
OR	iii.	Flowchart + Algorithm explanation -5 marks Overflow condition -3 marks	**8**
Q.4	i.	I/O interface -3 marks	**3**
	ii.	Definition interrupt -1 mark Any six types of interrupts. -1 mark of each (6 marks)	**7**
OR	iii.	Hardwired implementation of control unit. Diagram -3.5 marks Explanation -3.5 marks	**7**
Q.5	i.	Define pipelining -1 mark Advantages -3 marks	**4**
	ii.	What is pipeline hazard? -3 marks Explain its types. -3 marks	**6**
OR	iii.	What is cache coherence? -3 marks How is it eliminated? -3 marks	**6**
Q.6		Attempt any two:	
	i.	Set-associative mapping for cache memory. Diagram -1 mark Explanation -4 marks	**5**
	ii.	Contemporary memory hierarchy structure. Diagram -2 marks Explanation -3 marks	**5**
	iii.	What is cache memory and why is it important? Cache Memory -3 marks Importance -2 marks	**5**

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