Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2019

EC3EV01 / EI3EV01 Design for Testability

Programme: B.Tech. Branch/Specialisation: EC/EI

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Design for testability is considered in production for chips because **1**

(a) Manufactured chips are faulty and are required to be tested

(b) The design of chips are required to be tested

(c) Many chips are required to be tested within short interval of time which yields timely delivery for the customers.

(d) All of these

ii. Which fault causes output floating? **1**

(a) Stuck-open (b) Stuck-at

(c) Stuck-on (d) IDDQ

iii. Large number of input vectors are used to set a particular node (1) or (0), to propagate an error at the node to output makes the circuit low on: **1**

(a) Testability (b) Observability

(c) Controllability (d) All of these

iv. Divide and Conquer approach to large and complex circuits for testing is found in: **1**

(a) Simplified automatic test pattern generation technique

(b) Partition and Mux Technique

(c) Scan based technique

(d) All of these

v. The circuits with poor observability are: **1**

(a) ROM

(b) PLA

(c) Sequential circuits with long feedback loops

(d) All of these

P.T.O.

vi. Test patterns produced by _____ have both high and least toggle rates **1**
(a) Random pattern generator (b) Counters
(c) LFSR (d) CA

vii. In level sensitive aspect, when an input change occurs, the response in **1**
(a) Dependent of components
(b) Dependent on wiring delays
(c) Independent of wiring delays
(d) Independent of input combinations

viii. Boundary scan test is used to test **1**
(a) Pins (b) Multipliers
(c) Boards (d) Wires

ix. The signature analysis method can be represented mathematically as **1**
(a) R(x) = P(x) * C(x) (b) R(x) = P(x) / C(x)
(c) R(x) = C(x) / P(x) (d) R(x) = C(x) * P(x)

x. Self-checking technique consists of **1**
(a) Supplying coded input data
(b) Receiving coded output data
(c) Supplying all possible input sequence
(d) All of these

Q.2 i. Draw the VLSI design flow diagram. **2**
ii. How many types of fault are in VLSI system? Give brief classification. Explain each of them with the help of example. **8**
OR iii. Explain the concept of testing in VLSI circuit with the help of suitable example. **8**

Q.3 i. Explain forward trace and backward trace. **2**
ii. Explain the working principle of D algorithm for test generation with the help of example. **8**
OR iii. Explain FAN algorithms and PODEM algorithms with suitable example. **8**

Q.4 i. Explain functional fault models. **2**
ii. Write an example which used to test sequential circuits for the iterative combinational circuits. **8**

OR iii. What is automatic test pattern generator? Explain using stuck at fault in combinational circuits. **8**

Q.5 i. Explain boundary scan design. **4**
ii. Describe full and partial scan designing for sequential circuits. **6**
OR iii. Explain Ad-hoc testable design techniques. **6**

Q.6 i. What is Built in self test and how it is useful in VLSI system? **3**
ii. Explain built-in logic block observer with suitable example. **7**
OR iii. Write logic equation explaining the logic BIST random test pattern for testability factor. **7**

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Marking Scheme
EC3EV01 / EI3EV01 Design for Testability

Q.1	i.	Design for testability is considered in production for chips because (c) Many chips are required to be tested within short interval of time which yields timely delivery for the customers.		**1**
	ii.	Which fault causes output floating? (a) Stuck-open		**1**
	iii.	Large number of input vectors are used to set a particular node (1) or (0), to propagate an error at the node to output makes the circuit low on: (a) Testability		**1**
	iv.	Divide and Conquer approach to large and complex circuits for testing is found in: (b) Partition and Mux Technique		**1**
	v.	The circuits with poor observability are: (c) Sequential circuits with long feedback loops		**1**
	vi.	Test patterns produced by _____ have both high and least toggle rates (b) Counters		**1**
	vii.	In level sensitive aspect, when an input change occurs, the response in (c) Independent of wiring delays		**1**
	viii.	Boundary scan test is used to test (c) Boards		**1**
	ix.	The signature analysis method can be represented mathematically as (b) $R(x) = P(x) / C(x)$		**1**
	x.	Self-checking technique consists of (a) Supplying coded input data		**1**
Q.2	i.	VLSI design flow diagram.		**2**
	ii.	Classification of fault are in VLSI system Example	4 marks 4 marks	**8**
OR	iii.	Concept of testing in VLSI circuit Example	6 marks 2 marks	**8**
Q.3	i.	Forward trace Backward trace.	1 mark 1 mark	**2**
	ii.	Working principle of D algorithm for test generation Definition of Singular cover PDC PDCF Example	 2 marks 2 marks 2 marks 2 marks	**8**
OR	iii.	FAN algorithms with example PODEM algorithms with example	4 marks 4 marks	**8**
Q.4	i.	Functional fault models.		**2**
	ii.	Iterative combinational circuits Example of procedure	3 marks 5 marks	**8**
OR	iii.	Definition of automatic test pattern generator Explanation of combinational ATPG	2 marks 6 marks	**8**
Q.5	i.	Boundary scan design. Diagram Explanation	 2 marks 2 marks	**4**
	ii.	Full scan designing for sequential circuits Partial scan designing for sequential circuits	3 marks 3 marks	**6**
OR	iii.	Ad-hoc testable design techniques 2 marks for each technique	 (2 marks *3)	**6**
Q.6	i.	Definition of Built in self test Uses in VLSI system	2 marks 1 mark	**3**
	ii.	Built-in logic block observer architecture Example	4 marks 3 marks	**7**
OR	iii.	Logic BIST random test pattern for testability factor Diagram Logic equation Explanation	 2 marks 2 marks 3 marks	**7**

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