Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering / Science
End Sem Examination May-2024
CS3CO35 / BC3CO61 / BC3CO40
Microprocessor & Interfacing

Programme: B.Tech./ B.Sc. Branch/Specialisation: CSE All / CS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which of the following is not true about address bus? **1**
(a) It consists control pins 21 to 28
(b) It is a bidirectional
(c) It is 16-bits in length
(d) Lower Bus address line AD_0–AD_7 are called line number

ii. How many flip-flops are there in flag register in 8085 microprocessor? **1**
(a) 4 (b) 7 (c) 5 (d) 10

iii. A memory connected to microprocessor has 20 address line and 16 data line, what will be the memory capacity: **1**
(a) 8 KB (b) 1 MB (c) 16 MB (d) 64 KB

iv. The instruction that stores the contents of register pair on to the stack is: **1**
(a) POP F (b) PUSH SP
(c) PUSH B (d) None of these

v. In which mode the CPU periodically read an internal flag of 8279 to check whether any key pressed or not with key processor: **1**
(a) Interrupt mode (b) Polled mode
(c) Decoded mode (d) Encoded mode

vi. Intel 8251 is also known as: **1**
(a) Programmable peripheral interface
(b) Programmable timer interface
(c) Programmable display interface
(d) Programmable serial communication interface

vii. Which of the following is not a property of TRAP interrupt in microprocessor? **1**
(a) It is a non-maskable interrupt
(b) It is of highest priority
(c) It uses edge trigger signal
(d) It is a vectored interrupt

viii. For I/O read machine cycle, values of $S_1$and S_2 are: **1**
(a) S_1=1, S_2 =1 (b) S_1=0, S_2=0
(c) S_1=0, S_2=1 (d) S_1=1, S_2=0

ix. What is the full form of CISC? **1**
(a) Complex Instruction Set Computer
(b) Complicated Information Set Computer
(c) Command Instruction Set Computer
(d) None of these

x. Intel ICH is used to control- **1**
(a) Timing sequence (b) Clock sequence
(c) RESET sequence (d) None of these

Q.2 i. What is ALE? How does ALE operate? **2**
ii. Differentiate microcomputer and microprocessor. **3**
iii. Draw and explain internal architecture of 8085 microprocessor. **5**
OR iv. What is DMA? Explain its working with block diagram. **5**

Q.3 i. Define stack and subroutine. **2**
ii. Explain the addressing modes of 8085 microprocessor with example. **8**
OR iii. Write an assembly language programme to subtract 29H from 18H and store the result in memory location 200D. **8**

Q.4 i. Explain chip interface to microprocessor with appropriate example. **3**
ii. Draw and explain pin configuration of programmable peripheral Interface (8255). **7**
OR iii. Interface a 1KB EPROM and 2KB RAM with microprocessor 8085. The address allotted to 1KB EPROM should be 2000H to 22FFH. Assign the address range to the 2KB RAM. **7**

Q.5 i. What is the difference between hardware interrupt and software interrupt? **4**
ii. Draw and explain timing diagram of opcode fetch cycle. **6**
OR iii. Draw timing diagram of instruction: MVI B, 43H and if clock frequency is 2MHz then calculate clock period. **6**

Q.6 Attempt any two:
i. Explain system with intel core2 duo processor. **5**
ii. What is intel architecture? Explain its working. **5**
iii. Explain intel atom architecture. **5**

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Marking Scheme
CS3CO35 Micro Processor & Interfacing

Q.1	i)	Which of the following not true about address bus:- b) it is bidirectional	**1**
	ii)	How many flip-flop are there in flag register in 8085 microprocessor:- c) 5	**1**
	iii)	1 mark awarded to students those who have attempted.	**1**
	iv)	The instruction that the general purpose register, pointer, index register on to the stack is:- c) PUSH (A)	**1**
	v)	In which mode the CPU periodically read an internal flag of 8279 to check whether any key pressed or not with key processor: - b) Polled Mode	**1**
	vi)	Intel 8251 is also known as:- d)programmable Serial Communication Interface	**1**
	vii)	What of the following is not a property of TRAP interrupt in microprocessor:- c) It uses edge trigger signal	**1**
	viii)	1 mark awarded to students those who have attempted.	**1**
	ix)	What is the full form of CSIS:- a) Complex Instruction set computer	**1**
	x)	Intel ICH is used to control:- c) RESET sequence	**1**
Q.2	i.	What is ALE. How does ALE operate. Defining ALE - 1mark ALE operation - 1mark	**2**
	ii.	Differentiate between Microcomputer and Microprocessor. Microcomputer -1.5 marks Microprocessor - 1.5 marks	**3**
	iii.	Draw and explain internal architecture of 8085 microprocessor. Architecture -3 marks Explanation -2 marks	**5**

OR	iv.	What is DMA. Explain its working with block diagram. DMA definition -1 mark Working -2 marks Diagram - 2marks	**5**
Q.3	i.	Define Stack and Subroutine. Stack definition -1 mark Subroutine -1 mark	**2**
	ii.	Explain the addressing modes of 8085 microprocessor with its example. Addressing mode with its type -5 marks Example -3 marks	**8**
OR	iii.	Write an assembly language programme to subtract 29H from 18H and store the result in memory location 200D. Step marking -2marks each	**8**
Q.4	i.	Explain chip interface to microprocessor with appropriate example Explanation chip interface to microprocessor with diagram -1.5 marks Example -1.5 marks	**3**
	ii.	Draw and explain pin configuration of programmable peripheral Interface (8255). Pin diagram -4marks Explanation -3 marks	**7**
OR	iii.	Interface a 1KB EPROM and 2KB RAM with microprocessor 8085. The address allotted to 1KB EPROM should be 2000H to 22FFH. Assign the address range to the 2KB RAM. solution -4marks Diagram -3marks	**7**
Q.5	i.	What is the difference between Hardware interrupt and Software interrupt? Hardware interrupt + example - 2marks Software interrupt+ example - 2 marks	**4**
	ii.	Draw and explain timing diagram of opcode fetch cycle. Timing Diagram (Detailed with proper marking) - 4 marks Explanation - 2 marks	**6**
OR	iii.	Draw timing diagram of instruction:- MVI B, 43H And if clock frequency is 2MHz than calculate clock period. Timing diagram - 5 marks	**6**

	Clock period calculation	- 1 marks	
Q.6	Attempt any two		
i.	Explain system with Intel Core2 duo processor.		**5**
	Diagram	-2.5marks	
	Explanation	-2.5marks	
ii.	What is intel architecture. Explain its working.		**5**
	Architecture	-2.5marks	
	Working	-2.5marks	
iii.	Explain Intel Atom architecture.		**5**
	Architecture	-2.5marks	
	Explanation	-2.5marks	

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