Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering / Science
End Sem Examination Dec 2024
CS3CO33 / EC3CO07 / IT3CO26 / BC3CO38
Digital Electronics

Programme: B.Tech./B.Sc. Branch/Specialisation: CSE All/ EC/ IT/ Computer Science

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

			Marks	BL	PO	CO	PSO
Q.1	i.	What are the canonical forms of Boolean Expressions? (a) OR and XOR (b) NOR and XNOR (c) MAX and MIN (d) SOM and POM	**1**	1	1,2, 3,6	1	1,3, 4
	ii.	Convert $(0.345)_{10}$ into an octal number- (a) $(0.16050)_8$ (b) $(0.26050)_8$ (c) $(0.24040)_8$ (d) None of these	**1**	1	1,2, 3,6	1	1,3, 4
	iii.	What is the function of an enable input on a multiplexer chip? (a) To apply Vcc (b) To connect ground (c) To active the entire chip (d) To active one half of the chip	**1**	1	1,2, 3,6	2	1,3, 4
	iv.	How many two input AND, OR and EXOR gates are required for the configuration of full adder? (a) 1, 2, 2 (b) 2, 1, 2 (c) 3, 1, 2 (d) 4, 0, 1	**1**	1	1,2, 3,6	2	1,3, 4
	v.	In S-R flip-flop, if Q = 0 the output is said to be _____. (a) Set (b) Reset (c) Previous state (d) Current state	**1**	1	1,2, 3,6	3	1,3, 4

P.T.O.

vi.	Finite state machines are used for- (a) Deterministic test patterns (b) Algorithmic test patterns (c) Random test patterns (d) Pseudo random test patterns	**1**	1	1,2, 3,6	3	1,3, 4
vii.	Why ROMs are called non-volatile memory? (a) They lose memory when power is removed (b) They do not lose memory when power is removed (c) They lose memory when power is supplied (d) They do not lose memory when power is supplied	**1**	1	1,2, 3,6	4	1,3, 4
viii.	PLA is used to implement _____. (a) A complex sequential circuit (b) A simple sequential circuit (c) A complex combinational circuit (d) A simple combinational circuit	**1**	1	1,2, 3,6	4	1,3, 4
ix.	Which of the following is the most widely employed logic family? (a) Emitter-coupled logic (b) Transistor-transistor logic (c) CMOS logic family (d) NMOS logic	**1**	1	1,2, 3,6	5	1,3, 4
x.	CMOS gates are commercially available as which of the following series? (a) 1000 (b) 2000 (c) 3000 (d) 4000	**1**	1	1,2, 3,6	5	1,3, 4
Q.2 i.	Determine the values- (a) Find 2's compliment of 1110111 (b) $(1101.1)_2 = (\ )_{10}$ (c) $(1110101)_2 = (\ )_{Gray\ code}$ (d) $(3FD)_{16} = (\ )_2$	**4**	3	1,2, 3,6	1	1,3, 4
ii.	Given Y(a,b,c,d)= ∑(0,1,3,5,7,10,14,15) draw the K-map and obtain the simplified expression. Realize the minimum expression using basic gates.	**6**	3	1,2, 3,6	1	1,3,4
OR iii.	Simplify using Quine Mc-Clusky method. F(a,b,c,d)=∑(0,1,2,5,7,8,9,10,13,15).	**6**	3	1,2, 3,6	1	1,3, 4

Q.3 i.	Design a XOR & XNOR gate using NAND Gate.	**3**	3	1,2, 3,6	2	1,3, 4
ii.	Design a 3:8 decoder using basic gates.	**7**	3	1,2, 3,6	2	1,3, 4
OR iii.	Design a binary to gray code converter.	**7**	3	1,2, 3,6	2	1,3, 4
Q.4 i.	State any three differences between sequential and combinational circuits.	**3**	2	1,2, 3,6	3	1,3, 4
ii.	Realize a JK flip flop using SR flip flop.	**7**	3	1,2, 3,6	3	1,3, 4
OR iii.	What is a shift registers? Mention the uses of shift registers. Draw and explain the 4-bit SISO.	**7**	3	1,2, 3,6	3	1,3, 4
Q.5 i.	What does burning a ROM mean? What are the major drawbacks of the EEPROM?	**4**	2	1,2, 3,6	4	1,3, 4
ii.	What is Programmable Logic Array? What is its application? How it is different from PAL?	**6**	2	1,2, 3,6	4	1,3, 4
OR iii.	Compare a static and dynamic RAM cell. Write its applications.	**6**	2	1,2, 3,6	4	1,3, 4
Q.6	Attempt any two:					
i.	Compare all the IC logic families based on (at least three)- (a) Power consumption (b) Fan out (c) Power dissipation (d) Propagation delay (e) Noise margin	**5**	2	1,2, 3,6	5	1,3, 4
ii.	Design a TTL logic circuit for a 3-input NAND gate.	**5**	2	1,2, 3,6	5	1,3, 4
iii.	Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.	**5**	2	1,2, 3,6	5	1,3, 4

******

Marking Scheme
CS3CO33 Digital Electronics

Q.1	i)	c and d both (**1-mark award for attempt)**	**1**
	ii)	b. (0.26050)8	**1**
	iii)	c. To active the entire chip	**1**
	iv)	b. 2, 1, 2	**1**
	v)	b. Reset	**1**
	vi)	a. deterministic test patterns b. algorithmic test patterns (**A and B both correct)**	**1**
	vii)	b. They do not lose memory when power is removed	**1**
	viii)	c. A complex combinational circuit	**1**
	ix)	c. CMOS	**1**
	x)	d. 4000	**1**
Q.2	i.	1) 0001001 2) 13.5 3) 1001111 4) 001111111101	**4**
	ii.	1 mark for K-Map filling,2.5 marks for minimized expression & 2.5 marks for implementation through basic gates.	**6**
OR	iii.	6 marks for method	**6**
Q.3	i.	1.5 marks for each	**3**
	ii.	7 marks for solution	**7**
OR	iii.	7 marks for solution	**7**
Q.4	i.	1 mark for each difference	**3**
	ii.	7 marks for solution	**7**
OR	iii.	2 marks for definition, 2 marks for uses,3 marks for SISO	**7**
Q.5	i.	1 mark for meaning. 3marks drawbacks	**4**
	ii.	2 marks for definition,2 marks for application? 2 marks for difference	**6**
OR	iii.	4 marks for comparison 2 marks for applications?	**6**
Q.6			
	i.	1 mark each	**5**
	ii.	5 marks for explanation	**5**
	iii.	5 marks for explanation	**5**

******