Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem Examination Dec 2024

EC3CO24 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

			Marks	BL	PO	CO	PSO
Q.1	i.	Which step is the first step in the execution of a complete instruction? (a) Fetch (b) Decode (c) Execute (d) Write back	**1**	1	01	1	
	ii.	Which of these, is not CPU registers? (a) Accumulator (b) MAR (c) PC (d) Shift Register	**1**	1	01	2	
	iii.	The sign magnitude representation of -10 is- (a) 10001010 (b) 11111010 (c) 1010 (d) 11110101	**1**	3	03	2	
	iv.	If x is 2's complement and y is the binary number, then _____. (a) x=y (b) x=y+1 (c) x=y'+1 (d) x=y'	**1**	3	03	2	
	v.	The pipelining process is also called as _____. (a) Superscalar operation (b) Assembly line operation (c) Von Neumann cycle (d) None of these	**1**	1	01	1	
	vi.	The situation wherein the data of operands are not available is called _____. (a) Data hazard (b) Stock (c) Deadlock (d) Structural hazard	**1**	2	02	2	

P.T.O.

	vii.	In super-scalar processors, _____ mode of execution is used. (a) In-order (b) Post order (c) Out of order (d) None of these	**1**	1	01	1
	viii.	Multicore architecture is required _____. (a) To increase the performance (b) To reduce the power consumption (c) Both (a) and (b) (d) None of these	**1**	1	01	1
	ix.	Because of virtual memory, the memory can be shared among _____. (a) Processes (b) Threads (c) Instructions (d) None of these	**1**	1	01	2
	x.	The last on the hierarchy scale of memory devices is _____. (a) Main memory (b) Secondary memory (c) TLB (d) Flash drives	**1**	1	01	2
Q.2	i.	What is Von Neumann Machine Architecture?	**2**	1	01	2
	ii.	Define what is MAR and PC.	**3**	1	01	1
	iii.	Explain single bus organization with neat diagram.	**5**	1	02	2
OR	iv.	Explain Micro programmed control unit with neat diagram.	**5**	1	02	1
Q.3	i.	Explain what this ADD R1, R2, R3 instruction is doing.	**2**	3	03	2
	ii.	Compare between RISC and CISC architecture.	**3**	2	02	2
	iii.	Explain Floating point representation with one example.	**5**	2	02	3
OR	iv.	Discuss any five addressing modes.	**5**	1	02	2
Q.4		Attempt any two:				
	i.	How pipelining performance is defined? Also discuss the role of cache memory in improving the pipelining performance.	**5**	2	02	2
	ii.	What are the different type of data hazard? Explain any one data hazard in detail.	**5**	2	01	2

	iii.	Why does instruction hazard occur? What measures may be taken to avoid these hazards?	**5**	2	02	2
Q.5		Attempt any two:				
	i.	How program is different from process? Also discuss the different stages of process.	**5**	2	02	2
	ii.	What is superscalar operation? Explain with proper diagram.	**5**	2	02	1
	iii.	Explain Flynn's Taxonomy with proper diagram.	**5**	2	02	1
Q.6		Attempt any two:				
	i.	Explain the internal organization of main memory with proper diagram.	**5**	2	01	3
	ii.	What is shared memory system? Explain with diagram. Also discuss the classification of shared memory system.	**5**	2	02	2
	iii.	What is the need of cache mapping? Explain any one cache mapping technique with proper diagram.	**5**	2	02	2

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Marking Scheme

EC3CO24 Computer System Architecture

Q.1	i)	a) Fetch	**1**
	ii)	c) Shift Register	**1**
	iii)	a) 10001010	**1**
	iv)	c) x=y'+1	**1**
	v)	b) Assembly line operation	**1**
	vi)	a) Data hazard	**1**
	vii)	c) Out of order	**1**
	viii)	c) for both a and b	**1**
	ix)	a) processes	**1**
	x)	b) Secondary memory	**1**
Q.2	i.	Definition	**2**
	ii.	MAR and PC (1.5 marks each)	**3**
	iii.	Explanation 3marks diagram 2 marks	**5**
OR	iv.	Explanation 3marks diagram 2 marks	**5**
Q.3	i.	Explanation 2 marks	**2**
	ii.	Each comparison is of 0.5	**3**
	iii.	Explanation 3marks example 2 marks	**5**
OR	iv.	Each addressing modes of 1 marks	**5**
Q.4	i.	Pipelining performance definition 2.5 marks role of cache memory 2.5 marks	**5**
	ii.	type of data hazard 2 marks explanation of data hazard 3 marks	**5**
OR	iii.	Why does instruction hazard occur, 2.5 marks measures may be taken 2.5 marks	
Q.5	i.	Difference 1 marks different stages of process 4 marks	**5**
	ii.	Explanation 3marks diagram 2 marks	**5**
OR	iii.	Explanation 3marks diagram 2 marks	**5**
Q.6	i.	Explanation 3marks diagram 2 marks	**5**
	ii.	Explanation 2marks diagram 1 marks classification 2	**5**
OR	iii.	Need of cache mapping 1marks Explanation 3marks diagram 1 marks	**5**

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