*Total No. of Questions: 6* *Total No. of Printed Pages:3*

**Enrollment No.....**

Faculty of Engineering

End Sem Examination May-2023

EC3CO17 Linear Integrated Circuits & Applications

Programme: B.Tech. Branch/Specialisation: EC

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which is not the internal circuit of operational amplifier? **1**

(a) Differential amplifier (b) Level translator

(c) Output driver (d) Clamper

ii. Which of the following is not preferred for input stage of Op-amp? **1**

(a) Dual input balanced output

(b) Differential input single ended output

(c) Cascaded DC amplifier

(d) Single input differential output

iii. When does the op-amp said to operate in common-mode configuration? **1**

(a) When the input voltage are equal

(b) When input voltage is equal to the output voltage

(c) When same voltage is applied to both input terminal of an op-amp

(d) When different voltage is applied to both input and terminal of an op-amp

iv. Define the common-mode rejection ratio (CMRR) of op-amp. **1**

(a) CMRR=$A_D/A_{CM}$ (b) CMRR=$A_{CM}/ A_D$

(c) CMRR=$V_{OCM}/A_{CM}$ (d) CMRR=$A_D*A_{CM}$

v. Filters are classified as- **1**

(a) Analog or digital (b) Passive or active

(c) Audio or radio frequency (d) All of these

P.T.O.

vi. Find out the incorrect statement about active and passive filters. **1**
(a) Gain is not attenuated in active filter
(b) Passive filters are less expensive
(c) Active filter does not cause loading of source
(d) Passive filters are difficult to tune or adjust

vii. How to overcome mistriggering on the positive pulse edges in the monostable circuit? **1**
(a) Connect a RC network at the input
(b) Connect an integrator at the input
(c) Connect a differentiator at the input
(d) Connect a diode at the input

viii. A monostable multivibrator has R = 120kΩ and the time delay T = 1000ms, calculate the value of C? **1**
(a) 0.9µF (b) 1.32µF (c) 7.5µF (d) 2.49µF

ix. Which is not considered as a linear voltage regulator? **1**
(a) Fixed output voltage regulator
(b) Adjustable output voltage regulator
(c) Switching regulator
(d) Special regulator

x. To get a maximum output current, IC regulation are provided with- **1**
(a) Radiation source (b) Heat sink
(c) Peak detector (d) None of these

Q.2 i. What are the characteristics of ideal Op-Amp? **2**
ii. Why is the current mirror circuit used in differential amplifier stage? **3**
iii. Draw and explain the configuration of current follower. **5**
OR iv. Define following terms related to Op-Amp: slew rate, CMRR and Offset voltage. **5**

Q.3 i. Define feedback amplifier with its type. **2**
ii. Derive mathematical expression for voltage gain in non-inverting amplifier configuration. **8**
OR iii. Explain the operation of triangular wave generator. **8**



Q.4 i. List various characteristics of Op-Amp filter. **3**
ii. Explain the purpose and operation of an Op-Amp low-pass filter. Draw the circuit diagram and explain how the components are chosen to achieve the desired cutoff frequency. **7**
OR iii. Demonstrate a clear understanding of Chebyshev filter, its operation, and applications. **7**

Q.5 i. How does a 555-timer work? **4**
ii. Derive expression to calculate the upper and lower threshold voltages of a Schmitt trigger circuit? **6**
OR iii. How do you calculate the output waveform of a clipper circuit for an input waveform and clipping level? **6**

Q.6 Attempt any two:
i. What are the advantages and disadvantages of using a series regulator over a shunt regulator and vice versa? **5**
ii. What are some common causes of poor line and load regulation, and how can they be mitigated? **5**
iii. How do you calculate the ripple voltage in an unregulated power supply? **5**

******

# Scheme of Marking

Faculty of Engineering
End Sem Examination May-2023
EC3CO17 Linear Integrated Circuit and Applications
Programme: B.Tech. | Branch/Specialisation:EC/EI

**Note: The Paper Setter should provide the answer wise splitting of the marks in the scheme below.**

| | | | |
|---|---|---|---|
| Q.1 | i) | D | 1 |
| | ii) | C | 1 |
| | iii) | C | 1 |
| | iv) | A | 1 |
| | v) | D | 1 |
| | vi) | B | 1 |
| | vii) | C & A | 1 |
| | viii) | C | 1 |
| | ix) | C | 1 |
| | x) | B | 1 |
| | | | |
| Q.2 | i. | At Least four Characteristics 0.5 marks each | 2 |
| | ii. | 1 marks diagram 2 marks explanation | 3 |
| | iii. | ~~2+3~~ 1-Marks Circuit dia, 4 explanation | 5 |
| OR | iv. | ~~1.5+1.5+2~~ CMRR-2 marks, PSR-1.5. OV-1.5 | 5 |
| | | | |
| Q.3 | i. | 1+1 dyition + type | 2 |
| | ii. | 2+6 | 8 |
| OR | iii. | 2+6 | 8 |
| | | | |
| Q.4 | i. | ~~Draw~~ atleast 3 Characteristics | 3 |
| | ii. | ~~3+1+3~~. Purpose - 2, dia - 1, operation 3, 1- design | 7 |
| OR | iii. | 2+3+2 | 7 |
| | | | |
| Q.5 | i. | 1- diagram, 3 explanation. | 4 |



| | | | |
|---|---|---|---|
| | ii. | 3+3 1-dia, explanation ~~3~~ 3.5 marks. 3.5 for derivation | 6 |
| OR | iii. | ~~3+3~~ 3 marks explanation, 1 marks diagram 1.5 + 1.5 Cases. | 6 |
| | | | |
| Q.6 | | | |
| | i. | 2.5 + 2.5 | 5 |
| | ii. | 2.5 + 2.5 | 5 |
| | iii. | ~~2.6~~ + 2.5 | 5 |

******