

Total No. of Questions: 6

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Enrollment No.....



Faculty of Engineering
End Sem Examination May-2023
EC3EL08 Computer Organization & Architecture
Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs.

Maximum Marks: 60

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

- Q.1 i. Which of the following is not a type of computer on the basis of operation? **1**
(a) Remote (b) Hybrid (c) Analog (d) Digital
- ii. Which of the following is not a characteristic of a computer? **1**
(a) Diligence (b) I.Q. (c) Accuracy (d) Versatility
- iii. In which processor, multiple tasks are performed in single instruction- **1**
(a) RISC (b) CISC (c) Both (a) and (b) (d) None of these
- iv. In the case of Zero-address instruction method, the operands are stored in _____. **1**
(a) Registers (b) Accumulators
(c) Push down stack (d) Cache
- v. Whenever the data is found in the cache memory it is called as _____. **1**
(a) HIT (b) MISS (c) FOUND (d) ERROR
- vi. Which of the following is not a write policy to avoid Cache Coherence? **1**
(a) Write through (b) Write within
(c) Write back (d) Buffered write
- vii. When the processor executes multiple instructions at a time it is said to use _____. **1**
(a) Single issue (b) Multiplicity
(c) Visualization (d) Multiple issues
- viii. In super-scalar processors, _____ mode of execution is used. **1**
(a) In-order (b) Post order
(c) Out of order (d) None of these

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- ix. Any electronic holding place where data can be stored and retrieved later whenever required is _____. **1**
(a) Memory (b) Drive (c) Disk (d) Circuit
- x. What is the location of the internal registers of CPU? **1**
(a) Internal (b) On-chip (c) External (d) Motherboard

- Q.2 Attempt any two: **5**
- i. What are the functional units and components of computer organization? Explain it. **5**
- ii. Discuss the fundamental concept of instruction execution. **5**
- iii. What are the four main components available in a micro programmed control unit? Explain it. **5**
- Q.3 Attempt any two: **5**
- i. How to convert binary representation to fixed-point representation? **5**
- ii. Can you compare floating-point values for equality? Justify it. **5**
- iii. What is the difference between RISC and CISC instruction format? **5**
- Q.4 Attempt any two: **5**
- i. How Does CPU Cache Work? What are L1, L2, and L3 Cache? **5**
- ii. How do you calculate pipeline performance? Explain it. **5**
- iii. What is data instruction hazards in computer architecture? **5**
- Q.5 Attempt any two: **5**
- i. Is pipelining a superscalar technique? **5**
- ii. What is the difference between scalar and superscalar pipeline? **5**
- iii. What type of architecture is multicore? How many threads are in a core? **5**
- Q.6 Attempt any two: **5**
- i. What is the internal organization of semiconductor memory? **5**
- ii. What are the different classification of memory? **5**
- iii. Differentiate uniform memory Access (UMA) and non-uniform memory access (NUMA). **5**

MCQ

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Q.1

- (i) Remote
- (ii) I.Q.
- (iii) CISC
- (iv) Push Down stack.
- (v) HIT
- (vi) write within
- (vii) Multiple issues.
- (viii) out of order
- (ix) Disc
- (x) on-chip

Q.2

- (i) function unit - 2
Components of comp. - 3
- (ii) ~~full~~ Diagram - 1.5
Control function - 2, Explain - 1.5
- (iii) Diagram - 2
Explanation - 3

Q.3

- (i) Single & Double precision with example - 2.5 each
- (ii) (i) Explanation 5 marks with Example
- (iii) 5-differences, carry each one marks.

Q.4

- (i) Working reason - 2 marks.
L1, L2, L3 each - 1 marks.
- (ii) Explanation with Example - 5 marks
- (iii) Definition - 2 marks
Types carry each - 1 marks (3 marks for each)

- Q.5
- (i) Explanation - 5 marks
 - (ii) 5 differences carries one marks each.
 - (iii) Types - 2.5 marks
 - Thread explanation - 2.5 marks

Q.6

- (i) Diagram - 2 marks
- Explanation - 3 marks
- (ii) Explanation - 5 marks
- (iii) 5 differences carries one marks each.