Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination May-2023
IT3CO32 Microprocessor & Microcontroller

Programme: B.Tech. Branch/Specialisation: IT

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which of the following are the components of a microprocessor? **1**
(a) ALU (b) Register array
(c) Control unit (d) All of these

ii. Which of the following sequence that a microprocessor follows? **1**
(a) Fetch, decode, execute (b) Fetch, execute, decode
(c) Decode, fetch, execute (d) Execute, decode, fetch

iii. Which is used to store critical piece of data during subroutines and interrupts- **1**
(a) Stack (b) Queue (c) Accumulator (d) Data register

iv. The 1 MB byte of memory can be divided into _____. **1**
(a) 64 Kbyte (b) 33 Kbyte
(c) 34 Kbyte (d) None of these

v. In 8257 (DMA) each of the four channels has- **1**
(a) A pair of two 8-bit registers (b) A pair of two 16-bit register
(c) One 16-bit register (d) One 8-bit register

vi. In 8251A, the pin that controls the rate at which the character is to be transmitted is- **1**
(a) TXC (active low) (b) TXC (active high)
(c) TXD (active low) (d) TXD (active high)

vii. The internal RAM memory of the 8051 is- **1**
(a) 32 bytes (b) 64 bytes (c) 128 bytes (d) 256 bytes

viii. Which of the following instruction will move the contents of the accumulator to register 6? **1**
(a) MOV 6R, A (b) MOV R6, A
(c) MOV A, 6R (d) MOV A, R6

P.T.O.

ix. Which processors include multi-clocks? **1**
(a) Complex instruction set computer
(b) Reduced instruction set computer
(c) ISA
(d) ANNA

x. ARM processors were basically designed for- **1**
(a) Main frame system (b) Distributed system
(c) Mobile system (d) Super computers

Q.2 i. Explain the addressing modes of 8085 microprocessor. **2**
ii. Explain the de-multiplexing of address/data in 8085. **3**
iii. Explain in detail concept of memory I/O device interfacing. **5**
OR iv. How does the microprocessor differentiate between data and instruction? Also define instruction cycle. **5**

Q.3 i. Describe interrupt vector table of 8086 microprocessor. **2**
ii. Explain the architecture of 8086 microprocessor and also explain which factor helps the speed up operation of 8086 microprocessor. **8**
OR iii. Explain the minimum mode configuration and flag register of 8086 microprocessor. **8**

Q.4 i. Explain the modes of DMA transfer. **3**
ii. Discuss the organization and architecture of USART with a functional block diagram. **7**
OR iii. List the difference between 8253 and 8254 also give the interfacing scheme of 8257 with 8086. **7**

Q.5 i. Explain data transfer instruction set of 8051. **4**
ii. Explain the memory organization and interrupt of 8051. **6**
OR iii. With the help of block diagram explain the architecture, features and addressing modes of 8051. **6**

Q.6 Attempt any two:
i. Write down the salient features of 80286, 80386, 80486 and Pentium microprocessor. **5**
ii. Explain the concept of RISC and CISC in detail. **5**
iii. Explain the ARM instruction set architecture with example. **5**

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Marking Scheme

IT3CO32 [T]- Microprocessor & Microcontroller

Q.1	i)	(d) All the above	**1**
	ii)	(a) fetch, decode, execute	**1**
	iii)	(a) Stack	**1**
	iv)	(b) 64 Kbyte	**1**
	v)	(b) a pair of two 16-bit register	**1**
	vi)	(a) TXC (active low)	**1**
	vii)	(c) 128 bytes	**1**
	viii)	(b) MOV R6, A	**1**
	ix)	(a) Complex instruction set computer	**1**
	x)	(c) Mobile system	**1**
Q.2	i.	Elaborate the addressing modes of 8085 microprocessor system.	**2**
	ii.	Draw the block diagram of Central processing unit suitable diagram?	**3**
	iii.	Explain the concept of memory I/O device interfacing?	**5**
OR	iv.	Write down the difference between data and instruction? 4 marks Also define instruction cycle.1 marks	**5**
Q.3	i.	Explain interrupt vector concept in 8086 microprocessors.	**2**
	ii.	Explain the architecture of 8086 microprocessor with operations. Diagram – 4 Marks Operation - 4 Marks .	**8**
OR	iii.	Define minimum mode configuration and flag register of 8086 microprocessor. minimum mode- 5 Marks Flag register- 3 Marks	**8**
Q.4	i.	Explain the modes of DMA transfer or controller.	**3**
	ii.	Explain architecture of USART with a functional block diagram. Architecure ----3 marks Explanation- 4 marks	**7**
OR	iii.	Write down the difference between 8053 and 8254 also give the interfacing scheme of 8257 with 8086.	**7**

Differences 8053 & 8254 - 2 Marks
8257 interfacing schemes- 5 Marks

Q.5	i.	Enlist the data transfer instruction set with example of 8051.	**4**
	ii.	Explain the memory organization and interrupt of 8051. 8051 Memory organization - 3 Marks Interrupt 8051 - 3 Marks	**6**
OR	iii.	Explain the architecture 2 Marks, features 2 Marks. and addressing modes of 8051. 2 Marks	**6**
Q.6			
	i.	Write down the salient features of 80286, 80386, 80486 and Pentium microprocessor.	**5**
	ii.	Define RISC and CISC in detail. 2.5 Marks Each	**5**
	iii.	Explain the ARM instruction set architecture 3 Marks. with example. 2 Marks	**5**

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