Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2019

IT3CO20 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: IT

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Controller of computer system transfers data from device to **1**
(a) Cache (b) Registers (c) Indexes (d) Buffers

ii. ISP stands for _____ **1**
(a) Instruction Set Processor
(b) Information Standard Processing
(c) Interchange Standard Protocol
(d) Interrupt Service Procedure

iii. In case of, Zero-address instruction method the operands are stored in _____ **1**
(a) Registers (b) Accumulators
(c) Push down stack (d) Cache

iv. A _____ gate is used to detect the occurrence of an overflow. **1**
(a) NAND (b) XOR (c) XNOR (d) AND

v. The approach where the memory contents are transferred directly to the processor from the memory is called _____ **1**
(a) Read-later (b) Read-through
(c) Early-start (d) None of these

vi. _____ is the bottleneck, when it comes computer performance. **1**
(a) Memory access time (b) Memory cycle time
(c) Delay (d) Latency

vii. In DMA transfers, the required signals and addresses are given by the **1**
(a) Processor (b) Device drivers
(c) DMA controllers (d) The program itself

P.T.O.

viii. When the R/W bit of the status register of the DMA controller is set to 1. **1**
(a) Read operation is performed
(b) Write operation is performed
(c) Read & Write operation is performed
(d) None of these

ix. To increase the speed of memory access in pipelining, we make use of _____ **1**
(a) Special memory locations (b) Special purpose registers
(c) Cache (d) Buffers

x. The situation where in the data of operands are not available is called _____ **1**
(a) Data hazard (b) Stock
(c) Deadlock (d) Structural hazard

Q.2 i. Draw and explain block diagram of general purpose register architecture of CPU. **2**

ii. What is instruction cycle? Explain different phases of instruction cycle and show flow chart for instruction cycle. **3**

iii. What is the need of Von Neumann Model in computer system organization? **5**

OR iv. How Register Transfer Language work is in computer system explain in detailed? **5**

Q.3 i. Evaluate (A+B)*(C+D) by one address, two address and three address. **2**

ii. Explain the working principal of micro program sequencer with neat block diagram. **8**

OR iii. What is the difference between Microprogrammed and hardwired control unit? **8**

Q.4 i. Explain floating point representation with example. **3**

ii. Explain booth's algorithm. Show the step by step multiplication using Booth's algorithm to multiply the number (+15) and (-13) in binary. **7**

OR iii. How cache is used in cache organization. Explain mapping techniques With the help of diagram? **7**

Q.5 i. Explain DMA controller with block diagram. What is meant by block transfer. **4**

ii. Explain handshaking method of asynchronous data transfer with diagram. **6**

OR iii. What is the basic concept of bus control and how does it works? **6**

Q.6 Attempt any two:

i. Discuss Arithmetic and Instruction pipelines. **5**

ii. Discuss all factor which affect the performance of pipelining processor based systems. **5**

iii. Explain the terms Array and vector processor. **5**

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Marking Scheme
IT3CO20 Computer System Architecture

Q.1	i.	Controller of computer system transfers data from device to (d) Buffers	**1**
	ii.	ISP stands for _____ (a) Instruction Set Processor	**1**
	iii.	In case of, Zero-address instruction method the operands are stored in _____ (c) Push down stack	**1**
	iv.	A _____ gate is used to detect the occurrence of an overflow. (b) XOR	**1**
	v.	The approach where the memory contents are transferred directly to the processor from the memory is called _____ (c) Early-start	**1**
	vi.	_____ is the bottleneck, when it comes computer performance. (b) Memory cycle time	**1**
	vii.	In DMA transfers, the required signals and addresses are given by the (c) DMA controllers	**1**
	viii.	When the R/W bit of the status register of the DMA controller is set to 1. (a) Read operation is performed	**1**
	ix.	To increase the speed of memory access in pipelining, we make use of _____ (c) Cache	**1**
	x.	The situation where in the data of operands are not available is called _____ (a) Data hazard	**1**
Q.2	i.	General purpose register architecture of CPU.	**2**
		Diagram 1 mark	
		Explanation 1 mark	
	ii.	Instruction cycle 1 mark	**3**
		Phases of instruction cycle 1 mark	
		Flow chart for instruction cycle. 1 mark	
	iii.	Need of Von Neumann Model in computer system organization	**5**
		1 mark for each (1 mark * 5)	
OR	iv.	Register Transfer Language work is in computer system	**5**
		1 mark for each (1 mark * 5)	
Q.3	i.	(A+B)*(C+D) by one address, two address and three address.	**2**
		Formula 1 mark	
		Solution 1 mark	
	ii.	Working principal of micro program sequencer 5 marks	**8**
		Block diagram. 3 marks	
OR	iii.	Difference between Microprogrammed and hardwired control unit	**8**
		2 marks for each point (2 marks * 4)	
Q.4	i.	Floating point representation 2 marks	**3**
		Example 1 mark.	
	ii.	Booth's algorithm 2 marks	**7**
		Step by step multiplication using Booth's algorithm 2 marks	
		Final result 3 marks	
OR	iii.	Cache is used in cache organization	**7**
		1 mark for each point (1 mark * 4) 4 marks	
		Mapping techniques with diagram	
		1 mark for each (1 mark * 3) 3 marks	
Q.5	i.	DMA controller with block diagram	**4**
		0.5 mark for each (0.5 mark * 4) 2 marks	
		Block transfer	
		0.5 mark for each (0.5 mark * 4) 2 marks	
	ii.	Handshaking method of asynchronous data transfer	**6**
		0.75 mark for each point (0.75 mark * 6) 4.5 marks	
		Diagram. 1.5 marks	
OR	iii.	Basic concept of bus control 3 marks	**6**
		Its working 3 marks	
Q.6		Attempt any two:	
	i.	Arithmetic 2.5 marks	**5**
		Instruction pipelines. 2.5 marks	
	ii.	Factor which affect the performance of pipelining processor	**5**
		0.5 mark for each point (0.5 mark * 10)	
	iii.	Array processor. 2.5 marks	**5**
		Vector processor. 2.5 marks	

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