Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem Examination May-2023

EC3CO12 VLSI Design

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. In MOSFET devices the N-channel type is better than the P – Channel type in the following respect- **1**

(a) It has better immunity (b) It is Faster

(c) It is TTL compatible (d) It has better drive capability

ii. How many TG are required to implement 4 x 1 mux? **1**

(a) 3 (b) 4 (c) 5 (d) 6

iii. In the CMOS inverter circuit if the transconductance parameters of NMOS and PMOS transistor are $Kn=Kp=\mu nC_{OX}Wn/Ln=\mu pC_{OX}Wp/Lp=$ 40 $\mu A/V^2$ and threshold voltages are $VT = 1V$, V_{GS}=2.5V, V_{DD}=5 V then the current I_D is- **1**

(a) 0 A (b)25 µA (c) 45 µA (d) 90 µA

iv. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? **1**

(a) Static dissipation (b) Dynamic dissipation

(c) Both (a) and (b) (d) Open Circuit dissipation

v. Two states are said to be equivalent states if they have exactly same- **1**

(a) Inputs (b) Next state (c) Output (d) Both (b) and (c)

vi. In a sequence detector, if the required bit is at its input while checking the sequence bit by bit, the detector moves to- **1**

(a) Previous state (b) Next state

(c) present state (d) Null state

vii. If there are 7 states in any sequential circuit, then its merger table will contain _____ squares(cells). **1**

(a) 10 (b) 11 (c) 21 (d) 20

P.T.O.

viii. When a circuit goes through a unique sequence of unstable states then it is called as- **1**
(a) Hazards (b) Glitch (c) Cycle (d) Race

ix. In modern ICS _____ is used as gate material. **1**
(a) Polysilicon (b) Si (c) Cu (d) Al

x. Which gives scalable design rules? **1**
(a) Micron rules (b) Layer rules
(c) Thickness rules (d) Lambda rules

Q.2 i. What is body effect? **2**

ii. Explain the term pass transistor with example. **3**

iii. Explain the operation of negative edge-triggered register using complementary switch. **5**

OR iv. Describe the equation for source to drain current in the three regions of operation of a PMOS transistor and draw the VI characteristics. **5**

Q.3 i. Define rise time, fall time and propagation delay. **3**

ii. What is PDP? Derive expression for dynamic power dissipation. **7**

OR iii. Draw and explain the DC characteristics of a CMOS inverter with necessary conditions for the different regions of operation. **7**

Q.4 i. Discuss mealy to moore machine conversion with example. **4**

ii. Design a sequence detector which detects sequence "0110" for input X and produce output Z as '1'. Realize the hardware (overlapping allowed). **6**

OR iii. Determine the minimal state table equivalent to the following using merger graph method: **6**

Present State	Next state, output	
	X = 0	X = 1
A	B,0	C,1
B	A,1	E,0
C	D,0	A,1
D	C,1	E,0
E	A,1	F,0
F	E,0	F,1

Q.5 i. What is fundamental mode & pulse mode operation? **2**

ii. What do you mean by race? Explain types of races with proper example. **3**

iii. Find race free state assignment for following flow table: **5**

(a)	c	d	(a)
a	d	(b)	(b)
d	(c)	b	a
(d)	(d)	(d)	b

OR iv. What is hazard? Find the circuit that has no static hazards and implement the Boolean function $F(A,B,C,D)=\sum m(1,5,6,7)$. **5**

Q.6 Attempt any two:

i. Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. **5**

ii. Describe architecture of FPGA. **5**

iii. What are layout design rules? Design the layout of CMOS inverter with suitable design rules. **5**

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9/05/23

Scheme of Marking

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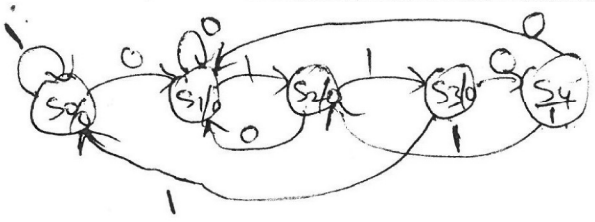
e: The Paper Setter should provide the answer wise splitting of the marks in scheme below.

1	i)	(b) It is Faster	1
	ii)	(d) 6	1
	iii)	(c) 45 μA	1
	iv)	(b) Dynamic dissipation	1
	v)	d. both b and c	1
	vi)	b. Next state	1
	vii)	(c) 21	1
	viii)	(c) cycle	1
	ix)	(a) Polysilicon	1
	x)	(d) lambda rules	1
2	i.	definition	2
	ii.	definition	1.5,1.5
	iii.	diagram & working	2.5,2.5
R	iv.	diagram & working	2.5,2.5
3	i.	Each definition	3
	ii.	Definition & derivation	3,4
R	iii.	Characteristics & diagram with equations	3,2,2
4	i.	Conversion with example	2,2
	ii.	Solution with hardware	3,3

Q.4(iii)



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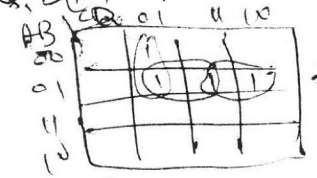
OR	iii.	PS | NS X=0 X=1 | Z X=0 X=1 A | B A | 0 1 B | A E | 1 0 E | A F | 1 0 F | E F | 0 1 A ≡ C B ≡ D	3,3
Q.5	i.	definition	2
	ii.	Race with example	3
	iii.	solution	5
OR	iv.	Definition & solution	2,3
Q.6			
	i.	Steps & diagram	2,3
	ii.	Architecture diagram & explanation	2,3
	iii.	Definition &design	2,3

Q.5(iv) $f = \Sigma m(1,5,6,7)$ ******



$\Rightarrow f = A'c'D + A'BD + ABC$

Hazard free.

Q.5-(iii)

	00	01	11	10
0	a	d	(g)	c
1	b	(f)		(e)

(i) d↔c via(g)
(ii) d↔b via(f)
(iii) c↔b via(e)