

Enrollment No.....



Programme: B.Tech.

Branch/Specialisation: EE

Faculty of Engineering

End Sem Examination Dec 2024

EE3CO57 Analog & Digital Circuits

Duration: 3 Hrs.**Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

		Marks	BL	PO	CO	PSO
Q.1	i. The battery connection required to forward bias a p-n junction is:	1	01	01	01	01
	(a) +ve terminal to p and -ve terminal to n (b) -ve terminal to p and +ve terminal to n (c) -ve terminal to p and -ve terminal to n (d) None of these					
	ii. The optical signals are detected by:	1	01	01	01	01
	(a) Photo diode (b) Zener diode (c) PIN diode (d) GUNN diode					
	iii. If an emitter current is changed by 4mA, the collector current changes by 3.5mA. the value of β will be:	1	03	01	03	02
	(a) 7 (b) 0.875 (c) 0.5 (d) 3.5					
	iv. The frequency response of RC coupling is:	1	01	01	01	01
	(a) Good (b) Very good (c) Excellent (d) Poor					
	v. Which of the following statement is correct for JFET?	1	02	01	02	01
	(a) The JFET is mostly referred to as a depletion mode device (b) The JFET is usually ON when there is no potential difference between the gate and source terminal (c) The JFET has small input impedance (d) None of these					

Marking Scheme

EE3CO57 (T) Analog & Digital Circuits (T)

				Explain the criteria under which a transistor works as an amplifier and an oscillator. 4 marks			
Q.1	i)	(a) +ve terminal to p and -ve terminal to n	1	Q.4	i.	State De Morgan Laws. Explain NAND and NOR DTL gates.	1 mark 2 marks on each
	ii)	(a) photo diode	1		ii.	Why is a FET called voltage-controlled device advantages of MOSFET compared to a normal FET?	3 marks 4 marks
	iii)	(a) 7	1	OR	iii.	Working construction of MOSFET draws its characteristics.	3 marks 2 marks 2 marks
	iv)	(d) poor	1	Q.5	i.	Theorems properties of Boolean Algebra.	2 marks 2 marks
	v)	(b) the JFET is usually ON when there is no potential difference between the gate and source terminal.	1		ii.	What is full adder implement full adder using two half adders.	3 marks 3 marks
	vi)	(c) Narrow P-channel MOSFET	1	OR	iii.	Design 16:1 multiplexer using 8:1 multiplexer. (1 marks on each step)	6
	vii)	(b) 3 bits	1				
	viii)	(c) NAND gates	1	Q.6	i.	difference between flip-flop and latch (1 marks on each step)	5
	ix)	(d) binary data	1		ii.	random-access memory and read-only memory.	5
	x)	(c) Static shift register	1		iii.	Differentiate between ripple counters and synchronous counters. (1 mark on each step)	5
Q.2	i.	Explain the formation of depletion region in a PN Junction diode.	2				
	ii.	PN diode in forward bias	1.5 marks	3			
		PN diode in reverse bias	1.5 marks				
	iii.	Derive an expression for I_{dc} and I_{rms} half wave rectifier circuit find its maximum efficiency.	2.5 2.5	5			
OR	iv.	Explain the operation of tunnel diode with suitable V-I characteristics energy band diagrams.	2.5 marks 2.5 marks	5		*****	
Q.3	i.	thermal runaway	1 mark	2			
		thermal stability	1 mark				
	ii.	Explain RC coupled amplifier	3 marks	8			
		Diagram	2 marks				
		Application	3 marks				
OR	iii.	different regions	4 marks	8			