Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination Dec-2023
RA3CO26 Digital Electronics

Programme: B.Tech. Branch/Specialisation: RA

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. The given hexadecimal number $(1E.53)_{16}$ is equivalent to which of the following Octal number- **1**
(a) $(35.684)_8$ (b) $(36.246)_8$ (c) $(34.340)_8$ (d) $(35.599)_8$

ii. According to Boolean law: A + 1 = _____? **1**
(a) 1 (b) A (c) 0 (d) A'

iii. In RTL NOR gate, the output is at logic 1 only when all inputs are at- **1**
(a) logic 0 (b) logic 1 (c) +10V (d) Floating

iv. Which insulating layer used in the fabrication of MOSFET? **1**
(a) Aluminium oxide (b) Silicon nitride
(c) Silicon dioxide (d) Aluminium nitrate

v. Total number of inputs in a half adder is _____. **1**
(a) 2 (b) 3 (c) 4 (d) 1

vi. In a multiplexer, the selection of a particular input line is controlled by _____. **1**
(a) Data controller (b) Selected lines
(c) Logic gates (d) Both (a) and (b)

vii. In digital logic, a counter is a device which _____. **1**
(a) Counts the number of outputs
(b) Stores the number of times a particular event or process has occurred
(c) Stores the number of times a clock pulse rises and falls
(d) Counts the number of inputs

viii. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories. **1**
(a) 2 (b) 3 (c) 4 (d) 5

ix. The first step in the design of memory decoder is _____. **1**
(a) Selection of a EPROM (b) Selection of a RAM
(c) Address assignment (d) Data insertion

x. ROM consist of _____. **1**
(a) NOR and OR arrays (b) NAND and NOR arrays
(c) NAND and OR arrays (d) NOR and AND arrays

Q.2 i. Convert $(ABF)_{16}$ to base 2 and base 8 system. **2**

ii. What is Boolean algebra? Explain with their basic theorems. **3**

iii. Perform the subtraction of binary numbers using 1's complement and 2's complement- **5**
(a) 10101-1101 (b) 1110-1010

OR iv. Minimize the following using K-map Y1=Σm(0,1,3,5,9)+Σd(2,6,7). **5**

Q.3 i. Define transistor as switch with suitable diagram. **4**

ii. Explain the working of PMOS and NMOS transistor with suitable diagram. **6**

OR iii. Classify TTL Logic and explain any one of them with suitable diagram. **6**

Q.4 Attempt any two:

i. Explain full adder with diagram using two half adder and truth table. **5**

ii. What is demultiplexer? Draw and explain 8*1 multiplexer with truth table. **5**

iii. Explain 2-Bit magnitude comparator with suitable diagram and truth table. **5**

Q.5 i. What is SR Latch? Define setup time and hold time. **4**

ii. What is Ripple Counter? Explain Johnson counter with its logic and timing diagram. **6**

OR iii. Explain JK Flip-Flop with suitable diagram. What was the problem in RS Flip-Flop which is solved in JK Flip-Flop? **6**

Q.6 Attempt any two:

i. Compare RAM and ROM. (any five comparison) **5**

ii. What is PAL? Explain with its block diagram and logic circuit. **5**

iii. Explain internal construction and memory decoding process in detail. **5**

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Marking Scheme

RA3CO26 (T)-Digital Electronics

Q.1	i.	The given hexadecimal number $(1E.53)_{16}$ is equivalent to which of the following Octal number b) **$(36.246)_8$**	**1**
	ii.	According to Boolean law: A + 1 = ? a) **1**	**1**
	iii.	In RTL NOR gate, the output is at logic 1 only when all the inputs are at a) **logic 0**	**1**
	iv.	Which insulating layer used in the fabrication of MOSFET? c) **Silicon dioxide**	**1**
	v.	Total number of inputs in a half adder is _____ a) **2**	**1**
	vi.	In a multiplexer, the selection of a particular input line is controlled by _____ b) **Selected lines**	**1**
	vii.	In digital logic, a counter is a device which _____ b) **Stores the number of times a particular event or process has occurred**	**1**
	viii.	Based on how binary information is entered or shifted out, shift registers are classified into _____ categories. c) 4	**1**
	ix.	The first step in the design of memory decoder is _____ c) **Address assignment**	**1**
	x.	ROM consist of _____ c) **NAND and OR arrays**	**1**

Q.2	i.	1 Mark for each conversion	**1+1**
	ii.	Definition 1 Mark ? Explanation of basic theorems 2 Marks	**1+2**
	iii.	**2**.5 marks for each solution a) 10101-1101 b) 1110-1010	**2.5+2.5**
OR	iv.	Minimization 5 marks $Y1=\Sigma m(0,1,3,5,9)+\Sigma d(2,6,7)$	**5**
Q.3	i.	Definition 3 Mark diagram 1 Mark	**3+1**
	ii.	Working of PMOS and NMOS transistor 3 Marks each	**3+3**
OR	iii.	Classification 1 Mark explanation 3 Mark with suitable diagram 2 Mark	**1+3+2**
		Attempt any two:	
Q.4	i.	Explanation of Full Adder 2 Mark, diagram 1 Mark and truth table 2 Mark	**2+1+2**
	ii.	Demultiplexer definition 2 Mark explaination of 8*1 multiplexer with truth table 3 Mark	**2+3**
	iii.	Explaination 1.5 Marks diagram 1.5 Marks and truth table 5 Marks	**1+2+2**
Q.5	i.	Definition of SR Latch 2 Marks Definition of setup time 1Mark and Definition of hold time 1 mark	**2+2**
	ii.	Definition of Ripple Counter 2 Marks Explanation of Johnson counter 2 Marks logic and timing diagram 1 Marks each	**2+2+2**
OR	iii.	Explanation of JK Flip-Flop 3 Mark diagram of 1 Mark. Reason 2 Marks	**3+1+2**
Q.6		Attempt any two:	

i. 1 mark for each comparison (Any 5 comparison) **5**

ii. Definition of PAL 2 Marks its block diagram 2 Marks and logic circuit 1 Mark **2+2+1**

iii. Internal construction **2.5** memory decoding process **2.5 narks** **2.5+2.5**

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