Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination May-2023
EC3EV05 VLSI for Wireless Communication

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. The effects of small-scale multipath propagation are- **1**
(a) Changes in signal strength
(b) Random frequency modulation
(c) Time dispersion
(d) All of these

ii. QPSK system uses a phase shift of- **1**
(a) Π (b) Π /2 (c) Π /4 (d) 2 Π

iii. LNA's are placed at- **1**
(a) Transmitter back end (b) Receiver back end
(c) Receiver front end (d) Transmitter Front End

iv. The "front end" of a receiver can include- **1**
(a) The tuner (b) The RF amplifier
(c) The mixer (d) All of these

v. Insertion loss in dB are given by- **1**
(a) dB=10log(Pi/Po) (b) dB=10log(Po/Pi)
(c) dB=10log(Pi/Pi-Po) (d) dB=10log(Po/Pi-Po)

vi. What is the purpose of the tuned circuit? **1**
(a) Local oscillator
(b) Amplify RF signals
(c) Mix oscillator and input signals
(d) Select desired signal and reject all others

vii. What is SNR of 10 bit Ideal ADC? **1**
(a) 51.34 dB (b) 71.67 dB (c) 81.96 dB (d) 61.96 dB

P.T.O.

viii. Which one is fastest ADC? **1**
(a) Dual slope ADC (b) Flash ADC
(c) Counter ramp ADC (d) Successive approximation ADC

ix. The output voltage of phase detector is- **1**
(a) Phase voltage (b) Free running voltage
(c) Error voltage (d) None of these

x. An oscillator can stop working when there is- **1**
(a) Elimination of triggered pulses
(b) An increase in transistor gain
(c) Reduction in transistor gain
(d) No change in transistor gain

Q.2 i. Define term frequency reuse. **2**
ii. Explain Fading & its types. **3**
iii. Explain Non-ideal effects in MOSFFT. **5**
OR iv. Explain BPSK modulator. **5**

Q.3 i. Why do we need a receiver front end? **3**
ii. What are the objectives of matching network in LNA? Elaborate parameters of LNA. **7**
OR iii. Describe RF receiver using heterodyne architecture. **7**

Q.4 i. Explain different types of feedthrough. **4**
ii. Discuss CMOS based single balanced mixer. **6**
OR iii. Describe operation of Gilbert mixer. **6**

Q.5 i. Define resolution, quantization error & throughput in ADC. **3**
ii. Explain SAR ADC. **7**
OR iii. Describe binary weighted DAC. **7**

Q.6 Attempt any two:
i. Explain working of Phase Detector. **5**
ii. Describe functioning of VCO. **5**
iii. Elaborate operating principle of Ring Oscillator. **5**

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Marking Scheme

EC3EV05[T]- VLSI for Wireless Communication

Q.1	i)	d) All of these	**1**
	ii)	b) Π /2	**1**
	iii)	**c) More than one stages**	**1**
	iv)	d) all of the above	**1**
	v)	a) dB=10log(Pi/Po)	**1**
	vi)	d) select desired signal and reject all others	**1**
	vii)	d) 61.96 dB	**1**
	viii)	b) Flash ADC	**1**
	ix)	c) Error voltage	**1**
	x)	c) Reduction in transistor gain	**1**
Q.2	i.	Definition.	**2**
	ii.	Fading & its types	**3**
	iii.	derivation	**5**
OR	iv.	Working & diagram	**3,2**
Q.3	i.	Reasons for receiver front end requirment.	**3**
	ii.	Explanation about objectives of matching network & parameters of LNA.	**3,4**
OR	iii.	illustrate RF receiver with neat diagram.	**3,4**
Q.4	i.	explain	**4**
	ii.	Explanation with neat diagram	**3,3**
OR	iii.	Explanation and illustrate.	**3,3**
Q.5	i.	Definition. 1 Marks for Each	**3**
	ii.	Working & diagram	**4,3**
OR	iii.	Working & diagram	**4,3**
Q.6			
	i.	working with diagram	**3,2**
	ii.	functioning & diagram	**3,2**
	iii.	Operational principle & diagram	**3,2**

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