Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination Dec-2023
EE3CO50 Analog & Digital Electronics

Programme: B.Tech. Branch/Specialisation: EE

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. The majority charge carries in an NPN transistors are- **1**
(a) Electrons (b) Holes
(c) Trivalent atoms (d) Pentavalent atoms

ii. PNP transistor has the following arrangement **1**
(a) P type base, N type emitter, P type collector
(b) P type emitter, N type base, P type collector
(c) P type collector, N type base, N type emitter
(d) P type emitter, N type collector, P type base

iii. The gain of an amplifier with feedback is known as _____ gain. **1**
(a) High (b) Open loop (c) Closed loop (d) Low

iv. Which oscillator is characterized by a split capacitor in its tank circuit? **1**
(a) RC phase shift oscillator (b) Colpitts oscillator
(c) Wien bridge oscillator (d) None of these

v. NAND gate combination is: **1**
(a) OR and NOT gate (b) NOT and NOR gate
(c) NOT and AND gate (d) All of these

vi. If A = 1 and B = 0, then in terms of Boolean algebra, $A + \overline{B}$ = **1**
(a) B (b) $\overline{A}$ (c) A (d) None of these

vii. Which of the following circuit has its output dependent only upon the present input? **1**
(a) Analog Circuits (b) Flip Flops
(c) Combinational Circuits (d) Sequential Circuits

viii. _____ are an example of a combinational circuit. **1**
(a) Shift Registers (b) Multiplexers
(c) Counters (d) Flip-Flops

ix. A Shift register in which the output of the last flip-flop is connected to the input of the first flip-flop **1**
(a) BCD counter (b) Parallel counter
(c) Ripple counter (d) Ring counter

x. In JK Flipflop, If the present state is 0 and the next state is 1, then: **1**
(a) J = 1 & k = don't care (b) J = 1 & k = 1
(c) J = don't care & k = 1 (d) J = 0 & k = 0

Q.2 i. Compare Bipolar Junction Transistor and Field Effect Transistor. **2**
ii. Explain the characteristics of JFET with a diagram. **8**
OR iii. Explain the Hybrid parameter configurations of BJT. **8**

Attempt any two:

Q.3 i. Explain Darlington amplifier with a neat diagram. **5**
ii. Explain Class-A and Class-B Configuration of Power Amplifier. **5**
iii. Explain Colpitts Oscillator with a neat diagram. **5**

Q.4 i. Define Ex-OR and Ex-NOR Gate with Truth Table **3**
ii. Compare Resistance Transistor Logic (RTL), Transistor Transistor Logic (TTL) and Diode Transistor Logic (DTL). **7**
OR iii. Implement all Logic Gates using NAND & NOR Gates with Truth Table. **7**

Q.5 i. Explain Full Adder with Truth Table and Logic Diagram. **4**
ii. Design Multiplexer for the following expression. **6**
F(A,B,C,D) = AB+CD
OR iii. Solve the following expression using K-Map **6**
F(A,B,C,D) = ∑m(0,2,4,6,8,9,10,12,13,15)

Q.6 i. Compare Combinational and Sequential Logic circuits. **4**
ii. Convert SR Flip-flop to JK Flip-flop. **6**
OR iii. Explain random access memory and read only memory with its characteristics. **6**

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