Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2022

EC3CO12 VLSI Design

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. How is the current proportional to aspect ratio? **1**

(a) Directly (b) Inversly

(c) Not Proportional (d) Square of aspect ratio

ii. The Substrate Fermi potential of φ is___. **1**

(a) Negative in nmos positive in pMOS

(b) Negative in nmos negative in pMOS

(c) Positive in nmos negative in pMOS

(d) Positive in nmos positive in pMOS

iii. In the region where inverter exhibits gain, the two transistors are in _____ region. **1**

(a) Linear (b) Cut-off

(c) Non-saturation (d) Saturation

iv. If both transistors are in Saturation, then they act as___. **1**

(a) Current source (b) Voltage source

(c) Divider (d) Buffer

v. Number of states required to simulate a computer with memory capable of storing '3' words each of length '8' is ____. **1**

(a) $3x2^8$ (b) 2^3x8 (c) $2^{(3+8)}$ (d) None of these

vi. There are _____ tuples in finite state machine. **1**

(a) 4 (b) 5 (c) 6 (d) Unlimited

vii. Table that is not a part of asynchronous analysis procedure is___. **1**

(a) Transition table (b) State table

(c) Flow table (d) Excitation table

P.T.O.

viii. In case of asynchronous FSM change in the internal stage of the circuit is reflected by- **1**
(a) Vertical move (b) Horizontal move
(c) Diagonal move (d) Upward move

ix. The chemical used for shielding the active areas to achieve selective oxide growth is___. **1**
(a) Silver Nitride (b) Silicon nitride
(c) HCL (d) Polysilicon

x. The process by which aluminium is grown over the entire wafer, and the contact cuts is___. **1**
(a) Sputtering
(b) CVD
(c) Epitaxial growth
(d) Ion implantation

Q.2 i. Define the terms w.r.t MOSFET - Channel length Modulation **2**

ii. Explain the working of transmission gate. Design XOR gate using Transmission Gate. **3**

iii. Derive the expression for threshold voltage for nMOS transistor. **5**

OR iv. Derive the expression for linear and saturation current of MOS transistor. **5**

Q.3 i. Explain noise margin in detail. **2**

ii. Compare the voltage transfer charactertics of inverter having resistive load and n-type MOSFET load. **8**

OR iii. Draw and explain VTC curve for CMOS inverter. Derive the expression for V_{IL}, V_{IH} , V_{OH},V_{OL} for CMOS inverter **8**

Q.4 i. Compare Mealy & Moore machine. **3**

ii. Design a Finite State Machine for modulo-8 converter that converts Binary to Gray code. Implement it using JK flip flop **7**

OR iii. Minimize the number of states in the following state table **7**

Present state	Next state, output	
	x=0	x=1
a	f,0	b,0
b	d,0	c,0
c	f,0	e,0
d	g,1	a,0
e	d,0	c,0
f	f,1	b,1
g	g,0	h,1
h	g,1	a,0

Tabulate the reduced state table and draw state diagram.

Q.5 i. State and compare the mode of operation of asynchronous machines. **4**

ii. Define and explain the following with example: **6**
(a) Critical path (b) Non-critical path (c) Races (d) Cycles

OR iii. Minimize the state table given below also encircle the stable state in each row: **6**

Present state	Next state, output			
	00	01	10	11
a	a,0	b,1	-	d,0
b	b,1	b,1	c,1	e,1
c	-	b,1	c,1	e,1
d	a,0	b,1	-	d,0
e	a,0	e,0	f,0	e,1
f	-	e,0	f,0	d,0

Q.6 Attempt any two:

i. Compare the logic structure of CPLD & FPGA **5**

ii. Explain with diagram IC fabrication steps for n-well process **5**

iii. Write layout design rules for – minimum separation between two layers, minimum Overlap of two layers, minimum Layer width(3each). Using these design rules design CMOS inverter **5**

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Marking Scheme
EC3CO12 VLSI Design

Q.1	i.	How is the current proportional to aspect ratio? (b) Inversly		**1**
	ii.	The Substrate Fermi potential of φ is___. (a) Negative in nmos positive in pMOS		**1**
	iii.	In the region where inverter exhibits gain, the two transistors are in _____ region. (d) Saturation		**1**
	iv.	If both transistors are in Saturation, then they act as___. (a) Current source		**1**
	v.	Number of states required to simulate a computer with memory capable of storing '3' words each of length '8' is ____. (d) None of these		**1**
	vi.	There are _____ tuples in finite state machine. (b) 5		**1**
	vii.	Table that is not a part of asynchronous analysis procedure is___. (d) Excitation table		**1**
	viii.	In case of asynchronous FSM change in the internal stage of the circuit is reflected by- (a) Vertical move		**1**
	ix.	The chemical used for shielding the active areas to achieve selective oxide growth is___. (b) Silicon nitride		**1**
	x.	The process by which aluminium is grown over the entire wafer, and the contact cuts is___. (a) Sputtering		**1**

Q.2	i.	Definition	2 Marks	**2**
	ii.	Explain the working of transmission gate.	1 Mark	**3**
		Design XOR gate using Transmission Gate.	2 Marks	
	iii.	All Parameters	2 Marks	**5**
		Description	3 Marks	
OR	iv.	Linear Current Derivation	2.5 Marks	**5**
		Saturation current Derivation	2.5 Marks	

Q.3	i.	Noise margin in detail.	(As per explanation)	**2**
	ii.	Each Comparison	(2 Marks*4)	**8**
OR	iii.	Derive the expression for		**8**
		V_{IL}	2 Marks	
		V_{IH}	2 Marks	
		V_{OH}	2 Marks	
		V_{OL}	2 Marks	

Q.4	i.	Each difference	1 Mark*3	**3**
	ii.	State Diagram	2 Marks	**7**
		Transistion table	2 Marks	
		K- map	2 Marks	
		Implementation	2 Marks	
OR	iii.	Merger table/merger graph/partition method	2 Marks	**7**
		Equivalent state	1 Mark	
		Reduce state table	2 Marks	
		Reduced state diagram	1 Mark	

Q.5	i.	Each Comparison	(1 Mark*4)	**4**
	ii.	Define and explain the following with example:		**6**
		(a) Critical path	1.5 Marks	
		(b) Non-critical path	1.5 Marks	
		(c) Races	1.5 Marks	
		(d) Cycles	1.5 Marks	
OR	iii.	Encircle stable state	1 Mark	**6**
		Minimization	3 Marks	
		Reduced state table	2 Marks	

Q.6		Attempt any two:		
	i.	Each difference	(1.5 Marks)	**5**
	ii.	Each step	(0.5 Marks*10)	**5**
	iii.	Layout Design Rule	2 Marks	**5**
		Inverter layout design	3 Marks	

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