Q.6		Attempt any two:								
	i.	Describe the different types of semiconductor memory technologies. Compare and contrast their characteristics, including speed, volatility, and usage.	**5**	3	2	5	2			
	ii.	What are write policies in cache memory (write-through vs. write-back)? Explain the advantages and disadvantages of each policy concerning data integrity and performance.	**5**	3	2	5	2			
	iii.	Discuss the various cache replacement algorithms (e.g., LRU, FIFO, Random) used in cache memory systems.	**5**	3	2	5	2			

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Total No. of Questions: 6 *Total No. of Printed Pages:4*

Enrollment No.....

Faculty of Engineering

End Sem Examination Dec 2024

EN3ES14 Computer Organization & Architecture

Programme: B.Tech. Branch/Specialisation: CSBS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

			Marks	**BL**	**PO**	**CO**	**PSO**
Q.1	i.	Which of the following is NOT a Boolean operation? (a) AND (b) OR (c) ADD (d) NOT	**1**	1	1	1	1
	ii.	Which addressing mode uses the contents of a register as the effective address of the operand? (a) Immediate addressing (b) Register addressing (c) Direct addressing (d) Register indirect addressing	**1**	1	1	1	1
	iii.	In floating-point representation, the mantissa represents which of the following? (a) The exponent (b) The precision of the number (c) The sign of the number (d) The base of the number	**1**	2	1	1	1
	iv.	In non-restoring division, when a negative remainder is obtained, what is the next step? (a) Add the divisor and shift (b) Subtract the divisor again (c) Reverse the bits (d) Stop the calculation	**1**	2	1	1	1
	v.	What is the role of an interrupt in process state transitions? (a) To halt the CPU (b) To synchronize memory (c) To switch processes between states (d) To reduce process execution time	**1**	2	2	2	1

vi.	In I/O transfer techniques, which method allows an I/O device to send data without CPU intervention? (a) Program-controlled I/O (b) Interrupt-driven I/O (c) Direct Memory Access (DMA) (d) Software interrupts	**1**	2	2	2	1
vii.	What is the main advantage of pipelining in CPU design? (a) Simplified control logic (b) Increased instruction throughput (c) Reduced power consumption (d) Easier debugging	**1**	2	2	2	1
viii.	In parallel processing, what is meant by "data parallelism"? (a) Performing multiple tasks at the same time (b) Distributing different instructions across multiple processors (c) Applying the same operation to different pieces of data simultaneously (d) Executing different algorithms concurrently	**1**	2	2	2	1
ix.	What is the primary purpose of memory interleaving? (a) To increase the total memory capacity (b) To improve access speed by allowing simultaneous access to multiple memory banks (c) To reduce power consumption in memory chips (d) To simplify the memory hierarchy	**1**	2	2	2	1
x.	Which cache mapping technique allows each memory block to be mapped to exactly one cache line? (a) Fully associative mapping (b) Set-associative mapping (c) Direct-mapped cache (d) Hybrid mapping	**1**	2	2	2	1

Q.2	i.	Differentiate between combinational and sequential circuits.	**2**	2	2	1	1
	ii.	Explain the instruction execution cycle of a CPU.	**3**	2	2	1	2
	iii.	List and briefly describe five addressing modes commonly used in CPU instruction sets with example of each.	**5**	2	2	2	1
OR	iv.	Explain the difference between fixed-point and floating-point representations with examples.	**5**	2	1	2	1
Q.3	i.	Describe the shift-and-add technique for binary multiplication with example.	**3**	3	2	2	1
	ii.	Describe the structure of IEEE 754 floating-point representation, explaining the significance of the sign bit, exponent, and mantissa.	**7**	3	2	2	1
OR	iii.	Describe Booth's multiplication algorithm with flowchart and explain how it optimizes binary multiplication for signed numbers.	**7**	3	3	2	1
Q.4	i.	Describe the role of Direct Memory Access (DMA) in I/O transfers.	**4**	3	2	3	1
	ii.	Discuss the types of interrupts and exceptions and explain how they affect process state transitions in a multitasking environment.	**6**	3	3	3	2
OR	iii.	Explain the importance of interrupt-driven I/O in real-time systems and how it enhances system responsiveness compared to polling.	**6**	3	3	3	1
Q.5	i.	What are the main benefits of parallel processors? Provide two examples.	**4**	2	2	4	1
	ii.	Describe the concept of cache coherency in parallel processing and explain how the MESI protocol helps maintain coherency in multi-core systems.	**6**	3	3	4	2
OR	iii.	Explain the three types of pipeline hazards—structural, data, and control hazards, giving an example of each.	**6**	3	2	4	1

Marking Scheme

EN3ES14 Computer Organisation and Architecture

Q.1	i)	**Ans:- c) ADD**	**1**
	ii)	**Ans:- d) Register indirect addressing**	**1**
	iii)	**Ans:- b) The precision of the number**	**1**
	iv)	**Ans:- a) Add the divisor and shift**	**1**
	v)	**Ans:- c) To switch processes between states**	**1**
	vi)	**Ans:- c) Direct Memory Access (DMA)**	**1**
	vii)	**Ans:- b) Increased instruction throughput**	**1**
	viii)	**Ans:- c) Applying the same operation to different pieces of data simultaneously**	**1**
	ix)	**Ans:- b) To improve access speed by allowing simultaneous access to multiple memory banks**	**1**
	x)	**Ans:- c) Direct-mapped cache**	**1**

Q.2	i.	Differentiate between combinational and sequential circuits. **(2 differences, 1 mark for each difference)**	**2**
	ii.	Explain the instruction execution cycle of a CPU. **(Explanation with diagram 3 marks)**	**3**
	iii.	List and briefly describe five addressing modes commonly used in CPU instruction sets with example of each. **(5 addressing modes, 1 mark each)**	**5**
OR	iv.	Explain the difference between fixed-point and floating-point representations with examples. **(5 differences, 1 mark for each difference)**	**5**
Q.3	i.	Describe the shift-and-add technique for binary multiplication with example. **(Description 2 marks, example 1 mark)**	**3**
	ii.	Describe the structure of IEEE 754 floating-point representation, **(4 marks)** explaining the significance of the sign bit **(1 mark)**, exponent **(1 mark)**, and mantissa **(1 mark)**.	**7**
OR	iii.	Describe Booth's multiplication algorithm **(3 marks)**, with flowchart **(2 marks)**, and explain how it optimizes binary multiplication for signed numbers. **(2 marks)**,	**7**
Q.4	i.	Describe the role of Direct Memory Access (DMA) in I/O transfers. **(Description 4 marks)**,	**4**
	ii.	Discuss the types of interrupts and exceptions, **(4 marks)**, and explain how they affect process state transitions in a multitasking environment. **(2 marks)**,	**6**
OR	iii.	Explain the importance of interrupt-driven I/O in real-time systems **(3 marks)**, and how it enhances system responsiveness compared to polling. **(3 marks)**,	**6**
Q.5	i.	What are the main benefits of parallel processors? **(3 marks)**, Provide two examples. **(1 mark)**,	**4**
	ii.	Describe the concept of cache coherency in parallel processing and **(3 marks)**, explain how the MESI (Modified, Exclusive, Shared, Invalid) protocol helps maintain coherency in multi-core systems. **(3 marks)**,	**6**
OR	iii.	Explain the three types of pipeline hazards—structural, data, and control hazards, giving an example of each. **(2 marks each)**,	**6**
Q.6		**Attempt any Two**	
	i.	Describe the different types of semiconductor memory technologies. Compare and contrast their characteristics, including speed, volatility, and usage. **(5 differences, 1 mark for each difference)**	**5**
	ii.	What are write policies in cache memory (write-through vs. write-back)? **(3 marks)**, Explain the advantages and disadvantages of each policy concerning data integrity and performance. **(2 marks)**,	**5**
	iii.	Discuss the various cache replacement algorithms (e.g., LRU, FIFO, Random) used in cache memory systems. **(5 marks)**,	**5**

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