Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem Examination Dec 2024

EC3EV07 VLSI Technology

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

			Marks	BL	CO	PO	PSO
Q.1	i.	What is the primary purpose of a cleanroom in VLSI technology? (a) To keep the temperature low (b) To minimize particulate contamination (c) To reduce energy consumption (d) To improve airflow	**1**	1	1	1, 2	1
	ii.	Which crystalline orientation is most commonly used in VLSI wafer fabrication? (a) (100) (b) (110) (c) (111) (d) (101)	**1**	1	1	1, 2	1
	iii.	Which factor primarily affects the growth rate of silicon dioxide in thermal oxidation? (a) Ambient pressure (b) Crystal orientation (c) Oxidizing species and temperature (d) Wafer thickness	**1**	2	2	1, 2	1
	iv.	In solid-state diffusion, which parameter has the greatest effect on the impurity profile? (a) Temperature (b) Humidity (c) Pressure (d) Chamber material	**1**	2	2	1, 2	1
	v.	Chemical Vapor Deposition (CVD) is commonly used to deposit: (a) Aluminum (b) Polysilicon (c) Gold (d) Glass	**1**	1	3	1, 2	1

vi.	In mask generation, the mask typically represents: (a) The device layout pattern (b) The electrical properties of a device (c) The chemical composition of a device (d) The mechanical strength of a device	**1**	1	3	1, 2	1
vii.	Which metallization technique uses a high-energy beam to deposit material on a wafer? (a) CVD (b) Sputtering (c) Evaporation (d) Annealing	**1**	1	4	1, 2	1
viii.	The masking sequence is critical for: (a) Defining the layer patterns for MOS and bipolar devices (b) Cleaning the wafer surfaces (c) Adjusting the deposition temperature (d) Determining crystal orientation	**1**	1	4	1, 2	1
ix.	CMOS design rules primarily aim to: (a) Define etching requirements (b) Control oxide growth (c) Standardize layout dimensions for reliable fabrication (d) Control thermal expansion	**1**	1	5	1, 2	1
x.	Which design rule is essential to avoid unwanted overlap in CMOS circuits? (a) Poly-silicon overlap (b) Active-to-active separation (c) Metal-to-metal spacing (d) Gate-to-gate distance	**1**	2	5	1, 2	1
Q.2	i. Define single crystal material.	**2**	1	1	1, 2	1
	ii. Explain the importance of cleanroom environments in VLSI fabrication.	**3**	2	1	1, 2	1
	iii. Explain the wafer cleaning process and describe common wet chemical etching techniques used in VLSI manufacturing.	**5**	2	1	1, 2	1
OR	iv. Describe the Czochralski (CZ) method for silicon crystal growth with neat diagram and explain its significance in VLSI wafer production.	**5**	2	1	1, 2	1

Q.3	i. Define wet & dry oxidation with example.	**3**	2	2	1, 2	1
	ii. Describe Fick's Diffusion Model in brief.	**7**	2	2	1, 2	1
OR	iii. Explain the process of ion implantation with neat diagram and its advantages over diffusion for impurity incorporation.	**7**	2	2	1, 2	1
Q.4	i. What is epitaxial growth?	**2**	1	3	1, 2	1
	ii. Describe the process of mask generation and its role in photolithography for VLSI fabrication.	**8**	2	3	1, 2	1
OR	iii. Elaborate the Chemical Vapour Deposition (CVD) technique for the deposition of polysilicon, silicon dioxide & silicon nitride.	**8**	2	3	1, 2	1
Q.5	i. What is multilevel metallization? Why is it essential in modern VLSI circuits?	**4**	2	4	1, 2	1
	ii. Describe the evaporation and sputtering techniques used in metallization and their significance in VLSI technology.	**6**	2	4	1, 2	1
OR	iii. Explain the masking sequence and process flow for fabricating MOS devices.	**6**	2	4	1, 2	1
Q.6	Attempt any two:					
	i. Explain the importance of layout design rules in VLSI and describe common rules for the silicon gate NMOS process.	**5**	2	5	1, 2	1
	ii. Provide a simple layout example and explain how design rules are applied in the layout process.	**5**	3	5	1, 2	1
	iii. Discuss how layout design rules affect the scalability and performance of VLSI circuits.	**5**	3	5	1, 2	1

******

Marking Scheme

EC3EV07 (T) VLSI Technology (T)

Q.1	i)	B) To minimize particulate contamination	**1**
	ii)	A) (100)	**1**
	iii)	C) Oxidizing species and temperature	**1**
	iv)	A) Temperature	**1**
	v)	B) Polysilicon	**1**
	vi)	A) The device layout pattern	**1**
	vii)	B) Sputtering	**1**
	viii)	A) Defining the layer patterns for MOS and bipolar devices	**1**
	ix)	C) Standardize layout dimensions for reliable fabrication	**1**
	x)	C) Metal-to-metal spacing	**1**
Q.2	i.	definition	**2**
	ii.	At least 3 points about importance	**3**
	iii.	Explain & wet ethcing	**2.5,2.5**
OR	iv.	Describe the Czochralski (CZ) method, diagram, siginificance	**2,2,1**
Q.3	i.	Definition with example	**1.5,1.5**
	ii.	define Model with equations	**3,4**
OR	iii.	process with neat diagram & advantage	**3,2,2**
Q.4	i.	Definition	**2**
	ii.	Process & significance	**6,2**
OR	iii.	CVD for 3 materials	**3,2.5,2.5**
Q.5	i.	Definition & importance	**2,2**
	ii.	Description of both & significance	**5,1**
OR	iii.	Explanation & flow	**4,2**
Q.6			
	i.	importance of layout design rules	**5**
	ii.	example and explain	**3,2**
	iii.	affect the scalability and performance	**2.5,2.5**

******