Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2019

EC3EL08 / EI3EL08 Computer Organization and Architecture

Programme: B.Tech. Branch/Specialisation: EC/EI

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Second generation of computers were based on: **1**
(a) Vacuum tubes (b) Transistors
(c) IC (d) VLSI

ii. In micro-programmed approach, the control signals are generated by _____. **1**
(a) System programs (b) Machine instructions
(c) Utility tools (d) None of these

iii. In IEEE double precision floating point format, the size of the mantissa is _____. **1**
(a) 32 bit (b) 64 bit (c) 72 bit (d) 52 bit

iv. The addressing mode, where you directly specify the operand value is: **1**
(a) Immediate (b) Direct
(c) Definite (d) Relative

v. Which is a method of decomposing a sequential process into sub operations? **1**
(a) Pipeline (b) CISC (c) RISC (d) Database

vi. The situation where in the data of operands are not available is called _____. **1**
(a) Deadlock (b) Stock
(c) Data hazard (d) Structural hazard

vii. The throughput of a superscalar processor is: **1**
(a) Less than 1 (b) 1
(c) More than 1 (d) Not known

viii. Which of the following is used to speed-up the processing? **1**
(a) Pipeline (b) Vector processing
(c) Both (a) & (b) (d) None of these

P.T.O.

ix. The fastest data access is provided using _____. **1**
(a) Caches (b) DRAM (c) SRAM (d) CPU Registers

x. The correspondence between the main memory blocks and those in the cache is given by _____. **1**
(a) Hash function (b) Mapping function
(c) Assign function (d) None of these

Q.2 i. What is meant by Von-Neumann Architecture? **2**

ii. Enlist three benefits of using multiple-bus architecture compared to single-bus architecture. **3**

iii. Discuss the five generations of electronic computers. **5**

OR iv. Explain the Hardwired CPU control unit with the help of its block diagram. **5**

Q.3 i. Convert the decimal number (-12.25) into IEEE 754 single precision floating point format. **3**

ii. What do you mean by a floating point number? Explain the IEEE 754 single precision format for binary floating point numbers. **7**

OR iii. What is an addressing mode? Explain any five types of addressing modes with example of each. **7**

Q.4 i. How does an instruction pipeline improves the speed of execution? **2**

ii. What do mean by pipeline hazards? Draw and explain data and instruction hazard with example. **8**

OR iii. Describe the four stage instruction pipelining with diagram. **8**

Q.5 i. Draw the state transition diagram of a process. **2**

ii. What is a superscalar processor? Explain its operation with a diagram. **8**

OR iii. What is Flynn's taxonomy for parallel processing? Explain its four type of computer structures with diagram. **8**

Q.6 Explain any two with the help of diagram:

i. Computer Memory hierarchy **5**

ii. Use of Cache memory **5**

iii. Virtual Memory Organization **5**

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Marking Scheme

EC3EL08 / EI3EL08 Computer Organization and Architecture

Q.1	i.	Second generation of computers were based on: (b) Transistors	**1**
	ii.	In micro-programmed approach, the control signals are generated by _____. (b) Machine instructions	**1**
	iii.	In IEEE double precision floating point format, the size of the mantissa is _____. (d) 52 bit	**1**
	iv.	The addressing mode, where you directly specify the operand value is: (a) Immediate	**1**
	v.	Which is a method of decomposing a sequential process into sub operations? (a) Pipeline	**1**
	vi.	The situation where in the data of operands are not available is called _____. (c) Data hazard	**1**
	vii.	The throughput of a superscalar processor is: (c) More than 1	**1**
	viii.	Which of the following is used to speed-up the processing? (c) Both (a) & (b)	**1**
	ix.	The fastest data access is provided using _____. (d) CPU Registers	**1**
	x.	The correspondence between the main memory blocks and those in the cache is given by _____. (b) Mapping function	**1**
Q.2	i.	Von-Neumann Architecture	**2**
	ii.	Three benefits of using multiple-bus architecture compared to single-bus architecture. 1 mark for each (1 mark * 3)	**3**
	iii.	Five generations of electronic computers. 1 mark for each (1 mark * 5)	**5**
OR	iv.	Hardwired CPU control unit Block diagram. 2 marks Description 3 marks	**5**
Q.3	i.	Convert the decimal number (-12.25) into IEEE 754 single precision floating point format. Mantissa = 110001 1 mark E' = 10000010 1 mark Answer 1 mark	**3**
	ii.	Floating point number 2 marks IEEE 754 single precision format 5 marks	**7**
OR	iii.	Addressing mode 2 marks Any five types of addressing modes with example 1 mark for each (1 mark * 5) 5 marks	**7**
Q.4	i.	Instruction pipeline improves the speed of execution	**2**
	ii.	Pipeline hazards 2 marks Data hazard with example 3 marks Instruction hazard with example 3 marks	**8**
OR	iii.	Four stage instruction pipelining with diagram. 2 marks for each (2 marks * 4)	**8**
Q.5	i.	State transition diagram of a process.	**2**
	ii.	Superscalar processor 2 marks Its operation 4 marks Diagram. 2 marks	**8**
OR	iii.	Flynn's taxonomy for parallel processing 2 marks Its four type of computer structures with diagram. 1.5 marks for each (1.5 marks * 4) 6 marks	**8**
Q.6		Explain any two with the help of diagram:	
	i.	Computer Memory hierarchy Diagram 2 marks Description 3 marks	**5**
	ii.	Use of Cache memory Diagram 2 marks Description 3 marks	**5**
	iii.	Virtual Memory Organization Diagram 2 marks Description 3 marks	**5**

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