Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem Examination Dec-2023

EN3ES14 Computer Organization & Architecture

Programme: B.Tech. Branch/Specialisation: CSBS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which of the following is not an addressing mode commonly found in instruction sets? **1**

(a) Immediate (b) Direct

(c) Parallel (d) Indexed

ii. Fixed-point number representation is suitable for: **1**

(a) Precise mathematical calculations

(b) Representing non-integer values

(c) Efficient storage of whole numbers

(d) Handling large floating-point numbers

iii. Multiplying (1000) by (1001) will produce the product- **1**

(a) 1001000 (b) 1001001

(c) 10001000 (d) 10011000

iv. Booth algorithm gives procedure for multiplying binary integers in- **1**

(a) Unsigned representation

(b) Signed magnitude representation

(c) 2's complement representation

(d) None of these

v. What is the main role of interrupts in process state transitions in multitasking operating systems? **1**

(a) To terminate processes

(b) To switch between processes

(c) To allocate memory resources

(d) To control the CPU clock speed

P.T.O.

vi. How does a control unit coordinate the execution of instructions in a CPU? **1**
(a) By managing memory access
(b) By issuing I/O operations
(c) By generating control signals
(d) By performing arithmetic calculations

vii. Pipeline hazards in computer architecture can lead to: **1**
(a) Increased performance (b) Reduced throughput
(c) Improved cache coherency (d) Lower clock speeds

viii. What is the primary goal of parallel processors in computing? **1**
(a) Reducing cache size
(b) Increasing clock speed
(c) Enhancing single-threaded performance
(d) Improving overall processing throughput

ix. In a write-back cache policy, when is data written from the cache to main memory? **1**
(a) Immediately upon each write operation
(b) Only when cache eviction occurs
(c) Never
(d) At the end of each program execution

x. What is the primary purpose of semiconductor memory technologies like DRAM (Dynamic Random-Access Memory) in memory system design? **1**
(a) Non-volatile storage (b) Fast data processing
(c) Long-term data retention (d) Secondary storage

Q.2 i. How do these functional blocks (CPU, memory, I/O, control unit) interact to execute a program on a computer? **2**

ii. Explain the concept of Register Transfer Language (RTL) interpretation of instructions in a CPU. **3**

iii. Describe various addressing modes used in instruction sets and provide examples for each. **5**

OR iv. Explain the principles of fixed-point and floating-point number representations in computer systems. Discuss the advantages and disadvantages of fixed-point and floating-point representations in numerical computing. **5**

Q.3 i. Walk through the steps of a restoring division algorithm for binary numbers. **3**

ii. Draw the flowchart for restoring division. Divide 448/17, Show Quotient and Remainder. **7**

OR iii. Explain the Booth's Algorithm with the help of flowchart. Multiply (-9)*(-13) using Booth Algorithm, Give each step. **7**

Q.4 i. Explain how conditional branching is handled in both hardwired and micro-programmed control units. **2**

ii. Describe the role of interrupts in process state transitions and multitasking operating systems. **3**

iii. Compare and contrast program-controlled, interrupt-driven, and DMA I/O transfer methods. When would each be most suitable? **5**

OR iv. How does the control unit of a simple hypothetical CPU coordinate and control the execution of instructions? **5**

Q.5 i. What is throughput in the context of pipelining, and how is it related to the clock cycle time and pipeline stages? **4**

ii. Discuss the various pipeline hazards that can occur in a processor pipeline. What are some techniques to mitigate these hazards? **6**

OR iii. Explain the concept of cache coherency in the context of parallel processors. Why is it important, and how is it achieved? **6**

Q.6 Attempt any two:

i. Explain the concept of memory interleaving and its significance in memory organization. How does it improve memory performance? **5**

ii. Discuss the trade-offs between cache size and block size in cache memory design. How does the choice of block size impact cache performance? **5**

iii. Explain the purpose of cache mapping functions (e.g., direct-mapped, set-associative, fully associative). How do these functions impact cache memory design and performance? **5**

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Marking Scheme

Computer Organization and Architecture-EN3ES14 (T)

Q.1	i)	c) Parallel		**1**
	ii)	c) Efficient storage of whole numbers.		**1**
	iii)	a)1001000		**1**
	iv)	c) 2's complement representation		**1**
	v)	b) To switch between processes		**1**
	vi)	c) By generating control signals		**1**
	vii)	b) Reduced throughput		**1**
	viii)	d) Improving overall processing throughput		**1**
	ix)	b) Only when cache eviction occurs		**1**
	x)	b) Fast data processing		**1**
Q.2	i.	(CPU, memory, I/O, control unit)	(As per Explanation)	**2**
	ii.	Concept of Register Transfer Language	(As per Explanation)	**3**
	iii.	Type with example	(Each type * 1)	**5**
OR	iv.	Principles of fixed-point and floating-point.	(As per Explanation)	**5**
Q.3	i.	Flow Chart	(As per Explanation)	**3**
	ii.	Flowchart. Procedure Right Answer	3 Marks 3 Marks 1 Marks	**7**
OR	iii.	Ans: Final Product = (0001110101)	(7 Marks)	**7**
Q.4	i.	Explanation	(2 Marks)	**2**
	ii.	Diagram Example	1 Mark 2 Marks	**3**
	iii.	Comparison Reason for most suitable	3 Marks 2 Marks	**5**
OR	iv.	Control Logic diagram Explanation	2 Marks 3 Marks	**5**
Q.5	i.	Throughput in the context of pipelining Related to the clock cycle time and pipeline stages	2 Marks 2 Marks	**4**
	ii.	Various pipeline Techniques to mitigate these hazards	4 Marks 2 Marks	**6**
OR	iii.	Concept of cache coherency. Important Achieved Attempt any two.	4 Marks 1 Mark 1 Mark	**6**
Q.6	i.	Memory interleaving and its significance in memory Improve memory performance	3 Marks 2 Marks	**5**
	ii.	Explanation Block size impact cache performance	3 Marks 2 Marks	**5**
	iii.	Purpose of cache mapping functions Impact cache memory design and performance	(1 Marks*each) 2 Marks	**5**

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