Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2022

EC3EV03 Low Power VLSI Design

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. For implementing 4-input Static NAND Logic, ___PMOS are connected in _____& ___ NMOS are connected in: **1**

(a) 4, Series, 4, Parallel (b) 4, Parallel, 4, Series

(c) 4, Series, 4, Series (d) 4, Parallel, 4, Parallel

ii. Dynamic power dissipation is a function of: **1**

(a) Drain Current (b) Rise Time & fall time

(c) Capacitance (d) All of these

iii. GIDL stands for- **1**

(a) Gate-Induced Drain Leakage

(b) Gate-Induced Drain Lowering

(c) Gate-Influenced Drain Lowering

(d) Gate-Influenced Drain Leakage

iv. 'K' stands for _____ in High-K material. **1**

(a) Dielectric Constant (b) Material Constant

(c) Temperature (d) Potential

v. Technology scaling _____ the internal capacitances on the chip, while _____ capacitances remain approximately constant. **1**

(a) Destroys, external (b) Increases, external

(c) Reduces, external (d) Dominates, external

vi. The Power dissipation which is a function of rise and fall time is _____. **1**

(a) Glitching power dissipation

(b) Leakage power dissipation

(c) Static power dissipation

(d) Short Circuit power dissipation

P.T.O.

vii. The type of adder Braun's Multiplier employ is _____. **1**
(a) Ripple Carry Adder only
(b) Carry Propagate adder only
(c) Carry Save & Carry Propagate adder
(d) Carry Save & Ripple Carry Adder

viii. In DRAM the number of MOS transistors required for storing a 1-bit data is_____. **1**
(a) 4 (b) 3 (c) 2 (d) 1

ix. _____Power estimation determines the major active component during a particular duration. **1**
(a) Higher level (b) Architectural
(c) Gate Level (d) Instruction level

x. Glitching Power estimation can be obtained by identifying_____. **1**
(a) Frequency of switching (b) Instruction delays
(c) Propagation delay (d) Dynamic Hazards

Q.2 i. Explain the significance of Low power design in VLSI. **3**

ii. Describe in detail the working of MOS inverter using Static logic. Identify and enlist the power dissipation factors in the circuit. **7**

OR iii. Which transistor technology is preferably used for VLSI chip designing? Give proper explanation. **7**

Q.3 i. What is Threshold Roll-off? **2**

ii. What are High-K dielectrics? Mention their significance in low power designing. **3**

iii. What is power supply gating? Discuss its types. Demonstrate with relevant diagram. **5**

OR iv. Discuss the following in detail: **5**
(a) DIBL (b) Hot carrier injection

Q.4 i. Discuss the Short circuit and Glitching power dissipation in MOS circuits. **4**

ii. What is technology Scaling? Compare various types of scaling. **6**

OR iii. Illustrate with an example the parallel and pipelined architectural approaches for reducing dynamic power dissipation. **6**

Q.5 Attempt any two:

i. Discuss the adder architectures for low power VLSI design. **5**

ii. Explain Booth multiplication with an example. Compare its performance with Braun's multiplier. **5**

iii. Illustrate the reading and writing operation in DRAM. Identify various factors of power dissipation in its architecture? **5**

Q.6 Write Short note on any two:

i. Probabilistic techniques for Power estimation. **5**

ii. Software based Power Estimation **5**

iii. Logic synthesis for low power design **5**

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Marking Scheme
EC3EV03 Low Power VLSI Design

Q.1	i.	For implementing 4-input Static NAND Logic, ___PMOS are connected in _____& ___ NMOS are connected in: (b) 4, Parallel, 4, Series		**1**
	ii.	Dynamic power dissipation is a function of: (c) Capacitance		**1**
	iii.	GIDL stands for- (b) Gate-Induced Drain Lowering		**1**
	iv.	'K' stands for _____ in High-K material. (a) Dielectric Constant		**1**
	v.	Technology scaling _____ the internal capacitances on the chip, while _____ capacitances remain approximately constant. (c) Reduces, external		**1**
	vi.	The Power dissipation which is a function of rise and fall time is _____. (d) Short Circuit power dissipation		**1**
	vii.	The type of adder Braun's Multiplier employ is _____. (c) Carry Save & Carry Propagate adder		**1**
	viii.	In DRAM the number of MOS transistors required for storing a 1-bit data is_____. (d) 1		**1**
	ix.	_____Power estimation determines the major active component during a particular duration. (b) Architectural		**1**
	x.	Glitching Power estimation can be obtained by identifying_____. (d) Dynamic Hazards		**1**
Q.2	i.	3 Points (in explanation)	(1 mark*3)	**3**
	ii.	Working of MOS inverter		**7**
		Circuit diagram	2 Marks	
		Explanation	2 Marks.	
		Power dissipation (Any 6)	3 Marks	
OR	iii.	CMOS technology	1 Marks	**7**
		Merits/advantates (Atleast 6 adv.)	6 Marks	
Q.3	i.	Define Threshold Roll-off	(As per explanation)	**2**
	ii.	What are High-K dielectrics	1 Mark	**3**
		Significance in low power designing.	2 Marks	
	iii.	Power supply gating	2 Marks	**5**
		Discuss its types	1 Mark	
		Demonstrate with relevant diagram.	2 Marks	
OR	iv.	(a) DIBL	2.5 Marks	**5**
		(b) Hot carrier injection	2.5 Marks	
Q.4	i.	Short circuit and Glitching power	(2 Marks*2) .	**4**
	ii.	Define technology Scaling	2 Marks	**6**
		Types of scaling.	1 Mark	
		Compare (3 Points)	3 Marks	
OR	iii.	Parallel and pipelined architectural approaches	(3 Marks*2)	**6**
Q.5		Attempt any two:		
	i.	Adder architecture (Atleast two)	(2.5 Marks*2)	**5**
	ii.	Explain Booth multiplication with an example.	3 Marks	**5**
		Compare its performance with Braun's multiplier.	2 Marks	
	iii.	Reading and writing operation in DRAM.	3 Marks	**5**
		Power factors (atleast 4)	2 Marks	
Q.6		Write Short note on any two:		
	i.	Probabilistic techniques with example.	5 Marks	**5**
	ii.	Software based Power Estimation	(2.5 Marks*2)	**5**
	iii.	Logic synthesis (Atleast two methods)	(2.5 Marks*2)	**5**

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