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## Enrollment No.....



## Faculty of Engineering End Sem (Odd) Examination Dec-2017 CS3CO07 Micro Processor & Interfacing

Programme: B.Tech. Branch/Specialisation: CS

**Duration: 3 Hrs. Maximum Marks: 60** 

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers

	•			stead of only a,	b, c or d.	8
Q.1	i.	A microproce	ssor is ALU			1
		(a) And contro	ol unit on a sin	gle chip.		
		(b) And memo	ory on a single	chip.		
		(c) Register unit and I/O device on a single chip.				
		(d) Register u	nit and control	unit on a singl	e chip.	
	ii.	Output of the assembler in machine codes is referred to as				1
		(a) Object pro	gram	(b) Source pr	ogram	
		(c) Macroinst	ruction	(d) Symbolic	addressing	
	iii.	What is SIM?				1
		(a) Select inte	rrupt mask.	(b) Sorting in	terrupt mask.	
		(c) Set interru	pt mask.	(d) None of the	hese.	
	iv.	In order to compliment the lower nibble of accumulator one can use				1
		(a) ANI 0FH	(b) XRI 0FH	(c) ORI 0FH	(d) CMA	
	V.	In 8085 micro	oprocessor sys	tem with mem	nory mapped I/O, which	1
		of the following	ng is true?			
		(a) Devices have 8-bit address line				
		(b) Devices are accessed using IN and OUT instructions				
		(c) There can devices	be maximum	of 256 input	devices and 256 output	
		(d) Arithmetic the I/O dat	0 1	erations can be	directly performed with	
	vi.	Which one of	the following	ICs is used to i	nterface Keyboard and	1
Display?			•			
		(a) 8251	(b) 8279	(c) 8259	(d) 8253	
	vii.	The number o	f hardware inte	errupts present	in 8085 are	1
		(a) 5	(b) 8	(c) 16	(d) 10	
					P.T	.O.

	viii.	The cycle required to fetch and execute an instruction in 8085				
		microprocessor is which one of the following				
		(a) Clock cycle (b) Memory cycle				
		(c) Machine cycle (d) Instruction cycle.				
ix.	ix.	The operations executed by two or more control units are referred as				
		(a) Micro-operations (b) Macro-operations				
		(c) Multi-operations (d) Bi control-operations				
	х.	Intel core2 Duo is abit processor.	1			
		(a) 8 bit (b) 16 bit (c) 32 bit (d) 64 bit				
Q.2	i.	Specify the size of data, address, memory word and memory capacity of 8085 microprocessor.	2			
	ii.	Draw the block diagram of 8086 microprocessor and explain each block.	8			
OR	iii.	Sketch and explain the block diagram of 8085 microprocessor.				
Q.3	i.	Define stack and stack related instructions.	2			
	ii.	List out the five categories of the 8085 instructions and explain two examples of instruction for each group.	8			
OR	iii.	What are addressing modes? Explain different types with examples. Write a program to find the largest out of ten numbers.				
Q.4	i.	Suggest an arrangement to interface 8K X 8 size of ROM to 8085, specify the address range.	3			
	ii.	Draw and explain the block diagram of 8255 PPI.	7			
OR	iii.	Write a note on 8253 programmable interval timer.				
Q.5	i.	Mention the number of machine cycles and T states in one byte two	4			
		byte and three byte instruction.				
	ii.	With timing diagram explain the memory read operation in 8085.	6			
OR	iii.	Explain vectored and non-vectored interrupts of 8085.	6			
Q.6	i.	Write in brief about Intel quick path interconnect.	2			
	ii.	Write a note on Intel Core 2 duo processor.	8			
OR	iii.	Write a note on Intel Core i 7 Processor.	8			

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## CS3CO07 Micro Processor & Interfacing Marking Scheme

Q.1	i.	A microprocessor is ALU	1
	••	(d) Register unit and control unit on a single chip.	1
	ii.	Output of the assembler in machine codes is referred to as  (a) Object program	J
	iii.	What is SIM?	1
	111.	(c) Set interrupt mask.	
	iv.	In order to compliment the lower nibble of accumulator one can use (b) XRI 0FH	1
	v.	In 8085 microprocessor system with memory mapped I/O, which of the following is true?	1
		(d) Arithmetic and logic operations can be directly performed with the I/O data	
	vi.	Which one of the following ICs is used to interface Keyboard and Display?	1
		(b) 8279	
	vii.	The number of hardware interrupts present in 8085 are	J
	viii.	(a) 5 The cycle required to fetch and execute an instruction in 8085 microprocessor is which one of the following	1
		(d) Instruction cycle.	
	ix.	The operations executed by two or more control units are referred as (b) Macro-operations	1
	х.	Intel core2 Duo is abit processor.  (d) 64 bit	1
Q.2	i.	Size of data, address, memory word and memory capacity of 8085 microprocessor 0.5 mark each $(0.5 \text{ mark} * 4 = 2 \text{ marks})$	2
	ii.	Diagram of 8086 microprocessor – 4 marks	8
		Explanation – 4 marks	
OR	iii.	Block diagram of 8085 microprocessor – 4 marks Explanation – 4 marks	8
Q.3	i.	Definition – 1 mark Instructions – 1 mark	2

	11.	Categories of the 8085 instructions - 4 marks	8
		Examples of instruction – 4 marks	
OR	iii.	Definition of addressing modes – 2 marks	8
		Types with examples $-3$ marks	
		Program - 3 marks	
Q.4	i.	Arrangement to interface 8K X 8 size of ROM to 8085 – 1 mark	3
		Address range – 2 marks	
	ii.	Block diagram of 8255 PPI – 3 marks	7
		Explanation – 4 marks	
OR	iii.	Diagram of 8253 programmable interval timer – 3 marks	7
		Explanation – 4 marks	
Q.5	i.	Mention the number of machine cycles and T states in one byte two	4
		byte and three byte instruction 1.25 for each	
	ii.	Diagram of memory read operation in 8085 – 4 marks	6
		Explanation – 2 marks	
OR	iii.	Vectored and non-vectored interrupts of 8085 – 3 marks each	6
		(3  marks  * 2 = 6  marks)	
Q.6	i.	Definition and a bit explanation	2
	ii.	Intel Core 2 duo processor.	8
		Definition and features – 3 marks	
		Explanation – 5 marks	
OR	iii.	Intel Core i 7 Processor.	8
		Definition and features – 3 marks	
		Explanation – 5 marks	

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