Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination May-2023
CS3CO35 Microprocessor & Interfacing

Programme: B.Tech. Branch/Specialisation: CSE/All

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which of the following is true about microprocessors? **1**
(a) It has an internal memory
(b) It has interfacing circuits
(c) It contains ALU, CU, and registers
(d) It uses Harvard architecture

ii. Which of the following flag is used to mask INTR interrupt? **1**
(a) Zero flag (b) Auxiliary carry flag
(c) Interrupt flag (d) Sign flag

iii. Which of the following is a special-purpose register of microprocessor? **1**
(a) Program counter (b) Instruction register
(c) Accumulator (d) Temporary register

iv. How many address lines are present in 8086 microprocessors? **1**
(a) 16 (b) 20 (c) 32 (d) 40

v. Which of the following is true about MOV A, B instruction? **1**
(a) It means move the content of register A to register B
(b) It uses immediate addressing mode
(c) It doesn't affect the flag register
(d) It is a 2-byte instruction

vi. ISR stand for- **1**
(a) Interrupt save routine (b) Interrupt service routine
(c) Input stages routine (d) Interrupt service routing

vii. Which is a type of microprocessor that is designed with limited number of instructions? **1**
(a) CPU (b) RISC (c) ALU (d) MUX

P.T.O.

viii. How many 2k*8 ROM chips would be required to build a 16*8 memory system? **1**
(a) 2 (b) 4 (c) 8 (d) 16

ix. In stack organization the insertion operation is known as _____. **1**
(a) Pop (b) Push
(c) Both (a) and (b) (d) None of these

x. In direct memory access mode, the data transfer takes place- **1**
(a) Directly (b) Indirectly
(c) Directly and Indirectly (d) None of these

Q.2 i. What are flag register? Explain various flag registers of 8085. **3**
ii. With neat diagram explain the architecture of 8085. **7**
OR iii. With neat diagram explain the working of DMA controller. **7**

Q.3 i. Differentiate between microprocessor and microcontroller. **3**
ii. What are addressing modes in 8086? Discuss each with example. **7**
OR iii. Explain the purpose of the following signals in 8085: **7**
(a) READY (b) AD0-AD7 (c) HOLD (d) IO/ M
(e) INTR

Q.4 i. Discuss the importance of stack and subroutines in 8085 assembly language programming. **4**
ii. Describe the classifications of instructions in the 8085-instruction set. Provide an example for each classification. **6**
OR iii. Write an assembly language program to add two 8-bit numbers. **6**

Q.5 Attempt any two:
i. Explain the difference between hardware interrupts and software interrupts. Give an example of each type. **5**
ii. Compare and contrast the IO mapped I/O and memory-mapped I/O techniques. **5**
OR iii. Draw the timing diagram for the instruction "MOV A, M" and explain the T-states and machine cycles involved. **5**

Q.6 i. What is the intel architecture? **2**
ii. Explain the architecture of the intel atom processor. Describe its features and capabilities. **8**
OR iii. Describe the intel architecture and explain how an intel architecture System works. **8**

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CS3CO35 (T) Micro Processor & Interfacing

Answer of MSQ

1. c
2. c
3. a
4. b
5. c
6. b
7. b
8. c
9. b
10. a

Q.5 (i) 1 difference = 1 marks. Scan

Q5 (ii) 1 difference = 1 marks.

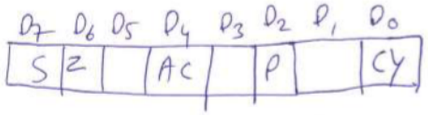
Q5 (iii) timing diagram = 3 marks,
T state & machine cycle. = 2 marks.

Q.6 (i) architecture/. = 2 marks.

(ii) block diagram
architecture of intel atom processor = 4 marks.
feature. and capability = 4 marks.

(iii) Intel architecture = 4 marks.
System works = 4 marks.

Q.2(i)



— 1 Marks

2 Marks for explanation.

Q.2 ii) 3 Marks diagram, explaination 4 marks.

Q2 (iii) Diagram — 3 marks, working 4 marks.

Q 3 (i) 3 difference = 3 marks.

Q 3 (ii) Addressing mode with example (min 5 mention)

Q 3 (iii) Ready (2 marks) AD0-AD7 (2 marks) HOLD (1 mark) IO/m (1 mark) INTR (1 mark)

Q 4 (i) Stack — 2 marks, Subroutines — 2 marks.

Q4 (ii) 1 marks for each.

Q4 (iii) Complete program with Comment.