*Total No. of Questions: 6* *Total No. of Printed Pages:3*

**Enrollment No.....**

# Faculty of Engineering

End Sem (Even) Examination May-2022

EE3CO08 / EX3CO08

Microprocessors & Microcontrollers

Programme: B.Tech. Branch/Specialisation: EE/EX

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The memory capacity of 8085 microprocessor is: **1**
(a) 64 KB (b) 1 MB (c) 16 MB (d) 640 B

ii. In 8085, which interrupt has the highest priority? **1**
(a) INTR (b) TRAP (c) RST 6.5 (d) RST 7.5

iii. The length of IP register in 8086 μP is: **1**
(a) 4 bit (b) 8 bit (c) 16 bit (d) 32 bit

iv. The BIU prefetches the instruction from memory and store them in: **1**
(a) Register (b) Queue (c) Memory (d) Stack

v. In 8255A, there are _____ I/O lines. **1**
(a) 12 (b) 24 (c) 20 (d) 10

vi. The _____ IC is useful for the generation of accurate time delay: **1**
(a) 8255 (b) 8253 (c) 8257 (d) 8259

vii. The 8051 μC has _____ 16-bit counter/timers: **1**
(a) 1 (b) 2 (c) 3 (d) 4

viii. The bit-addressable memory locations in 8051 μC are: **1**
(a) 10H - 1FH (b) 20H - 2FH
(c) 30H - 3FH (d) None of these

ix. ARM stands for: **1**
(a) Advanced Rate Machines
(b) Advanced RISC Machines
(c) Artificial Running Machines
(d) Aviary Running Machines

P.T.O.

| | | | |
|---|---|---|---|
| | x. | Which architecture provides separate buses for program and data memory?<br>(a) Harvard architecture (b) Von Neumann architecture<br>(c) Both (a) and (b) (d) None of these | **1** |
| Q.2 | i. | Explain how address de-multiplexing is carried out in 8085 μP? | **2** |
| | ii. | Differentiate between I/O mapped I/O and Memory mapped I/O interfacing techniques. | **3** |
| | iii. | Explain the addressing modes of 8085 μP with example of each one. | **5** |
| OR | iv. | Draw and explain the memory read cycle timing diagram of 8085 μP. | **5** |
| Q.3 | i. | Explain how the physical address is generated in 8086 μP? | **2** |
| | ii. | Differentiate between hardware & software interrupts of 8086 μP and explain the functions of the following pins:<br>(a) NMI (b) HOLD (c) READY (d) ALE<br>(e) TEST | **8** |
| OR | iii. | Classify all the group of instructions of 8086 μP and explain them with example of each group. | **8** |
| Q.4 | i. | Describe the transmitter block of 8251 programmable communication interface IC. | **3** |
| | ii. | Explain the DMA operations with a suitable diagram. Why is DMA controlled data transfers faster? | **7** |
| OR | iii. | Explain the operation of 8253 timer IC with its functional block diagram. | **7** |
| Q.5 | i. | Distinguish between the terms: microprocessor and microcontroller. | **3** |
| | ii. | Draw the schematic block diagram of 8051 microcontroller and explain the operation of each block. | **7** |
| OR | iii. | Describe the Timer operation of 8051 microcontroller and explain the following instructions with example:<br>(a) CJNE (b) SJMP (c) RETI (d) DJNZ<br>(e) SETB | **7** |



| | | | |
|---|---|---|---|
| Q.6 | | Attempt any two: | |
| | i. | Distinguish between Von Neumann and Harvard Architecture with diagram. | **5** |
| | ii. | Describe the salient features of a Pentium processor. | **5** |
| | iii. | Explain the register organization of ARM processor. | **5** |

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## Marking Scheme

## EE3CO08 / EX3CO08 Microprocessors & Microcontrollers

| | | | |
|---|---|---|---|
| Q.1 | i. | The memory capacity of 8085 microprocessor is:<br>(a) 64 KB | **1** |
| | ii. | In 8085, which interrupt has the highest priority?<br>(b) TRAP | **1** |
| | iii. | The length of IP register in 8086 μP is:<br>(c) 16 bit | **1** |
| | iv. | The BIU prefetches the instruction from memory and store them in:<br>(b) Queue | **1** |
| | v. | In 8255A, there are _____ I/O lines.<br>(b) 24 | **1** |
| | vi. | The _____ IC is useful for the generation of accurate time delay:<br>(b) 8253 | **1** |
| | vii. | The 8051 μC has _____ 16-bit counter/timers:<br>(b) 2 | **1** |
| | viii. | The bit-addressable memory locations in 8051 μC are:<br>(b) 20H - 2FH | **1** |
| | ix. | ARM stands for:<br>(b) Advanced RISC Machines | **1** |
| | x. | Which architecture provides separate buses for program and data memory?<br>(a) Harvard architecture | **1** |
| Q.2 | i. | Address de-multiplexing is carried out in 8085 μP? | **2** |
| | ii. | Difference b/w I/O mapped I/O and Memory mapped I/O interfacing techniques<br>1 mark for each (1 mark * 3) | **3** |
| | iii. | Addressing modes of 8085 μP with example of each one<br>1 mark for each (1 mark * 5) | **5** |
| OR | iv. | Memory read cycle timing diagram of 8085 μP<br>Diagram 3 marks<br>Explanation 2 marks | **5** |
| Q.3 | i. | Physical address is generated in 8086 μP | **2** |
| | ii. | Difference b/w hardware & software interrupts of 8086 μP<br>3 marks<br>(a) NMI (b) HOLD (c) READY (d) ALE<br>(e) TEST<br>1 mark for each (1 mark * 5) 5 marks | **8** |
| OR | iii. | Classify all the group of instructions of 8086 μP<br>Each instruction 1 mark (1 mark * 8) | **8** |
| Q.4 | i. | Transmitter block of 8251 programmable communication interface IC. | **3** |
| | ii. | DMA operations<br>Diagram 3 marks<br>Reason 2 marks<br>Explanation 2 marks | **7** |
| OR | iii. | Operation of 8253 timer IC 3 marks<br>Functional block diagram 4 marks | **7** |
| Q.5 | i. | Microprocessor and microcontroller<br>1mark for each (1 mark * 3) | **3** |
| | ii. | 8051 microcontroller<br>Schematic block diagram 3 marks<br>Operation of each block 4 marks | **7** |
| OR | iii. | Timer operation of 8051 microcontroller 2 marks<br>1 mark for each instruction with example<br>(1 mark * 5) 5 marks | **7** |
| Q.6 | | Attempt any two: | |
| | i. | Difference b/w Von Neumann and Harvard Architecture<br>3 marks<br>Diagram 2 marks | **5** |
| | ii. | Salient features of a Pentium processor<br>1 mark of each (1 mark * 5) | **5** |
| | iii. | Register organization of ARM processor<br>Explanation 2 marks<br>Diagram 3 marks | **5** |

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