Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2022

EC3EV01 Design for Testability

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The circuit should be tested at- **1**
(a) Design level (b) Chip level
(c) Transistor level (d) Switch level

ii. The stuck-at model is a _____ fault model. **1**
(a) Recurring (b) Equivalent (c) Simple (d) Logical

iii. For a n signal lines circuit _____ bridging faults are possible. **1**
(a) n (b) 2n (c) n^2 (d) n/2

iv. Data retention time comes under _____ fault. **1**
(a) Functional fault (b) Memory fault
(c) Parametric fault (d) Structural fault

v. Sequential circuit includes- **1**
(a) Delays
(b) Feedback
(c) Delays and feedback from input to output
(d) Delays and feedback from output to input

vi. Iterative test generation method suits for circuits with- **1**
(a) No feedback loops (b) Few feedback loops
(c) More feedback loops (d) Negative feedback loops only

vii. The fault simulation detects faults by- **1**
(a) Test generation
(b) Construction of fault Dictionaries
(c) Design analysis under faults
(d) All of these

viii. Boundary scan test is used to test- **1**
(a) Pins (b) Multipliers
(c) Boards (d) Wires

ix. Built-in self-test aims to- **1**
(a) Reduce test pattern generation cost
(b) Reduce volume of test data
(c) Reduce test time
(d) All of these

x. The parity check detection is done using- **1**
(a) OR gate (b) AND gate (c) XOR gate (d) NOR gate

Q.2 i. List and explain level of modeling. **2**

ii. Explain about fault-detection and redundancy **3**

iii. Define the following fault models using examples. **5**
(a) Cross-point fault (b) Multiple-stuck-at fault.

OR iv. Explain bridge fault mode and stuck on/open fault. **5**

Q.3 i. Explain the procedure involved in the path sensitization technique. **2**

ii. (a) Discuss in brief about D- algorithm. **8**
(b) Explain the Boolean difference method with an example.

OR iii. Explain the PODEM with an example. **8**

Q.4 Attempt any two:

i. Discuss about iterative method of fault diagnosis in sequential circuits using an example. **5**

ii. Describe the state table verification for sequential circuit. **5**

iii. What is functional fault model? Describe test generation based on functional fault models. **5**

Q.5 i. Differentiate between board level and system level DFT approaches. **4**

ii. List out the scan testing methods. **6**

OR iii. How is generic boundary scan handled? **6**

Q.6 Attempt any two:

i. Explain BIST architectures in detail. **5**

ii. Discuss the steps involved in design for self-test at board level. **5**

OR iii. Write short note on: **5**
(a) Exhaustive Testing (b) Pseudo Exhaustive Testing

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Scheme of Marking

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	Programme: B.Tech. | Branch/Specialisation:

Note: The Paper Setter should provide the answer wise splitting of the marks in the scheme below.

Q.1	i)	(b)	1
	ii)	(d)	1
	iii)	(c)	1
	iv)	~~(b)~~ (b) or (c)	1
	v)	(d)	1
	vi)	(b)	1
	vii)	(d)	1
	viii)	(c)	1
	ix)	(d)	1
	x)	(c)	1
Q.2	i.	1/2 marks for each level	
	ii.	1.5 marks for each	
	iii.	2.5 ~~faults~~ marks for each	
OR	iv.	1 mark - bridge fault, 2 marks each for Stuck on and open	
Q.3	i.	2 marks for 3 steps	
	ii.	4 marks for each section	
OR	iii.	Introduction - 2 marks, 6 marks explanation	
Q.4	i.	4 marks Intro. 4 marks Discussion with Example	
	ii.	2 marks Intro, 3 marks explanation with Example	
OR	iii.	2 marks definition, Description - 3 marks	
Q.5	i.	2 marks for each difference	
	ii.	2 marks for each method	
OR	iii.	Intro - 2 marks, diagram - 2 marks, discription - 2 marks	
Q.6			
	i.	Diagram - 2 marks, 3 marks theory for 2 each place	
	ii.	1.5 marks for each step	
	iii.	2.5 marks for each section	

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