Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Science / Engineering

End Sem (Odd) Examination Dec-2019

CA3CO02 Digital Electronics

Programme: BCA / BCA-MCA (Integrated) Branch/Specialisation: Computer Application

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Using 8-bits the 2's complement signed magnitude representation of $(-13)_{10}$ is **1**

(a) 11110011 (b) 01110011 (c) 11110010 (d) 01110010

ii. How many 2-input XOR, AND and OR gates are required to implement a full adder logic circuit? **1**

(a) 2, 2 and 2 (b) 2, 3 and 2 (c) 1, 3 and 1 (d) 2, 2 and 3

iii. If we want a two input AND gate to pass a signal connected at its one input, then its other input must be **1**

(a) Inverted (b) Low (c) High (d) Undefined

iv. The given K-map represents **1**

	0	1
0	1	1
1	1	0

(a) AND gate (b) OR gate (c) NOR gate (d) NAND gate

v. How many selection lines are required in an 64X1 multiplexer? **1**

(a) 7 (b) 5 (c) 6 (d) 8

vi. To generate a square wave of frequency 5kHz at the output Q of J-K flip-flop, the clock frequency should be **1**

(a) 5 kHz (b) 10 kHz (c) 2.5 kHz (d) 20 kHz

vii. In a modulo-16 counter the propagation delay of each flip-flop is 5nsec. The maximum clock frequency that can be used is **1**

(a) 50 MHz (b) 5 MHz (c) 20 MHz (d) 2 MHz

P.T.O.

viii. Which of the following is most power efficient logic family? **1**
(a) RTL (b) DTL (c) TTL (d) CMOS

ix. ROM is made up of **1**
(a) NAND and OR gates (b) Decoder and OR gates
(c) NOR gates and Decoder (d) NAND gates and Decoder

x. Which of the following is primary memory? **1**
(a) RAM and ROM (b) Hard Disk
(c) Compact Disk (d) Floppy Disk

Q.2 i. If A.B=0 and (A.C)'=0, then evaluate the Boolean expression for $f(A,B,C) = A'BC + A'B'+B'+C$. **2**

ii. Convert the numbers into desired base. **8**
(a) $(586.625)_{10} = (\quad)_2$ (b) $(F7A.B2)_{16} = (\quad)_8$
(c) $(754.12)_8 = (\quad)_{10}$ (d) $(11010010.1101)_2 = (\quad)_{10}$

OR iii. Explain the working of 4-bit binary parallel multiplier with proper logic diagram using IC-7483 and by an example. **8**

Q.3 i. What do you understand by radix or base of a number system? **2**

ii. (a) Implement a 2-input AND gate using diodes and explain its working for all input combinations. **8**
(b) Implement the given function $f(x,y,z)$ using NAND gates only.
$$f(x,y,z) = \Sigma_m(0,3,4,5,7)$$

OR iii. Find the minimal SOP and POS expression using K-map for **8**
$$f(x,y,z) = \Sigma_m(0,1,2,7,8,9,10,15)$$

Q.4 i. Explain 4x1 multiplexer with its block diagram, truth table, expression of output and logic diagram. **3**

ii. What is race-around condition? How it is eliminated by master slave flip-flop? **7**

OR iii. With the help of state table, K-map and logic diagram explain designing of a sequence generator that produces sequence 1011. **7**

Q.5 i. Explain serial-in serial-out shift register using J-K flip-flop. **4**

ii. Design a MOD-6 up counter using J-K flip-flop giving its state diagram, present state-next state table, excitation input table, excitation maps and logic circuit diagram. **6**

OR iii. Explain the working of 2-input CMOS-NAND and 2-input CMOS-NOR implementations for all possible input combinations. **6**

Q.6 Attempt any two:

i. Write any five difference between RAM and ROM. **5**

ii. Design 3-bit binary to gray code converter using ROM. **5**

iii. Write short note on: **5**
(a) Secondary memory and its types
(b) PROM and EPROM.

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Marking Scheme
CA3CO02 Digital Electronics

Q.1	i.	Using 8-bits the 2's complement signed magnitude representation of $(-13)_{10}$ is (a) 11110011		**1**
	ii.	How many 2-input XOR, AND and OR gates are required to implement a full adder logic circuit? (b) 2, 3 and 2		**1**
	iii.	If we want a two input AND gate to pass a signal connected at its one input, then its other input must be (c) High		**1**
	iv.	The given K-map represents (d) NAND gate		**1**
	v.	How many selection lines are required in an 64X1 multiplexer? (c) 6		**1**
	vi.	To generate a square wave of frequency 5kHz at the output Q of J-K flip-flop, the clock frequency should be (b) 10 kHz		**1**
	vii.	In a modulo-16 counter the propagation delay of each flip-flop is 5nsec. The maximum clock frequency that can be used is (a) 50 MHz		**1**
	viii.	Which of the following is most power efficient logic family? (d) CMOS		**1**
	ix.	ROM is made up of (b) Decoder and OR gates		**1**
	x.	Which of the following is primary memory? (a) RAM and ROM		**1**
Q.2	i.	Evaluate the Boolean expression		**2**
	ii.	Convert the numbers into desired base. 2 marks for each conversion	(2 marks*4)	**8**
OR	iii.	Logic diagram using	3 marks	**8**
		Explanation of working	3 marks	
		Example	2 marks	
Q.3	i.	Definition of radix or base of a number system		**2**
	ii.	(a) Implement a 2-input AND gate using diodes		**8**
		Implementation	1 mark	
		Working for all input combinations	2 marks	
		(b) Implement the given function $f(x, y, z)$		
		Minimization	2 marks	
		Implementation	3 marks	
OR	iii.	Find the minimal SOP and POS expression using K-map for For each minimal expression 2.5 marks (2.5 marks * 2) 1 mark for each K-Map (1 mark * 3)	5 marks 3 marks	**8**
Q.4	i.	4x1 multiplexer with its		**3**
		Block diagram	0.5 mark	
		Truth table	0.5 mark	
		Expression of output	1 mark	
		Logic diagram	1 mark	
	ii.	Explanation of race-around condition	2 marks	**7**
		Logic diagram of master slave flip-flop	2 marks	
		Explanation of master slave flip flop	3 marks	
OR	iii.	Designing of a sequence generator that produces sequence 1011.		**7**
		Explanation	1 mark	
		State table	2 marks	
		K-map and expression	2 marks	
		Logic diagram	2 marks	
Q.5	i.	Serial-in serial-out shift register using J-K flip-flop		**4**
		Logic diagram	2 marks	
		Explanation	2 marks	
	ii.	Design a MOD-6 up counter		**6**
		State diagram	1 mark	
		Present state-next state table	1 mark	
		Excitation input table	1 mark	
		Excitation maps and expressions	2 marks	
		Logic circuit diagram using J-K flip-flop	1 mark	
OR	iii.	Working of 2-input CMOS-NAND and 2-input CMOS-NOR		**6**
		Implementations		
		1 mark for each (1 mark * 2)	2 marks	
		All possible input combinations		
		2 marks for each (2 marks * 2)	4 marks	

Q.6		Attempt any two:		
	i.	Any five difference between RAM and ROM		**5**
		1 mark for each difference	(1 mark * 5)	
	ii.	Design 3-bit binary to gray code converter using ROM		**5**
		Explanation	1 mark	
		Truth table	1 mark	
		Expressions	1 mark	
		Logic diagram	2 marks	
	iii.	Write short note on:		**5**
		(a) Secondary memory and its types	2.5 mark	
		(b) PROM and EPROM.	2.5 marks	

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