Total No. of Questions: 6 *Total No. of Printed Pages:2*

Enrollment No.....

Faculty of Engineering
End Sem Examination May-2023
EE3CO08 / EX3CO08
Microprocessors & Microcontrollers

Programme: B.Tech. Branch/Specialisation: EE/EX

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which instruction is not present in 8085? **1**
(a) DAD (b) LXI (c) MUL (d) INX

ii. Which one of the following is not a vectored interrupt? **1**
(a) TRAP (b) INTR (c) RST 5.5 (d) RST 7.5

iii. PUSH operation in 8086 microprocessor- **1**
(a) Increase SP by 2 (b) Increase SP by 1
(c) Decrease SP by 2 (d) Decrease SP by 1

iv. Which is not valid? **1**
(a) MOV AX,[BX] (b) MOV AX,20[BX]
(c) MOV AX,[1000H] (d) MOV [2000H],[1000H]

v. Which is PIC (Programmable interrupt controller) controller? **1**
(a) 8259 (b) 8257 (c) 8253 (d) 8251

vi. HLDA stands for- **1**
(a) High Access (b) Hold Acknowledgement
(c) Hold Access (d) High Acknowledgement

vii. Bit addressable memory present in 8051 is- **1**
(a) 8 byte (b) 16 byte (c) 32 byte (d) 64 byte

viii. 8051 has crystal frequency of 20MHz its machine cycle is- **1**
(a) 1µs (b) 0.60 µs (c) 1.085 µs (d) 0.50 µs

ix. 80486 is _____ bit processor. **1**
(a) 32 (b) 16 (c) 64 (d) 128

P.T.O.

x. 80286 has _____ pins. **1**
(a) 32 (b) 68 (c) 40 (d) 70

Q.2 i. Define machine cycle, instruction cycle and T state. **3**
ii. Explain about memory read and write cycle, with neat sketch. **7**
OR iii. Draw and explain architecture of 8085 microprocessor. **7**

Q.3 i. Write the significance of instruction queue in 8086 microprocessors. How its size is decided? **4**
ii. Write an 8086 program to find largest number out of ten numbers stored at location 2000H:0600H? Also give comments. **6**
OR iii. Define addressing mode. Classify addressing modes for 8086 microprocessors with examples. **6**

Q.4 i. Why interfacing chips are needed? **3**
ii. Explain USART with neat diagram. **7**
OR iii. Draw and explain 8255 chip with CWR. **7**

Q.5 i. Differentiate between 8085/8086/8051 (any 3). **3**
ii. Interface 8051 microcontroller with memory of following specification: **7**
(a) 16 KB RAM
(b) 32 KB ROM
Also draw a suitable diagram.
OR iii. Classify instruction set of 8051. Describe any three with examples. **7**

Q.6 Attempt any two:
i. Write differences between Von Neumann architecture and Harvard architecture with block diagram. **5**
ii. Compare RISC and CISC in tabular format. **5**
iii. Write short note on ARM processor. **5**

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MARKING SCHEME
EE3CO08-EX3CO08 [T]
Microprocessors & Microcontrollers

Q.1	i.	Which instruction is not present in 8085? a. DAD b. LXI c. MUL d. INX	**c**
	ii.	Which one of the following is not a vectored interrupt? a. TRAP b. INTR c.RST 5.5 d. RST 7.5	**b**
	iii.	PUSH operation a. Increase SP by 16 bit b. Increase SP by 8 bit c. Decrease SP by 16 bit d. Decrease SP by 8 bit	**c**
	iv.	Which is not valid a.MOV AX,[BX] b. MOV AX,20[BX] c. MOV AX,[1000H] d. MOV [2000H],[1000H]	**d**
	v.	Which is PIC (Programmable interrupt controller) controller a. 8259 b.8257 c.8253 d.8251	**a**
	vi.	HLDA stands for a. High Access b. Hold Acknowledgement c. Hold Access d. High Acknowledgement	**b**
	vii.	Bit addressable memory present in 8051 is a. 8 byte b. 16 byte c. 32 byte d. 64 byte	**b**
	viii.	8051 has crystal frequency of 20MHz its machine cycle is a. 1µs b. 0.60 µs c. 1.085 µs d. 0.50 µs	**b**
	ix.	80486 is _____ bit processor a.32 b. 16 c.64 d. 128	**a**
	x.	80286 has _____pins a.32 b.68 c. 40 d.70	**b**
Q.2	i.	Define machine cycle, instruction cycle and T state? Definition of each 1 mark	**3**
	ii.	Explain about memory read and write cycle, with neat sketch? Memory read + diagram = 2+1.5 Memory write + diagram = 2+1.5	**7**
OR	iii.	Draw and explain architecture of 8085? Explanation +sketch = 4+3	**7**
Q.3	i.	Write the significance of instruction queue in 8086? How its size is decided? Significance 2 marks Size decision 2 marks	**4**
	ii.	Write an 8086 program to find largest number out of ten numbers stored at location 2000H: 0600H? Also give comments. ALP + comments =4+2	**6**
OR	iii.	Define addressing mode? Classify addressing modes for 8086 with examples? Definition + classification = 1+5	**6**
Q.4	i.	Why interfacing chips are needed? Detail 3 marks	**3**
	ii.	Explain USART with neat diagram? Explanation+ diagram= 4+3	**7**
OR	iii.	Draw and explain 8255 chip with CWR? Explanation+ diagram + CWR = 3+2+2	**7**
Q.5	i.	Differentiate between 8085/8086/8051 (any 3)	**3**
	ii.	Design a 8051 microcontroller with following specification: A) 16KB RAM B) 32KB ROM 3.5 Marks each	**7**
OR	iii.	Classify instruction set of 8051? Describe any 3 with examples Classify+ examples = 2+5	**7**
Q.6		Attempt any two:	
	i.	Write differences between Von Neumann architecture and Harvard architecture with block diagram? 2.5 Marks Each	**5**
	ii.	Compare RISC and CISC in tabular format? 5 parameter each has 1 marks	**5**
	iii.	Write short note on ARM processor? detail and diagram =3+2	**5**

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