Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering / Science

End Sem (Odd) Examination Dec-2022

CA3CO18 Digital Electronics

Programme: BCA/ BCA-MCA(Integrated) Branch/Specialisation: Computer Application

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. An OR gate can be imagined as- **1**
(a) Switches connected in series
(b) Switches connected in parallel
(c) MOS transistors connected in series
(d) All of these

ii. A Negative AND gate can also be treated as- **1**
(a) NOR Gate (b) OR Gate
(c) NAND Gate (d) AND Gate

iii. What would be hexadecimal of this Binary $(11001110)_2$? **1**
(a) CE (b) EC (c) 632 (d) EAC

iv. If A and B are the inputs of a half adder, the sum is given by- **1**
(a) A AND B (b) A XOR B
(c) A OR B (d) A XNOR B

v. Which flip flop does not consist of the race round problem? **1**
(a) JK flip flop (b) JK master slave
(c) T flip flop (d) None of these

vi. A digital multiplexer is a combinational circuit that selects- **1**
(a) One digital information from several sources and transmits the selected one
(b) Many digital information and convert them into one
(c) Many decimal inputs and transmits the selected information
(d) Many decimal outputs and accepts the selected information

vii. What is meant by parallel load of a shift register? **1**
(a) All FFs are present with data
(b) Each FF is loaded with data, one at a time
(c) Parallel shifting of data
(d) All FFs are set with data

P.T.O.

viii. A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it. **1**
(a) Register (b) Memory unit
(c) flip flop (d) Arithmetic logic unit

ix. Which factor determines the effectiveness of the cache? **1**
(a) Hit rate (b) Refresh cycle
(c) Refresh rate (d) Refresh time

x. USB storage device is a- **1**
(a) Secondary (b) Auxiliary (c) Tertiary (d) Primary

Q.2 i. Why NAND and NOR gates are called universal gates? **2**

ii. Minimize the following Boolean function- **8**
$F(A, B, C, D) = \Sigma m (3, 4, 5, 7, 9, 13, 14, 15)$

OR iii. Explain and state De-Morgan's theorem with truth table and logic diagrams. **8**

Q.3 i. What is ASCII code? Explain it. **2**

ii. Convert from one base to another. **8**
(a) $(1235)_{10} = (\ )_8$ (b) $(ABC)_{16} = (\ )_2$
(c) $(101101101)_2 = (\ )_8$ (d) $(5671)_{10} = (\ )_{16}$

OR iii. Design full adder with the help of two half adders. **8**

Q.4 i. Explain combinational and sequential circuit. **2**

ii. Design and explain Master slave flip flop. **8**

OR iii. What is encoder? Explain and design Octal to Binary encoder. **8**

Q.5 i. Which flip flop is used in designing registers? Why? **2**

ii. What is shift register? Design 4-bit left shift register. **8**

OR iii. Explain ring counter with the help of block diagram and truth table. **8**

Q.6 i. Why cache memory is needed? Explain it. **2**

ii. Explain the following terms: **8**
(a) Hard Disk (b) EPROM
(c) Virtual Memory (d) RAM

OR iii. Explain different memory access methods. **8**

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Marking Scheme
CA3CO18 Digital Electronics

Q.1	i.	An OR gate can be imagined as- (b) Switches connected in parallel		**1**
	ii.	A Negative AND gate can also be treated as- (c) NAND Gate		**1**
	iii.	What would be hexadecimal of this Binary $(11001110)_2$? (a) CE		**1**
	iv.	If A and B are the inputs of a half adder, the sum is given by- (b) A XOR B		**1**
	v.	Which flip flop does not consist of the race round problem? (b) JK master slave		**1**
	vi.	A digital multiplexer is a combinational circuit that selects- (a) One digital information from several sources and transmits the selected one		**1**
	vii.	What is meant by parallel load of a shift register? (a) All FFs are present with data		**1**
	viii.	A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it. (a) Register		**1**
	ix.	Which factor determines the effectiveness of the cache? (a) Hit rate		**1**
	x.	USB storage device is a- (a) Secondary		**1**
Q.2	i.	Why NAND and NOR gates are called universal gates?		**2**
	ii.	Minimize the following Boolean function-		**8**
		Drafting	4 marks	
		Minimization	4 marks	
OR	iii.	De-Morgan's theorem Statement	3 marks	**8**
		Truth table	2.5 marks	
		Logic diagrams	2.5 marks	
Q.3	i.	What is ASCII code? Explain it.		**2**
	ii.	Convert from one base to another. 2 marks for each		**8**
OR	iii.	Design full adder with the help of two half adders.		**8**
		Designing	4 marks	
		Truth table	4 marks	
Q.4	i.	Combinational	1 mark	**2**
		Sequential circuit.	1 mark	
	ii.	Design and explain Master slave flip flop.		**8**
		Designing	4 marks	
		Explanation	4 marks	
OR	iii.	Encoder	4 marks	**8**
		Design Octal to Binary encoder	4 marks	
Q.5	i.	Which flip flop is used in designing registers? Why?		**2**
	ii.	Shift register	4 marks	**8**
		Design 4-bit left shift register.	4 marks	
OR	iii.	Ring counter	3 marks	**8**
		Block diagram	2.5 marks	
		Truth table	2.5 marks	
Q.6	i.	Why cache memory is needed? Explain it.		**2**
	ii.	Explain the following terms: 2 marks for each (a) Hard Disk (b) EPROM (c) Virtual Memory (d) RAM		**8**
OR	iii.	Four memory access methods 2 marks for each		**8**

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