Total No. of Questions: 21

Enrollment No : _____

MEDICAPS UNIVERSITY

Faculty of Engineering

End Semester Examination May 2025

EC3EV01 Design for Testability

Programme	:	B.Tech.	**Branch/Specialisation**	:	EC
Duration	:	3 hours	**Maximum Marks**	:	60

Note: *All questions are compulsory. Internal choices, if any, are indicated. Assume suitable data if necessary. Notations and symbols have their usual meaning.*

Section 1 (Answer all question(s))

		Marks	CO	BL
Q1.	If any signal line is permanently connected to Vdd power supply then it causes- ○ Bridge fault ○ Transistor fault ○ Delay fault ◉ Stuck at fault	1	1	2
Q2.	Stuck open fault is a type of- ◉ Transistor fault ○ Behavioral fault ○ Logical fault ○ Power supply fault	1	1	1
Q3.	D- Algorithm was developed by- ○ P. Goel ◉ Roth ○ Fujiwara ○ Cheng	1	2	1
Q4.	Decisions are made only at primary inputs in _____ algorithm. ○ Path sensitization ○ D- algorithm ◉ PODEM ○ FAN	1	2	2
Q5.	Time frame expansion method belongs to- ○ Delay fault testing ◉ Structural testing ○ Power testing ○ Functional testing	1	2	2
Q6.	Which logic is used in sequential ATPG? ○ 2-valued ○ 4-valued ○ 7-valued ◉ 9-valued	1	2	1
Q7.	Which is not an Ad-hoc technique of DFT? ○ Avoid asynchronous logic feedbacks ○ Make flip-flops initializable ◉ Using gates with a large number of fan-in signals ○ Provide test control for difficult-to-control signals	1	3	2
Q8.	To make board testing convenient we use- ◉ Boundary scan ○ Ad hoc testing ○ Exhaustive testing ○ State table verification	1	3	1
Q9.	BIST stands for- ○ Binary input sequential testing ○ Binary input synchronous testing ○ Built in sequential test ◉ Built in Self Test	1	4	1

Q10. Testing in which circuit is partitioned in sub-circuits and then all possible input combinations are applied to each sub-circuit? **1 4 1**

- ○ Exhaustive testing
- ◉ Pseudo exhaustive testing
- ○ Pseudo random testing
- ○ Deterministic testing

Section 2 (Answer all question(s))

Marks CO BL

Q11. Define defect and fault for VLSI circuits. **2 1 1**

Rubric	Marks
Define defect Define fault	2

Q12. Discuss various stuck at faults in detail. **3 1 2**

Rubric	Marks
single stuck at 0 fault, single stuck at 1 fault,Multiple stuck at faults	3

Q13. (a) What do you mean by Bridging faults in ICs? How such faults are modelled? Explain with example. **5 1 2**

Rubric	Marks
Definition, types / models, example circuits	5

(OR)

(b) Discuss Transistor faults in detail.

Rubric	Marks
Definition, Stuck open fault, Stuck on fault	5

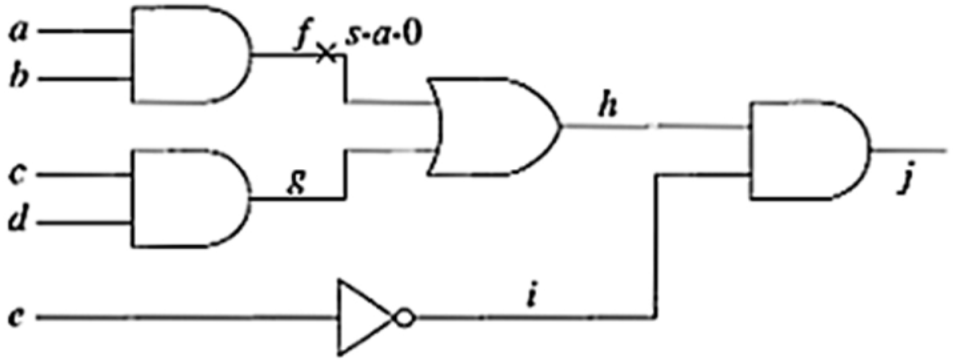
Section 3 (Answer all question(s))

Marks CO BL

Q14. How Boolean difference is defined? Discuss various properties of it. **4 2 2**

Rubric	Marks
Definition, Properties	4

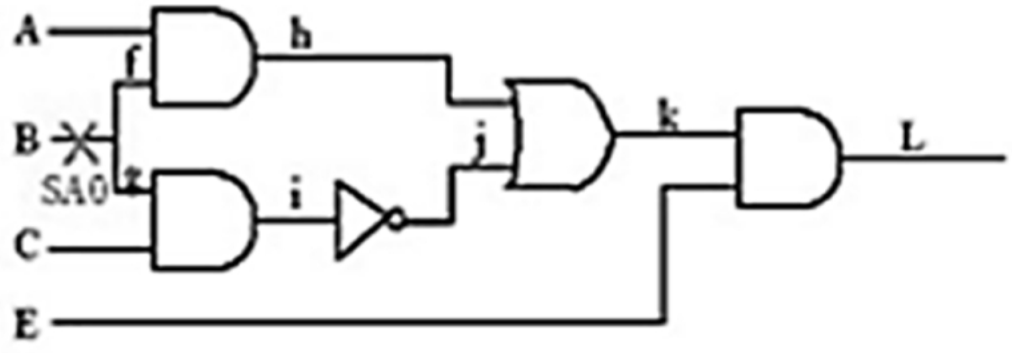
Q15. (a) Explain various steps of Path sensitization method of ATPG. Derive test vectors for given fault by using same method. **6 2 3**



Rubric	Marks
At least 3 Steps, solution	6

(OR)

(b) Derive test vectors for given fault using D-algorithm.



Rubric	Marks
fault activation, fault effect propagation, justification and test vecors	6

Section 4 (Answer all question(s))

Marks CO BL

Q16. Why ATPG for sequential circuit is more difficult than combinational circuit? Justify your answer. **3 2 2**

Rubric	Marks
1 marks for each reason	3

Q17. (a) Design a test experiment for given machine: **7 2 3**

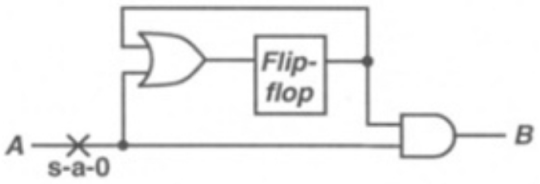
Present state	Input $x=0$	Input $x=1$
A	$C,1$	$D,0$
B	$D,0$	$B,1$
C	$B,0$	$C,1$
D	$C,0$	$A,0$

Next state, output

Rubric	Marks
Synchronizing/homing sequence,Distinguishing sequence,final test sequence	7

(OR)

(b) Show that a test for the fault A s-a-0 in the circuit cannot be obtained using the five-valued logic of the D-calculus. Obtain a test for this fault using the nine-valued logic.



Rubric	Marks
Showing inability of 5 valued logic,solution by 9 valued logic	7

Section 5 (Answer all question(s))

Q18. Discuss controllability and observability with examples. **Marks CO BL: 4 3 2**

Rubric	Marks
controllability and observability , example	4

Q19. (a) Discuss level sensitive scan design in detail. **6 3 2**

Rubric	Marks
Diagrams,Discussion	6

(OR)

(b) Explain Boundary scan architecture with appropriate diagrams.

Rubric	Marks
Diagrams,Explanation	6

Section 6 (Answer all question(s))

Q20. Write some advantages of BIST. **Marks CO BL: 3 4 2**

Rubric	Marks
At least 3 advantages	3

Q21. (a) Discuss test pattern generation techniques for BIST. Which one is preferred mostly? **7 4 3**

Rubric	Marks
At least 3 techniques: Preference	7

(OR)

(b) Write a note on BIST architecture.

Rubric	Marks
Diagrams, Discussion	7

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