*Total No. of Questions: 6* *Total No. of Printed Pages:3*

**Enrollment No.....**

Faculty of Engineering

End Sem (Even) Examination May-2019

EE3CO21 / EX3CO21 Digital Electronics

Programme: B.Tech. Branch/Specialisation: EE/EX

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated.Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Convert 59.7210 to BCD **1**

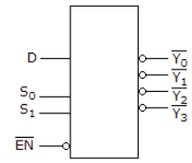
(a) 111011 (b) 01011001.011100100001

(c) 1110.11 (d) 01011001011100100001

ii. A binary number's value changes most drastically when the _____ is changed. **1**

(a) MSB (b) Frequency (c) LSB (d) Duty Cycle

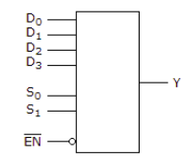
iii. For the device shown here, assume the D input is LOW, both S inputs are HIGH, and the $\overline{EN}$ input is HIGH. What is the status of the $\overline{Y}$ outputs? **1**




(a) All are High (b) All High except $\overline{Y}_0$

(b) All are Low (d) All Low except $\overline{Y}_0$

iv. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be LOW. What is the status of the Y output? **1**




(a) Low (b) High

(c) Don't Care (d) Cannot be Determined

P.T.O.

v. On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____. **1**
(a) Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0
(b) Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 0
(c) Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1
(d) Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 1

vi. If J = K (J and K are shorte(d) in a JK flip-flop, what circuit is made **1**
(a) SR flip-flop (b) Shorted JK flip-flop
(c) T Flip-flop (d) D Flip-Flop

vii. Which of the following memories uses one transistor and one capacitor as basic memory unit **1**
(a) SRAM (b) DRAM
(c) Both (a) and (b) (d) None of these

viii. The storage element for a static RAM is the _____ **1**
(a) Diode (b) Resistor (c) Capacitor (d) Flip-Flop

ix. Which logic family provide minimum power dissipation **1**
(a) TTL (b) CMOS (c) ECL (d) JFET

x. Using the schematic diagram of a TTL NAND gate, determine the state of each transistor (ON or OFF) when all inputs are high. **1**
(a) Q1-ON, Q2-OFF, Q3-ON, Q4-OFF
(b) Q1-ON, Q2-ON, Q3-OFF, Q4-OFF
(c) Q1-OFF, Q2-OFF, Q3-ON, Q4-ON
(d) Q1-OFF, Q2-ON, Q3-OFF, Q4-ON

Q.2 i. State and prove De Morgan's Theorem. **2**

ii. Convert $Y = A + B\bar{C} + AB + \bar{A}BC$ into standard SOP form **3**

iii. Minimize the following expression: using Tabulation Method **5**
f = ∑m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)

OR iv. Minimize the following logic function using K-maps and realize using NAND gate. **5**
F(A, B, C, D) = ∑m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)

Q.3 i. Implement the function using 8×1 multiplexer using $F = \sum(0, 1, 3, 4, 8, 9, 15)$ **4**



ii. Draw the logic diagram of binary to octal decoder and explain the working in detail. **6**

OR iii. Design a 4-bit magnitude comparator with 3 outputs: A>B, A=B, A<B. **6**

Q.4 i. Realize JK flip flop using SR flip flop. **4**

ii. Design a MOD-5 Ripple counter using a 3-bit ripple counter. **6**

OR iii. Explain in detail about ring counter with its logic diagram, state diagram and its sequence table. **6**

Q.5 Attempt any two:

i. Draw a RAM cell and explain its working in details. **5**

ii. Write short note on with suitable schematic **5**
(a) Programmable Logic Array (PLA)
(b) Static and Dynamic MOS RAM

iii. Explain in brief EPROM and EEPROM. **5**

Q.6 Attempt any two:

i. Explain briefly the operation of TTL NAND gate with the help of a neat diagram. **5**

ii. Compare the performance of TTL and CMOS logic. **5**

iii. Explain the features of CMOS. **5**

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## Marking Scheme
## EE3CO21 / EX3CO21 Digital Electronics

| | | | |
|---|---|---|---|
| Q.1 | i. | Convert 59.7210 to BCD<br>(b) 01011001.011100100001 | **1** |
| | ii. | A binary number's value changes most drastically when the _____ is changed.<br>(a) MSB | **1** |
| | iii. | For the device shown here, assume the D input is LOW, both S inputs are HIGH, and the $\overline{EN}$ input is HIGH. What is the status of the $\bar{Y}$ outputs?<br>(a) All are High | **1** |
| | iv. | For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be LOW. What is the status of the Y output?<br>(a) Low | **1** |
| | v. | On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____.<br>(c) Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1 | **1** |
| | vi. | If J = K (J and K are shorted) in a JK flip-flop, what circuit is made<br>(c) T Flip-flop | **1** |
| | vii. | Which of the following memories uses one transistor and one capacitor as basic memory unit<br>(b) DRAM | **1** |
| | viii. | The storage element for a static RAM is the _____<br>(d) Flip-Flop | **1** |
| | ix. | Which logic family provide minimum power dissipation<br>(b) CMOS | **1** |
| | x. | Using the schematic diagram of a TTL NAND gate, determine the state of each transistor (ON or OFF) when all inputs are high.<br>(d) Q1-OFF, Q2-ON, Q3-OFF, Q4-ON | **1** |
| Q.2 | i. | De Morgan's Theorem.<br>Statement 1 mark<br>Proof 1 mark | **2** |
| | ii. | Convert $Y = A + B\bar{C} + AB + \bar{A}BC$ into standard SOP form<br>Complete solution | **3** |
| | iii. | Minimize the following expression: using Tabulation Method<br>Prime implicants 3.5 marks<br>Essential prime implicants 1.5 marks | **5** |
| OR | iv. | K-maps value feed 1 mark<br>Grouping 1 mark<br>Equation 1 mark<br>Diagram using NAND gate 2 marks | **5** |
| Q.3 | i. | Implementation | **4** |
| | ii. | Binary to octal decoder<br>Truth table 2 marks<br>K-Map + Equation 2 marks<br>Circuit diagram 2 marks | **6** |
| OR | iii. | 4-bit magnitude comparator with 3 outputs: A>B, A=B, A<B.<br>Truth table 2 marks<br>K-Map + Equation 2 marks<br>Circuit diagram 2 marks | **6** |
| Q.4 | i. | Realize JK flip flop using SR flip flop.<br>Truth table 2 marks<br>Circuit diagram 2 marks | **4** |
| | ii. | Design a MOD-5 Ripple counter using a 3-bit ripple counter.<br>Truth table 2 marks<br>K-Map + Equation 2 marks<br>Circuit diagram 2 marks | **6** |
| OR | iii. | Ring counter<br>Truth table 2 marks<br>K-Map + Equation 2 marks<br>State diagram 1 mark<br>Circuit diagram 1 mark | **6** |
| Q.5 | | Attempt any two: | |
| | i. | RAM cell<br>Diagram 2 marks<br>Working 3 marks | **5** |
| | ii. | Write short note on with suitable schematic<br>(a) Programmable Logic Array (PLA) 2.5 marks<br>(b) Static and Dynamic MOS RAM 2.5 marks | **5** |

| | | | | |
|---|---|---|---|---|
| | iii. | EPROM | 2.5 marks | **5** |
| | | EEPROM. | 2.5 marks | |
| Q.6 | | Attempt any two: | | |
| | i. | Operation of TTL NAND gate | | **5** |
| | | Diagram | 2.5 marks | |
| | | Explanation | 2.5 marks | |
| | ii. | Comparison b/w performance of TTL and CMOS logic. | | **5** |
| | | At least 10 points 0.5 mark for each | (0.5 mark * 10) | |
| | iii. | Features of CMOS. | 2.5 marks | **5** |
| | | Diagram | 2.5 marks | |

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