| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Q.4 | i. | Convert Decimal Number $(15.50)_{10}$ into 32-bit single precision floating point binary number using IEEE-754 floating point representation. | **3** | 3 | 3 | 1 | 2 |
| | ii. | Explain Booth's algorithm. Show step by step process for multiplication using Booth's algorithm to Multiply the number (-7) and (+5) in binary. | **7** | 3 | 3 | 1 | 1 |
| OR | iii. | Describe the memory hierarchy in computer systems, including the roles of cache memory, main memory, and secondary storage. Discuss how this hierarchy improves system performance by balancing speed, cost, and capacity. | **7** | 2 | 2 | 3 | 1 |
| Q.5 | i. | Explain the purpose and types of input/output (I/O) devices in a computer system. Discuss how I/O devices differ from each other based on speed and functionality and provide examples of each type. | **3** | 2 | 1 | 3 | 2 |
| | ii. | Define the concept of handshaking in I/O communication. Explain how handshaking helps to synchronize data transfer between a computer and an I/O device and provide an example of how it works in practice. | **7** | 2 | 1 | 3 | 1 |
| OR | iii. | What is Direct Memory Access (DMA)? Explain how DMA data transfer works and describe its advantages over CPU-controlled data transfer methods. | **7** | 2 | 3 | 4 | 1 |
| Q.6 | | Attempt any two: | | | | | |
| | i. | Define RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) architectures. Compare their main characteristics and give examples of applications where each is beneficial. | **5** | 2 | 2 | 4 | 1 |
| | ii. | Explain the difference between an instruction pipeline and an arithmetic pipeline. Provide examples of each type and describe where they are commonly used. | **5** | 2 | 1 | 5 | 1 |
| | iii. | Describe pipeline hazards and their types, including data, structural, and control hazards. Discuss one method used to resolve each type of hazard. | **5** | 2 | 1 | 5 | 1 |

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*Total No. of Questions: 6* *Total No. of Printed Pages:4*

**Enrollment No.....**

# Faculty of Engineering
## End Sem Examination Dec 2024
## IT3CO31 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: IT

**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

| | | | **Marks** | **BL** | **PO** | **CO** | **PSO** |
|---|---|---|---|---|---|---|---|
| Q.1 | i. | Which component in the von Neumann architecture is responsible for storing both data and instructions?<br>(a) Control Unit<br>(b) Arithmetic Logic Unit (ALU)<br>(c) Memory Unit<br>(d) Input/Output System | **1** | 1 | 1 | 1 | 1 |
| | ii. | Which of the following is a type of machine instruction that modifies the content of registers?<br>(a) Transfer instruction<br>(b) Arithmetic instruction<br>(c) Logical instruction<br>(d) Shift instruction | **1** | 1 | 1 | 2 | 1 |
| | iii. | In an Arithmetic Logic Unit (ALU), which of the following operations is not typically performed?<br>(a) Addition (b) Multiplication<br>(c) Comparison (d) Data Transfer | **1** | 1 | 1 | 1 | 1 |
| | iv. | In a stack-based organization, the operation that removes the top element from the stack is called:<br>(a) Push (b) Pop (c) Load (d) Fetch | **1** | 1 | 1 | 2 | 1 |
| | v. | In memory hierarchy, which type of memory is closest to the CPU and offers the fastest access times?<br>(a) Hard disk (b) Cache memory<br>(c) RAM (d) Secondary storage | **1** | 1 | 1 | 3 | 1 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| vi. | In fixed-point binary arithmetic, what happens if an addition operation produces a result larger than the allocated bits?<br>(a) Overflow occurs<br>(b) The result is stored as is<br>(c) The sign bit is adjusted<br>(d) The result is rounded to zero | **1** | 1 | 1 | 2 | 1 |
| vii. | Which of the following is a characteristic of Direct Memory Access (DMA) data transfer?<br>(a) The CPU handles each data transfer individually<br>(b) It requires handshaking for every data word transferred<br>(c) Data transfer occurs through programmed I/O<br>(d) Data transfer occurs without CPU intervention | **1** | 1 | 1 | 4 | 1 |
| viii. | The concept of "handshaking" in I/O communication refers to:<br>(a) A process where the CPU manages multiple I/O devices at once<br>(b) A method to directly transfer data from I/O to memory<br>(c) A signal exchange protocol to synchronize data transfer<br>(d) A technique to buffer data for future transfers | **1** | 1 | 1 | 4 | 1 |
| ix. | Which of the following is a primary characteristic of Reduced Instruction Set Computer (RISC) architecture?<br>(a) Simple and fewer instructions with uniform instruction length<br>(b) Instructions that combine multiple operations<br>(c) Multiple addressing modes for each instruction<br>(d) A large set of complex instructions | **1** | 1 | 1 | 3 | 1 |
| x. | A pipeline stall can be used to resolve which type of hazard in pipeline processing?<br>(a) Data Hazard (b) Structural Hazard<br>(c) Control Hazard (d) All of these | **1** | 1 | 1 | 5 | 1 |
| Q.2 i. | Describe the roles of the Program Counter (PC) and Accumulator (AC) in the execution of a program. | **2** | 2 | 1 | 2 | 1 |
| ii. | Define register transfer language (RTL) and explain its role in computer design. | **3** | 2 | 1 | 1 | 1 |



| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| iii. | Describe the Von Neumann architecture and explain its primary components. How does this model influence the organization and design of modern computers? | **5** | 3 | 2 | 2 | 1 |
| OR iv. | What is an instruction cycle? Describe its main phases, such as fetch, decode, and execute. How do these phases work together to complete an instruction? | **5** | 2 | 2 | 2 | 1 |
| Q.3 i. | Define direct addressing and indirect addressing in the context of memory access. Provide a brief example of each. | **2** | 2 | 2 | 2 | 1 |
| ii. | At memory address 200, two words instructions, load to AC is stored with a mode bit as a most significant bit, at location 201 the address stored is 500. At location 202 next instructions is stored. The following numbers are stored at different memory locations as shown:<br>If the content of PC is 200, while the content of register R1 is 400, XR register is 100. If all the numbers and address are in decimal number, find out content of AC and effective address for the following addressing modes-<br>(a) Direct address (b) Indirect address<br>(c) Relative address (d) Indexed address | **8** | 3 | 3 | 4 | 2 |
| OR iii. | Compare and contrast hardwired control and microprogrammed control in controller design. Explain the advantages and disadvantages of each approach and discuss scenarios where one is preferred over the other. | **8** | 2 | 2 | 1 | 1 |

| Memory location (Address) | Memory content |
|---|---|
| 399 | 450 |
| 400 | 700 |
| 500 | 800 |
| 600 | 900 |
| 702 | 325 |
| 800 | 300 |

## Marking Scheme

IT3CO31 (T) Computer System Architecture (T)

| | | | |
|---|---|---|---|
| Q.1 | i) | C) Memory Unit | **1** |
| | ii) | B) Arithmetic instruction | **1** |
| | iii) | D) Data Transfer | **1** |
| | iv) | B) Pop | **1** |
| | v) | A) Overflow occurs | **1** |
| | vi) | B) Cache memory | **1** |
| | vii) | D) Data transfer occurs without CPU intervention | **1** |
| | viii) | C) A signal exchange protocol to synchronize data transfer | **1** |
| | ix) | A) Simple and fewer instructions with uniform instruction length | **1** |
| | x) | D) All of the above | **1** |

| | | | |
|---|---|---|---|
| Q.2 | i. | Describe the roles of the Program Counter (PC) and Accumulator (AC) in the execution of a program. | **2** |
| | ii. | Define register transfer language (RTL) and explain its role in computer design. | **3** |
| | iii. | Describe the Von Neumann architecture and explain its primary components. 3M<br>How does this model influence the organization and design of modern computers? 2M | **5** |
| OR | iv. | What is an instruction cycle? 1M<br>Describe its main phases, such as fetch, decode, and execute. 2M<br>How do these phases work together to complete an instruction? 2M | **5** |

| | | | |
|---|---|---|---|
| Q.3 | i. | Define direct addressing and indirect addressing in the context of memory access. Provide a brief example of each. | **2** |
| | ii. | At memory address 200, two words instructions, load to AC is stored with a mode bit as a most significant bit, at location 201 the address stored is 500. At location 202 next instructions is stored. The following numbers are stored at different memory locations as shown: | **8** |

| Memory location (Address) | Memory content |
|---|---|
| 399 | 450 |
| 400 | 700 |
| 500 | 800 |
| 600 | 900 |
| 702 | 325 |
| 800 | 300 |

If the content of PC is 200, while the content of register R1 is 400, XR register is 100. If all the numbers and address are in decimal number, find out content of AC and effective address for the following addressing modes-
(i) Direct address 2M
(ii) Indirect address 2M
(iii) Relative address 2M
(iv) Indexed address 2M

| | | | |
|---|---|---|---|
| OR | iii. | Compare and contrast hardwired control and microprogrammed control in controller design. 3M<br>Explain the advantages and disadvantages of each approach and discuss scenarios where one is preferred over the other. 5M | **8** |

| | | | |
|---|---|---|---|
| Q.4 | i. | Convert Decimal Number $(15.50)_{10}$ into 32-bit single precision floating point binary number using IEEE-754 floating point representation. | **3** |
| | ii. | Explain Booth's algorithm. Show step by step process for multiplication using Booth's algorithm to Multiply the number (-7) and (+5) in binary. | **7** |
| OR | iii. | Describe the memory hierarchy in computer systems, including the roles of cache memory, main memory, and secondary storage. 3M<br>Discuss how this hierarchy improves system performance by balancing speed, cost, and capacity. 4M | **7** |

| | | | |
|---|---|---|---|
| Q.5 | i. | Explain the purpose and types of input/output (I/O) devices in a computer system. 1M<br>Discuss how I/O devices differ from each other based on speed and functionality, and provide examples of each type. 2M | **3** |
| | ii. | Define the concept of handshaking in I/O communication. 2M<br>Explain how handshaking helps to synchronize data transfer between a computer and an I/O device 3M | **7** |

P.T.O.

provide an example of how it works in practice. 2M

OR iii. What is Direct Memory Access (DMA)? 2M **7**
Explain how DMA data transfer works and 2M
Describe its advantages over CPU-controlled data transfer methods. 3M

Q.6 Attempt any two:

i. Define RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) architectures. 1M **5**
Compare their main characteristics and give examples of applications where each is beneficial. 4M

ii. Explain the difference between an instruction pipeline and an arithmetic pipeline. 2M **5**
Provide examples of each type and describe where they are commonly used. 3M

iii. Describe pipeline hazards and their types, including data, structural, and control hazards. 2M **5**
Discuss one method used to resolve each type of hazard. 3M

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