Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2022

EC3CO07 / EE3CO21 / EX3CO21 Digital Electronics

Programme: B.Tech. Branch/Specialisation: EC/EE/EX

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The binary equivalent of $(0.6875)_{10}$ is_____. **1**

(a) $(0.1011)_2$ (b) $(0.1101)_2$ (c) $(0.1110)_2$ (d) $(0.0111)_2$

ii. For the given binary numbers X=1010100 and Y=1000011, the result of X-Y and Y-X respectively is- **1**

(a) 0110001 and 1001110 (b) 1010001 and 0101110

(c) 1101110 and 0010001 (d) 0010001 and 1101110

iii. The simplified minimum literal representations for the Boolean expressions $x+x'y$ and $x(x'+y)$ respectively is- **1**

(a) $x'y$ and $x+y'$ (b) $x+y'$ and $x'+y$

(c) $x+y$ and xy (d) xy and $x+y$

iv. For the given Boolean function $F=A'C+A'B+AB'C+BC$, the minimal sum of products expression is- **1**

(a) $F= A'C+A'B$ (b) $F= C+A'B$

(c) $F=AB'C+BC$ (d) $F=A'C+A'B+AB'C$

v. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates. **1**

(a) AND or OR gates (b) XOR or XNOR gates

(c) NOR or NAND gates (d) AND or NOR gates

vi. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? **1**

(a) 0 to 2^n (b) 0 to $2^n + 1$ (c) 0 to $2^n - 1$ (d) 0 to $2^{n+1/2}$

vii. The 32 x 8 memory would contain _____words, each _____bits long, for a total capacity of _____bits. **1**

(a) 32, 8, 256 (b) 8, 32, 256

(c) 32, 32, 256 (d) 8, 8, 256

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viii. PLA contains _____. **1**
(a) AND and OR arrays (b) NAND and OR arrays
(c) NOT and AND arrays (d) NOR and OR arrays

ix. TTL devices consume substantially _____ power than equivalent CMOS devices at rest. **1**
(a) Less (b) More (c) Equal (d) Very High

x. CMOS behaves as a/an _____. **1**
(a) Adder (b) Subtractor (c) Inverter (d) Comparator

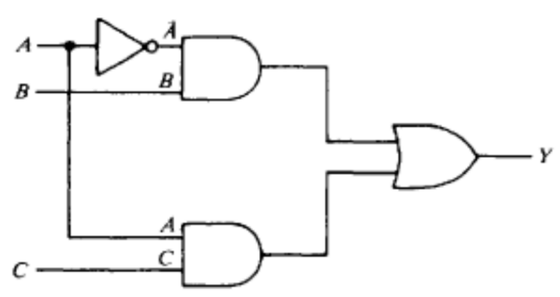
Q.2 i. Convert decimal 153 to octal using division method. **2**

ii. What is a Boolean function? How it can be represented? Explain by taking an example. **3**

iii. Find the complement of the functions $F_1=x'yz'+x'y'z$ and $F_2= x(y'z'+yz)$ **5**

OR iv. Express the Boolean function $F=A+B'C$ in a sum of minterms. **5**

Q.3 i. What is the Boolean expression for the AND-OR logic diagram? **2**



ii. Design a combinational circuit that converts BCD to excess-3 code converter by implementing the truth table and logic circuit. **8**

OR iii. Implement the following function using a Multiplexer: $F(A,B,C,D)=\sum(0,1,3,4,8,9,15)$ **8**

Q.4 i. Enumerate the differences between combinational circuit and sequential circuit with suitable examples. **3**

ii. What is a Master-slave flip flop? Draw the logic diagram of a master-slave D flip flop. Use NAND gates. **7**

OR iii. Design and implement a mod-6 asynchronous counter using T-flip flops **7**

Q.5 i. A certain memory has a capacity of 8K x 16. **4**
(a) How many data input and data output lines does it have?
(b) How many address lines does it have?
(c) What is its capacity in bytes?

ii. Explain ROM with a block diagram. How a ROM is organized? What are the various types of ROMs? Explain in detail. **6**

OR iii. Write a short note on Programmable Logic Devices with explanation of PLA and PAL. **6**

Q.6 Attempt any two:

i. Give a comparative analysis of logic families TTL, ECL, MOS, CMOS and IIL on the basis of commonly used specific parameters. **5**

ii. What are the different techniques of interfacing TTL and CMOS? Explain in detail. **5**

iii. With the help of a neat circuit diagram, explain the working of **5**
(a) A MOS inverter
(b) A two-input MOS NAND gate
(c) A two-input MOS NOR gate.

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Marking Scheme

EC3CO07 / EE3CO21 / EX3CO21 Digital Electronics

Q.1	i.	The binary equivalent of $(0.6875)_{10}$ is_____. (a) $(0.1011)_2$		**1**
	ii.	For the given binary numbers X=1010100 and Y=1000011, the result of X-Y and Y-X respectively is- (d) 0010001 and 1101110		**1**
	iii.	The simplified minimum literal representations for the Boolean expressions $x+x'y$ and $x(x'+y)$ respectively is- (c) $x+y$ and xy		**1**
	iv.	For the given Boolean function $F=A'C+A'B+AB'C+BC$, the minimal sum of products expression is- (b) $F= C+A'B$		**1**
	v.	A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates. (c) NOR or NAND gates		**1**
	vi.	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? (c) 0 to $2^n - 1$		**1**
	vii.	The 32 x 8 memory would contain _____words, each _____bits long, for a total capacity of _____bits. (a) 32, 8, 256		**1**
	viii.	PLA contains _____. (a) AND and OR arrays		**1**
	ix.	TTL devices consume substantially _____ power than equivalent CMOS devices at rest. (b) More		**1**
	x.	CMOS behaves as a/an _____. (c) Inverter		**1**
Q.2	i.	Convert decimal 153 to octal using division method. As per solution		**2**
	ii.	Boolean function It can be represented	2 marks 1 mark	**3**
	iii.	Complement of the functions $F_1=x'yz'+x'y'z$ $F_2= x(y'z'+yz)$	2.5 marks 2.5 marks	**5**
OR	iv.	Boolean function $F=A+B'C$ in a sum of minterms As per the solution		**5**
Q.3	i.	Boolean expression for the AND-OR logic diagram		**2**
	ii.	Design a combinational circuit Implementing the truth table and logic circuit Explanation	2 marks 3 marks 3 marks	**8**
OR	iii.	Implement function using a Multiplexer: 1 mark for each	(1 mark * 8)	**8**
Q.4	i.	Differences b/w combinational circuit and sequential circuit with examples. 1 mark for each difference	(1 mark * 3)	**3**
	ii.	Definition of Master-slave flip flop Logic diagram of a master-slave D flip flop	3 marks 4 marks	**7**
OR	iii.	Diagram Implement a mod-6 asynchronous counter using T-flip flops	3 marks 4 marks	**7**
Q.5	i.	(a) Data input and data output lines (b) Address lines (c) Its capacity in bytes	2 marks 1 mark 1 mark	**4**
	ii.	Explanation of ROM Block Diagram Types of ROMs	2 marks 2 marks 2 marks	**6**
OR	iii.	Programmable Logic Devices with explanation of PLA PAL	 3 marks 3 marks	**6**
Q.6		Attempt any two:		
	i.	Comparative analysis of logic families TTL, ECL, MOS, CMOS and IIL on the basis of commonly used specific parameters 1 mark for each parameter	 (1 mark * 5)	**5**
	ii.	Techniques of interfacing TTL CMOS	2.5 marks 2.5 marks	**5**
	iii.	With the help of a neat circuit diagram, explain the working of (a) A MOS inverter (b) A two-input MOS NAND gate (c) A two-input MOS NOR gate	 1 mark 2 marks 2 marks	**5**

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