Total No. of Questions: 22

Enrollment No : _____

MEDICAPS UNIVERSITY

Faculty of Engineering

End Semester Examination May 2025

EC3EV03 Low Power VLSI Design

Programme	:	B.Tech.	**Branch/Specialisation**	:	EC
Duration	:	3 hours	**Maximum Marks**	:	60

Note: *All questions are compulsory. Internal choices, if any, are indicated. Assume suitable data if necessary. Notations and symbols have their usual meaning.*

Section 1 (Answer all question(s))

		Marks	CO	BL
Q1.	The typical quiescent power dissipation of low-power CMOS circuits is- ○ 01 mW ○ 0.5 mW ◉ 2 nW ○ 50 nW	1	1	2
Q2.	Static power reduction technique is- ○ Power gating ○ Multiple threshold voltages ○ Variable threshold voltages ◉ All of these	1	2	1
Q3.	What is the design flow of VLSI system? I. architecture design II. market requirement III. logic design IV. HDL coding ◉ II-I-III-IV ○ IV-I-III-II ○ III-II-I-IV ○ I-II-III-IV	1	1	2
Q4.	Mechanism affects the subthreshold leakage current is- ○ DIBL effect ○ Narrow width affect ○ Effect of channel length ◉ All of these	1	2	1
Q5.	To reduce power dissipation in a circuit, C (Capacitance) must be- ○ Maximum ◉ Minimum ○ Infinite ○ 10F	1	3	1
Q6.	If C=0.2F, V_{DD}=3V and f=0.5Hz than dynamic power will be- ○ 0.5 Watt ◉ 0.9 Watt ○ 1.9 Watt ○ 2.0 Watt	1	3	3
Q7.	The completion time for multiplication time in Braun method is- ○ n ○ 2n ○ 3n ◉ 4n	1	4	1
Q8.	The storage element present in DRAM is- ○ Diode ◉ Capacitor ○ MOSFET ○ Flip-flop	1	4	1
Q9.	The primary reason for applying probabilistic analysis is- ○ Computational efficiency ○ Signal correlations ○ Spurious Transition ◉ Signal glitches	1	5	2

Q10. Which type of simulation mode is used to check the timing performance of a design? **1 5 2**

- ○ Behavioural
- ○ Switch-level
- ○ Transistor-level
- ◉ Gate-level

Section 2 (Answer all question(s))

Marks CO BL

Q11. Derive the noise margins for CMOS inverter. **2 1 2**

Rubric	Marks
Noise Margin	2

Q12. Draw the static CMOS logic circuit for expression- $Y = (D(A = BC))'$. **3 1 3**

Rubric	Marks
Construct CMOS logic circuit	3

Q13. (a) Explain the static and dynamic power dissipation in CMOS circuit with necessary diagram and expressions. **5 1 2**

Rubric	Marks
Definition	1
Explanation with expression	4

(OR)

(b) List out the sources of power dissipation in VLSI circuits and explain any two in detail.

Rubric	Marks
Name the sources	1
Explanation	4

Section 3 (Answer all question(s))

Marks CO BL

Q14. Explain charge leakage mechanism in MOS transistors. **3 2 2**

Rubric	Marks
Explanation	3

Q15. (a) What are the advantages and challenges of using high-k dielectrics in semiconductor devices? **7 2 2**

Rubric	Marks
Advantages	4
Challenges	3

(OR)

(b) Draw the block diagram of a typical low power chip based on variable-threshold CMOS circuits and explain its operation.

Rubric	Marks
Block Diagram	2
Description	5

Section 4 (Answer all question(s))

Marks CO BL

Q16. Explain how voltage scaling helps to reduce power dissipation in a CMOS integrated circuit. **3 3 3**

Rubric	Marks
Explanation	3

Q17. (a) Describe low power VLSI design techniques at algorithmic level. **7 3 3**

Rubric	Marks
Name the techniques	2
Description	5

(OR)

(b) Explain how pipelined and parallel architecture help to reduce power dissipation in low power VLSI design.

Rubric	Marks
pipelined architecture	3.5
parallel architecture	3.5

Section 5 (Answer all question(s))

Marks CO BL

Q18. Draw the carry look ahead adder architecture and identify its key components. **4 4 3**

Rubric	Marks
carry look ahead adder architecture	2
key components	2

Q19. (a) What is Braun Multiplier? Estimate its architecture, performance and speed consideration. **6 4 3**

Rubric	Marks
Define Braun Multiplier	1
architecture	2
performance	1
speed consideration	2

(OR)

(b) Write the different techniques to reduce power dissipation in a SRAM.

Rubric	Marks
Name the techniques.	2
Description	4

Section 6 (Answer any 2 question(s))

Marks CO BL

Q20. Analyse probabilistic power estimation technique at the circuit level. **5 5 4**

Rubric	Marks
Analyze	5

Q21. Explain different techniques of software power estimation. **5 5 3**

Rubric	Marks
Name different techniques	1
Description	4

Q22. Compute the transition density and static probability of Y=AB + C given P(a) = 0.2, P(b) = 0.3, P(c) = 0.4, D(a) = 1, D(a) = 2, D(a) = 3. **5 5 5**

Rubric	Marks
transition density, D(y) = [P(b){1 - P(c)} * 1] + [P(a){1 - P(c)} * 2] + [{1 – P(a)P(b)} * 3] = 3.24	3
static probability, P(y) = P(a)P(b) + P(c) - P(a)P(b)P(c) = 0.436	2

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