| | | | |
|---|---|---|---|
| Q.5 | i. | What is I/O Interface? Why the I/O interface is required? Draw and explain I/O interface. | **4** |
| | ii. | What is serial and parallel data transmission? Explain the handshaking method for asynchronous data transfer. | **6** |
| OR | iii. | What are data transfer modes? Explain the programmed I/O, Interrupt initiated I/O and DMA mode of data transfer. | **6** |
| Q.6 | | Attempt any two: | |
| | i. | What is pipeline processing? Explain the arithmetic pipelining with the help of an example. Also draw the space time diagram for a four-segment pipeline showing the time it takes to process eight tasks. | **5** |
| | ii. | What is an Array processor? Describe the types of Array processor. | **5** |
| | iii. | A Non- pipelined system takes 100 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 20 ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speed up that can be achieved? | **5** |

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*Total No. of Questions: 6* *Total No. of Printed Pages:4*

**Enrollment No.....**

# Faculty of Engineering

## End Sem (Even) Examination May-2022

## CS3CO22 / IT3CO20 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: CSE/IT

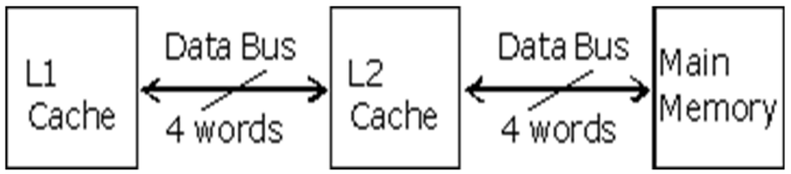
**Duration: 3 Hrs.** **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

| | | | |
|---|---|---|---|
| Q.1 | i. | What are the major components of a CPU?<br>(a) Control Unit, Register Set, Arithmetic Logic Unit<br>(b) Control Unit, Memory Unit, Arithmetic Logic Unit<br>(c) Memory Unit, Arithmetic Logic Unit, Auxiliary Memory<br>(d) Register Set, Control Unit, Memory Unit | **1** |
| | ii. | Consider the following sequence of micro-operations:<br>MBR ← PC<br>MAR ← X<br>PC ← Y<br>Memory ← MBR<br>Which one of the following is a possible operation performed by this sequence?<br>(a) Instruction fetch<br>(b) Operand fetch<br>(c) Conditional branch<br>(d) Initiation of interrupt service | **1** |
| | iii. | The addressing mode/s, which uses the PC instead of a general purpose register is _____.<br>(a) Indexed with offset (b) Relative<br>(c) Direct (d) Both (a) and (c) | **1** |
| | iv. | A word whose individual bits represent a control signal is _____.<br>(a) Command Word (b) Control word<br>(c) Co-ordination word (d) Generation word | **1** |

v. In IEEE754 Floating point representation of 64-bit binary number (Double precision) have following format: **1**
(a) 1-bit for Sign, 11-bit for Exponent, 52-bit for Mantissa
(b) 1-bit for Sign, 16-bit for Exponent, 47-bit for Mantissa
(c) 1-bit for Sign, 18-bit for Exponent, 45-bit for Mantissa
(d) 2-bit for Sign, 11-bit for Exponent, 51-bit for Mantissa

vi. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer? **1**




(a) 2 nanoseconds (b) 20 nanoseconds
(c) 22 nanoseconds (d) 88 nanoseconds

vii. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is- **1**
(a) Exceptions (b) Signal Handling
(c) Interrupts (d) DMA

viii. The DMA transfers are performed by a control circuit called as- **1**
(a) Device Interface (b) DMA Controller
(c) Data Controller (d) Overlooker

ix. In pipelining, the Speedup ratio, $S= nt_n/(k+n-1)t_p$, where k denotes as_____ . **1**
(a) No. of registers (b) No. of Segment
(c) No. of clock cycles (d) No. of Tasks

x. Which are not the conflicts occurred in instruction pipelining. **1**
(a) Resource conflicts (b) Data dependency
(c) Branch difficulties (d) Operand forwarding



Q.2 i. What is Register? Explain the function of Accumulator (AC) and MAR? **2**

ii. A digital computer has a common bus system for 8 register of 8 bit each. The bus is constructed with multiplexers- **3**
(a) How many selection inputs are there in each multiplexer?
(b) What size of multiplexer is needed?
(c) How many multiplexer are there in the bus?

iii. Draw Von-Neumann Model? Explain the subsystem of Von Neumann model? What is meant by Von-Neumann bottleneck? **5**

OR iv. What is Instruction cycle? Draw and explain the fetch, decode and execute phase of basic instruction cycle? **5**

Q.3 i. Write any three differences between hardwired and micro-programmed control unit with example? **3**

ii. What is addressing mode? Which addressing modes are used to show the displacement of program into memory? Explain following addressing modes with an example- **7**
(a) Direct addressing (b) Indirect addressing
(c) Relative addressing (d) Indexed addressing mode

OR iii. What is stack based organization? Write an algorithm for implementing PUSH and POP operation, when stack memory is constructed through 64 registers set for stack-based organization. Write a program to evaluate following arithmetic expression in zero-address instruction format: X= (A+B) * (C+D). **7**

Q.4 i. Convert Decimal Number $(+138.78)_{10}$ into 32-bit single precision floating point binary number using IEEE-754 floating point representation. **3**

ii. Explain the Booth's Algorithm with flowchart. **7**
Multiply (-29) * (+19) using booth's multiplication algorithm?

OR iii. What is CAM (Content Addressable Memory)? Explain the types of cache updating schemes. A cache is having 60% hit ratio for read operation. Cache access time is 30 ns and main memory access time is 100 ns, 50% operations are read operation. What will be the average access time for read operation? **7**

# Marking Scheme
## CS3CO22 / IT3CO20 Computer System Architecture

Q.1 i. What are the major components of a CPU? **1**
(a) Control Unit, Register Set, Arithmetic Logic Unit

ii. Consider the following sequence of micro-operations: **1**

MBR ← PC
MAR ← X
PC ← Y
Memory ← MBR

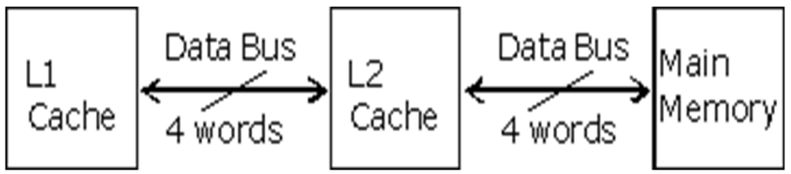
Which one of the following is a possible operation performed by this sequence?
(d) Initiation of interrupt service

iii. The addressing mode/s, which uses the PC instead of a general purpose register is _____. **1**
(b) Relative

iv. A word whose individual bits represent a control signal is _____. **1**
(b) Control word

v. In IEEE754 Floating point representation of 64-bit binary number (Double precision) have following format: **1**
(a) 1-bit for Sign, 11-bit for Exponent, 52-bit for Mantissa

vi. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer? **1**




(c) 22 nanoseconds

vii. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is- **1**
(c) Interrupts

viii. The DMA transfers are performed by a control circuit called as- **1**
(b) DMA Controller

ix. In pipelining, the Speedup ratio, $S= nt_n/(k+n-1)t_p$, where k denotes as_____ . **1**
(b) No. of Segment

x. Which are not the conflicts occurred in instruction pipelining. **1**
(d) Operand forwarding

| | | | | |
|---|---|---|---|---|
| Q.2 | i. | Definition of Register | 1 mark | **2** |
| | | Function of Accumulator (AC) and MAR | | |
| | | 0.5 mark for each (0.5 mark *2) | 1 mark | |
| | ii. | (a) Selection inputs are there in each multiplexer | 1 mark | **3** |
| | | (b) Size of multiplexer is needed | 1 mark | |
| | | (c) Multiplexer are there in the bus | 1 mark | |
| | iii. | Diagram of Von-Neumann Model | 1 mark | **5** |
| | | Subsystem of Von Neumann model | 3 mark | |
| | | Von-Neumann bottleneck | 1 mark | |
| OR | iv. | Instruction cycle definition | 1 mark | **5** |
| | | Draw the basic instruction cycle | 2 marks | |
| | | Explanation of phases | 2 marks | |
| Q.3 | i. | Any three differences b/w hardwired and micro-programmed control unit | | **3** |
| | | 1 mark for each | (1 mark * 3) | |
| | ii. | Addressing mode definition | 1 mark | **7** |
| | | Which addressing modes are used for displacement | 2 marks | |
| | | Addressing modes with an example | | |
| | | 1 mark for each (1 mark * 4) | 4 marks | |
| OR | iii. | Definition of stack based organization | 1 mark | **7** |
| | | Algorithm for implementing PUSH operation | 2 marks | |
| | | Algorithm for implementing POP operation | 2 marks | |
| | | Arithmetic expression in zero-address instruction | 2 marks | |
| Q.4 | i. | Convert Decimal Number $(+138.78)_{10}$ into 32-bit single precision | | **3** |
| | | As per the solution | | |
| | ii. | Booth's Algorithm flowchart | 3 marks | **7** |
| | | Multiplication using Booth's Algorithm | 4 marks | |

| | | | | |
|---|---|---|---|---|
| OR | iii. | Definition of CAM (Content Addressable Memory) | 1 mark | **7** |
| | | Types of cache updating schemes | 3 marks | |
| | | Average access time for read operation | 3 marks | |
| Q.5 | i. | Definition of I/O Interface | 1 mark | **4** |
| | | Reason for requirement of I/O interface | 1 mark | |
| | | Draw I/O interface and explain | 2 marks | |
| | ii. | Definition of serial and parallel data transmission | 2 marks | **6** |
| | | Handshaking method for asynchronous data transfer | | |
| | | 2 marks for each (2 marks * 2) | 4 marks | |
| OR | iii. | Definition of data transfer modes | 1 mark | **6** |
| | | Programmed I/O | 1 mark | |
| | | Interrupt initiated I/O | 2 marks | |
| | | DMA mode of data transfer | 2 marks | |
| Q.6 | | Attempt any two: | | |
| | i. | Definition of pipeline processing | 1 mark | **5** |
| | | Arithmetic pipelining | 2 marks | |
| | | Draw the space time diagram | 2 marks | |
| | ii. | Definition of Array processor | 1 mark | **5** |
| | | Types of Array processor | | |
| | | 2 marks for each (2 marks * 2) | 4 marks | |
| | iii. | Determine the speedup ratio | 3 marks | **5** |
| | | Maximum speed up | 2 marks | |

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