Enrollment No.

MEDI-CAPS UNIVERSITY
Knowledge is Power

Faculty of Engineering
Mid Sem I Examination March - 2023
CS3CO35 Microprocessor & Interfacing

Programme: B.Tech. Branch/Specialisation: CSE

Duration: 1.5 Hrs. **Maximum Marks: 30**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q. (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

			Marks	BL	CO	PO	PSO
Q.1	i.	What is maximum address capacity of 8085 Microprocessor? a. 64KB b. 1 MB c. 4 KB d. 32KB	1	BL02	CO1	PO3, PO11	
	ii.	There are _____ general purpose registers in 8085 processor a. 5 b. 6 c. 7 d. 8	1	BL01	CO1	PO3, PO11	
	iii.	Which of the following interrupt is non-vectored in 8085? a. RST 7.5 b. RST 6.5 c. TRAP d. INTR	1	BL02	CO1	PO3, PO11	
	iv.	What is stored in the H & L general-purpose register? a. Opcode b. Address of memory c. Address of next instruction d. Temporary data	1	BL01	CO2	PO3, PO5, PO11	
	v.	Which of the following is a 2-byte instruction? a. LDA 2500H b.MOV A, B c. IN 01H d. JMP 2085H	1	BL02	CO2	PO3, PO5, PO11	
	vi.	With respect to operating system which of	1	BL01			

	vi.	Which addressing mode execute its instructions within CPU without the necessity of reference memory for operands? a. Implied Mode b. Immediate Mode c. Direct Mode d. Register Mode		BL02	CO2	PO3, PO5, PO11
Q.2	i.	What do you mean by interrupt?	2		CO1	PO3
	ii.	Explain features of DMA operation.	2		CO1	PO3, PO11
	iii.	What is demultiplexing of Address/ Data lines in 8085 Microprocessor, why it is needed.	3		CO1	PO3, PO11
	iv.	Draw and explain architecture of 8085 Microprocessor.	5			PO3, PO11
OR	v.	Explain these PINs of 8085 Microprocessor: READY, ALE, TRAP, HOLD, RES'	5	BL		PO3, PO11
Q.3	i.	What is instruction set? explain.	2	BL02		
	ii.	What is subroutine? explain with example.	4	BL01	CO	
	iii.	Explain addressing modes of 8085 microprocessor with examples.	6	BL02	CO2	
OR	iv.	Explain these instructions with example: ADD, LXI, MOV, PUSH, XCHG, INX				

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