Marking Scheme

EC3CO20 (T) VLSI Design

Q.1	i)	A	**1**
	ii)	C	**1**
	iii)	C	**1**
	iv)	C	**1**
	v)	A	**1**
	vi)	B	**1**
	vii)	A	**1**
	viii)	D	**1**
	ix)	A	**1**
	x)	A	**1**
Q.2	i.	Pass transistor logic	**1**
		Demerits, remedies	**1**
	ii.	Y-chart	**1**
		VLSI design process	**2**
	iii.	Operation of MOSFET	**3**
		Equation for drain current in linear and saturation region	**2**
OR	iv.	Structure and working of a transmission gate	**3**
		4×1 multiplexer using transmission gates	**2**
Q.3	i.	DC transfer characteristics of CMOS inverter	**2**
	ii.	Two input CMOS XOR gate	**4, 4**
OR	iii.	Various types of power dissipation	**4**
		Expression for total power dissipation	**4**
Q.4	i.	Steps involved in the design	**3**
	ii.	Mealy and Moore machines	**7**
OR	iii.	Design the circuit with (a) JK flip-flops, (b) D flip-flops	**4, 3**
Q.5	i.	Hazards in combinational logic circuits	**2**
		Differentiate between static and dynamic hazards?	**2**
	ii.	Design an asynchronous circuit	**6**
OR	iii.	Design an asynchronous circuit	**6**
Q.6	i.	What is FPGA?	**1**
		Constructional details with diagram.	**3**
		Advantages of FPGA.	**1**
	ii.	Draw logic structure of an IC 7575 PLA	**2**
		Explain logic structure of an IC 7575 PLA	**2**
		Common method of PLA design interconnects.	**1**
	iii.	N-well CMOS IC fabrication	**5**

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Q.6 Attempt any two:

i. What is FPGA? Explain its constructional details with diagram. What are the advantages of FPGA? **5**

ii. Draw and explain logic structure of an IC 7575 PLA with 14 inputs and 8 outputs. Describe common method of PLA design interconnects. **5**

iii. Explain N-well CMOS IC fabrication sequence with the help of neat diagrams. **5**

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Total No. of Questions: 6 *Total No. of Printed Pages:4*

Enrollment No.....

Faculty of Engineering

End Sem Examination May-2024

EC3CO20 VLSI Design

Programme: B.Tech. Branch/Specialisation: EC

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. The design flow of VLSI system is- **1**

I. Architecture design
II. Market requirement
III. Logic design
IV. HDL coding

(a) II-I-III-IV (b) IV-I-III-II
(c) III-II-I-IV (d) I-II-III-IV

ii. Increasing V_{sb} _____ the threshold voltage. **1**

(a) Does not effect
(b) Decreases
(c) Increases
(d) Exponentially increases

iii. In CMOS Invertor, if p-transistor is conducting and has small voltage between source and drain, then it is said to work in **1**

(a) Linear region
(b) Saturation region
(c) Non saturation resistive region
(d) Cut-off region

iv. When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is: **1**

(a) 1 or V_{dd} or HIGH state
(b) 0 or ground or LOW state
(c) High impedance or floating(Z)
(d) None of these

v. Statement 1: Mealy machine reacts faster to inputs **1**
Statement 2: Moore machine has more circuit delays
Choose the correct option:
(a) Statement 1 is true and Statement 2 is true
(b) Statement 1 is true but Statement 2 is false
(c) Statement 1 is false and Statement 2 is true
(d) None of these

vi. Finite state machines are used for- **1**
(a) Deterministic test patterns
(b) Algorithmic test patterns
(c) Random test patterns
(d) Pseudo random test patterns

vii. How to eliminate critical races? **1**
Statement 1: Use transition state(s)
Statement 2: Use other secondary assignment, so that all transitions involve only 1 secondary change.
(a) Statement 1 is true and Statement 2 is true
(b) Statement 1 is true but Statement 2 is false
(c) Statement 1 is false and Statement 2 is true
(d) None of these

viii. If the value of the output remains at a static condition "0", but goes to logic 1 immediately during the changes of input states, then the hazards are known as- **1**
(a) Static 1 hazards (b) Static 2 hazards
(c) Dynamic hazards (d) Static 0 hazards

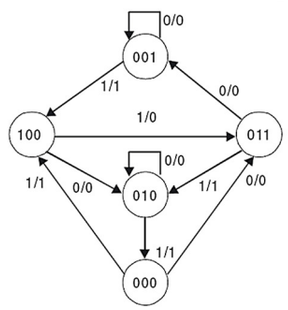
ix. The process by which Aluminium is grown over the entire wafer, also filling the contact cuts is? **1**
(a) Sputtering (b) Chemical vapour deposition
(c) Epitaxial growth (d) Ion Implantation

x. Positive photo resists are used more than negative photo resists because- **1**
(a) Negative photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo resists
(b) Positive photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the negative photo resists
(c) Negative photo resists are less sensitive to light
(d) Positive photo resists are less sensitive to light

Q.2 i. Explain pass transistor logic. What are its demerits and how it can be remedied? **2**
ii. Draw the Y-chart and explain VLSI design process. **3**
iii. Explain the operation of MOSFET with necessary diagrams. Also derive equation for drain current in linear and saturation region of operation. **5**
OR iv. Explain the structure and working of a transmission gate. Implement 4×1 multiplexer using transmission gates. **5**

Q.3 i. Draw and explain the DC transfer characteristics of CMOS inverter. **2**
ii. Draw the circuit diagram and layout of a two input CMOS XOR gate. **8**
OR iii. Explain the various types of power dissipation in CMOS inverter. Derive the expression for total power dissipation of a CMOS inverter. **8**

Q.4 i. Write down the steps involved in the design of synchronous sequential circuits. **3**
ii. Explain Mealy and Moore machines with the help of state diagram and state table. Take suitable example. **7**
OR iii. A sequential circuit has one input and one output. The state diagram is shown below. Design the circuit with (a) JK flip-flops, (b) D flip-flops. **7**



Q.5 i. How are hazards found in combinational logic circuits? Differentiate between static and dynamic hazards. **4**
ii. Design an asynchronous circuit that will output only the first pulse received and will ignore any other pulses. **6**
OR iii. Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output Z. The output Z = 1 if x_1 changes from 0 to 1, Z = 0 if x_2 changes from 0 to 1, and Z = 0 otherwise. Realize the circuit using D flip-flop. **6**