Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering / Science
End Sem Examination Dec-2023
CS3CO34 / BC3CO54 Computer System Architecture

Programme: B.Tech. / B.Sc Branch/Specialisation: CSE All / Computer Science

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. Which operation is extremely useful in serial transfer of data? **1**

(a) Logical micro-operation (b) Arithmetic micro-operation
(c) Shift micro-operation (d) All of these

ii. The average time required to reach a storage location in memory and obtain its contents is called- **1**

(a) Seek time (b) Turnaround time
(c) Access time (d) Transfer time

iii. If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10 ns memory) is- **1**

(a) 0.93 (b) 0.9 (c) 0.88 (d) 0.87

iv. The simplest method of controlling sequence of instruction execution is to have each instruction explicitly specify- **1**

(a) The address of next instruction to be run
(b) Address of previous instruction
(c) Both (a) and (b)
(d) None of these

v. In signed-magnitude binary division, if the dividend is $(11100)_2$ and divisor is $(10011)_2$ then the result is- **1**

(a) $(00100)_2$ (b) $(10100)_2$ (c) $(11001)_2$ (d) $(01100)_2$

vi. The addressing mode used in an instructions of the form ADD X Y is- **1**

(a) Absolute (b) Indirect (c) Index (d) None of these

vii. Which of the following memory unit communicates directly with the CPU? **1**

(a) Auxiliary memory (b) Main memory
(c) Secondary memory (d) None of these

P.T.O.

viii. TRAP is a _____ interrupt which has the _____ priority among all other interrupts. **1**
(a) Maskable, lowest
(b) Non-maskable, highest
(c) Maskable, second-lowest
(d) Non-maskable, second-highest

ix. Which one of the following is a characteristic of CISC (Complex Instruction Set Computer)? **1**
(a) Fixed format instructions
(b) Variable format instructions
(c) All instructions are executed in single clock cycle
(d) None of these

x. SMID represents an organization that _____. **1**
(a) Refers to a computer system capable of processing several programs at the same time
(b) Represents organization of single computer containing a control unit, processor unit and a memory unit
(c) Includes many processing units under the supervision of a common control unit
(d) None of these

Q.2 i. List the functional units of a computer system. **2**
ii. Design an 8x4 memory subsystem constructed from two 8x2 ROM chips. **3**
iii. Explain the different levels of hierarchy of bus systems. **5**
OR iv. What is micro-operation? List the different categories of micro-operations with example. **5**

Q.3 i. Define register indirect mode. **2**
ii. Compare assembly language with high level language. Write a program using assembly language of 8085 microprocessor to check whether a given number is odd or even. If the given number is even then display '1' on its SOD line. Give the flow chart also. **8**
OR iii. Define instruction cycle. Explain instruction cycle in detail with flowchart. **8**

Q.4 i. What do you mean by overflow and underflow in floating point numbers? **3**

ii. Explain Booth's Algorithm for multiplying binary integers. Also draw the flowchart to support your answer. **7**
OR iii. Discuss Hardware implementation of addition and subtraction of signed-magnitude data with the help of a neat block diagram. **7**

Q.5 i. How does cache inconsistency occur in caches due to process migration and I/O? **4**
ii. Consider the design of a three-level memory hierarchy with the following specifications for memory characteristics- **6**

Memory Level	Access time	Capacity	Cost/Kbyte
Cache	t1=25 ns	s1=512 Kbyte	c1=$1.25
Main Memory	t2=903 ns	s2=32 Mbyte	c2=$0.2
Disk array	t3=4 ns	s3=39.8 Gbytes	c3=$0.0002

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.
(a) Calculate the effective access time.
(b) Calculate the total memory cost.
OR iii. What is DMA controller? Explain with the help of block diagram. **6**

Q.6 Attempt any two:
i. Compare the characteristics of CISC and RISC Architecture. **5**
ii. Explain Flynn's classification of computer architecture. **5**
iii. Write a short note on arithmetic pipelining. **5**

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Marking Scheme
Computer System Architecture (T) CS3CO34 (T)- BC3CO54 (T)

Q.1	i)	(c) Logical micro operation	**1**
	ii)	(c) access time	**1**
	iii)	(b) 0.9	**1**
	iv)	(a) The address of next instruction to be run	**1**
	v)	(b) $(10100)_2$	**1**
	vi)	(c) index	**1**
	vii)	(b) Main memory	**1**
	viii)	(b) non-maskable, highest	**1**
	ix)	(b) variable format instructions	**1**
	x)	(c) includes many processing units under the supervision of a common control unit	**1**
Q.2	i.	List the functional unit of a computer System	(As per explanation)
	ii.	3 Marks to all.	
	iii.	A hierarchical bus system …..as I/O buses.	(As per explanation)
OR	iv.	The L bat is Micro	2 Marks
		List	3 Marks
Q.3	i.	In this mode, the data ….register A.	(As per explanation)
	ii.	8 Marks for attempting	
OR	iii.	Define instruction cycle.	3 Marks
		Instruction….flowchart.	5 Marks
Q.4	i.	overflow means ….. exponent field.	(As per explanations)
	ii.	Booth's ……registers.	(As per explanations)
OR	iii.	Addition …..Numbers	3 Marks
		Diagram of Hardware Implemention	4 Marks
Q.5	i.	n a example, the cache ……. of data.	(As per explanations)
	ii.	The effective memory access time	3 Marks
		Memory cost is calculated by;	3 Marks
OR	iii.	Explain	4 Marks
		Diagram	2 Marks
Q.6			
	i.	(As per explanation)	
	ii.	(As per explanation)	
	iii.	Flow chart diagram	2 Marks
		Explain	3 Marks

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