Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem Examination Dec-2023

IT3CO31 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: IT

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d. Assume suitable data if necessary. Notations and symbols have their usual meaning.

Q.1 i. During the execution of a program which gets initialized first? **1**

(a) MDR (b) IR (c) PC (d) MAR

ii. What is the purpose of the "opcode" in a machine instruction? **1**

(a) It specifies the memory address of the operand.

(b) It indicates the operation to be performed.

(c) It stores data values.

(d) It controls the flow of the program.

iii. In Micro programmed control unit, Micro program consisting of _____ is stored in control memory of control unit. **1**

(a) Instruction (b) Micro instruction

(c) Micro program (d) Macro instruction.

iv. The addressing mode/s, which uses the PC instead of a general purpose register is _____. **1**

(a) Indexed with offset (b) Relative

(c) Direct (d) Both (a) and (c)

v. Given the following binary number in 32-bit (single precision) IEEE-754 format: 01000001000101000000000000000000, What is the equivalent decimal value? **1**

(a) +8.25 (b) -8.25 (c) +9.25 (d) -9.25

vi. Whenever the data is found in the cache memory it is called as _____. **1**

(a) HIT (b) MISS

(c) FOUND (d) ERROR

vii. A handshake based protocol for data transfer is an example of _____ type of data transfer. **1**

(a) Synchronous (b) Asynchronous

(c) Indirect (d) Inter-leaving

viii. The DMA controller has _____ register. **1**
(a) 4 (b) 2 (c) 3 (d) 1

ix. Which of the following is not a common pipeline hazard? **1**
(a) Structural hazard (b) Data hazard
(c) Control hazard (d) Instruction hazard

x. In a pipeline, what is the purpose of the "Execute" stage? **1**
(a) To fetch the next instruction
(b) To decode the instruction
(c) To perform the operation specified by the instruction
(d) To write the result to memory

Q.2 i. Explain the address bus in computer system. **2**

ii. Describe Von-Neumann architecture. **3**

iii. Write a program to evaluate the arithmetic statement into two address, one address and zero address: **5**
X= (A+B)*(C+D)

OR iv. What is instruction cycle? Draw flow chart and explain fetch phase, decode phase, and execute phase of an instruction cycle. **5**

Q.3 i. How the CPU has organized with stack implementation? **2**

ii. What is the function of control unit? Explain hardwired and micro programmed control unit. **8**

OR iii. At memory address 200, two word instructions, load to AC is stored with a mode bit as a most significant bit, at location 201 the address stored is 500. At location 202 next instructions is stored. The following numbers are stored at different memory locations as shown: **8**

Memory location (Address)	Memory content
399	450
400	700
500	800
600	900
702	325
800	300

If the content of PC is 200, while the content of register R1 is 400, XR register is 100. If all the numbers and address are in decimal number, find out content of AC and effective address for the following addressing modes-
(a) Direct address (b) Indirect address
(c) Relative address (d) Indexed address

Q.4 i. Convert decimal number $(53.125)_{10}$ into 32-bit single precision floating point binary number using IEEE-754 floating point representation. **4**

ii. Explain Booth's Algorithm. Show the step-by-step multiplication using Booth's algorithm to multiply the number (+7) and (-3) in binary. **6**

OR iii. Consider a computer system with cache memory and main memory of size 32KB and 4GB respectively. The cache memory block size is 32B which uses direct mapping. Assume that the memory is byte addressable then find out the number of bits needed for cache indexing and tag bits respectively. **6**

Q.5 i. Difference between programmed I/O and Interrupt-initiated I/O. **4**

ii. What is serial and parallel data transmission? Draw and explain the concept of handshaking through source initiated and destination initiated method in asynchronous data transfer? **6**

OR iii. Explain direct memory access. What is meant by burst transfer and cycle stealing? **6**

Q.6 Attempt any two:

i. Explain the concept of instruction pipelining in a CPU. What are the stages of a typical instruction pipeline? **5**

ii. What are pipeline hazards in the context of instruction execution? How can they be mitigated or resolved? **5**

iii. In what scenarios would a vector processor be more advantageous than a pipelined processor? **5**

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