

DIRECT MEMORY ACCESS (DMA):-

Programmed I/O and interrupt I/O provide data transfer between the Microprocessor and external devices. However, there are various instances when data must be moved between memory and external devices.

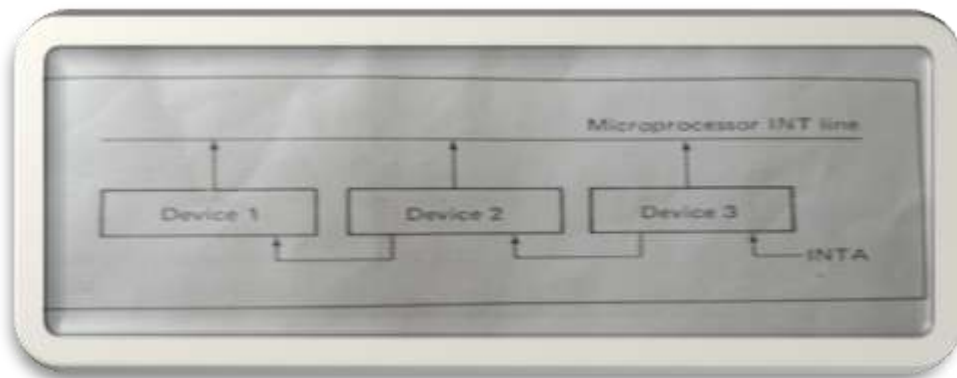


Fig (1) three devices connected to INT in a daisy chain

For example, a mass storage device, such as a cassette recorder, one may want to input or output programmed data to or from microcomputer RAM. Since the DMA performs data transfer memory and an external device without involving the CPU, the interface or controller chip must be perform memory read and write operations in similar way as microprocessor.

DMA controller chip typically provides by the following:-

- 1- the DMA controller chip puts the microprocessor in a hold state by means of the HOLD control signal. In this state the microprocessor stops executing the program and disconnect the address, data
- 2- the DMA controller chip takes over the microcomputer as soon as it receives the DMA acknowledge signal from the microprocessor. It puts RAM location on the address and the appropriate control signal on the control bus to transfer data between RAM and I/O device.

3- the DMA controller chip controls the RAM and an I/O device it transfers control of the system bus to the microprocessor by removing the microprocessor from the HOLD state.

processor halt DMA:-

In this type of DMA, data transfer is performed between the memory and peripheral device either by completely stopping the microprocessor until the transfer is completed or by technique called *cycle stealing*. In either case, the microprocessor is stopped for DMA operation. the first method transfers a complete block of data and is known as *block transfer DMA*

The decision of which type of DMA should be used depends on the length of the data block. If the data block is large, block transfer DMA is recommended. On the other hand, for small data blocks cycle stealing DMA is used. Also, if the microprocessor cannot be kept inactive in a particular application for the time needed for the block transfer, or cycle stealing DMA must be used. With either block transfer or cycle stealing, a DMA controller chip controls the DMA operation, and is independent of the microprocessor.

The DMA controller chip typically consists of:-

1. register:- containing the address of the data to be transferred to or from. The address register is incremented by 1 each time a byte is transferred. thus, data is transferred in a sequential order.
2. counter:- containing the length of the data to be transferred and is decremented by 1 each time a byte is transferred. When this counter reaches zero, the DMA transfer is completed.

The address register and the counter are normally loaded by the microprocessor.

We know describe the block transfer DMA and cycle stealing DMA:-

A. block transfer DMA:-this is the most common type of DMA used with microprocessors. As mentioned before in this type of DMA the peripheral device request the DMA transfer via DMA request line , which is connected directly or through a DMA controller chip to the microprocessor . the microprocessor completes the current instruction and sends a DMACK to the peripheral device in order to indicate that the bus can be used for DMA operation. The DMA controller chip then completes the DMA transfer and transfers the control of the bus to the microprocessor.

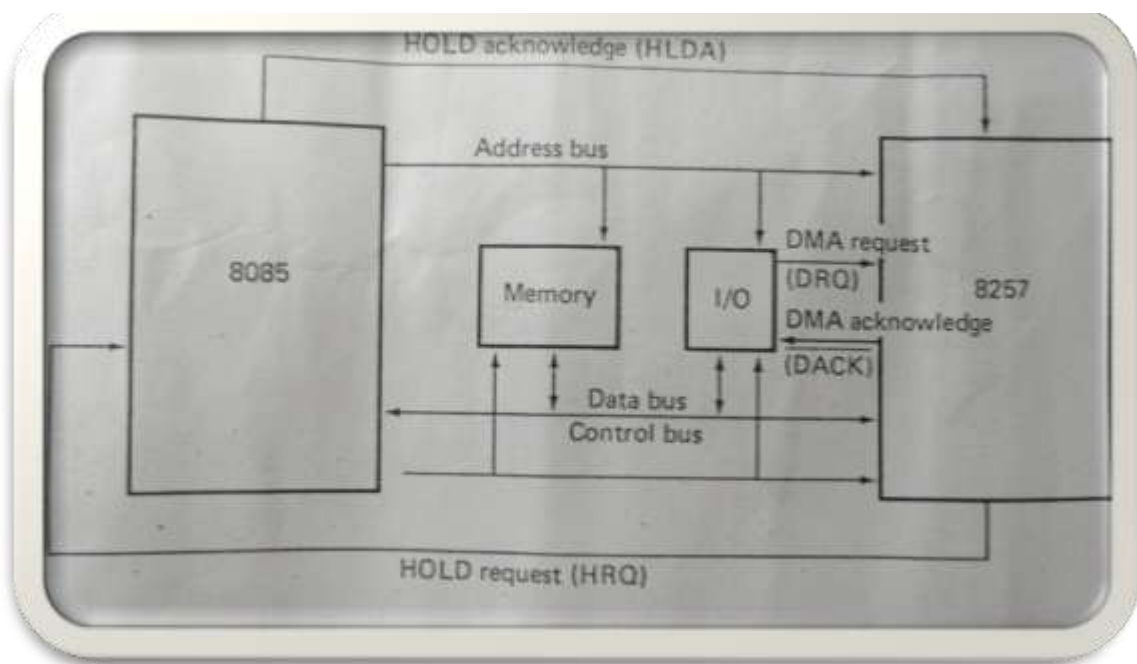


Fig (2) an 8085 interface

B. cycle stealing DMA:-in this technique , the DMA controller transfers a byte of data between the memory and peripheral device by stealing a clock cycle of the microprocessor . the DMA controller will complete the transfer by passing the microprocessor and generating proper signals to complete the transfer. Since the microprocessor is operated by an external clock, it is quite simple to stop the microprocessor momentarily.

This is accomplished by not providing the clock signal to the microprocessor. An INHIBIT signal is used for this purpose, which is normally HIGH and is logically AND with the system clock to generate the microprocessor clock, as shown in Fig(2).

The DMA controller stops the microprocessor by lowering the INHIBIT signal to LOW. A timing diagram is shown in Fig (3). The DMA controller then takes over the control of the microprocessor system bus for the time that microprocessor is stopped. Using cycle stealing, data is transferred 1 byte at a time. The DMA controller requests the microprocessor for each byte to be transferred.

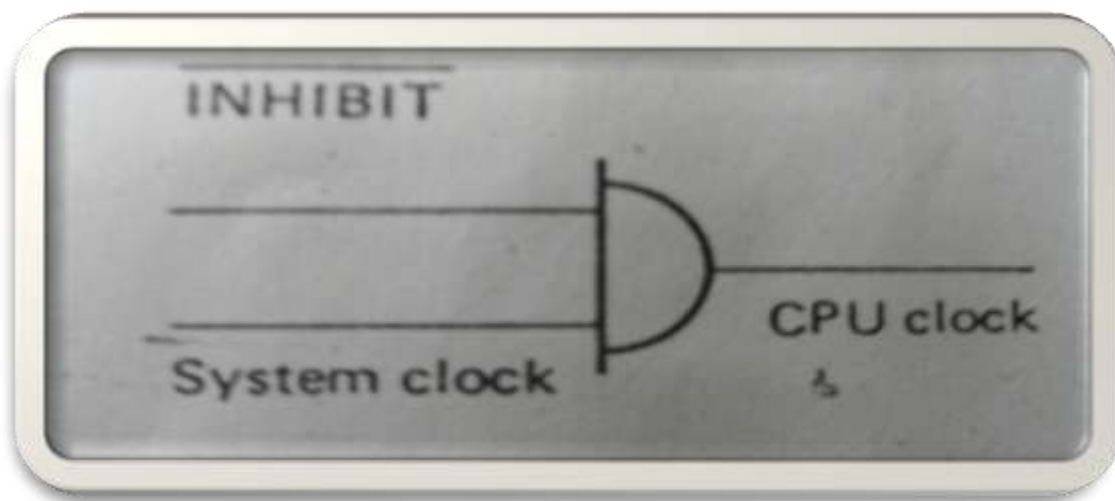


Fig (3):- cycle stealing DMA

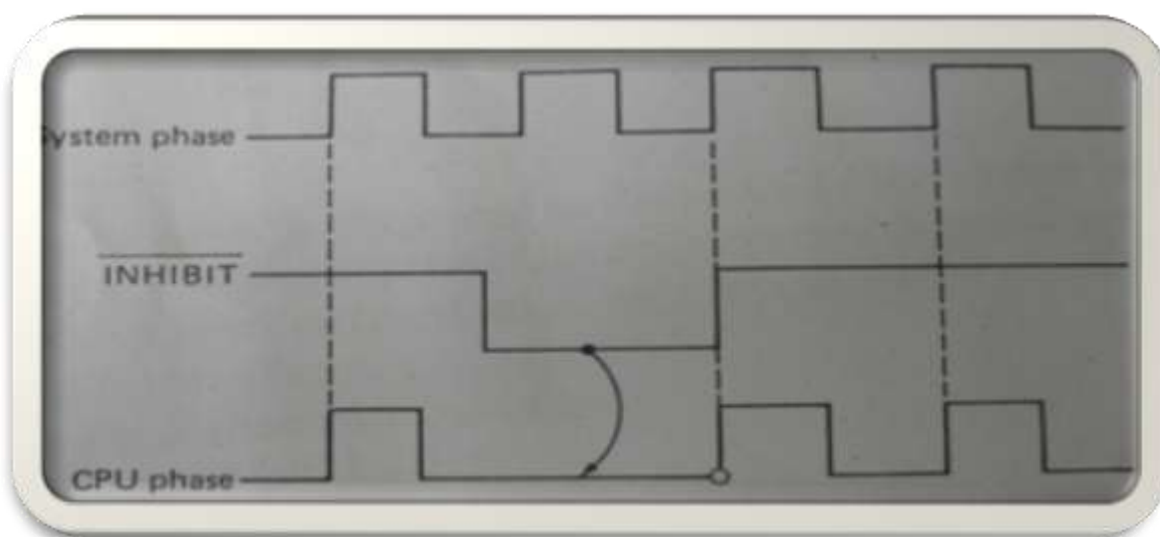


Fig (4) cycle stealing DMA timing diagram

Interleaved DMA:-

Interleaved DMA is a more complex type of DMA operation using this technique, the DMA controller takes over the system bus when the microprocessor is not using it. For example, the microprocessor doesn't use the bus when it performs internal operations, such as decoding an instruction or ALU operations. The DMA controller takes advantage of those times in order to transfer data, and this is called Interleaved DMA. One of the main characteristics of Interleaved DMA is that data transfer occurs without stopping the microprocessor. With Interleaved DMA, each data transfer includes 1 byte per instruction cycle.