Anurag Kar

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Education

Indian Institute of Technology - Kharagpur — West Bengal, India
Dual Degree B.Tech and M.Tech in EECE | GPA – 8.8/10 — *Aug. 2013 – May 2018*

Work Experience

CPU Verfication Engineer — Dec 2019 – Present
ARM — *Bengaluru, India*

- Part of a team responsible for verifying the latest ARM Cortex line of CPUs
- Ran RIS (Random Instruction Sequence) tools on emulator and FPGA platform and caught system level bugs
- Filed a bug which was categorized High Severity and resulted in erratum being added to the end user manual
- Wrote programs in Perl and Python to automate regression and debug tasks and also contributed to the repositories for all the internal tools used
- Wrote stimulus in C and ARM Assembly language to test specific blocks of the microarchitecture

System Validation Engineer — July 2018 – Dec 2019
Intel Corporation — *Bengaluru, India*

- Developed a python library of portable functions for test automation and debug. Library is widely in use by Intel teams across the globe in India, Israel and the U.S.
- Received a formal recognition for contribution to the latest Intel SoC bring up in Hillsboro, Oregon
- Regularly worked and interfaced with cross-site teams from Israel and the U.S.
- Part of the SoC debug task force, involved in working with several teams across Intel globally to work on critical debug issues and to come up with fixes
- Part of one of the first teams to test USB 4.0 compliance in the world

Research Experience

Australian National University — May 2017 – July 2017
Research Intern (Research School of Physics and Engineering) — *Canberra, Australia*

- Worked with Prof. Chennupati Jagadish and Dr. Dipankar Chugh to investigate single photon emitters from NV centres in hexagonal Boron Nitride
- Characterized samples using Photoluminiscence, Raman and g2 measurements
- Used MATLAB to plot and analyse data collected

IIT Kharagpur — July 2016 – May 2018
Student Researcher (VLSI Engineering Lab, Dept. of EECE) — *Kharagpur, India*

- Worked with Prof. P.K. Guha and Dr. Sayan Dey to create a Cr(VI) sensor with a limit of detection of 125 ppb
- Presented the results in an oral presentation at the EMRS Spring Meet 2017 in Strasbourg, France
- Published a paper based on this work in IEEE Transactions on Electron Devices journal

Achievements

2019 Recognized by the Intel Thunderbolt team in Oregon for contribution to SoC power-on activities
2017 Chennupati and Vidya Jagadish Endowment for research at ANU
2014 National Initiative for Undergraduate Sciences (NIUS) Physics scholar
2013 Among 12 students from Gujarat selected for the Indian National Physics Olympiad
2009 Duke University Talent Identification Program scholar

Publications

- **A. Kar**, S. Dey, D. Burman, S. Santra and P. K. Guha, "RGO/Ni2O3 Heterojunction-Based Reusable, Flexible Device for Cr(VI) Ion Detection in Water," in IEEE Transactions on Electron Devices, vol. 68, no. 2, pp. 780-785, Feb. 2021, doi: 10.1109/TED.2020.3045954

Presentations

- **A.Kar**, S.Dey, S. Santra, S.Ray and P.K. Guha, "RGO/Ni_2O_3 composite as a multifunctional material for efficient water quality monitoring (oral presentation only), EMRS Spring Meet,2017