BITS-Pilani Dubai Campus
I Sem 2021-22
Digital Design Laboratory ECE/INSTR/CS F215
Submission Report
Experiment No.- 2 (Familiarization of software tool and environment)

Name Anurag Kumar Jha **ID Number 2020A7PS0128U**

Run 1: Login to the Linux account and invoke cadence virtuoso

Important notes:

1. After you finish the simulations, always close the Virtuoso and all other cadence windows properly.
2. Also close the terminal from where you typed **virtuoso &**.
3. After that always logout from your account properly by clicking your username and then logout in top-right corner of the main screen.

NEVER SHUTDOWN THE PC ONLY LOGOUT FROM TOP RIGHT CORNER

Q: Are you successfully able to login to CentOS and cadence Virtuoso Window is invoked?

A: Yes, after creating a new login identity on the CentOS machine and running virtuoso

Run 2: Define logic gates and see the propagation delay

(a) Write verilog code and testbench for NOT gate using gate level modeling and see the waveforms.

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.

A:

```
// Gate level modeling code for NOT gate (a)
module NOTgate (z,a );
input a;
output z;
not #1 (z,a); //#1 is one unit delay from input to output
endmodule

module testbench_notgate;
reg p;
wire q;
initial begin
```

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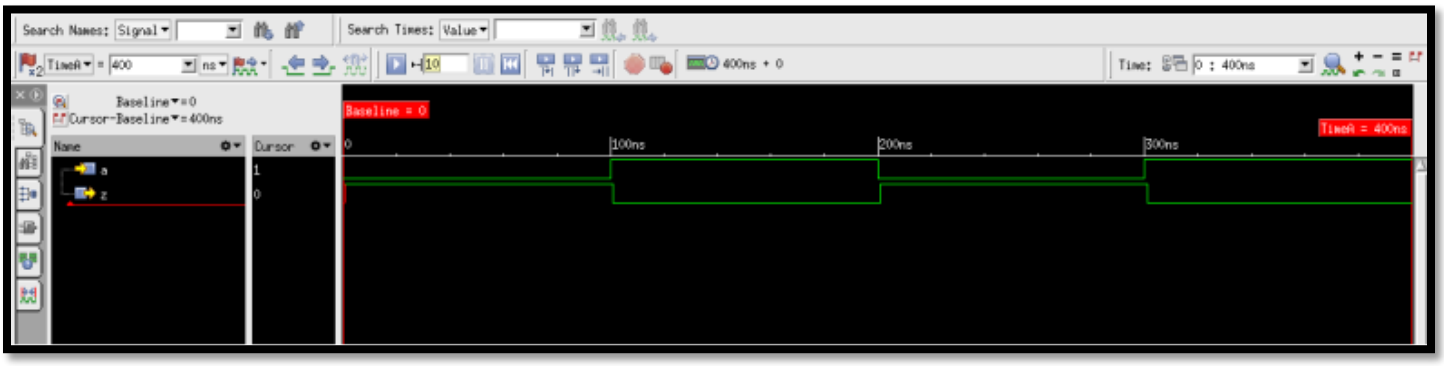
```
#000 p = 0;
#100 p=1;
#100 p =0;
#100 p=1;
#100 $stop;
end
NOTgate U1(q,p);
endmodule
```



(b) Use the above verilog code of NOT gate as a block and create a series of six NOT gates using structural modeling and see the output with and without delay by applying square wave at the input of first NOT gate.

Q: Paste the Image of your Simvision window where you get the waveforms for the above code.

A:

```
// Code for not gate chain
module not_chain (o1,o7);
output o7;
input o1;
wire o2,o3,o4,o5,o6;
notgate_gatelevel N1(o2,o1);
notgate_gatelevel N2(o3,o2);
```

```
notgate_gatelevel N3(o4,o3);
notgate_gatelevel N4(o5,o4);
notgate_gatelevel N5(o6,o5);
notgate_gatelevel N6(o7,o6);
endmodule
// Where module notgate_gatelevel is already defined in part (a) as below
module notgate_gatelevel (z,a );
input a;
output z;
not #1 (z,a);
endmodule
// testbench for not gate chain
module not_chain_tb;
reg o1;
wire o7;
not_chain NC1(o1, o7);
initial begin
#10 o1 = 0;
#10 o1 = 1;
#10 $stop
end
endmodule
```

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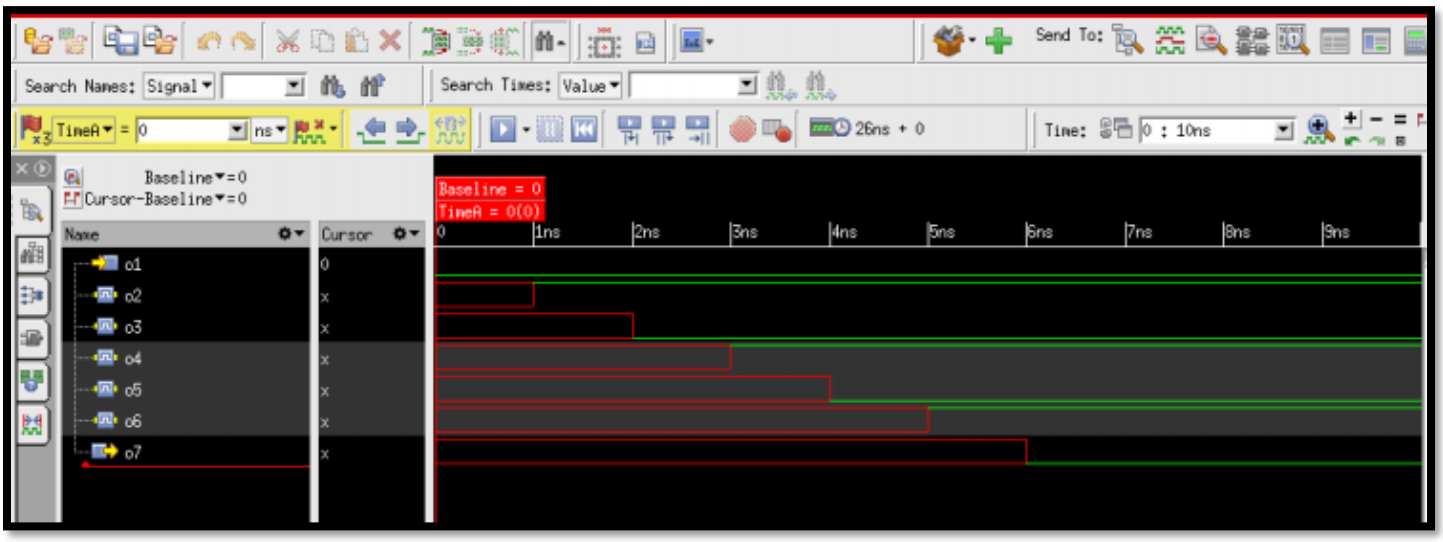

Run 3: Define logic gates using data flow, gate level modeling and behavioral modeling on www.edaplayground.com

Q: Note down the setting on the setting left side panel of the website for Simulation.

A: Testbench + Design: SystemVerilog/Verilog

UVM/OVM: None

Other Libraries:

- ☐ **Enable TL-Verilog**
- ☐ **Enable Easier UVM**
- ☐ **Enable VUnit**

Tools & Simulators: Cadence Xcelium 20.09

Compile Run Options: -timescale 1ns/1ns -sysv

Run Options: -access +rw

- ☐ **Use run.do Tcl file**
- ☐ **Open EPWave after run** ---Check this one
- ☐ **Download files after run**

(a) Verilog code and testbench for 2 input OR gate using gate level, data flow and behavioral modeling in one code.

Q: Paste the Image of your **EPWave** window where you get the waveforms for the above code.

A: https://www.edaplayground.com/x/NvBB

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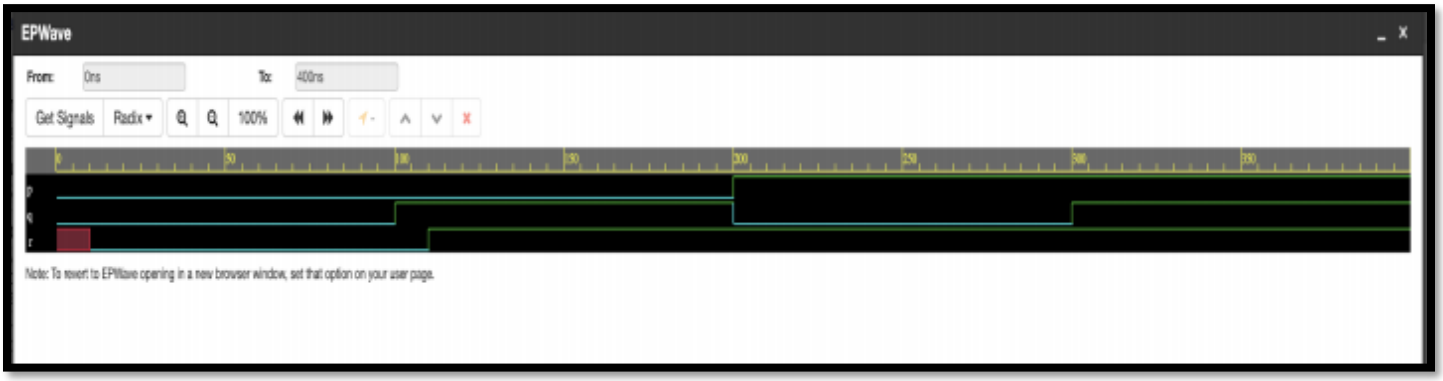
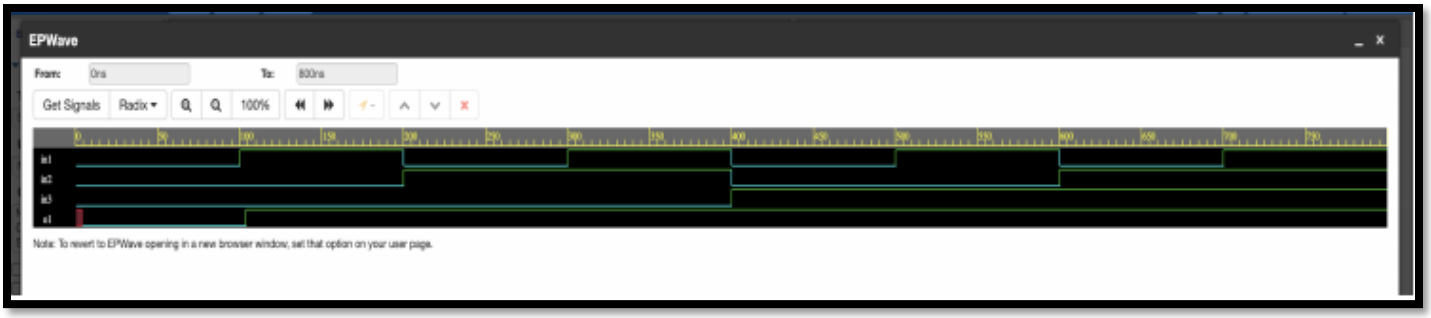
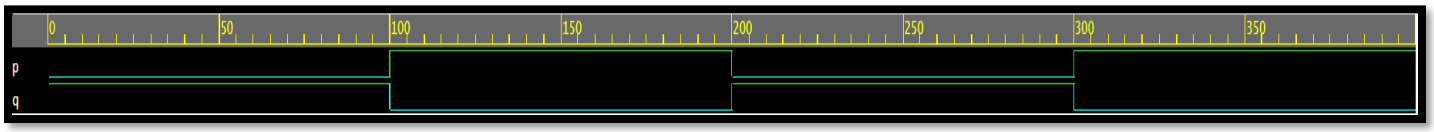


(b) Verilog code and testbench for 3 input OR gate using structural modeling using two 2-input OR gates.
Q: Paste the Image of your **EPWave** window where you get the waveforms for the above code.



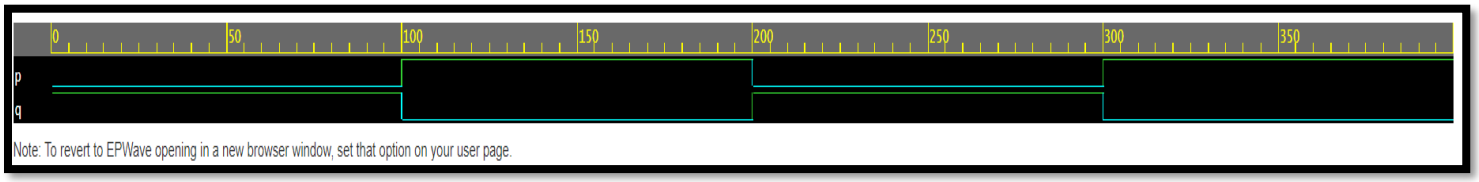
A: https://www.edaplayground.com/x/CeNr

(c) Write the verilog code and testbench for NOT gate using data flow modeling and see the waveforms.
Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.



A: https://www.edaplayground.com/x/S9rV

(d) Write the Verilog code and testbench for NOT gate using behavioral modeling and see the waveforms.
Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.



A: https://www.edaplayground.com/x/MqcQ

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Assignment: All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.
Copy-paste or type the unique URL of your assignment solution from website www.edaplayground.com for assignment questions. Please note that do not copy someone else's link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

(a) Write the single Verilog code and testbench for 3-input gates (NAND, XOR) using gate level modeling.

Ans: Link1:- https://www.edaplayground.com/x/fAcC

https://www.edaplayground.com/x/YRqk

(b) Verilog code and testbench for finding 1's complement of 8-bit binary number.

Ans: Link2: https://www.edaplayground.com/x/B3qk

(c) Write the Verilog code and testbench for NOT gate using data flow modeling and see the waveforms.

Ans: Link3: https://www.edaplayground.com/x/S9rV

(d) Write the Verilog code and testbench for NOT gate using behavioral modeling and see the waveforms.

Ans: Link4: https://www.edaplayground.com/x/MqcQ