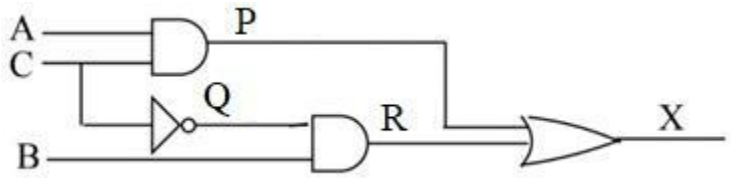
BITS-Pilani Dubai Campus
I Sem 2020-21
Digital Design Laboratory / ECE/INSTR/CS F215
Submission Report
Experiment No.- 3 (Implementation of Boolean Function)

Name: Anurag Kumar Jha **ID Number: 2020A7PS0128U**

Hardware runs
Run 1: AND-OR implementation
Diagram



Truth Table

A	B	C	P	Q	R	X
0	0	0	0	1	0	0
0	0	1	0	0	0	0
0	1	0	0	1	1	1
0	1	1	0	0	0	0
1	0	0	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

Q: For the above circuit diagram fill in the following details

A: **No. of AND gates used: 2**
No. of NOT gates used: 1
No. of OR gates used: 1
Total No. of ICs used: 3

No. of AND gate IC used: 1
No. of NOT gate IC used: 1
No. of OR gate IC used: 1

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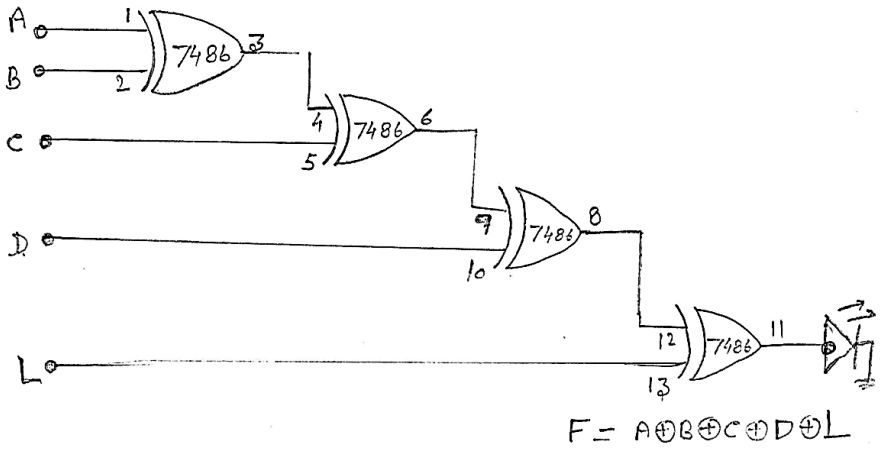
Run 2: Parity generator

Diagram



Q: How many XOR gates are used?
A: 4

Q: How many 7486 IC are used? Can the circuit be implemented using only **one** 7486 IC?
A: Only 1. Yes, this circuit is possible even with a single 7486 IC. A single 7486 IC has 4 XOR gates in it, which is exactly equal to the number of XOR gates used in this circuit. In addition to this, the XOR gate also contains a pin for input of 5V and another pin for Ground connection.

Q: Take any six-input combinations of your choice and complete the below table.

Truth Table

A	B	C	D	L	P
0	1	1	0	0	0
0	1	1	0	1	1
1	1	1	1	0	0
1	1	1	1	1	1
1	0	1	0	1	1
0	1	0	1	1	1

Software runs

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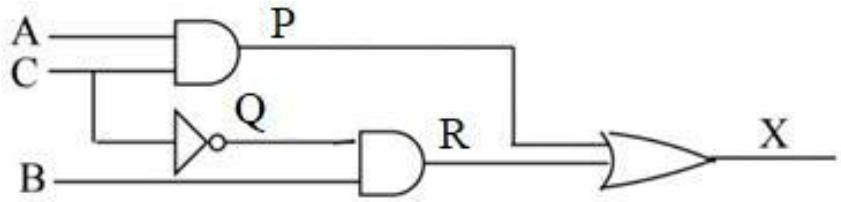
Run 3: Circuit implementation

(a) Implement the below circuit using Gate level modeling, write the code as well as its testbench.




```
// Verilog code for the above circuit
module circuit(X, A,B,C); //module name followed by list of ports
input A,B,C; //input port declarations, by default wire
output X; //output port declarations, by default wire
wire P, Q, R; //wire declaration for intermediary wires
and a1(P,A,C); //instance name is not compulsory. output of gate is always mentioned first
not (Q,C);
and (R,Q,B);
or (X,R,P); //2 input OR gate
endmodule

// testbench for the above code
module stimulus;
reg A,B,C,E; //reg is data type that makes variable retain value
wire X; //same variable names can be used
initial //statements within initial block have sequential execution
begin
A=0; B=0; C=0; E=0;
#10 A=0; B=1; C=0; E=0; //10 is 10ns delay
#10 A=0; B=0; C=1; E=1;
#10 $stop;
end
circuit mycircuit(X,A,B,C); //instantiating the design block taking care of port connection rules
endmodule
```

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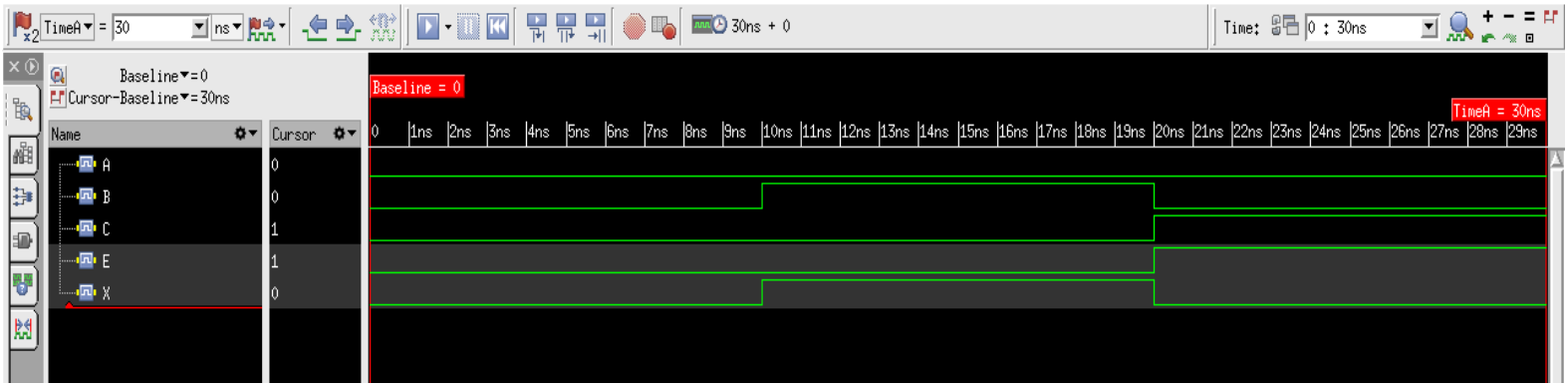
Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.
A:



Run 4: Error detection and error correction codes

Q: Write Verilog code and testbench for generating even parity Hamming code for 4-bit data. (Hint: P0 = D2^D1^D0, P1 = D3^D1^D0, P2 = D3^D2^D0)

A: Verilog Code-

```
//Verilog HDL for "LAB3", "LAB3_Run4_2" "functional"


module LAB3_Run4_2 (out, d);
    output[6:0] out;
    input[3:0] d;

    // Data bits
    assign out[4] = d[3];
    assign out[2] = d[2];
    assign out[1] = d[1];
    assign out[0] = d[0];
    // Parity bits
    assign out[6] = d[3]^d[2]^d[0];
    assign out[5] = d[3]^d[1]^d[0];
    assign out[3] = d[2]^d[1]^d[0];
endmodule

module testbench();
    reg [3:0] a;
    wire [6:0] b;

    initial begin
        #000 a = 4'b0000;
        #100 a = 4'b1011;
        #100 a = 4'b1001;
        #100 a = 4'b0011;
    $stop;
    end

    LAB3_Run4_2 G1 (b,a);
endmodule
```

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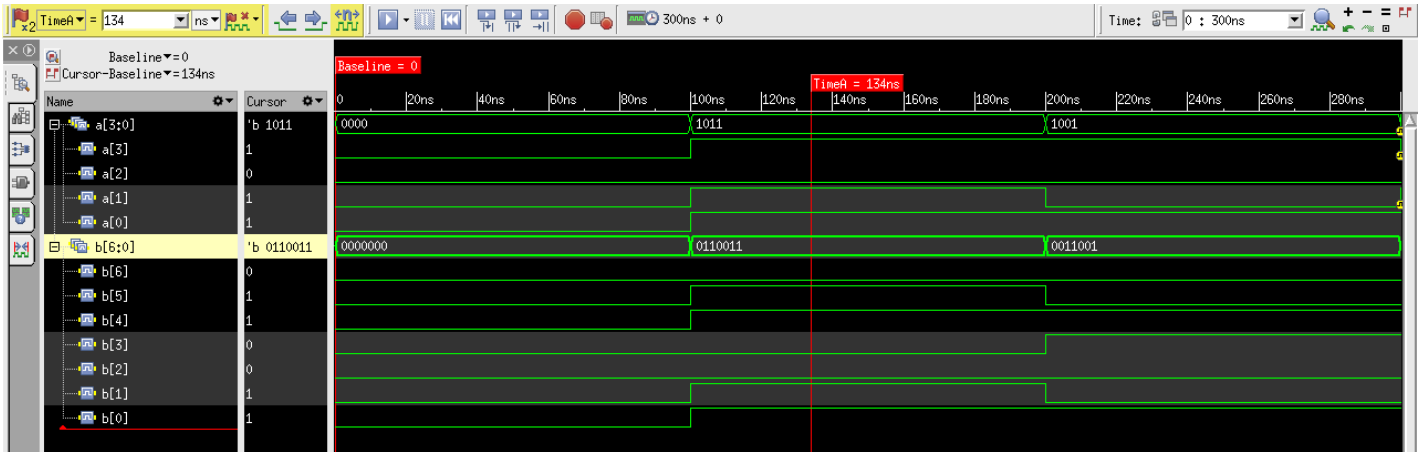
A:



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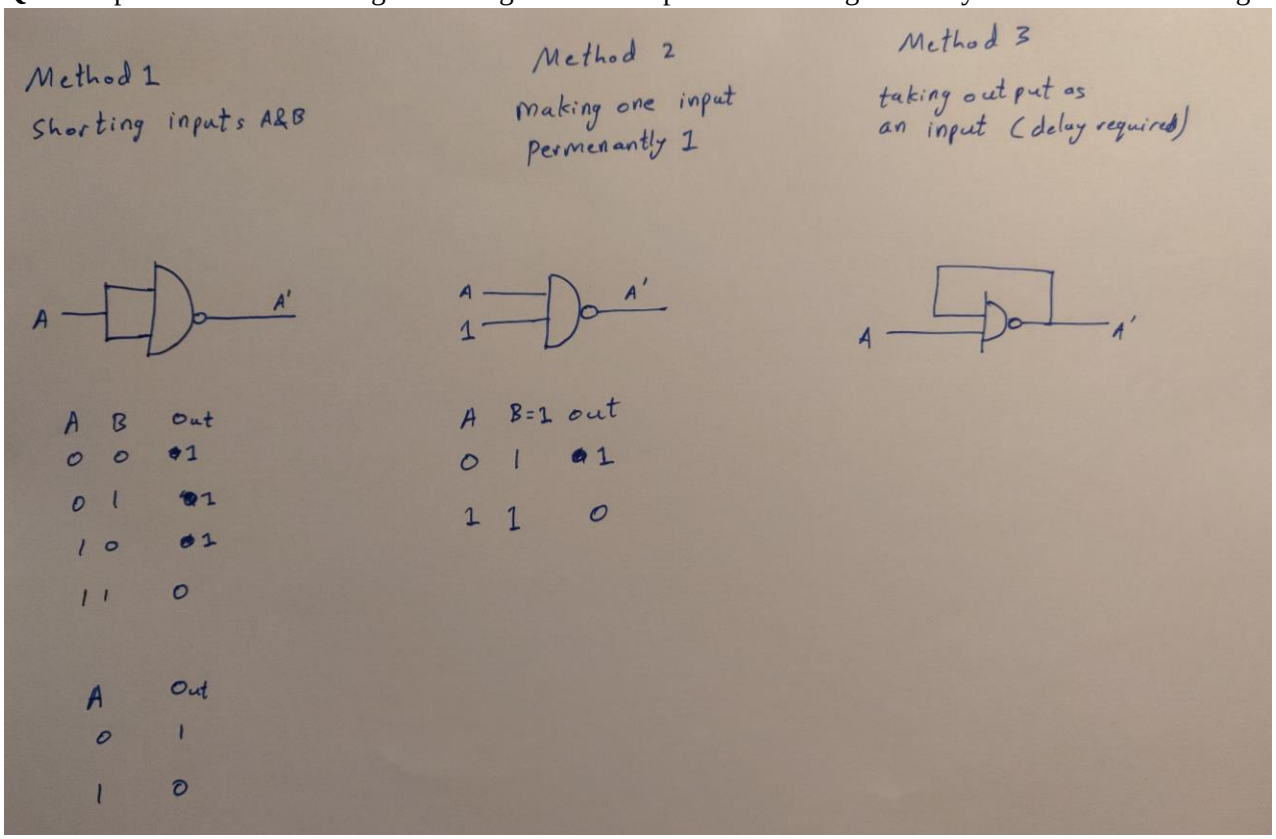
Assignment All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.
Copy-paste or type the unique URL of your assignment solution from website www.edaplayground.com for assignment questions. Please note that do not copy someone else's link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

Q1: Implement a NOT gate using one 2-input NAND gate only. Write its verilog code also.



Ans: Link1: https://www.edaplayground.com/x/vXPN

Q2: Write Verilog code and testbench using data flow modeling for Y = ABC + AB +AC.
Ans: Link2: https://www.edaplayground.com/x/hAYw

Q3: Write Verilog code and testbench for detecting even parity error in 4 bit (3+1) binary number.
Ans: Link3: https://www.edaplayground.com/x/L7Bt
Q4: Write Verilog code and testbench for generating even parity bit for 4-bit binary number. (Hint: you can use the structure of run-2 of this experiment also or y = A^B^C^D).
Ans: Link4: https://www.edaplayground.com/x/NGJR

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