S. No.	Task – Sub-Task	Expected Date of Completion	Current Status
1	*Create Github Repository*	April 23, 2018	Completed
2	*FPGA Board*		
2-a	Search and finalize an FPGA Board that can interface with Jupyter Notebook	May 1, 2018	Completed
2-b	Purchase the FPGA Board online	May 2, 2018	Completed
2-c	Learn how to use Vivado HLS Software	May 6, 2018	Yet to start
2-d	Receive the FPGA Board	May 10, 2018	Yet to start
2-e	Run a sample program made using Vivado on the FPGA Board	May 11, 2018	Yet to start
2-f	Install python libraries on the FPGA board that are necessary for machine learning	May 11, 2018	Yet to start
3	*Jupyter Notebook File*		
3-a	Import the VGG Model	May 2, 2018	Completed
3-b	Finalize a list of Test Classes	May 3, 2018	Pending
3-c	Download the Test Data	May 3, 2018	Pending
3-d	Pre-process the Test Data	May 4, 2018	Pending
3-e	Predict the Output Class	May 4, 2018	Pending
3-f	Print the Run-time	May 4, 2018	Pending
3-g	Print the Test Accuracy	May 4, 2018	Pending
4	*FPGA Implementation of VGGNet*		
4-a	Design the Vivado HLS model for the project	May 13, 2018	Yet to start
4-b	Generate Bitstream file	May 14, 2018	Yet to start
4-c	Create TCL file	May 14, 2018	Yet to start
4-d	Program the FPGA	May 14, 2018	Yet to start
4-e	Run the Jupyter Notebook File on the FPGA	May 14, 2018	Yet to start
4-f	Predict the Output Class	May 14, 2018	Yet to start
4-g	Print the Run-time	May 14, 2018	Yet to start
4-h	Print the Test Accuracy	May 14, 2018	Yet to start

Overall Project Status	18% Completed

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