Design and Analysis of CMOS Full adder

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Abstract— **This paper represents 28T conventional full adder design using standard CMOS design. This design is implemented on technology 28 nm using Synopsis tool. The analysis is carried out using several parameters like power consumption, delay and power delay product on various supply voltages. Full adders are the important components in application such as Digital signal processor, microcontroller, processor and data processing units.**

Keywords— **Full Adder, Technology, CMOS, Power**

I. INTRODUCTION

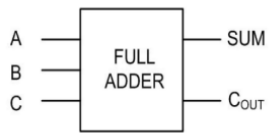
Designing of low-power and high speed Very Large-Scale Integration (VLSI) systems has pop up as highly demands in market due to fast-paced growing technologies in telecommunication and other power applications. Binary addition is the basic components found in most arithmetic and logic components. Hence the realization of Half adder and Full adder nowadays is essential in terms of delay and power consumption.

Full adder is designed for addition of two bits (A and B) with input carry C in such a way that can take eight inputs together from '000' to '111' and produces two one-bit output i.e. sum and carry out.
Equations of full adder based on the truth table-

$SUM = A \oplus (B \oplus C)$

$COUT = AB + BC + AC$ OR

$COUT = C (A \oplus B) + AB$



INPUT			OUTPUT	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig1: Block Diagram and Truth Table of Full Adder

The advantages of complementary CMOS logic circuit based full adder design are its layout regularity and stability at low voltage due to the complementary transistor pairs.

II. REFERENCE CIRCUIT DETAILS

The Fig2 shows the schematic of 28T conventional CMOS design Full Adder.

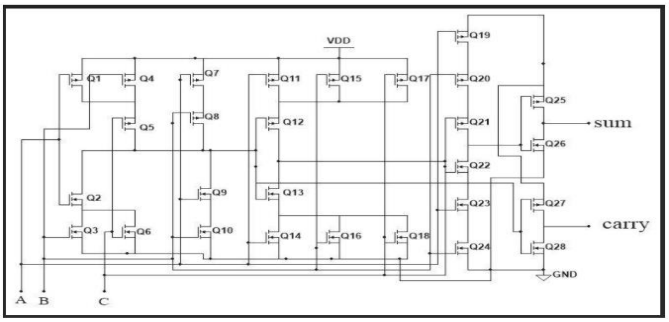


Fig2. Schematic of 28T conventional CMOS Full Adder

This design is based on complementary pull up and pull down topologies and having high noise margin and reliability. The CMOS full adder suffers from large power consumption and high delay. We will also calculate average power consumption by the above circuit.

III. REFERENCE WAVEFORM

This section presents simulation of reference waveform as shown in below Fig3. Conventional CMOS full adder considered in this work are simulated for getting proper outputs along with estimation of propagation delay and average power consumption.

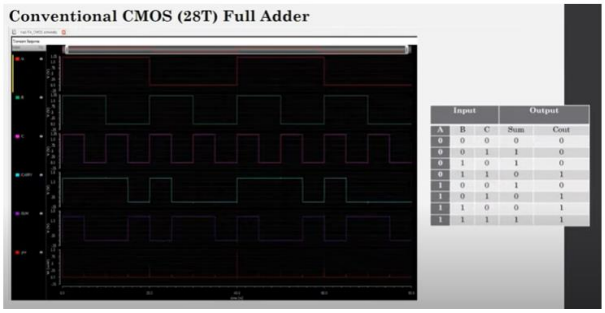


Fig3. Simulated waveform of CMOS full adder circuit

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