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ROLL : 20 4TH YEAR 2ND SEMESTER

VLSI

Q1 (a) In 1965, Gordon Moore predicted that the number of transistors on a die would grow exponentially doubling every 12 to 18 months. Moore, however, estimated that the possibilities of circuit and device cleverness were already becoming exhausted. The future developments, therefore, were to be based on bigger dice and finer dimensions. Accordingly, Moore revised his original growth rate estimate in 1975, and proposed that by the end of the decade, the number of components on the most complex chips would double about every two years.

Impact of Moore's Law:

There was an extremely rapid growth in the number of transistors being integrated into circuits on a single silicon chip. In 3 decades the number rose from tens to millions. Moore's Law brought significant developments to integration and scaling that were never imaginable before. But it also sucked all the talent to do mostly scaling |porting| integration type of engineering, instead of new innovations. Due to this, constraints on cost, verification, performance, area have now been reached.

(b) Verification is the predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.

Verification is done before silicon development. It is done at the time of product development for quality checking and bug fixing in design. Verification is done at the physical synthesis phase.

(c) Semiconductors are materials which have conductivity between conductors and ~~non~~ non-conductors or insulators. Semiconductors are made from pure elements, typically silicon or germanium, or compounds such as gallium ~~As~~ arsenide.

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Q2(a) Problems of BJT:

- BJTs have low thermal stability
- BJTs have a low switching frequency.
- They have a very complex base control and so requires ~~sk~~ skillful handling.
- They produce more noise.
- There is more power dissipation and current leakage.
- Power dissipation limits device density.
- BJTs are bulky requiring more space in the IC.

(b) There are two ~~k~~ kinds of power dissipation in CMOS – static and dynamic. The static ~~o~~ dissipation refers to the time when the CMOS is not in the process of switching states. The static power dissipation is very less because the current flowing through the IC is ~~zero~~ nearly zero. But, there is dynamic loss as well. It is the loss which occurs while the circuit switches from one logic state to another. Some power is used to charge the capacitors as well which is known as load capacitance. All these losses together results in power dissipation in CMOS.

In static condition the current through a CMOS is zero. However there is a small amount of static power consumption due to reverse bias. leakage between diffused regions and substrate of a CMOS. The source-drain diffusion and the n-well diffusion from parasitic diodes in the CMOS between n-well and substrate. These parasitic diodes contribute to power loss as they are reverse biased.

(c) λ-based design rules are design rules based on a single parameter λ. All paths in all layers will be dimesioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process.

Advantages:

- Simple for the designer.
- Wide acceptance
- Provide feature size independent way of setting out mask.
- If design rules are obeyed, masks will produce working circuits.
- Minimum feature size is defined as 2λ.
- Used to preserve topological features on a chip.
- Prevents shorting, opens, contacts from slipping ~~out~~ out of area to be contacted.

(d) Use of Silicon:

- Silicon allows a large variety of process steps to be possible without the problem of decomposition. (as in case of compound semiconductors)
- Silicon has a wider band gap than Ge thus a higher operating ~~temperature (~~ temperature. (125°c - 175°c vs 85°c).

- Silicon readily forms a native oxide (SiO_2).
- Silicon is cheap and abundant.

Use of SiO_2

- SiO_2 is a high quality insulator
- Protects and passivates underlying circuitry.
- Helps in patterning.
- Useful for dopant masking.

~~Q3~~ Q3(a).

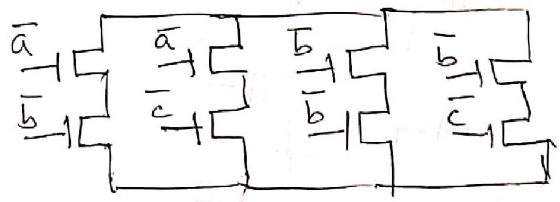
Advantages of single complex cell.

- There is negligible power dissipation as static state power consumption of CMOS circuits is very small.
- As CMOS are voltage driven, one gate can drive many more inputs which results in higher fanout.
- Single cell complex designs are thermally stable. They can operate steadily ~~at a~~ in a wide range of temperature.
- They are more immune to noise.

$$f = ab + bc = \overline{\overline{ab+bc}} = \overline{(\overline{ab})\cdot(\overline{bc})}$$
$$= \overline{(\bar{a}+\bar{b})\cdot(\bar{b}+\bar{c})} = \overline{(\bar{a}\bar{b}+\bar{a}\bar{c}+\bar{b}+\bar{b}\bar{c})}$$

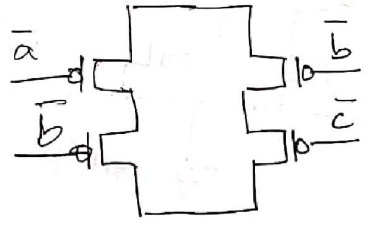
NMOS

Parallel Series.

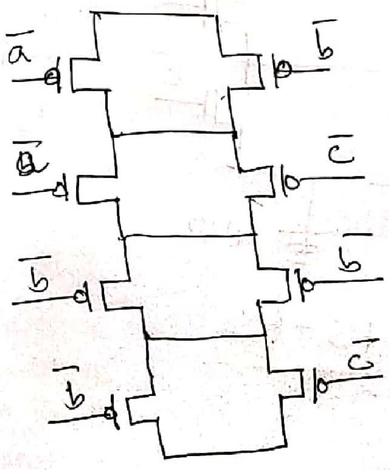


Series parallel.

PMOS

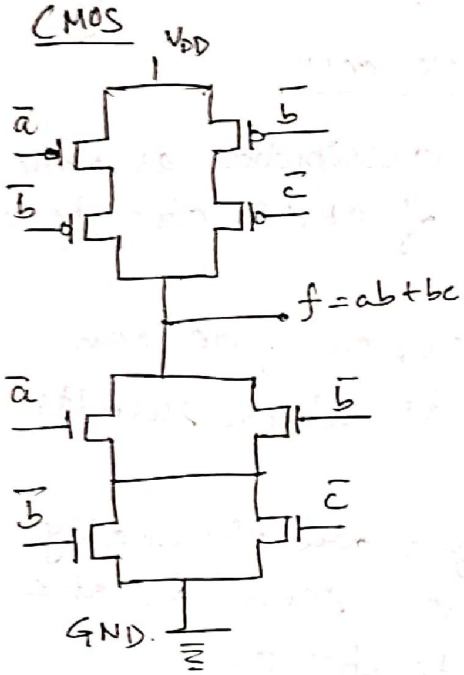


Series parallel

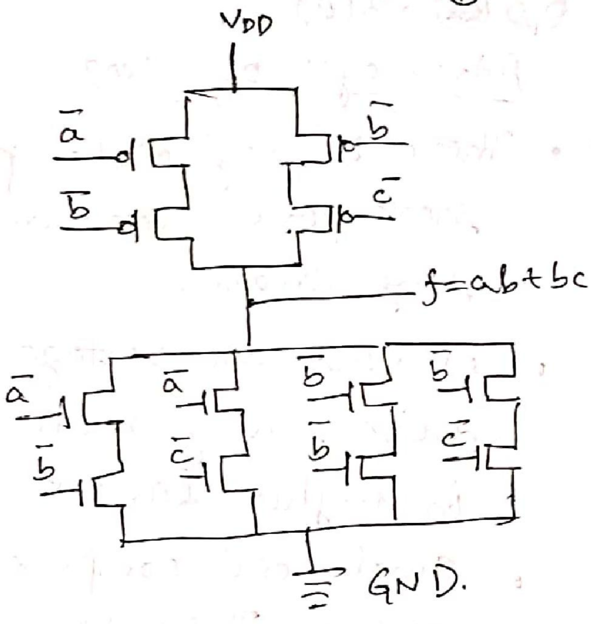


Parallel series.

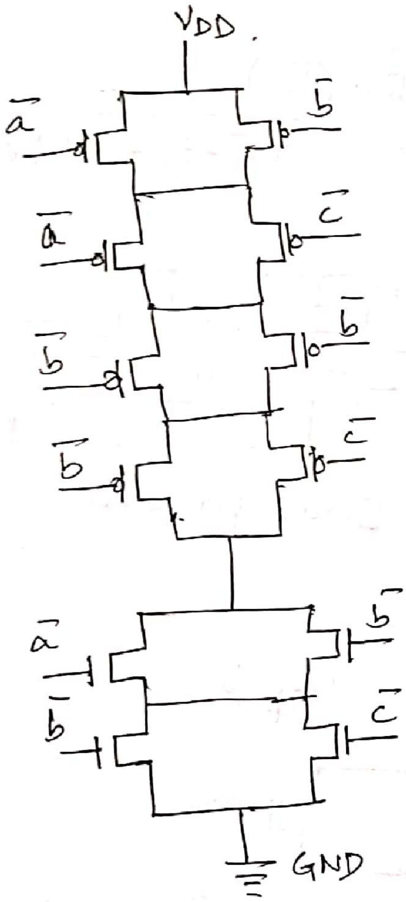
CMOS



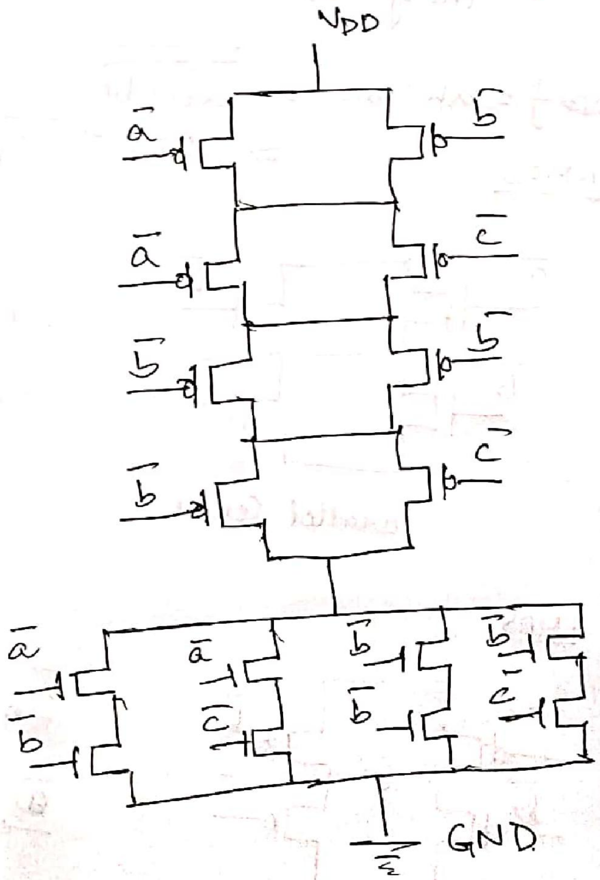
SP-PS.



SP-SP

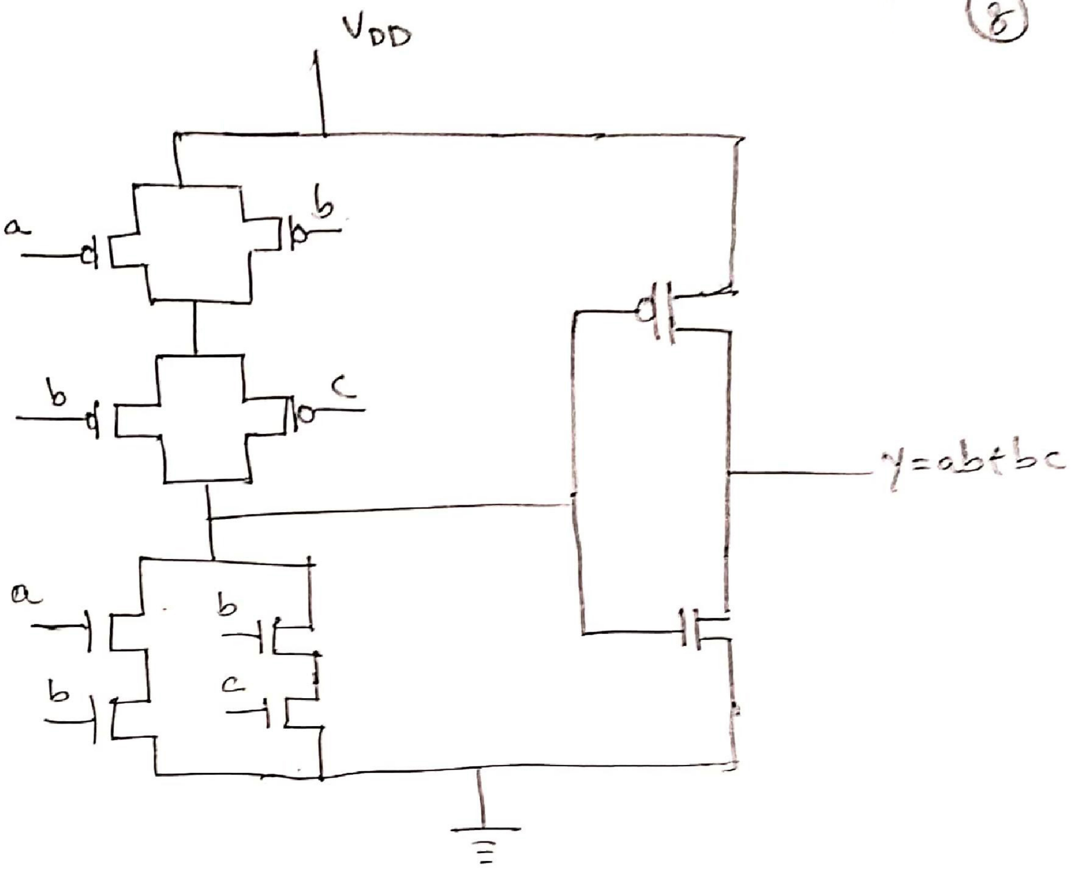


PS-PS.

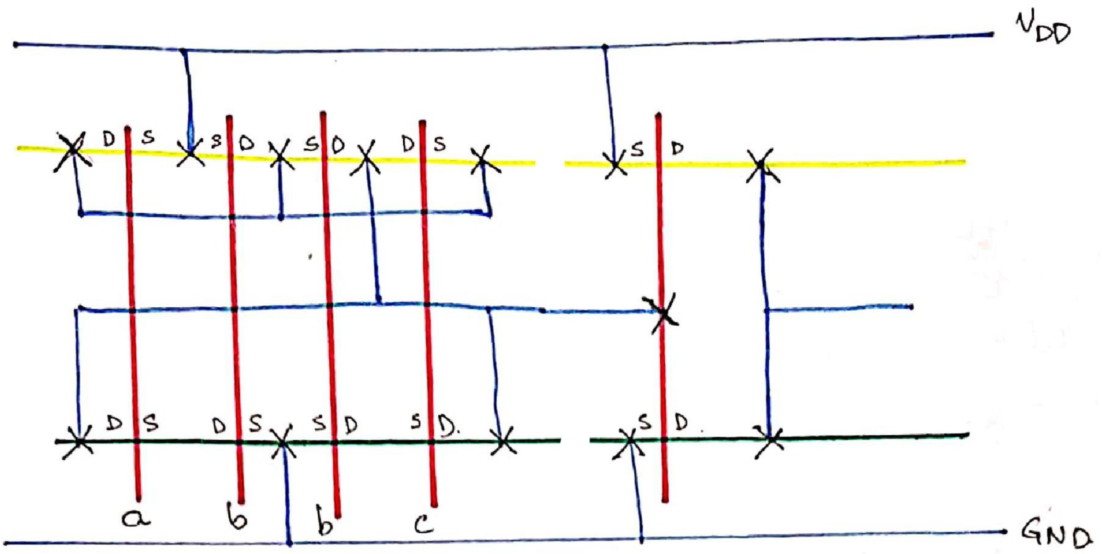


PS-SP

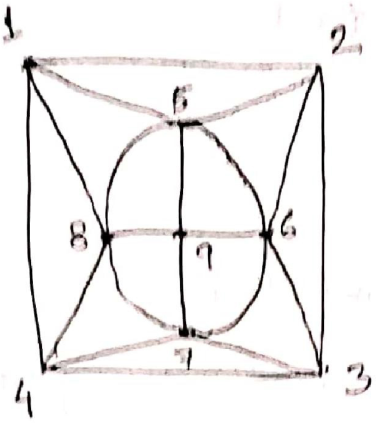
Q3(b)



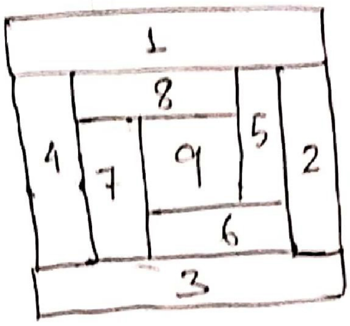
Stick diagram



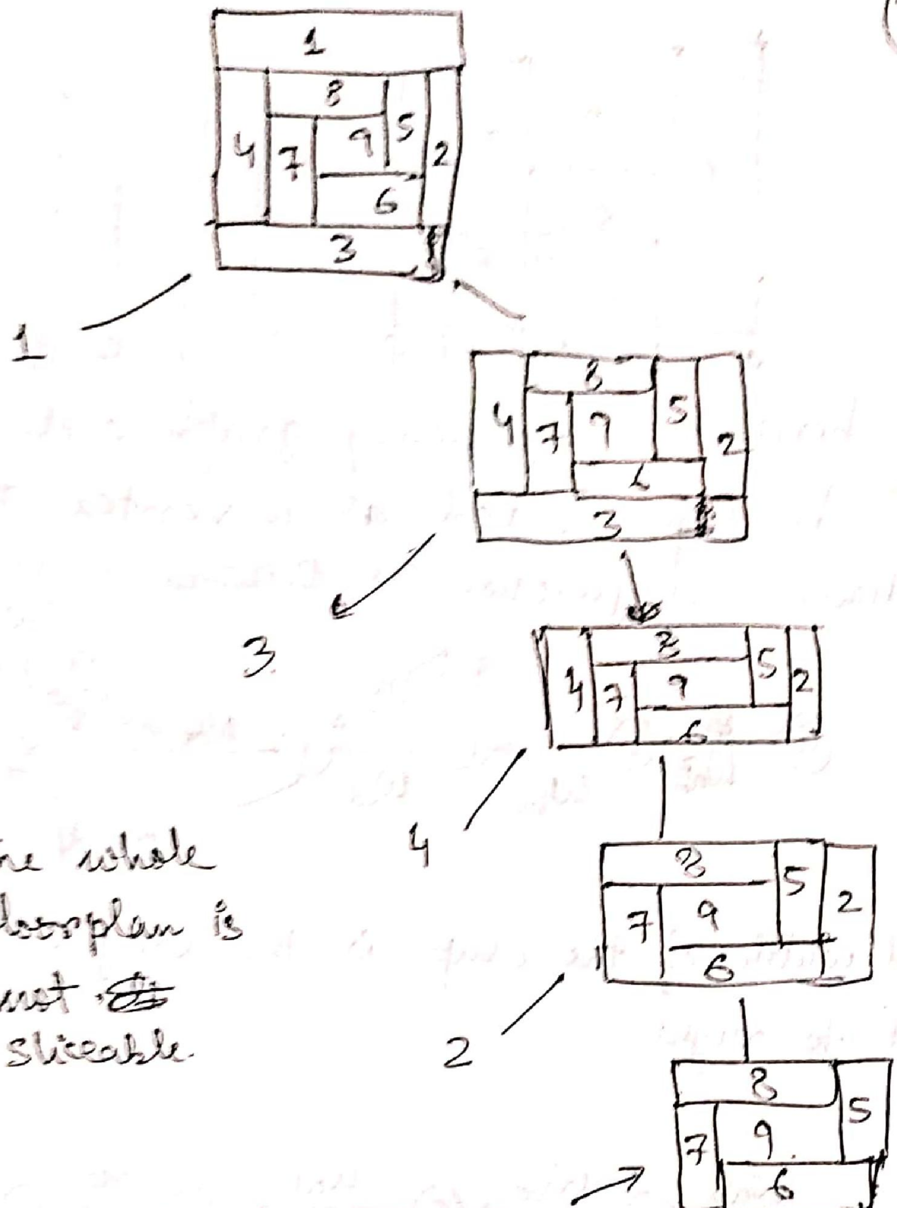
Q4 (a)



Rectangular Dual :



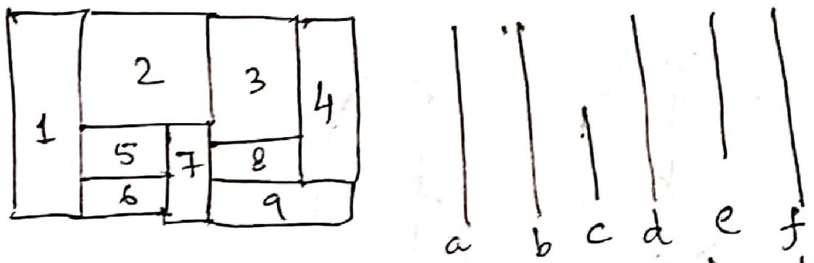
The given floor plan is not sliceable. We can initially divide the floor plan but later it is not possible.



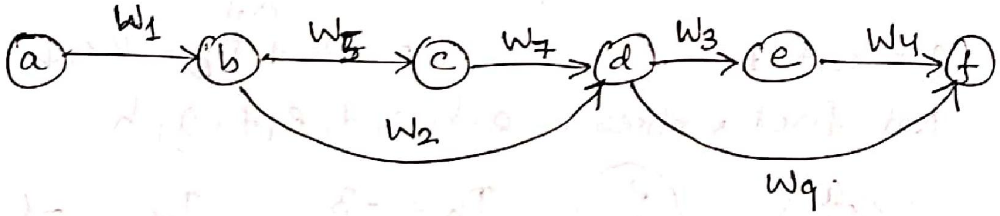
∴ The whole floorplan is not ~~sl~~ sliceable.

This floorplan is no longer sliceable.

Q4 (b)



In horizontal dependency graph each junction is represented as a vertex. Let W_i denote the width of chip i.

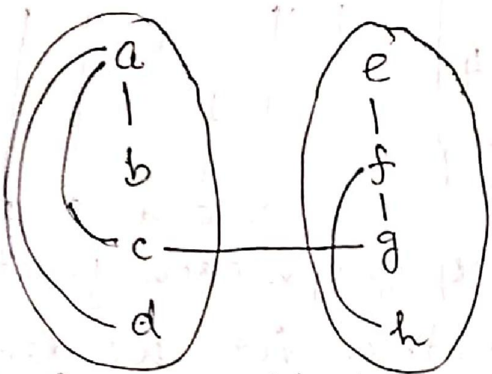


width of chip(W) = Longest path from left to right.

$$W = W_1 + \max(W_5 + W_7, W_2) + \max(W_3 + W_4, W_9).$$

W is the minimum width of the chip.

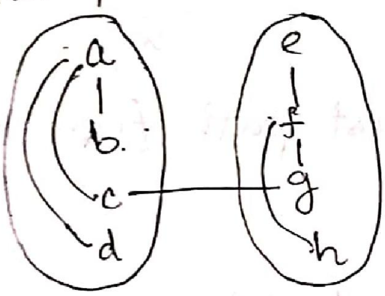
Q5 (a)



$C_{ab} = 1$ if edge exists b/w a, b else 0.
E_a be the external cost of vertex a.
I_a be the internal cost of vertex a.

$D_a = E_a - I_a$. g_{ab} = gain in swapping vertices a, b.
$= D_a + D_b - 2c_{ab}$

(1) Cut cost 1
Not fixed vertices : a, b, c, d, e, f, g, h.



$D_a = -3$ $D_e = -1$
$D_b = -1$ $D_f = -3$
$D_c = 0$ $D_g = 0$
$D_d = -1$ $D_h = -1$

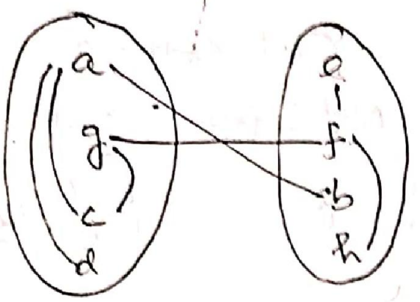
$g_{ae} = -4$ $g_{be} = -2$ $g_{ce} = -1$
$g_{af} = -6$ $g_{bf} = -4$ $g_{cf} = -3$
$g_{ag} = -3$ $g_{bg} = -1$ $g_{cg} = -2$
$g_{ah} = -4$ $g_{bh} = -2$ $g_{ch} = -1$

$g_{de} = -2$
$g_{df} = -4$
$g_{dg} = -1$
$g_{dh} = -2$

choose the one with maximum gain $\because g_{ce} = g_{bg} = g_{ch} = g_{dg} = -1$
$\therefore$ we can choose any one.
Say, we swap b, g.

$g_1 = -1$

② swap b, g



Cut cost : 2
Not fixed : a, c, d, e, f, h

$D'_a = -1$ $\quad D'_e = -1$

$D'_c = -2$ $\quad D'_f = -1$

$D'_d = -1$ $\quad D'_h = -1$

$g'_{ae} = -2$ $\quad g'_{ce} = -3$ $\quad g'_{de} = -2$

$g'_{af} = -2$ $\quad g'_{cf} = -3$ $\quad g'_{df} = -2$

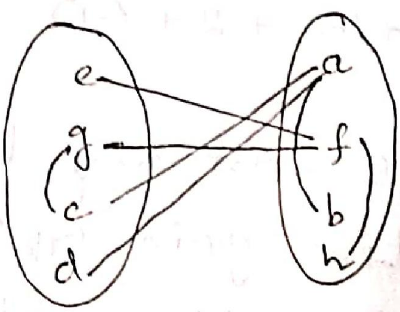
$g'_{ah} = -2$ $\quad g'_{ch} = -3$ $\quad g'_{dh} = -2$

$g_2 = -2$

Now swap a, e.

③ swap a, e.

Cut cost : 4
Not fixed : c, d, f, h



$D''_c = 0$ $\quad D''_f = 1$

$D''_d = 1$ $\quad D''_h = -1$

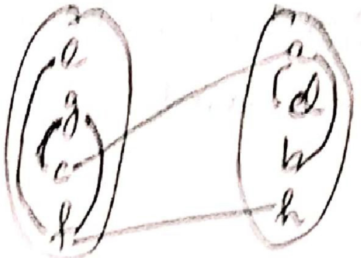
$g''_{cf} = 1$ $\quad g''_{df} = 2$

$g''_{ch} = -1$ $\quad g''_{dh} = 0$.

max gain $= g''_{df} = 2$ $\quad \therefore$ swap d, f.

$g_3 = 2$

④ Swap d, f (14)



Cut cost : 2

Not fixed : c, h.

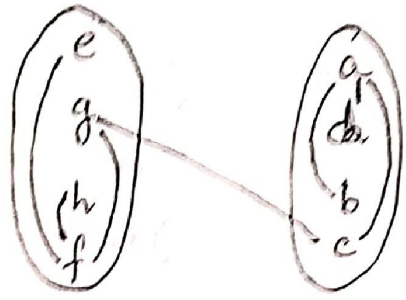
$D_c''' = 0 \qquad D_h''' = 1$

$g_{ch}''' = 1 \qquad g_4 = 1$

⑤ Swap c, h.

Cut cost : 1

Not fixed : –



This is one pass of the K-L Algorithm.

Total gain $G = \cancel{g_1 + g} \; \Sigma g_i$

$= -1 + (-2) + 2 + (1)$

$= 0$

∵ There does not exist any k for which the cumulative gain $G_k > 0$

∴ The original ~~parit~~ partition is optimal in itself.

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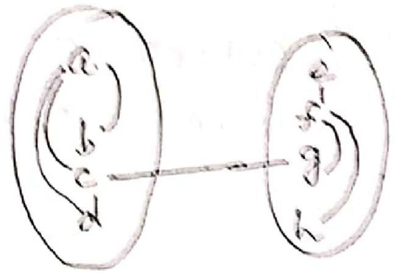
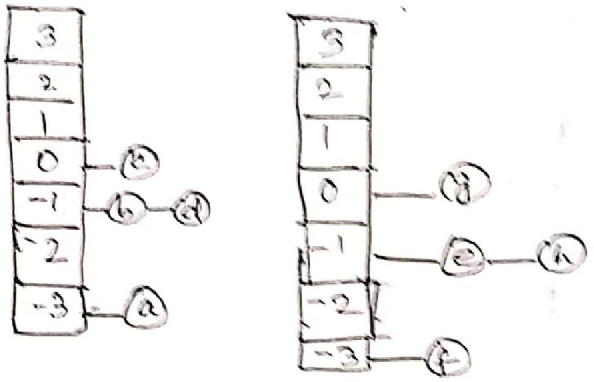
Q5(b).



(1)

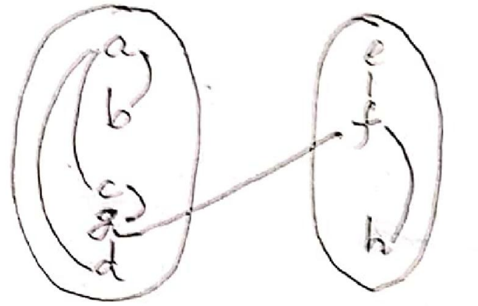


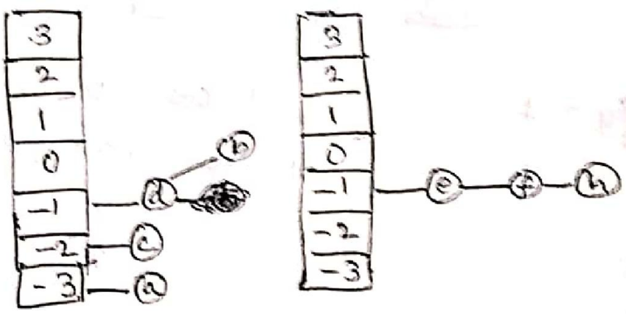
Fixed: —
Cutcost: 1

Now swap max gain. Say, ~~swap~~ move g

(2) Move g. $g_1 = 0$ (Gain)

Fixed: g
cut cost = 1.



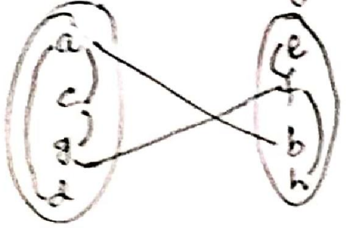


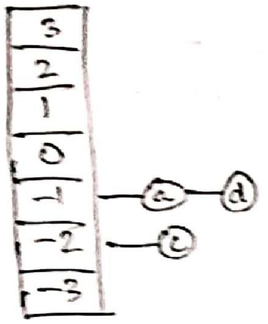
move b

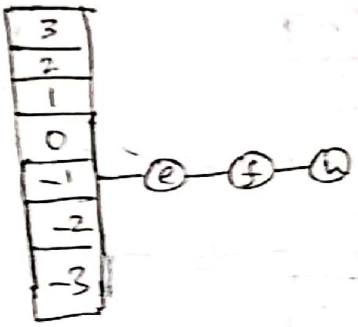
③ move b. $g_2 = -1$

Cut cost : 2

Fixed : g, b.



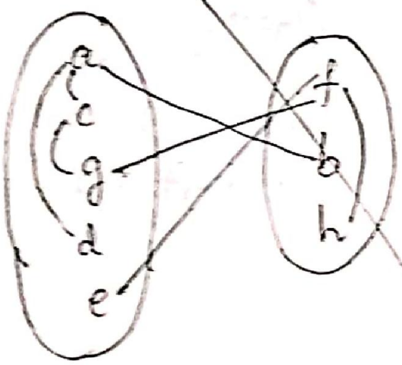


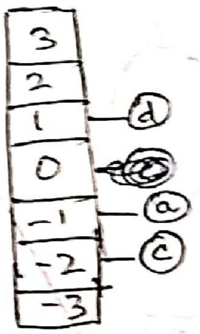


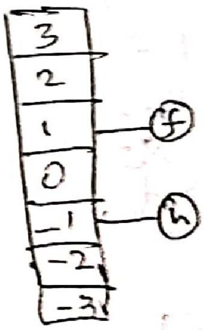
④ move e $g_3 = -1$

Cut cost : 3

Fixed : g, b, e.



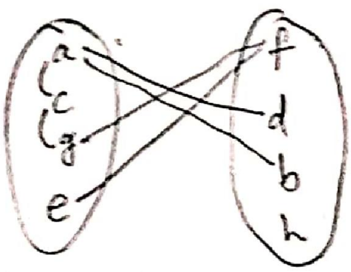




⑤ move d. $g_4 = 1$

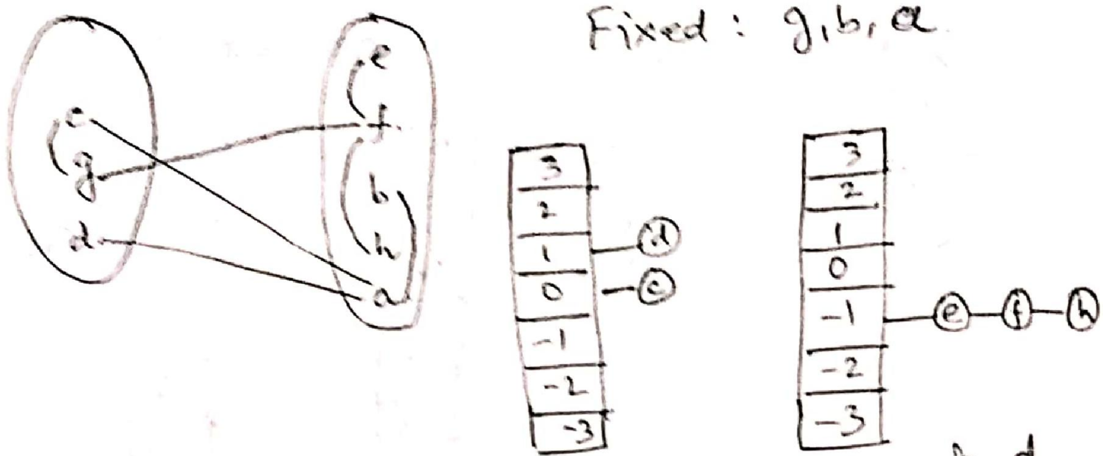
Cut cost : 2

Fixed : g, b, e, d.



4 move a. $g_3 = -1$ ~~cost~~ Cut cost : 3

Fixed : g, b, a

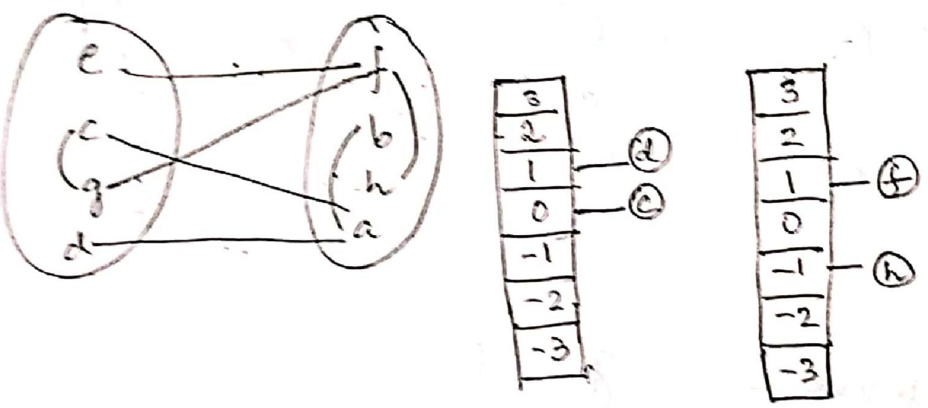


Now d has max. gain but if we swap d then balance will be lost.

∴ we have to swap from other partition.

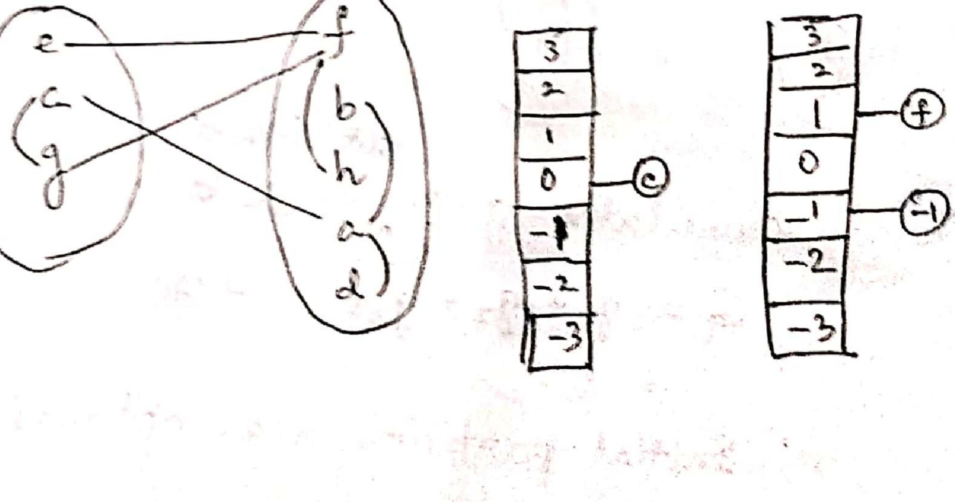
5 move e. $g_4 = -1$ Cut cost : 4.

Fixed : g, b, a, e



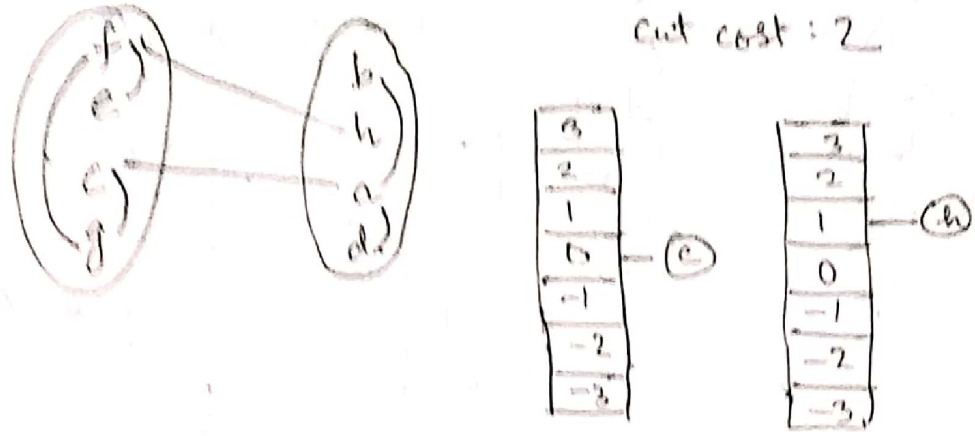
6 move d. $g_5 = 1$. Fixed : g, b, a, e, d

Cutcost : 3.



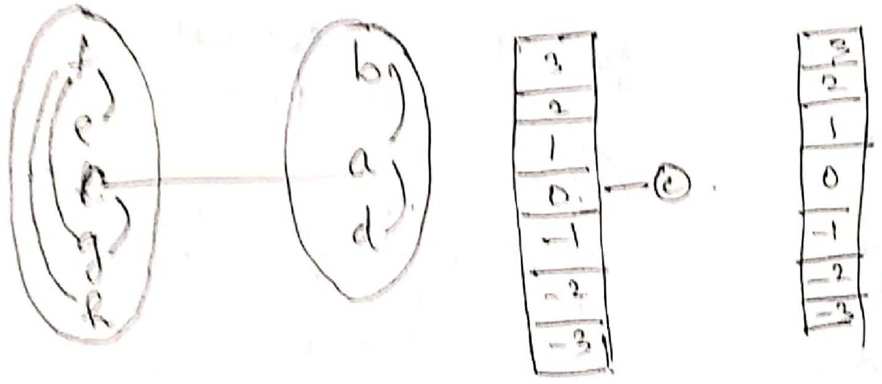
7. Move f $g_6 = 1$ Fixed: g, b, a, e, d, f

Cut cost: 2



8. move h $g_7 = 1$ Fixed: g, b, a, e, d, f, h.

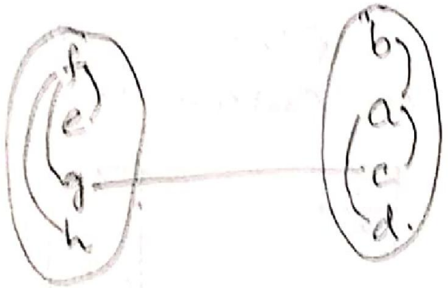
Cut cost: 1.



9. move c $g_8 = 0$.

Fixed: g, b, a, e, d, f, h, c

Cut cost = 1.



Total cumulative gain ~~such that~~ Σg_k

$G = g_1 + g_2 + g_3 + \dots + g_8$

$= 0$.

$\therefore$ Initial partition was optimal.