

Fabrication

Silicon vs. Germanium

Ge was used for transistors initially, but silicon took over in the late 1960s; WHY?

- (1) Large variety of process steps possible without the problem of decomposition (as in the case of compound semiconductors)
- (2) Si has a wider bandgap than Ge
=> higher operating temperature (125-175 °C vs. ~85 °C)
- (3) Si readily forms a native oxide (SiO_2)
 - high-quality insulator
 - protects and “passivates” underlying circuitry
 - helps in patterning
 - useful for dopant masking
- (4) Si is cheap and abundant (It is the second most abundant element in the earth's crust, after oxygen)

Silicon Disadvantages

- Low carrier mobility (μ) =>
slower circuits (compared to GaAs)

Material	Mobility (cm ² /V-s)
Si	$\mu_n = 1500, \mu_p = 460$
Ge	$\mu_n = 3900, \mu_p = 1900$
GaAs	$\mu_n = 8000, \mu_p = 380$

- Indirect bandgap:
 - ◆ Weak absorption and emission of light
 - ◆ Most optoelectronic applications not possible

Fabrication

Wafer Manufacturing

- Purify old sand to 99.999999%
- Grow a monocrystalline ingot Cylindrical "boule"
- Machine to a cylinder
- Grind a flat side for orientation
- Slice into wafers with diamond saw
- Coat with silicon dioxide

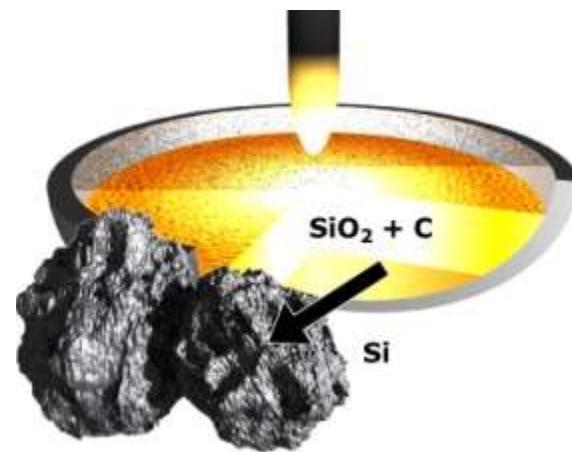
Wafers are typically 74 to 150 mm in diameter and 0.4 mm thick

Step 1: Obtaining the Sand

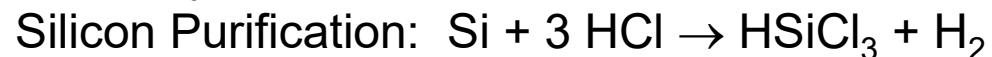
The sand has to be a very clean and good form of silicon. Most of the sand used for these processes is obtained from the beaches of Australia.

Step 2: Preparing the Molten Silicon Bath

Quartz sand (SiO_2) is reduced with carbon in an electric arc furnace at $> 1900^\circ\text{C}$ to metallurgical grade Silicon (> 98 % pure).

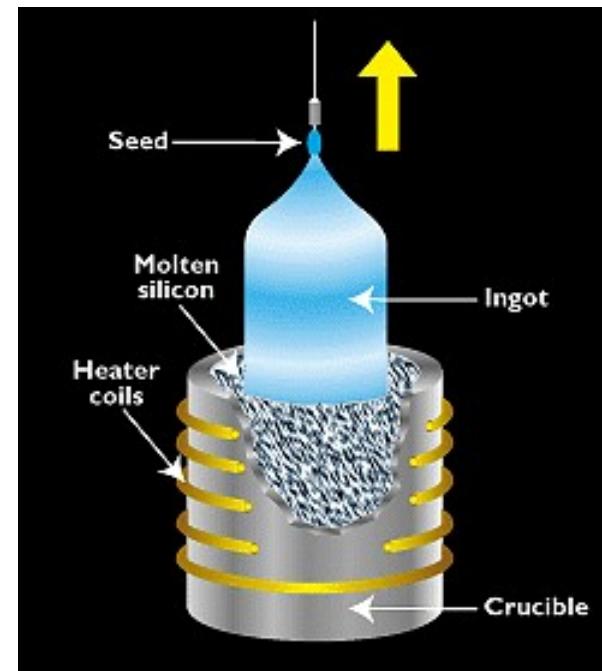
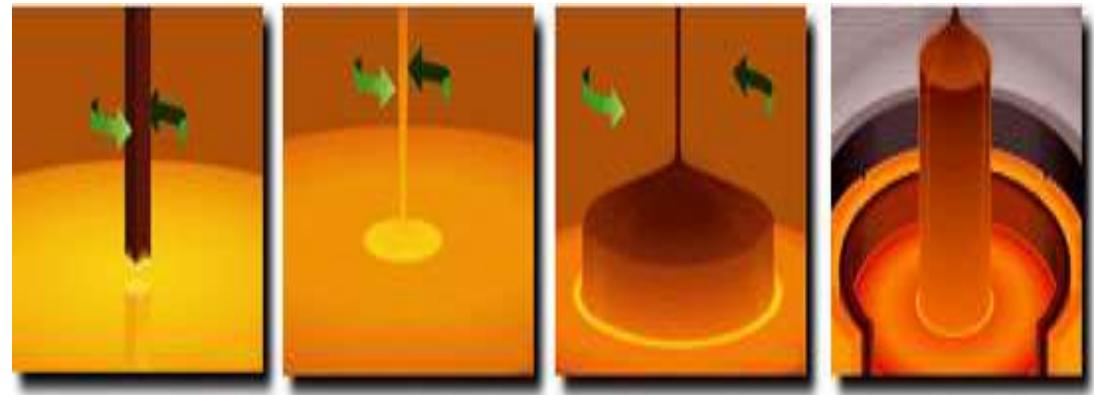


The metallurgical-grade Silicon is converted into trichlorosilane gas (HSiCl_3) using hydrochloric acid. Multiple distillation of HSiCl_3 improves the purity up to 99,999999 %.



Step 3: CRYSTAL GROWTH

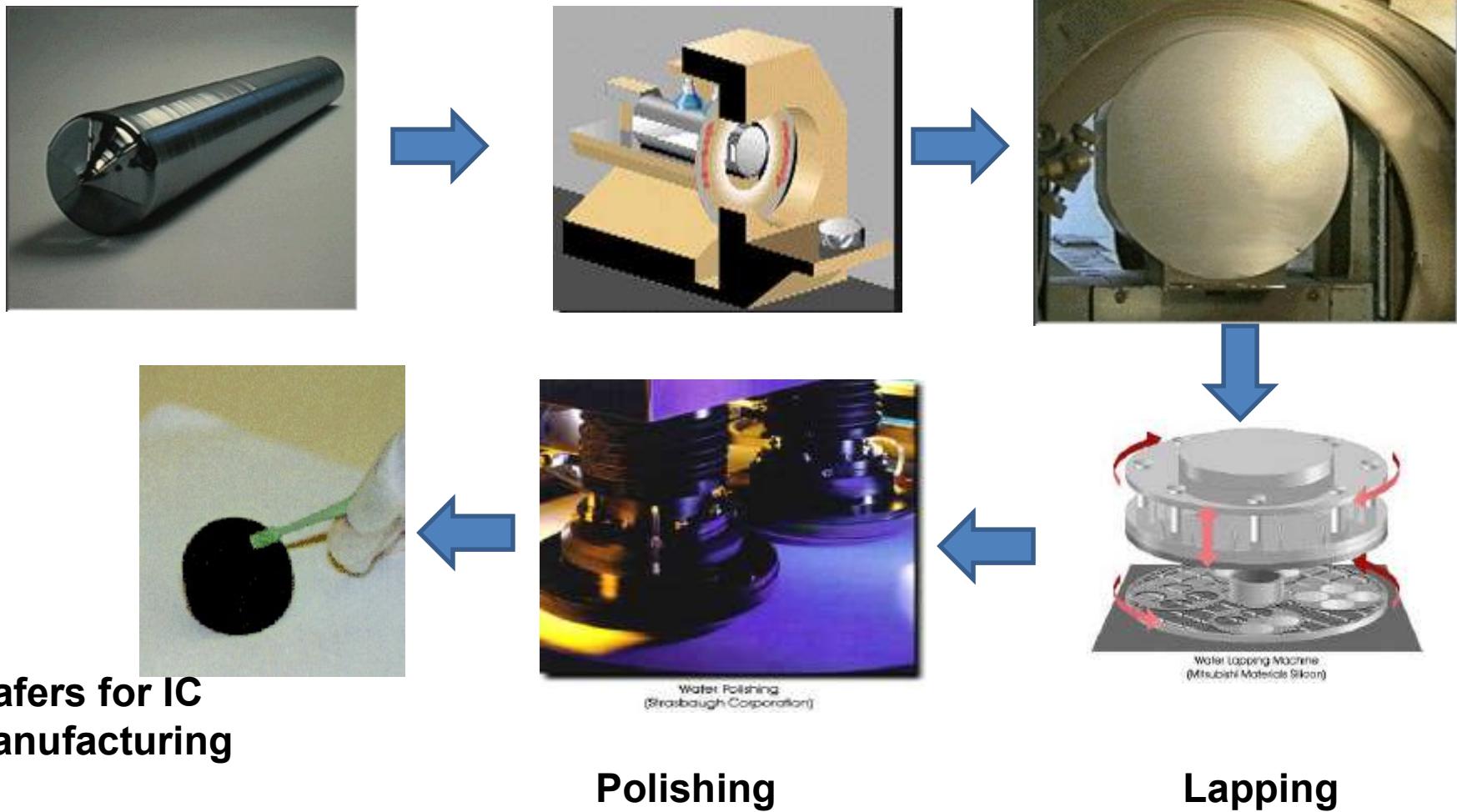
- Czochralski Process is a Technique in Making Single-Crystal Silicon
- A Solid Seed Crystal is Rotated and Slowly Extracted from a Pool of Molten Si
- Requires Careful Control to Give Crystals Desired Purity and Dimensions



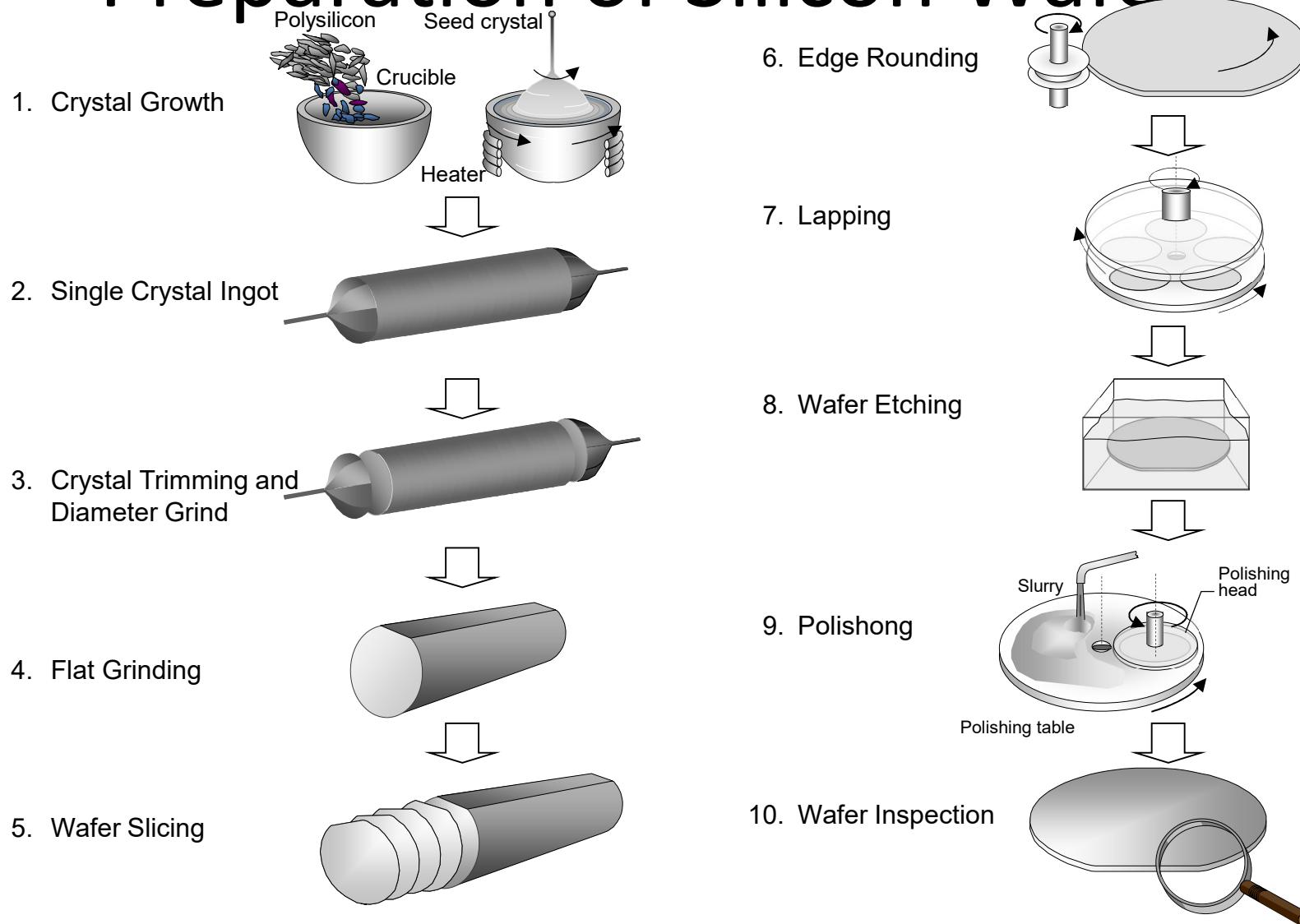
Step 4: Preparing the Wafers

Ingot is ground into the correct diameter for the wafers, the silicon ingot is sliced into very thin wafers. This is usually done with a diamond saw.

It is then polished after lapping



Preparation of Silicon Wafers



Fabrication: Basic Processing Steps

Each processing step requires that certain areas are defined on chip by appropriate masks.

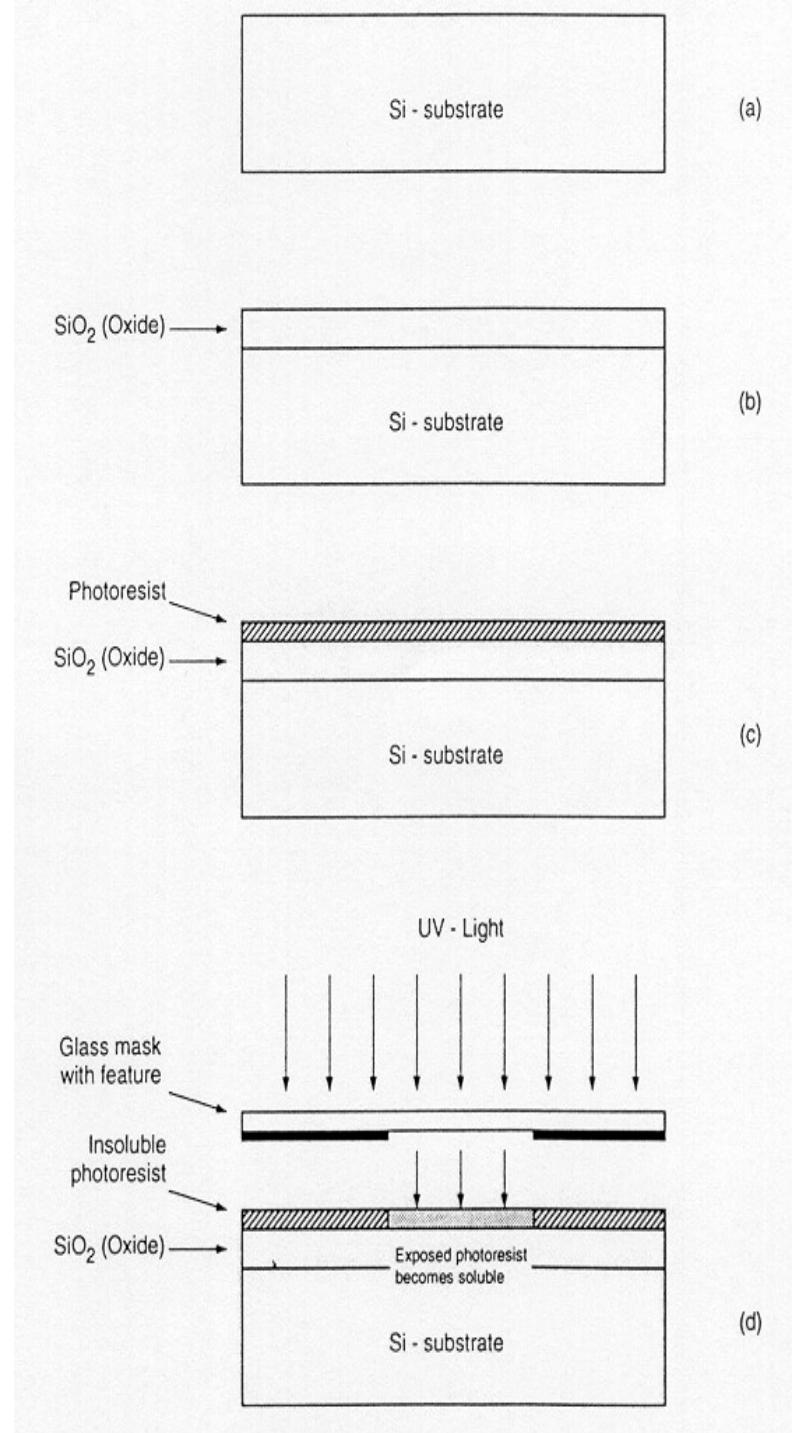
Consequently, the integrated circuit may be viewed as a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide.

In general, a layer must be patterned before the next layer of material is applied on chip. The process used to transfer a pattern to a layer on the chip is called **lithography**

Fabrication

- a) Starting Material: Lightly doped p-type Si substrate (required p impurities are introduced as the crystal is grown)
- b) Oxidize small layer, about $1\mu\text{m}$ thick
- c) Place photoresist (a light-sensitive, acid-resistant organic polymer) on top of SiO_2
- d) Place mask(pattern) above photoresist and expose it to UV light (mask defines those regions into which diffusion is to take place together with channels)

In the areas where the UV light strikes the photoresist, it is “exposed” and becomes soluble in certain solutes



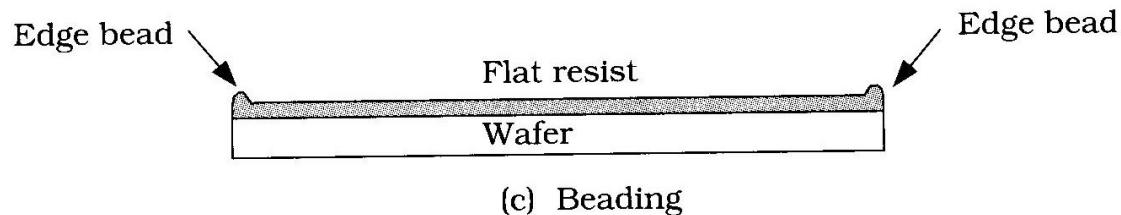
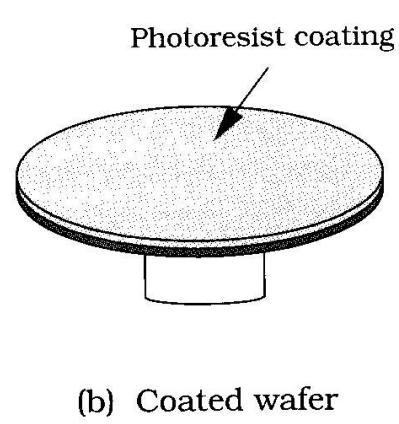
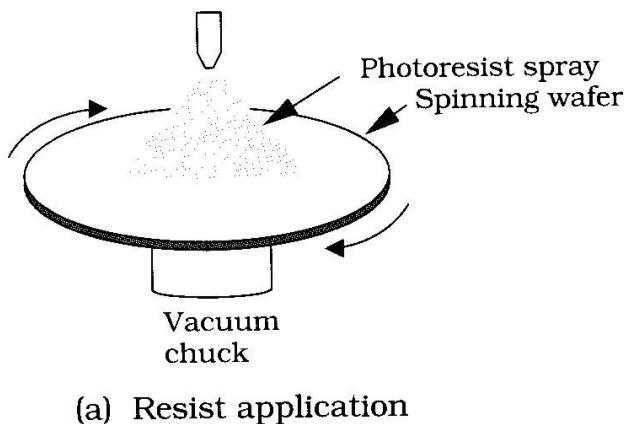
What is PhotoResist?

A light-sensitive, acid-resistant organic polymer

**If the UV light strikes the photoresist
(which is initially insoluble), becomes
soluble in certain solutes**

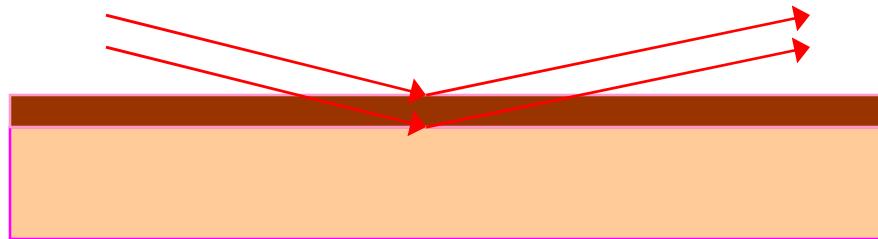
How is PhotoResist coated?

- PhotoResist normally comes in powder form, which is insensitive to light. It is **reconstituted into liquid form** by adding a solvent, typically alcohol.
- The wafer is mounted on a turntable, spinning slowly, and the photoresist is discharged into its center. **Centrifugal force spreads** the resist outward across the wafer.



PhotoResist

- The thickness that remains on the wafer is a function of the rate of wafer spin and the viscosity of the photoresist.
- The thickness is monitored by light diffraction, which is used to adjust the spin rate to reach the correct PR thickness.
- After the PR is applied, the wafer is heated (~160C) to **evaporate the solvent**, leaving a smooth surface

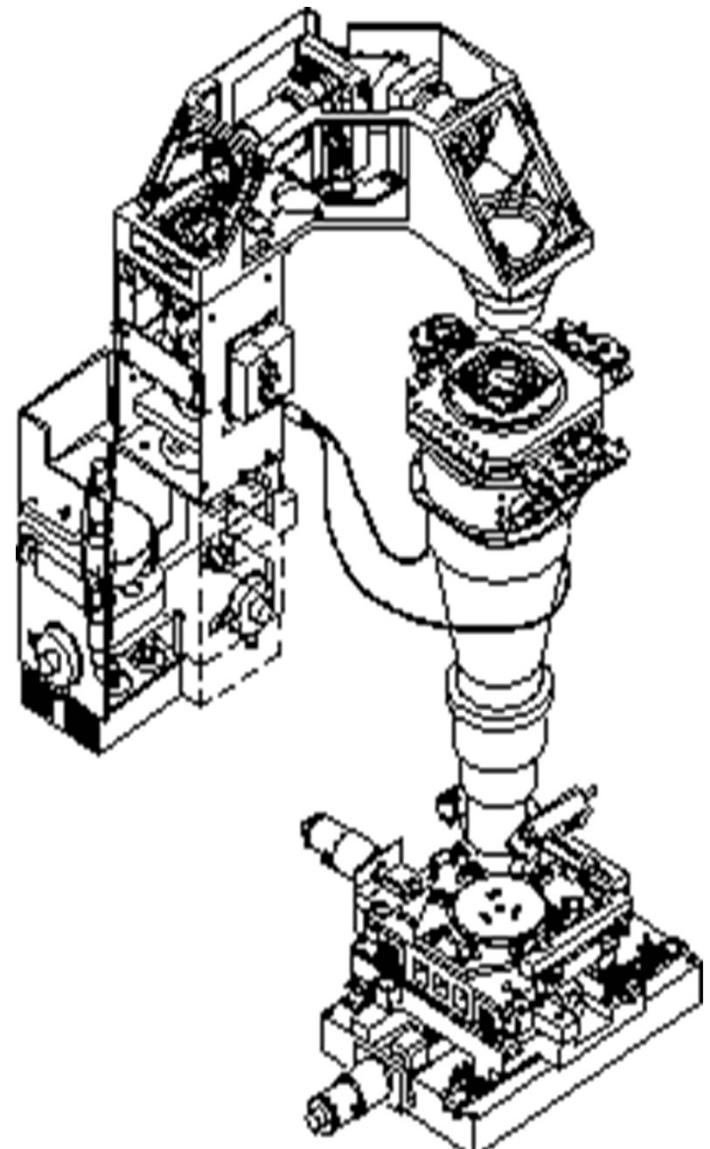
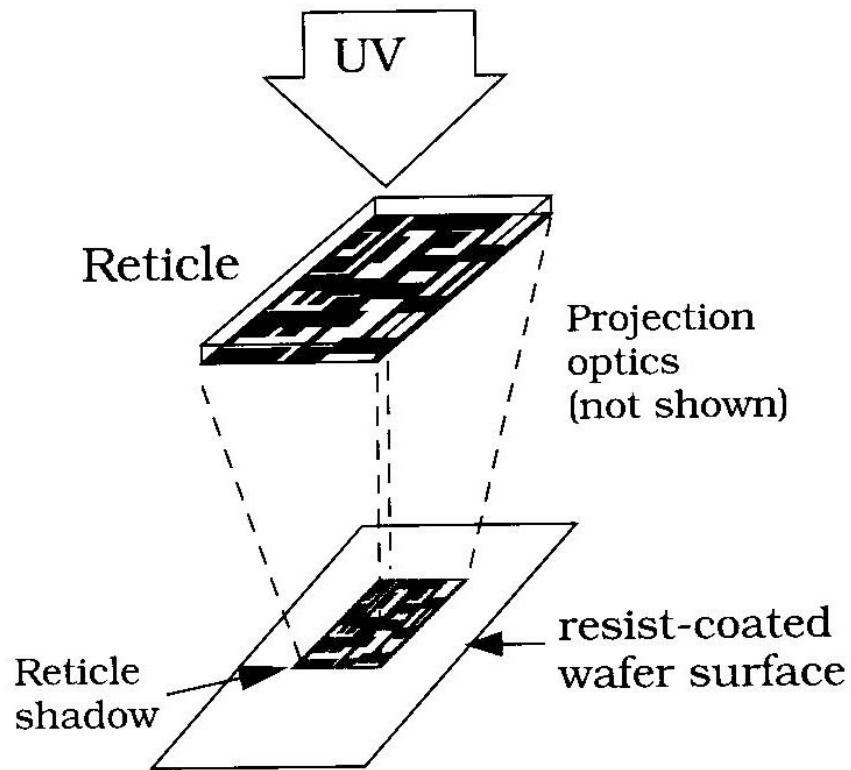


PhotoResist is used for two functions:

- Delineation for **Etching**. A blanket deposition is made on the wafer, then photoresist patterning covers the areas to be SAVED. After developing, the wafer is etched and all parts NOT COVERED by photoresist are removed.
- Delineation for **Deposition**. For ion implantation, areas are opened for doping the silicon. The photoresist absorbs all ions except for the areas which are open. In these areas (e.g. Drain or Source wells) the ions penetrate into the silicon.

Application of Ultraviolet Light

The wafer is protected from light, and is put into the photo-lithography tool. Light is focussed on the wafer, delineating the IC pattern.

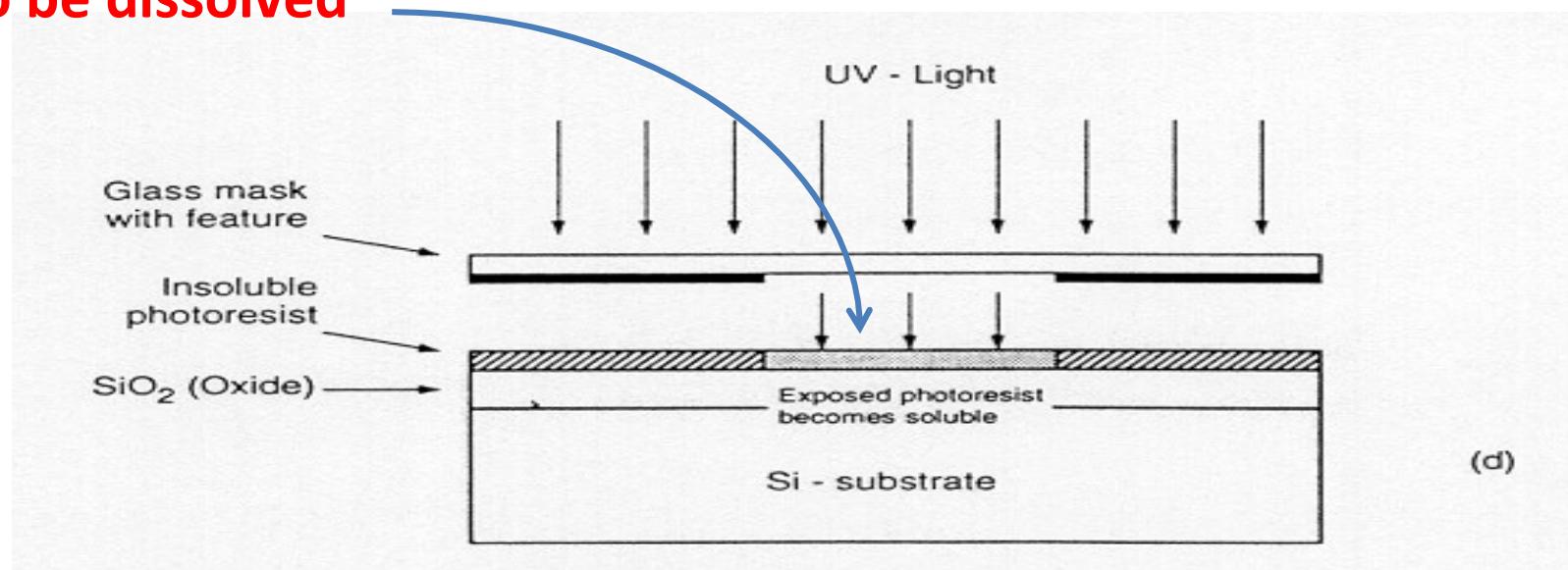


**Photo Lithography
Exposure Tool**

After application of UV light

- The wafer is removed and immersed in a **Developer Solution**. If the PR is “positive” resist, then those areas which received light will dissolve away. Negative resist reacts the opposite way, with those areas which were NOT exposed to light being dissolved. This step will leave holes in the resist layer.
- The wafer is then heated to harden the patterned resist so that it will withstand immersion into acids. A typical **hardening bake** is ~300C.
- The wafer then re-enters the processing line, for either **etching or deposition in the patterned holes**

To be dissolved



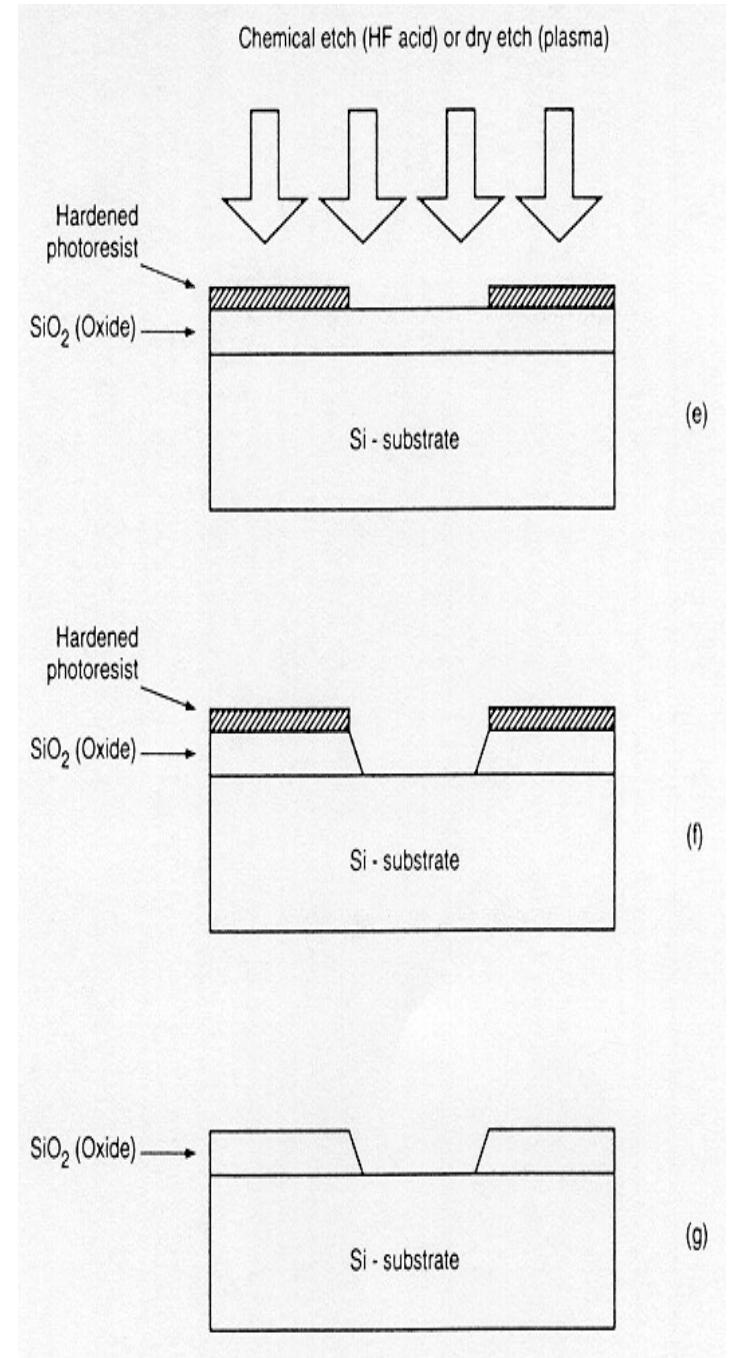
Basic Processing Steps

(e) After removal of unexposed portions of the photoresist, the silicon dioxide regions which are not covered by hardened photoresist can be etched away either by using a chemical solvent (HF acid) or by using a dry etch (plasma etch) process

(f) Note that at the end of this step, we obtain an oxide window that reaches down to the silicon surface

(g) The remaining (unexposed) photoresist can be stripped from the silicon dioxide surface by using another solvent, leaving the patterned silicon dioxide feature on the surface

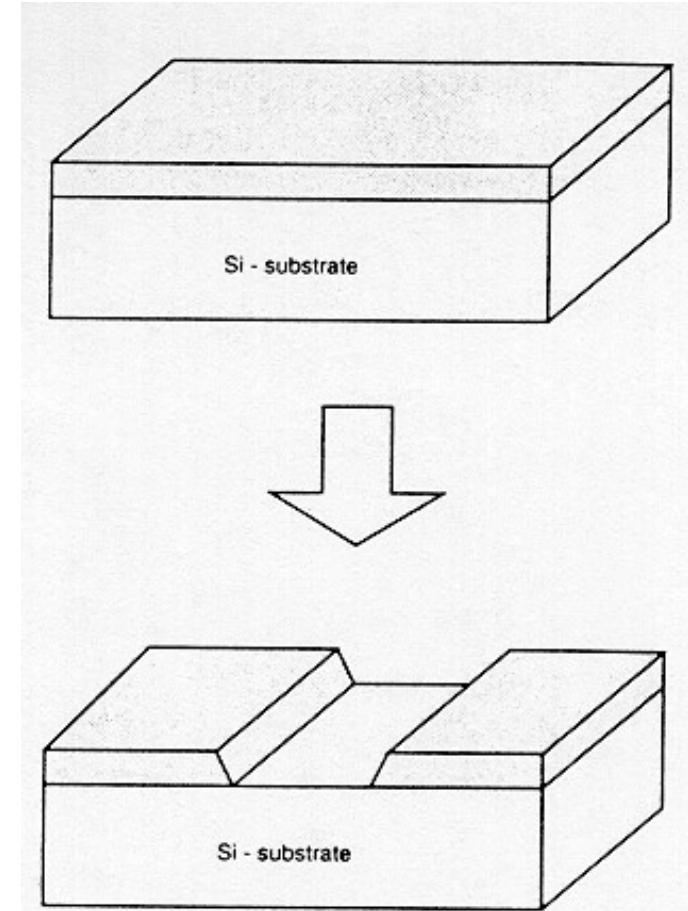
The fabrication of semiconductor devices requires several such pattern transfers to be performed on silicon dioxide, polysilicon



Basic Processing Steps

The result of a single lithographic patterning sequence on SiO_2 , without showing the intermediate steps. It took **9 steps** to make this simple hole:

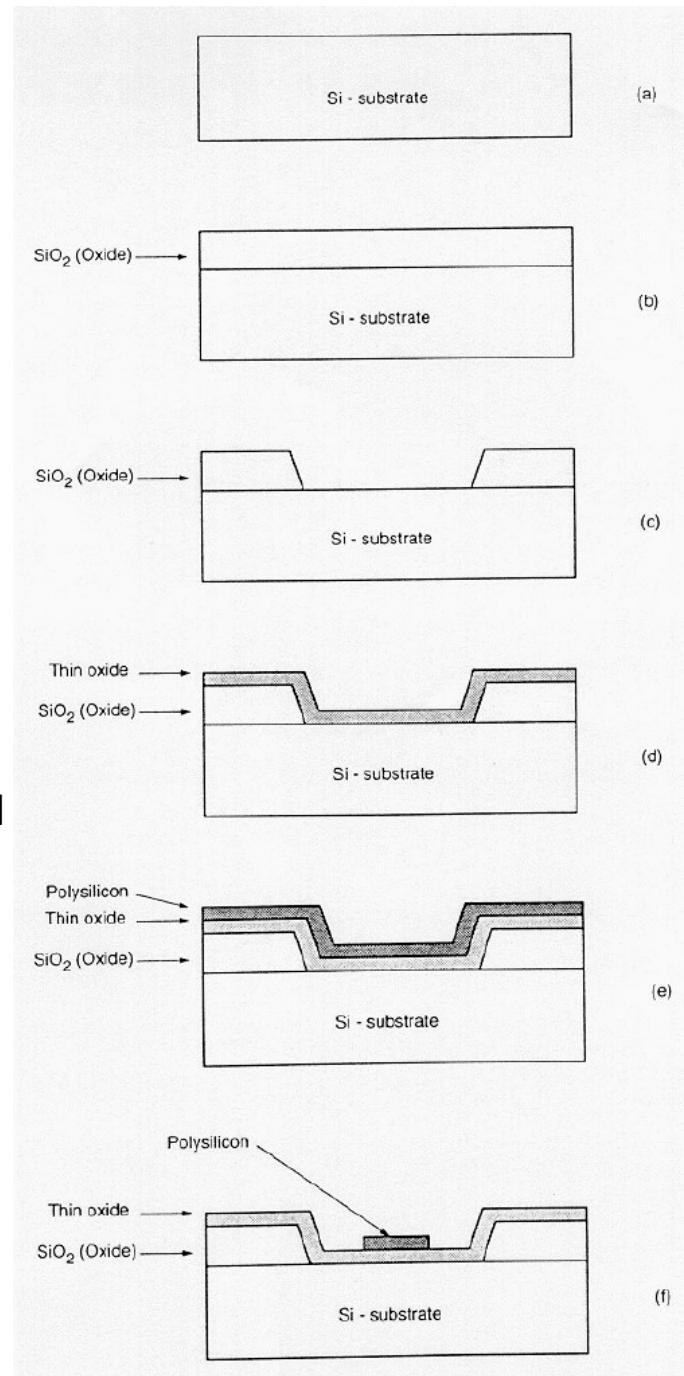
1. Oxidize silicon surface
2. Deposit photoresist
3. Anneal photoresist
4. Mount mask above silicon
5. Expose to UV light
6. Develop photoresist
7. Etch photoresist exposed to UV
8. Etch SiO_2 through photoresist hole
9. Remove photoresist



The fabrication of semiconductor devices requires several such pattern transfers to be performed on silicon dioxide, polysilicon, and metal

Making a NMOS Device

- a) Start with a silicon substrate
- b) A relatively thick silicon dioxide layer (5000\AA), also called **field oxide**, is created on the surface
- c) Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created
- d) The surface is covered with a thin, high-quality oxide layer (25\AA), which will eventually form the gate oxide of the MOS transistor
- e) On top of the thin oxide, a layer of polysilicon (polycrystalline silicon, 3000\AA) is deposited. Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms
- f) After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates. The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed



Polysilicon

One of the most popular nonmetallic conductors

Composed of a large number of nonaligned, randomly oriented, small silicon crystals

Chemically same to but electrically different from single crystal silicon

A good conductor when heavily doped, good resistor when lightly doped

Interconnection Materials

- **Polysilicon** interconnects are used to connect Gates and other short-distance connections which have minimal currents. Polysilicon is a very stable material that rarely interacts with nearby materials.
- **Metal** interconnects have 3-5x the speed of polysilicon (electron mobility is higher) and less resistance. However, metals may react with nearby materials, and may have to be encapsulated using nitrides (e.g. Si_3N_4 or TiN) to prevent unwanted reactions, or partial erosion in subsequent etching procedures. This is expensive. In Upper Metallurgy (not local interconnects) metal is always used because processing is simple: only Metal + SiO_2 .

Making a NMOS Device

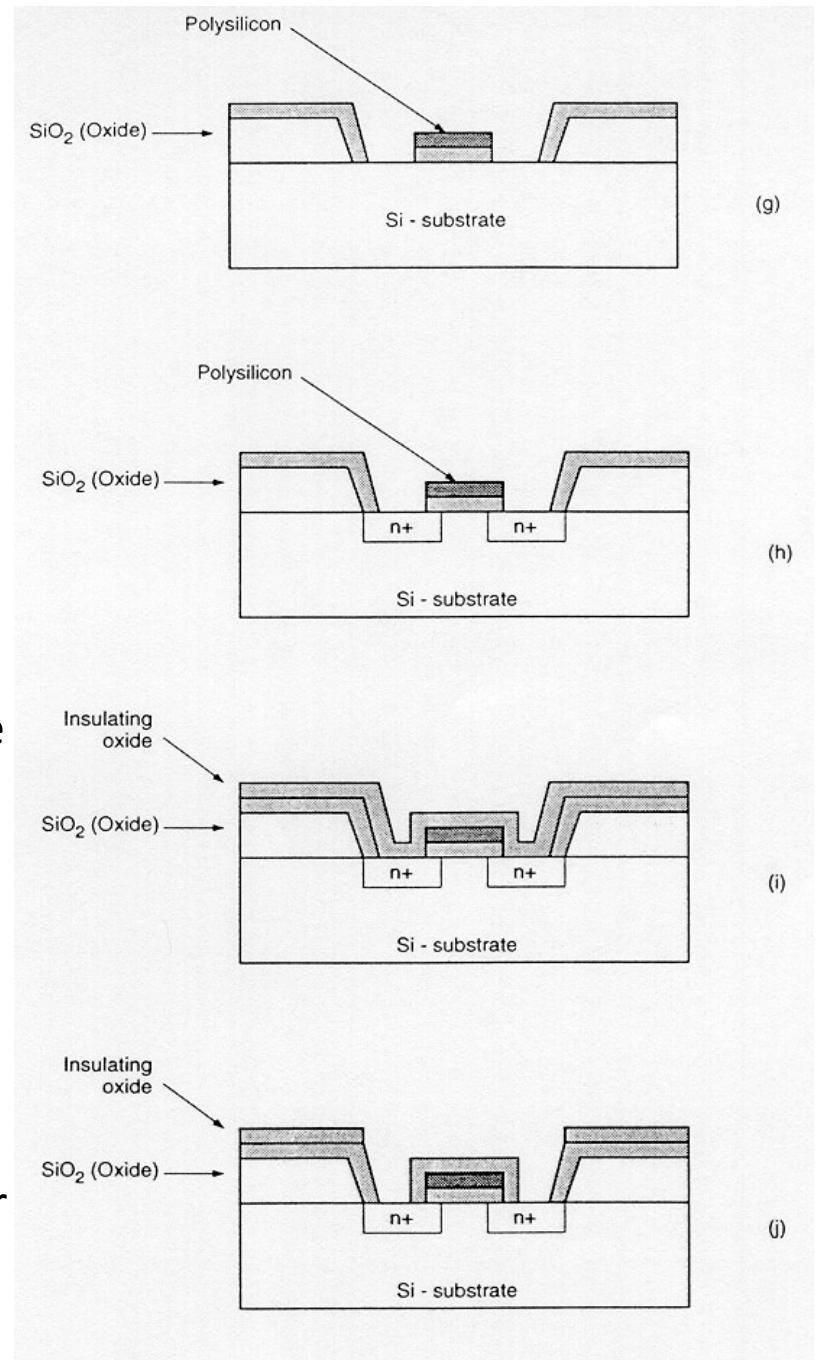
(g) The entire silicon surface is doped with a high concentration of impurities, either through diffusion or ion implantation (donor atoms to produce n-type doping)

(h) Doping penetrates the exposed areas on the silicon surface, ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity.

The polysilicon gate, which is patterned before doping actually defines the precise location of the channel region and, hence, the location of the source and the drain regions. Since this procedure allows very precise positioning of the two regions relative to the gate, it is also called **a self-aligned process**.

(i) Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide

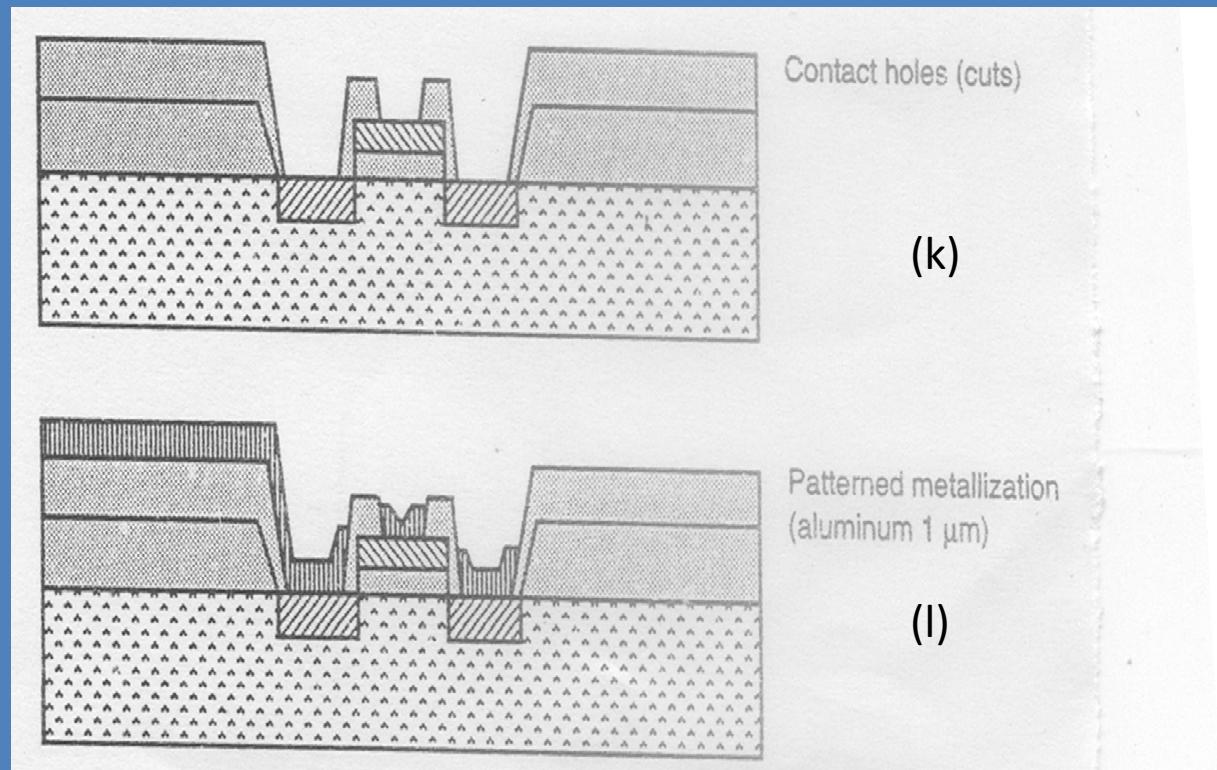
(j) The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions



Making a NMOS Device

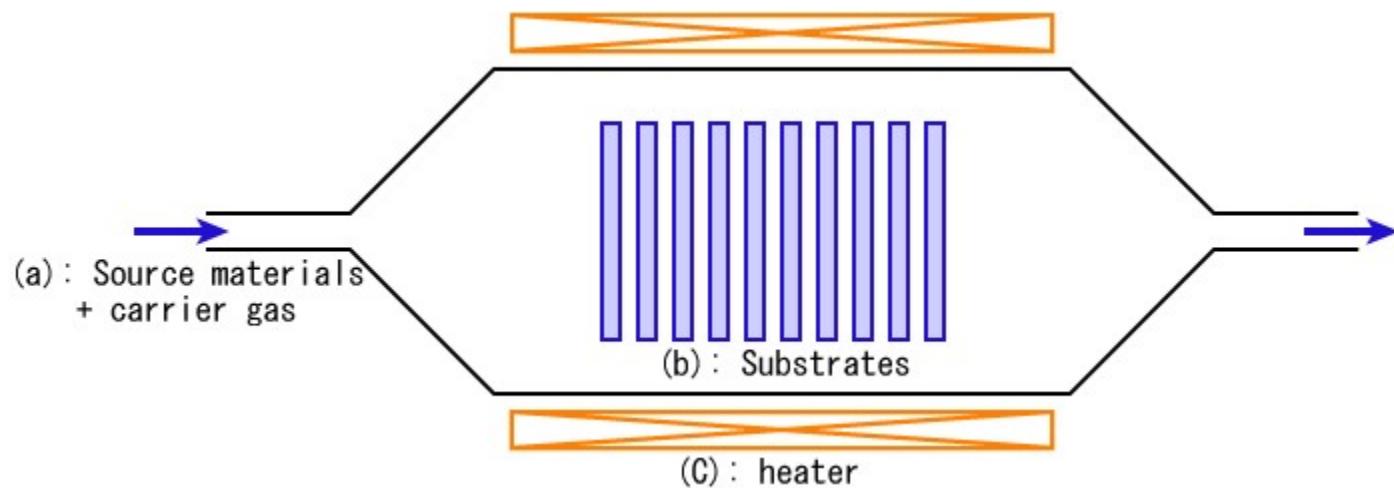
(k) Masked with photoresist and etched to expose selected areas of polysilicon gate and drain and source areas where connections are to be made

- (l) The surface is covered with evaporated aluminum (5000A) which form the interconnects. Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface.



- Usually, a second (and third) layer of metallic interconnect ($>5000\text{A}$) can also be added on top of this structure by creating another insulating oxide layer, cutting contact (via) holes, depositing, and patterning the metal.

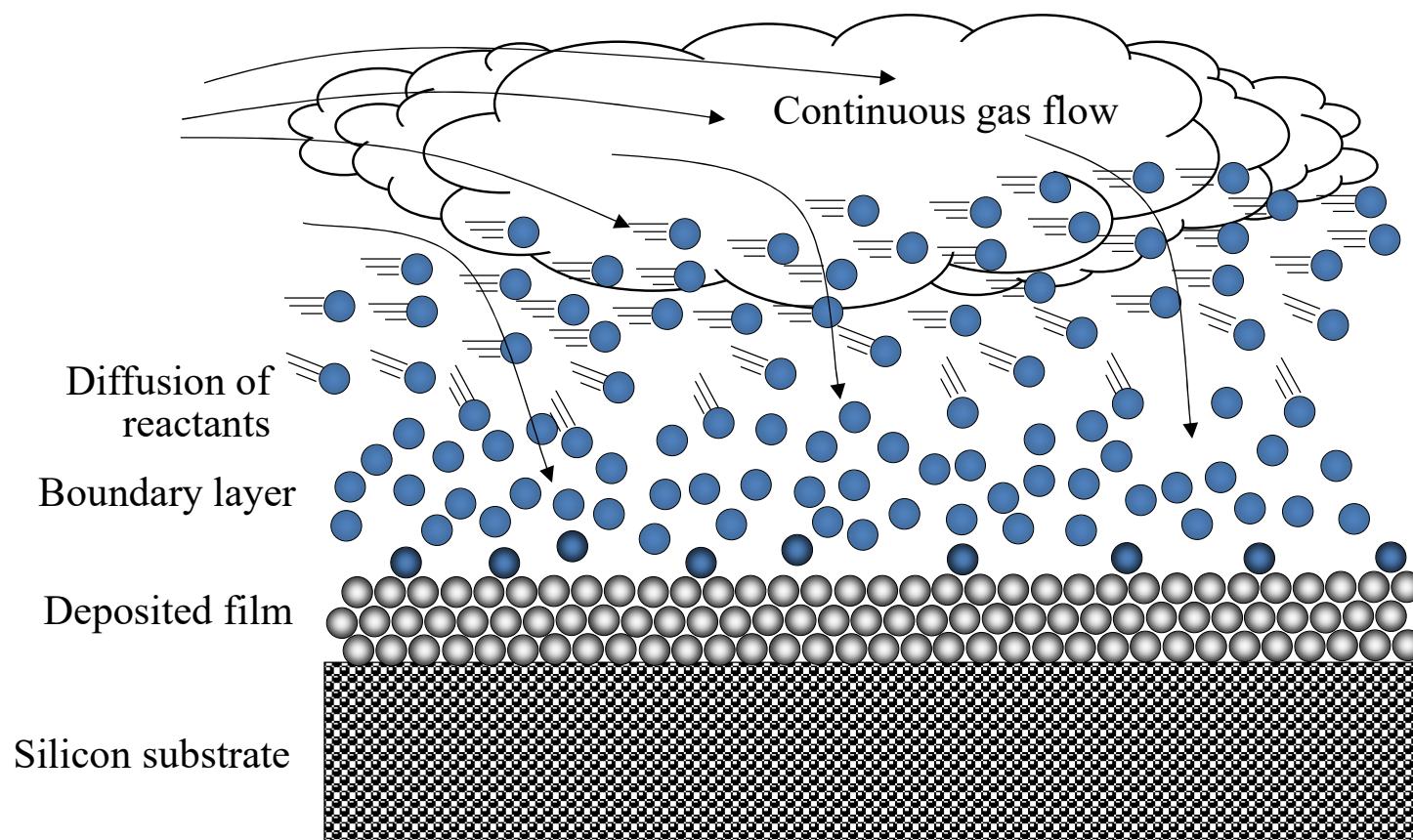
Chemical Vapor Deposition



http://en.wikipedia.org/wiki/Chemical_vapor_deposition

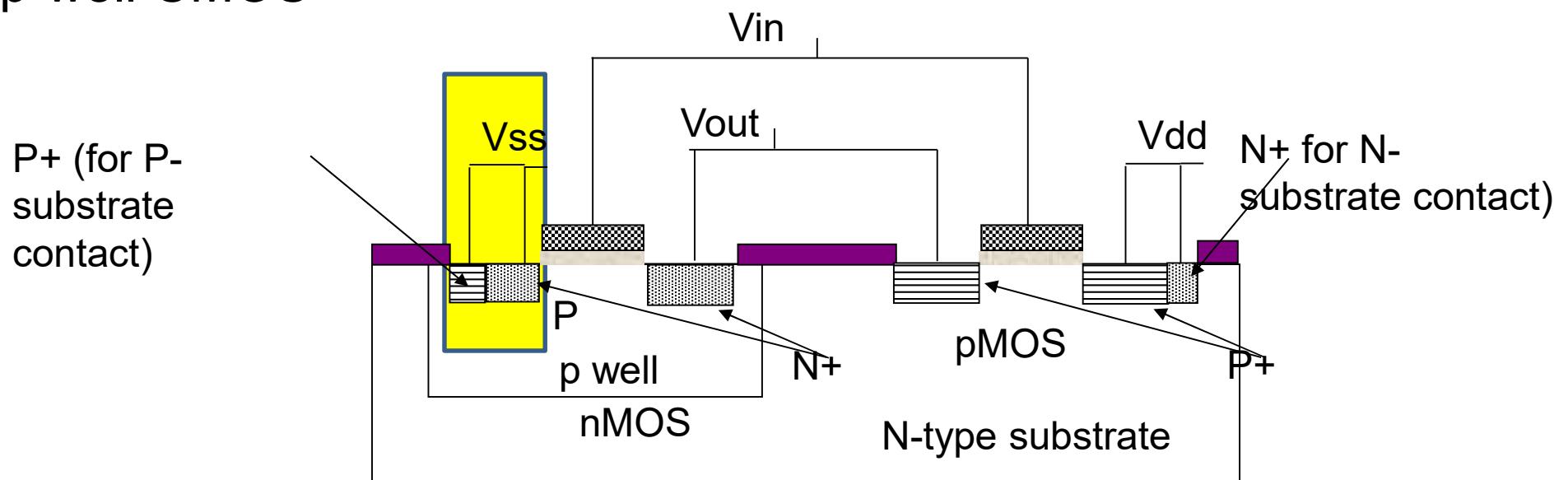
Chemical Vapour Disposition (CVD) Chemical Reactions

- $\text{SiH}_4(\text{gas}) + \text{O}_2(\text{gas}) \rightarrow \text{SiO}_2(\text{solid}) + 2\text{H}_2(\text{gas})$
- $\text{SiH}_4(\text{gas}) + \text{H}_2(\text{gas}) + \text{SiH}_2(\text{gas}) \rightarrow 2\text{H}_2(\text{gas}) + \text{PolySilicon (solid)}$



CMOS Fabrication

p-well CMOS

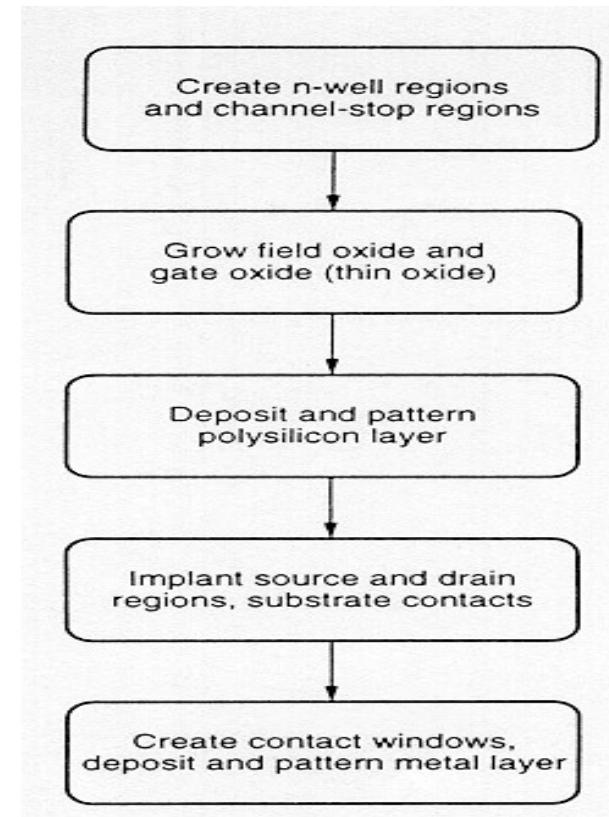
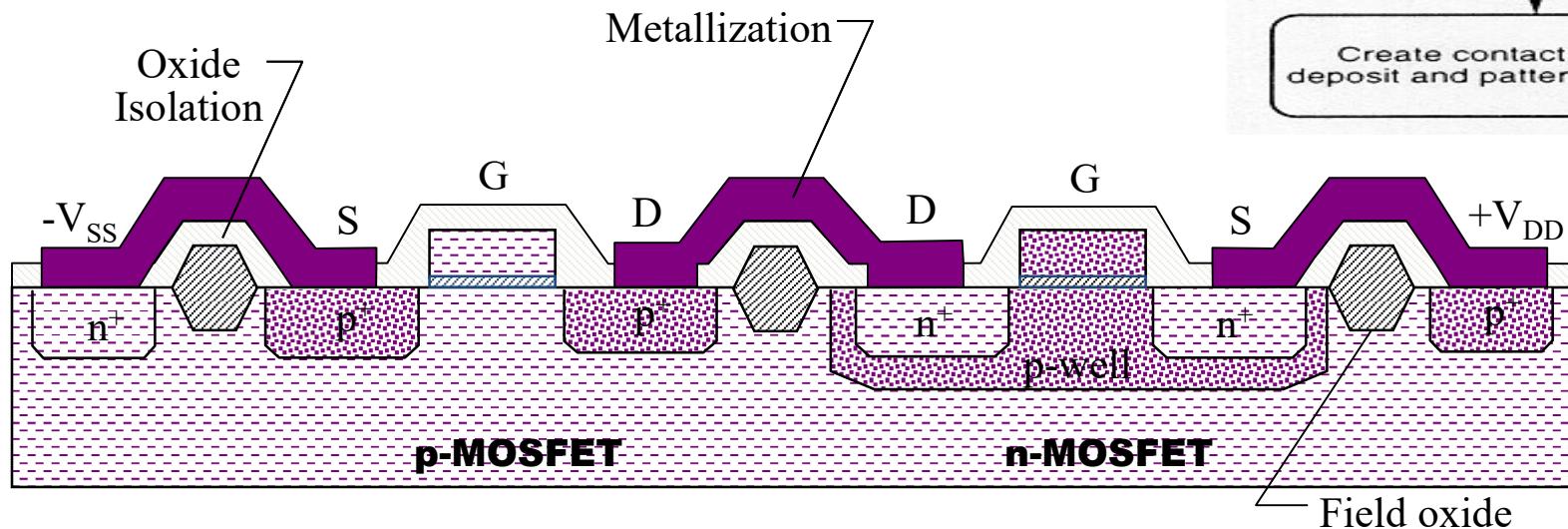


CMOS FABRICATION TECHNOLOGY

CMOS fabrication requires both nMOS and pMOS transistors to be built on the same chip substrate

To accommodate both nMOS and pMOS , special regions (called wells or tubs) must be created in which the semiconductor type is opposite to the substrate type

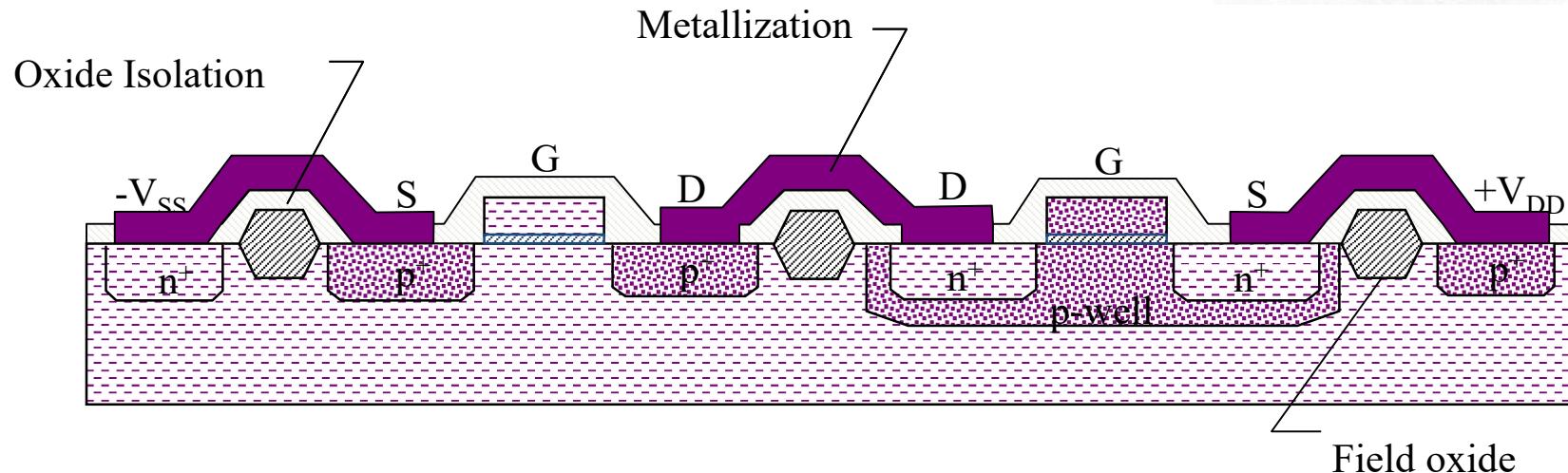
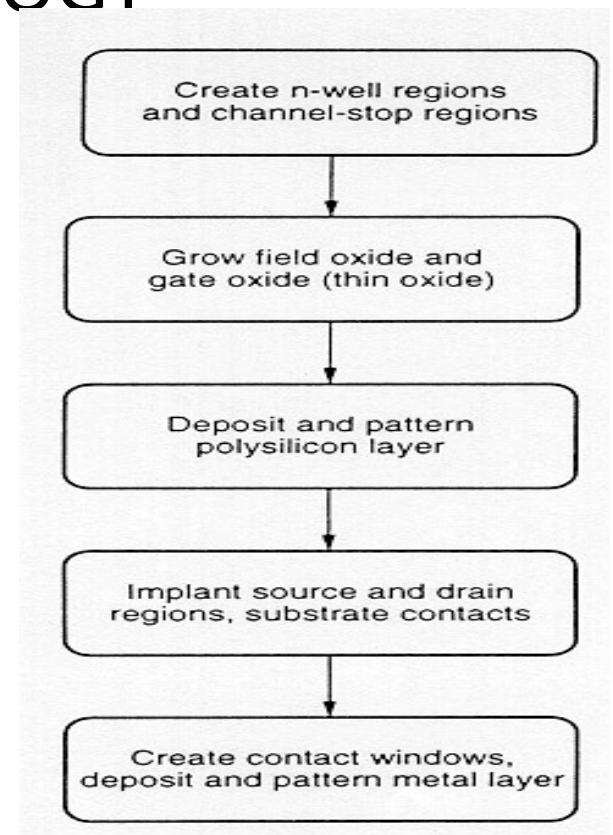
A p-well is created in an n-type substrate or, alternatively, an n- well is created in a p-type substrate.



CMOS FABRICATION TECHNOLOGY

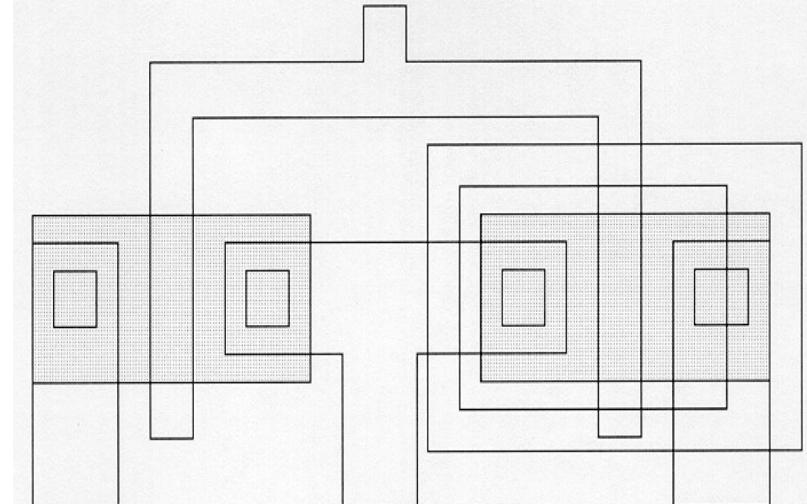
The simplified process sequence for the fabrication of CMOS integrated circuits on a p-type silicon substrate is shown.

- The process starts with the creation of the n-well regions for pMOS transistors, by impurity implantation into the substrate.
- Then, a thick oxide is grown in the regions surrounding the nMOS and pMOS active regions.
- The thin gate oxide is subsequently grown on the surface through thermal oxidation.
- These steps are followed by the creation of n+ and p+ regions (source, drain and channel-stop implants).
- Finally the metallization is created (creation of metal interconnects).

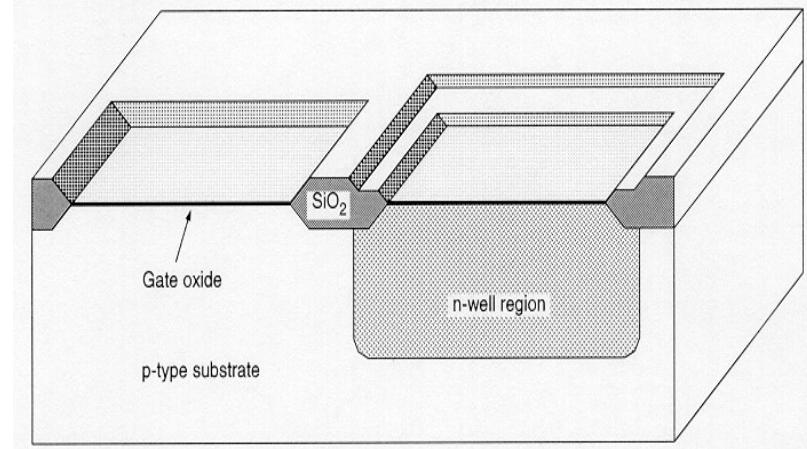


CMOS n-Well Process

- The n-well CMOS process starts with a moderately doped (impurity concentration $\sim 10^{16}/cm^3$) p-type silicon substrate. Then, an initial thick “**field**” oxide layer (**5000A**) is grown on the entire surface.
- The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide.
- Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined.
- Following the creation of the n-well region, a thick field oxide is grown around the transistor active regions, and a thin gate oxide (**25A**) is grown on top of the active regions.



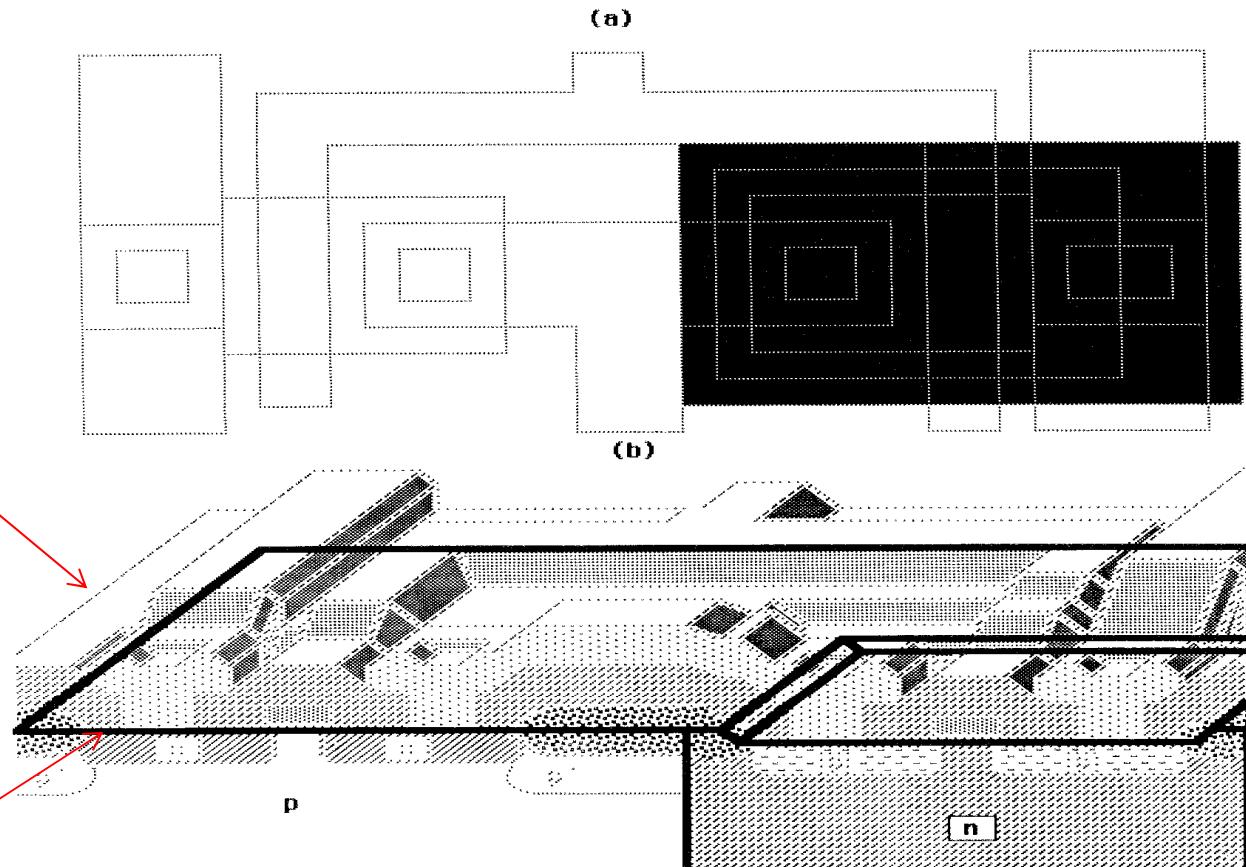
Top view of
lithographical mask



Cross-sectional view of
relevant areas

CMOS Fabrication Process

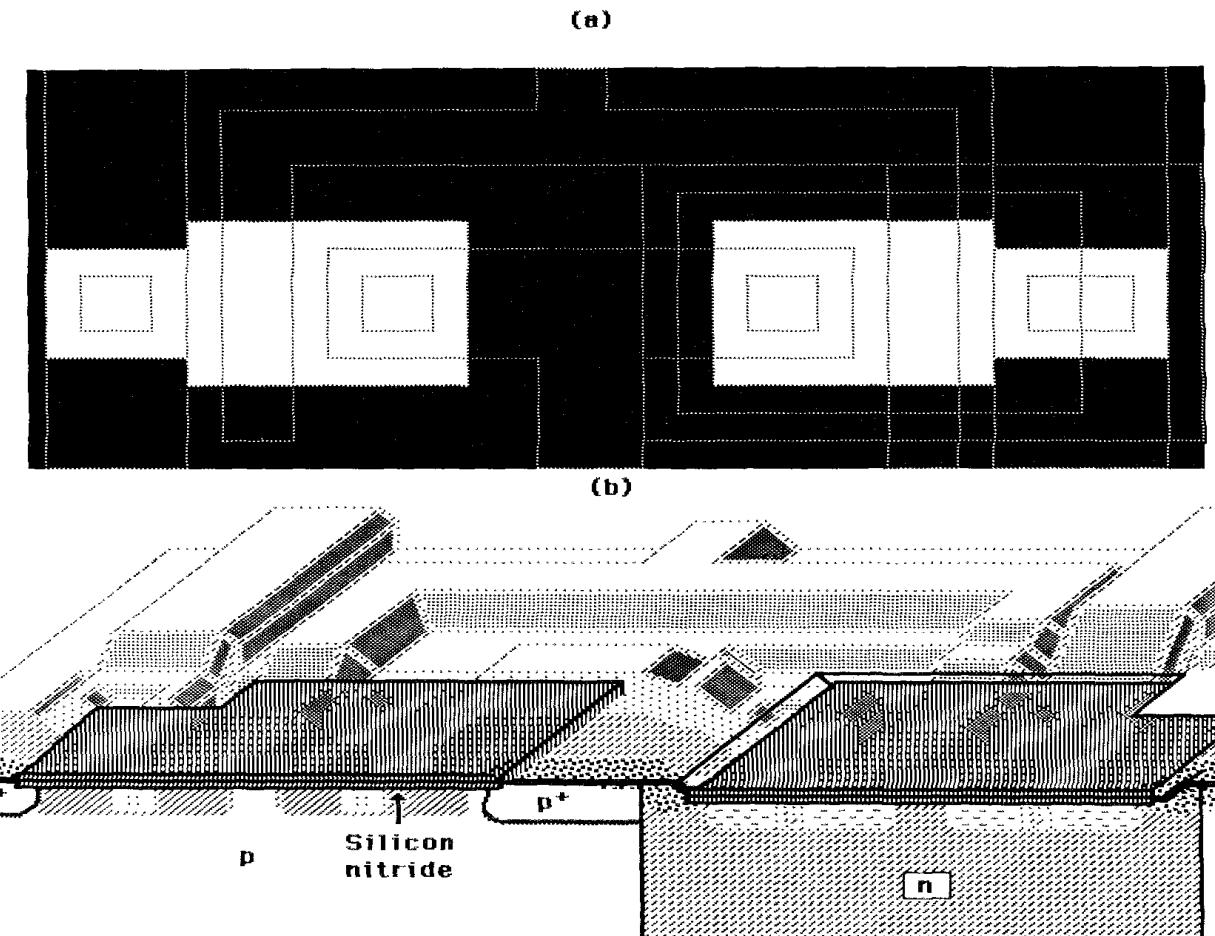
Dotted outline
is the final
circuit (for
reference).



Heavy line is
the current
process step

Well Implant and drive-in in the n-well CMOS Inverter
(a) Window in the mask (b) Cross section

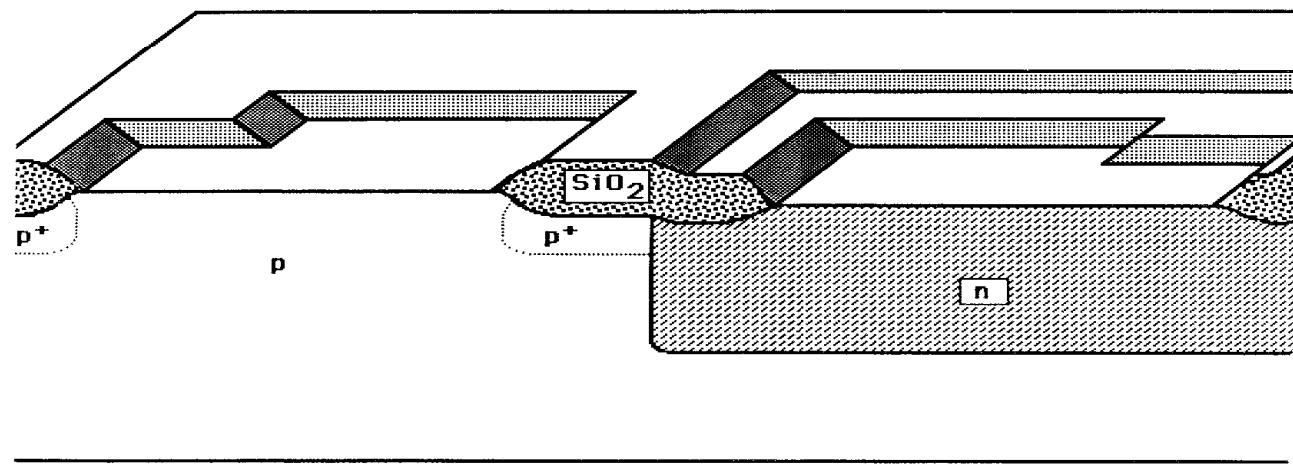
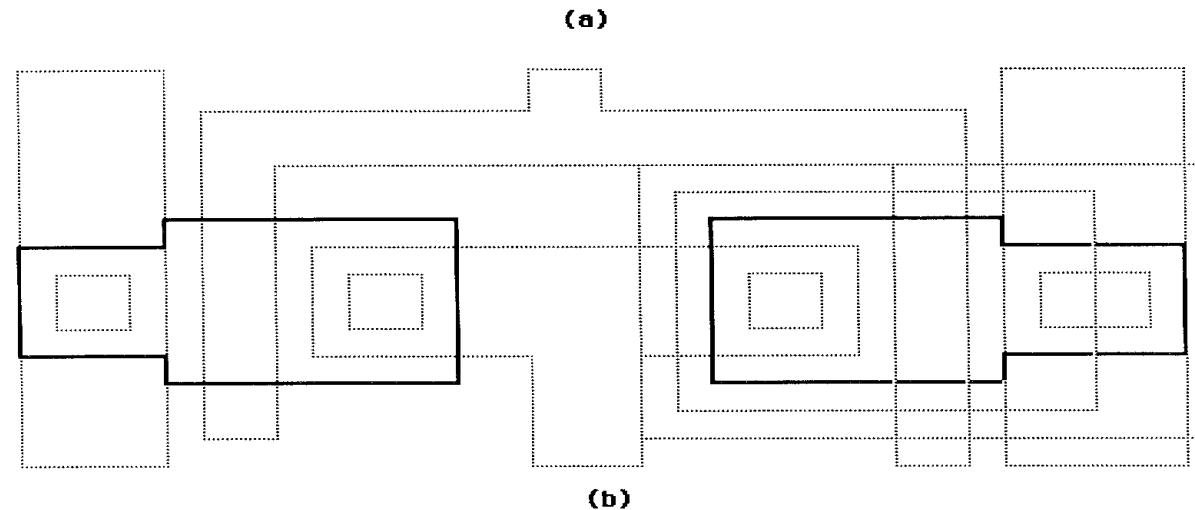
P+ Implant and Mask for Field Oxide Growth



Formation of active regions

(a) Window in the mask (b) Cross section

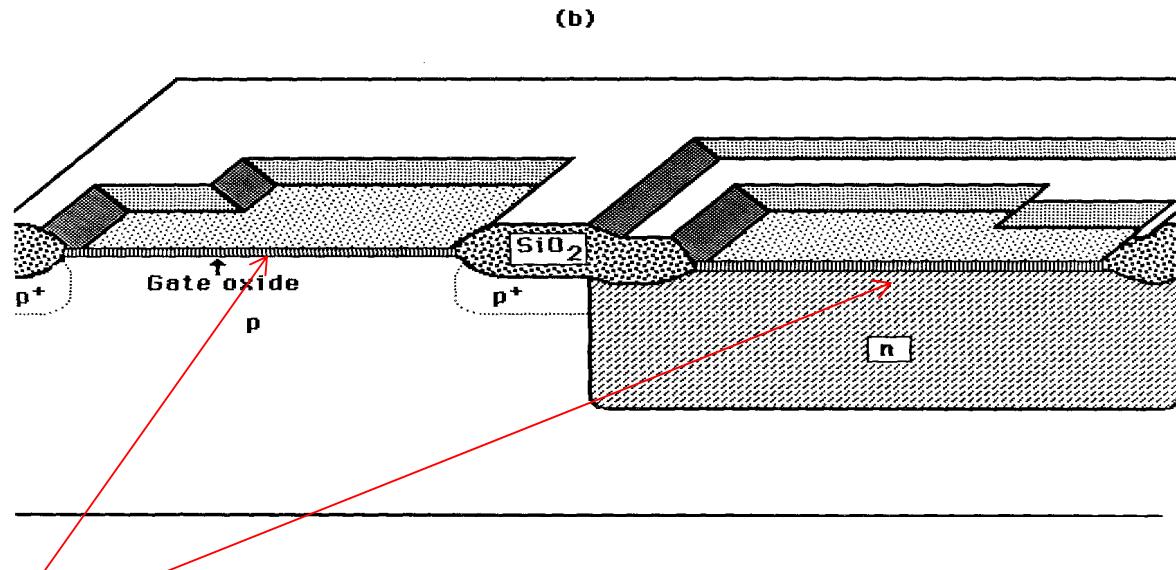
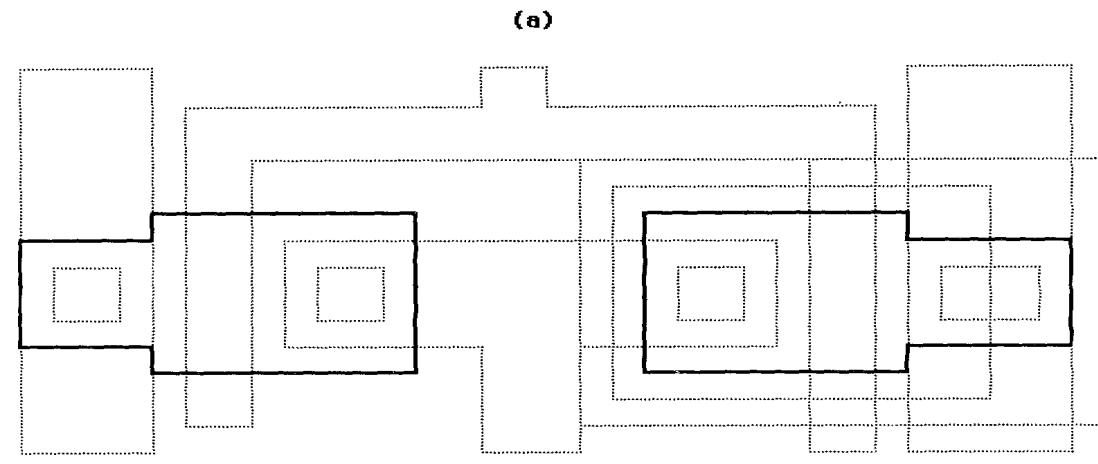
Thick Field Oxide Growth



Active regions

(a) Edges of active region in the mask (b) Cross

Gate Oxide Growth

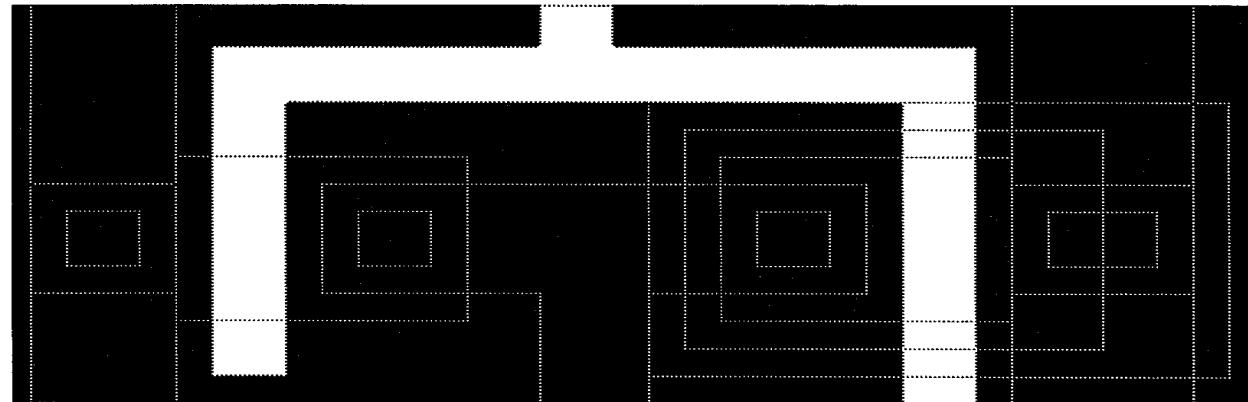


Before the next process step, by masking the wafer, the channel regions can be separately implanted. This extra step will allow adjustment of V_{tn} and V_{tp} by altering N_B locally under each gate.

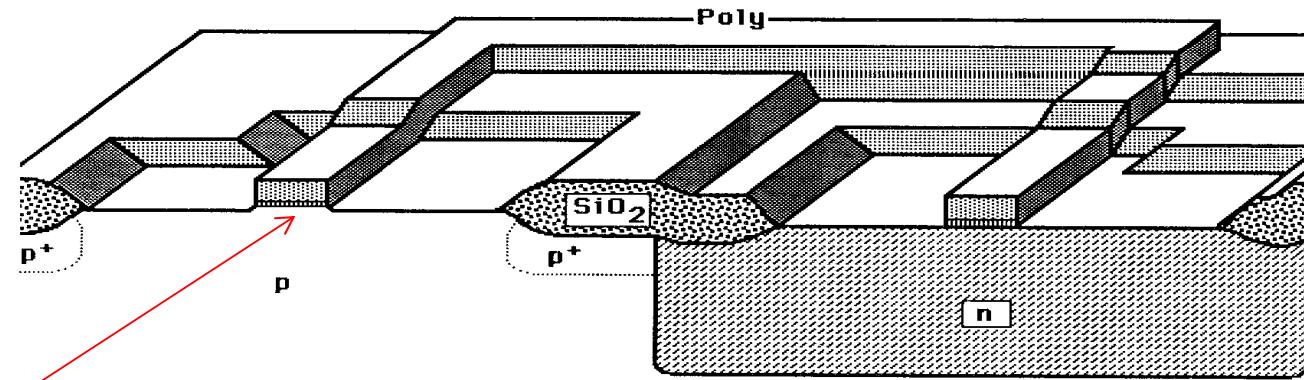
(a) Edges of gate oxide region (b) Cross section

Deposit Gate Poly Si Layer and Etch

(a)



(b)

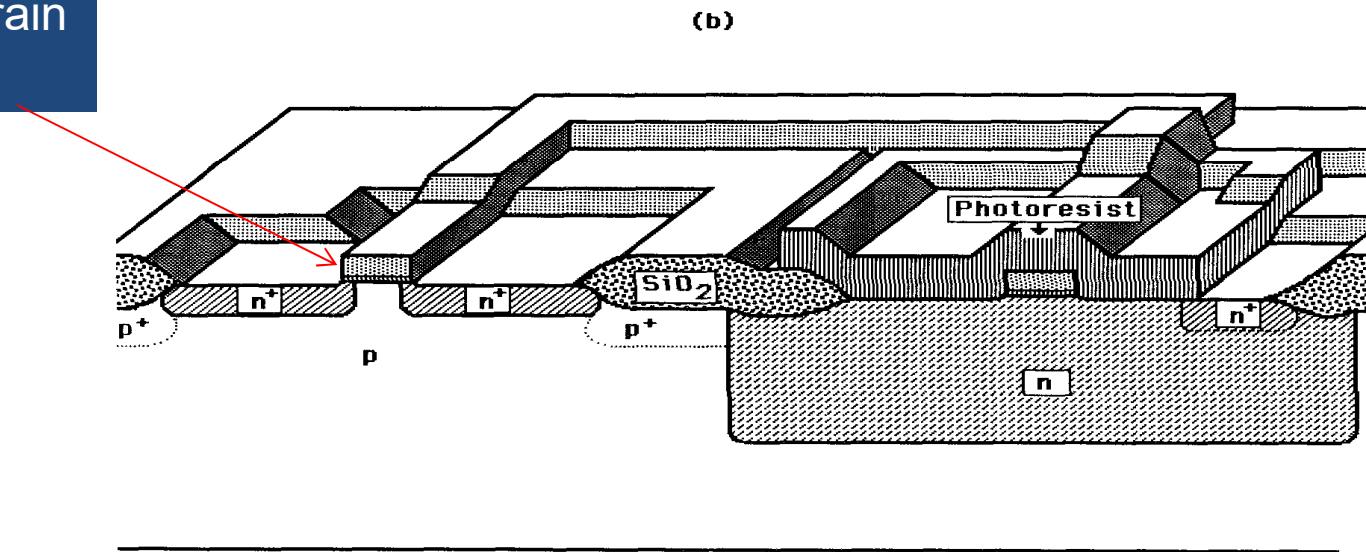
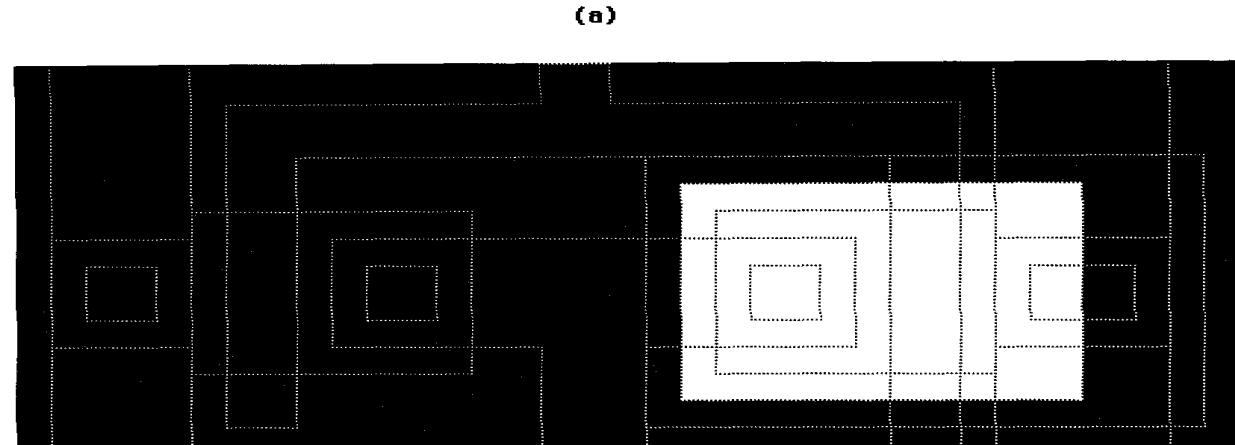


Avoid undercut of poly so that L is accurately transferred from the mask.

Polysilicon Region: (a) Window in the mask (b) Cross section

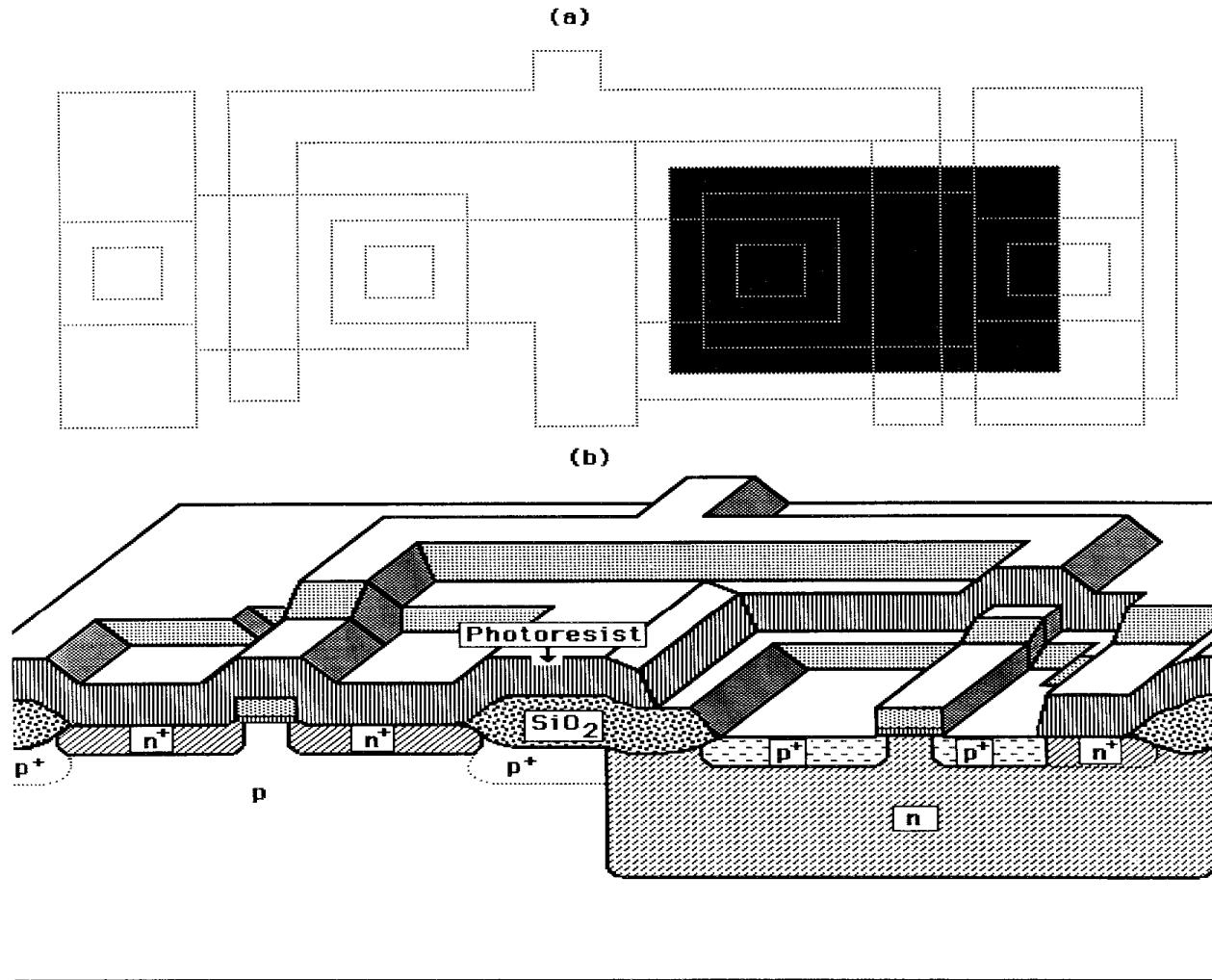
Implant n-Channel n+ Regions

Gate poly acts as mask
and thus alignment of gate and source/drain is



Implantation of n-channel transistor drain and source
(a) Window in the mask (b) Cross section

Implant n-Channel p+ Regions

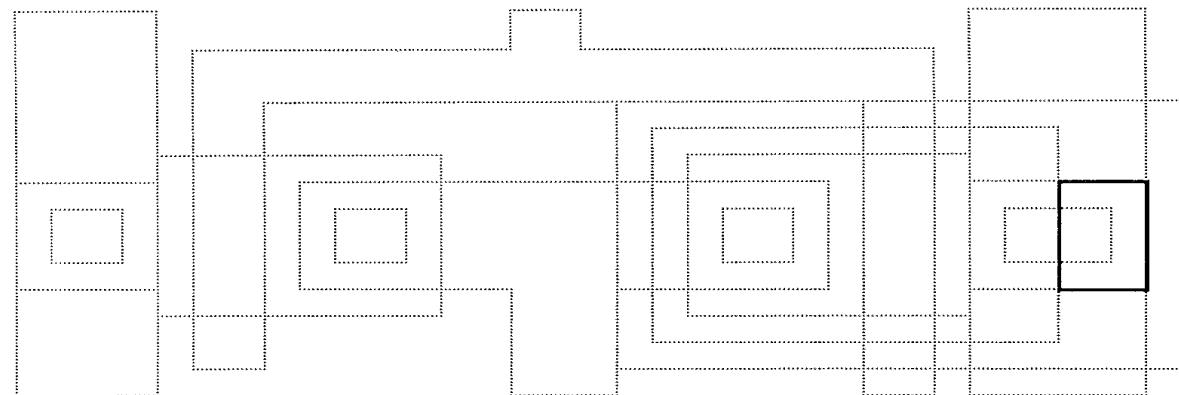


Implantation of p+ regions

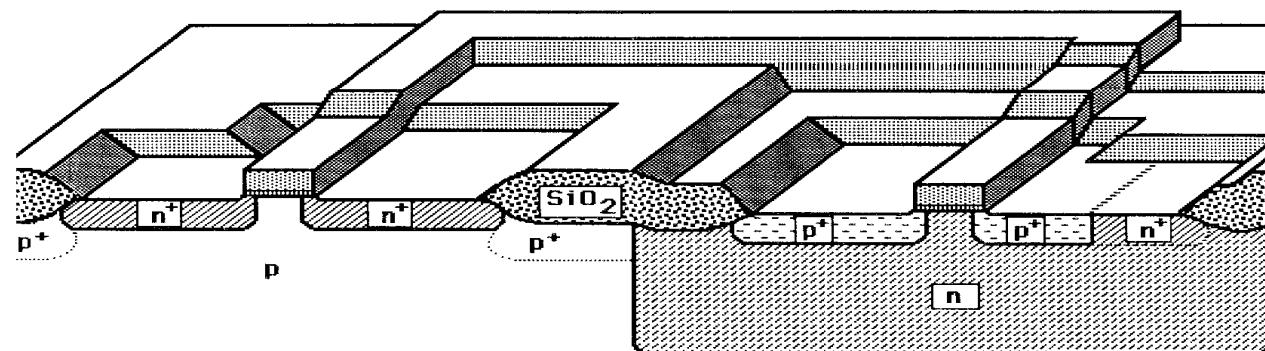
(a) Window in the negative of n-select mask (b) Cross section

Implant n-Well n+ Region

(a)

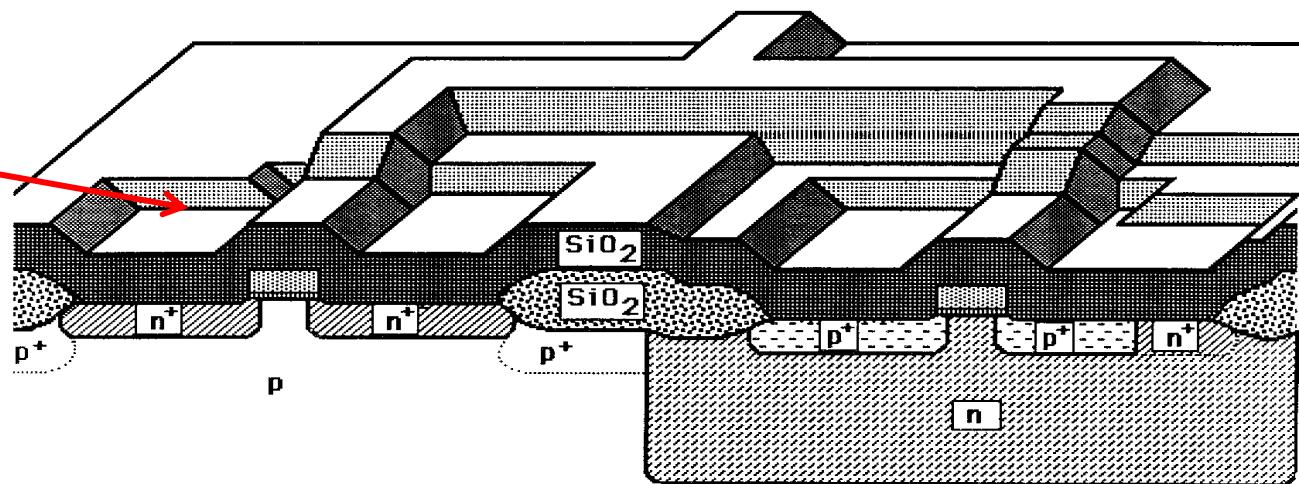
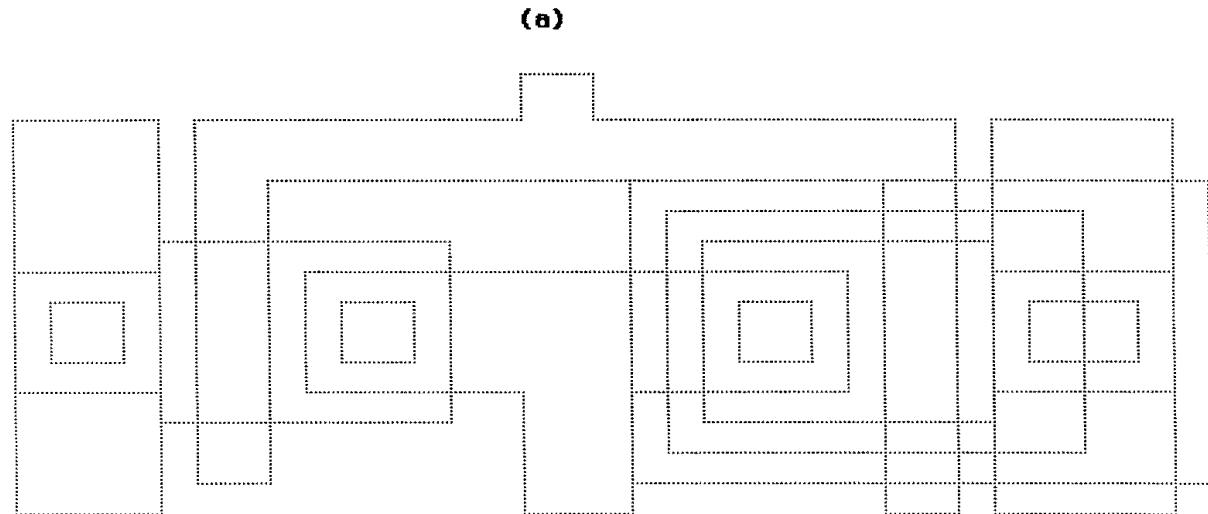


(b)



(a) Edges of drain region of p-channel (b) Cross section

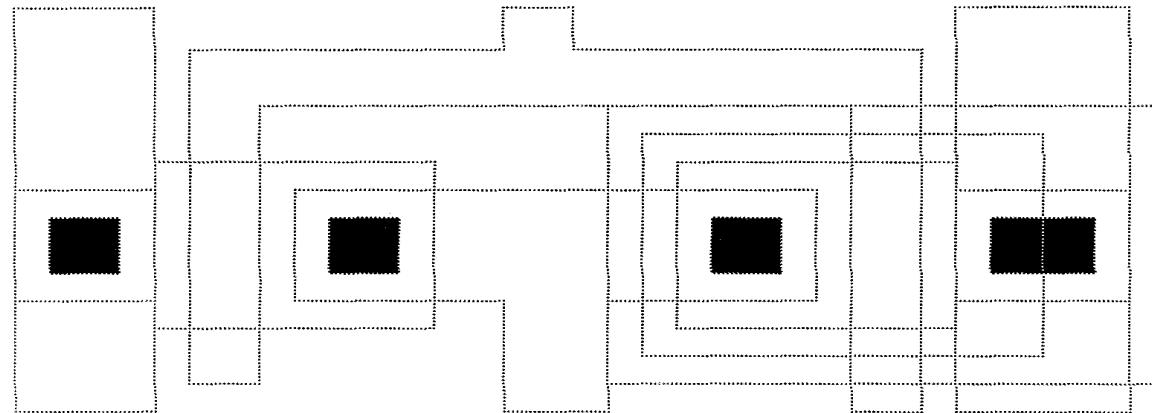
Abrupt
steps are
smoothed
over with
deposited
insulating
layer



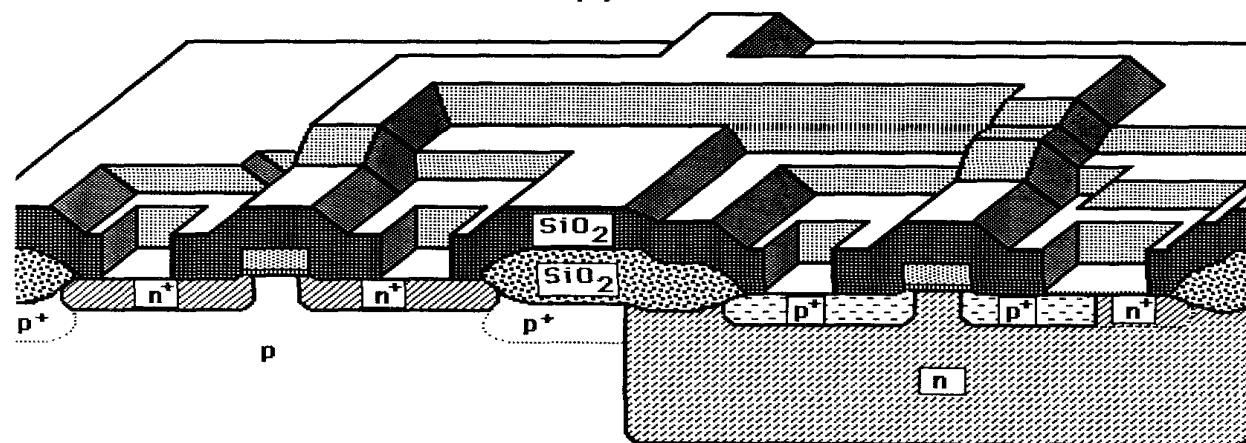
Deposition of CVD SiO₂

Open Contact Cuts

(a)

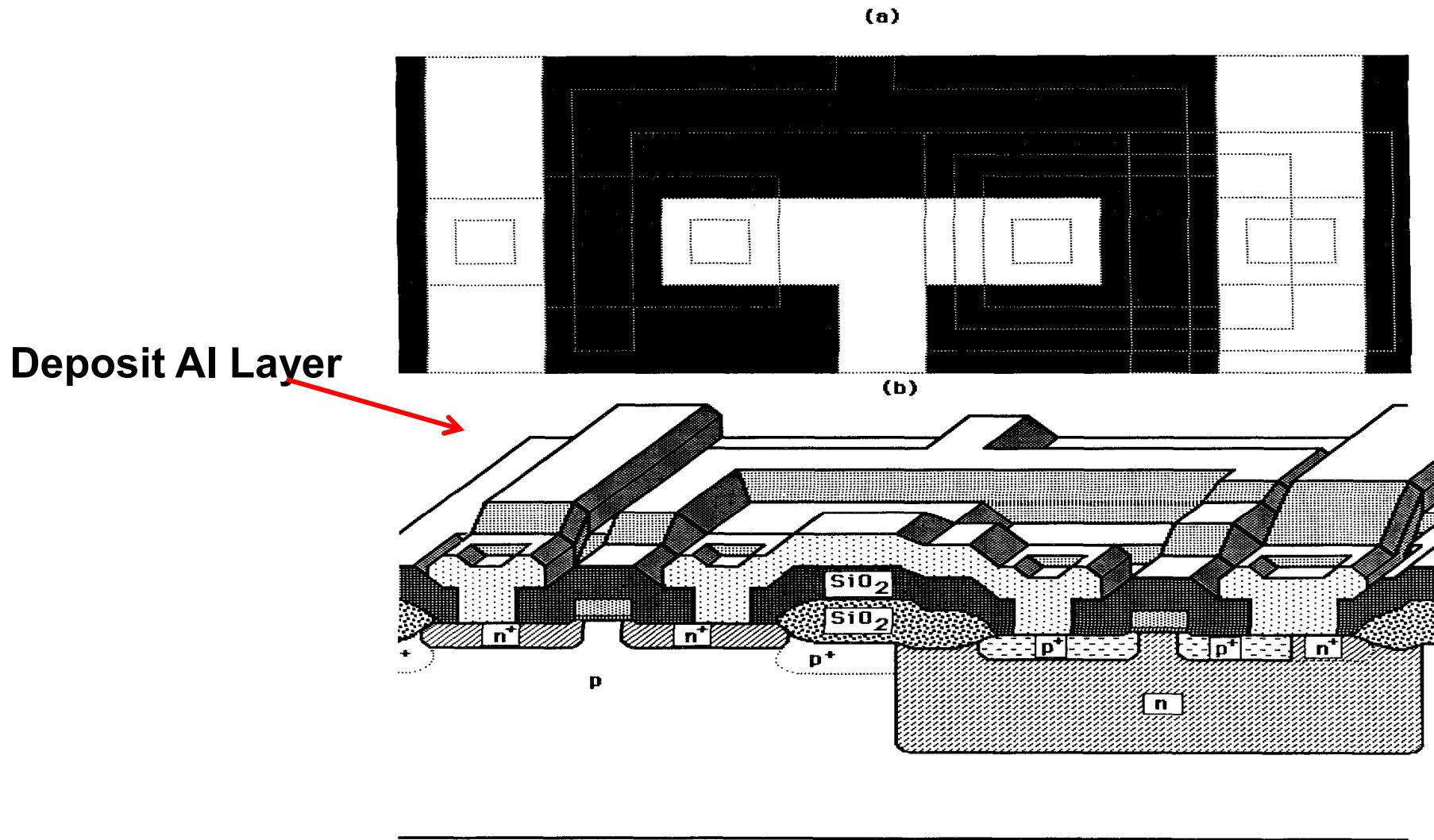


(b)



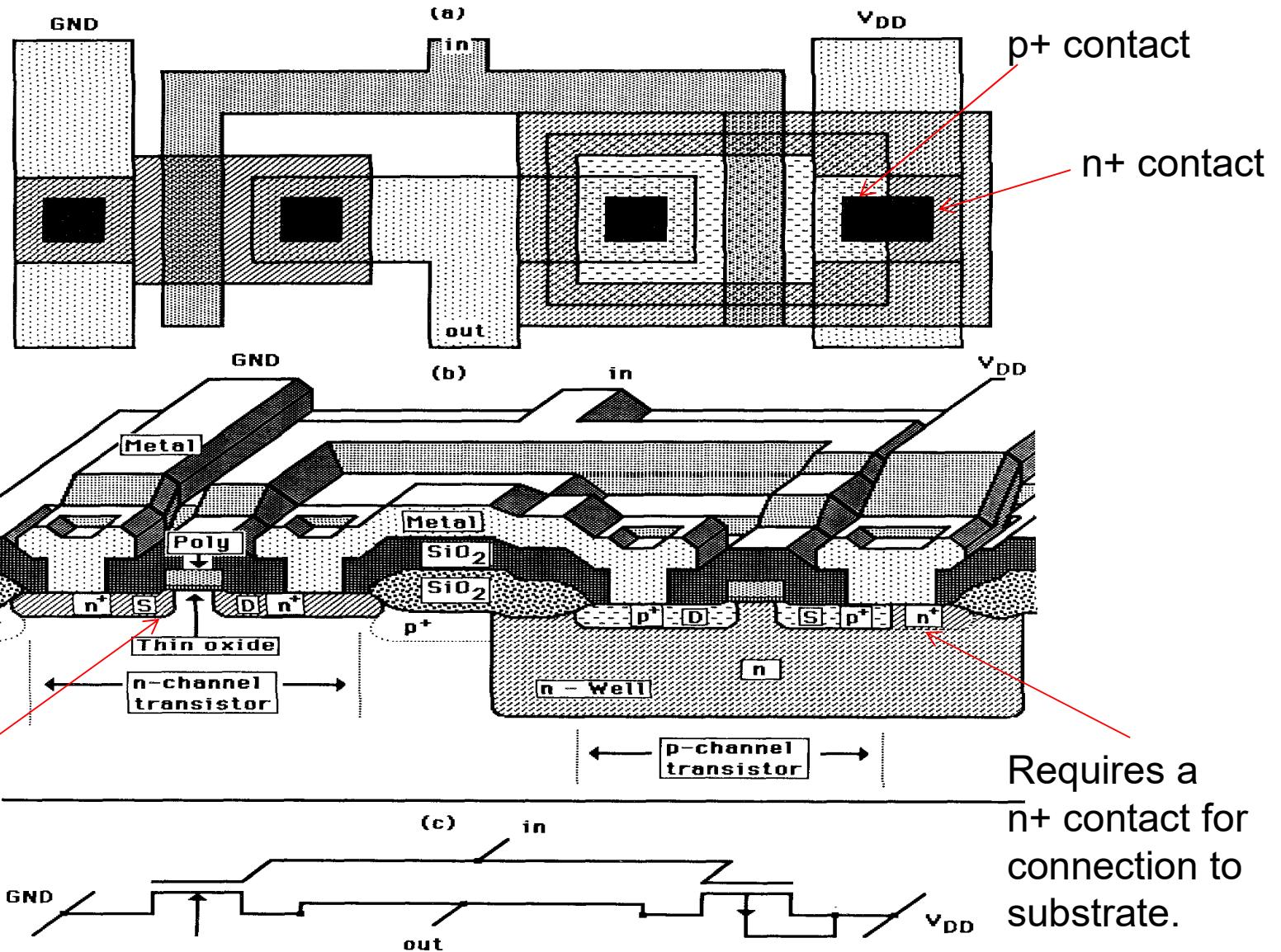
Contact cuts: (a) Window in the mask (b) Cross section

Metallization



(a) Window in the mask (b) Cross section

Final Circuit: CMOS Inverter

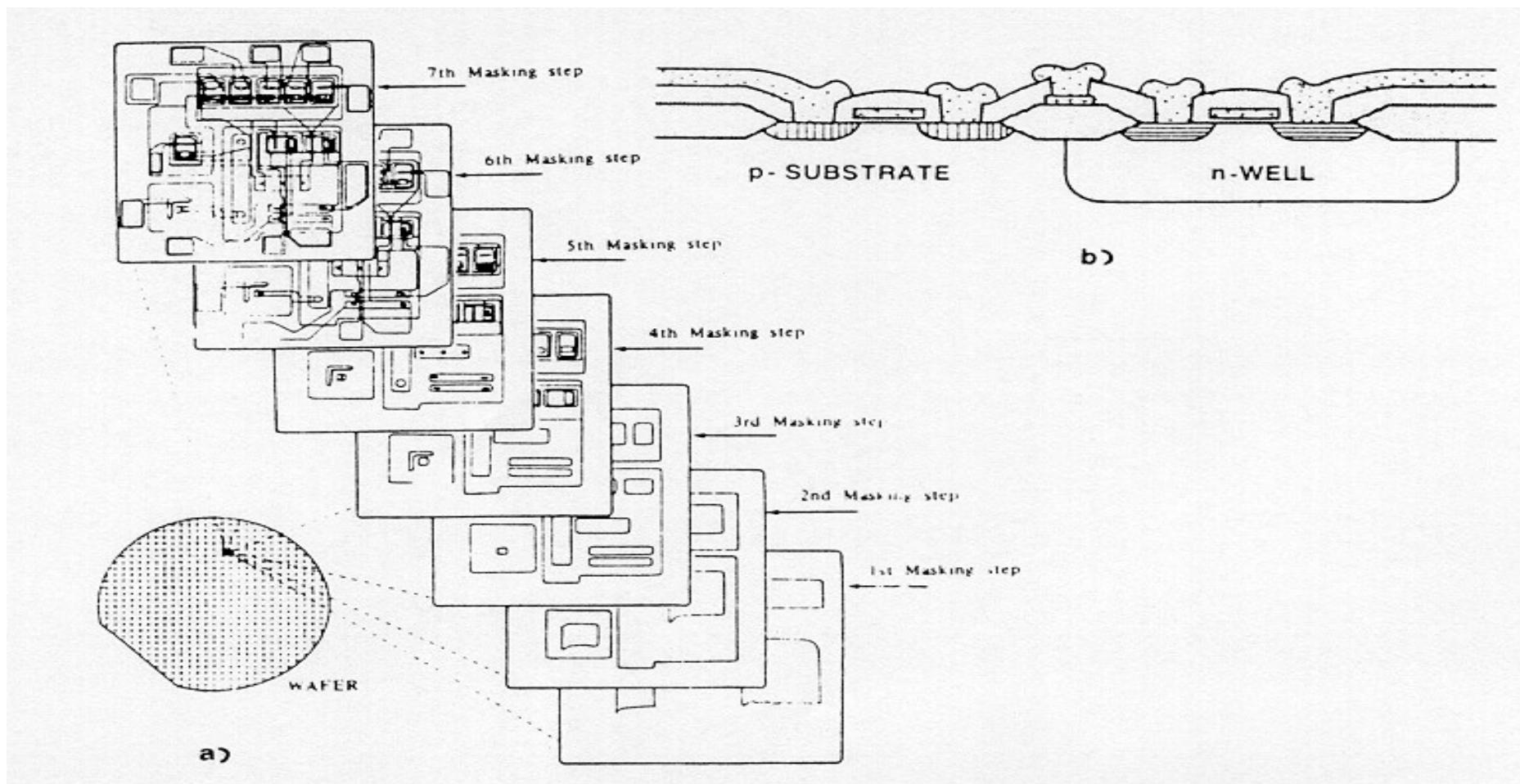


(a) Composite Layout (b) Cross Section (c) Electrical diagram

CMOS n-Well

The patterning process by the use of a succession of masks and process steps

A series of **SEVEN masking steps and 34 process steps** must be sequentially performed for the desired patterns to be created on wafer surface.



p-well	n-well
<ul style="list-style-type: none"> - NMOS device degraded - Device in the well is n-type with electron as carrier (higher mobility) - weakens faster NMOS 	<ul style="list-style-type: none"> - PMOS device degraded - Device in the well is p-type with hole as carrier - Weakens the already weak PMOS - Lower substrate bias effects on transistor threshold voltage and inherently lower parasitic capacitances associated with source and drain