COAA Lab Assignment 1 Report

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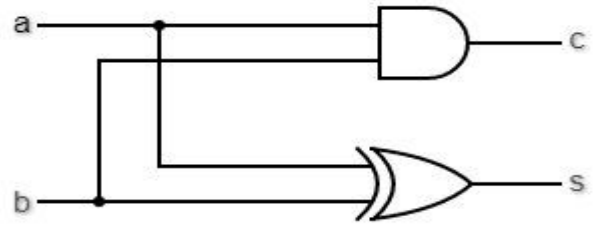
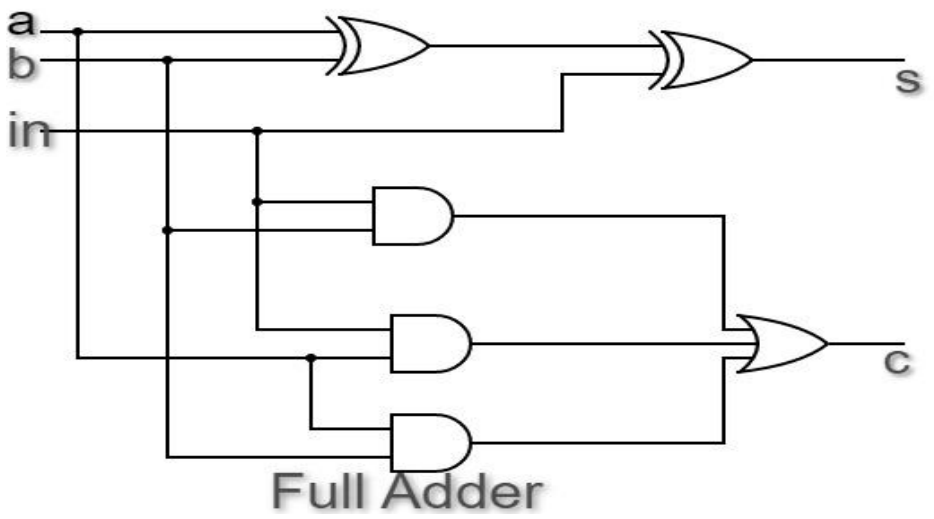
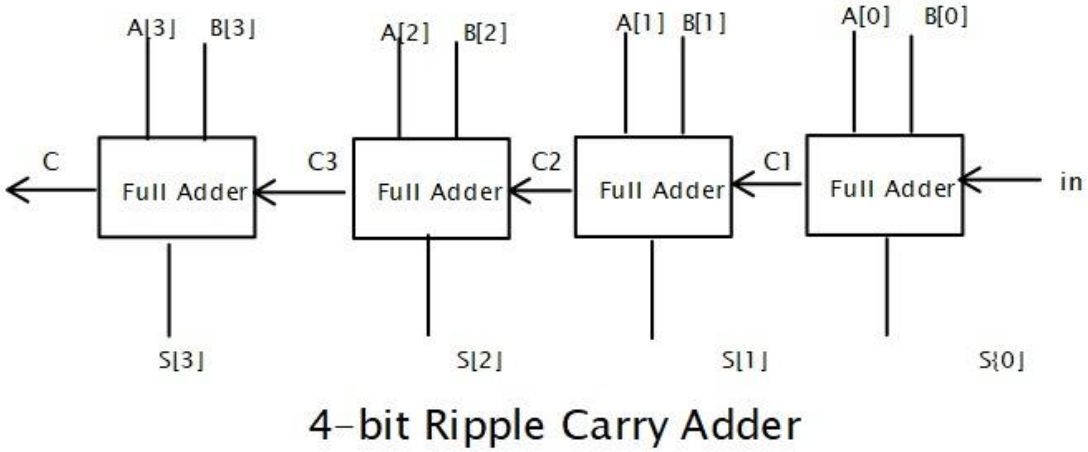
1. Ripple Carry Adder

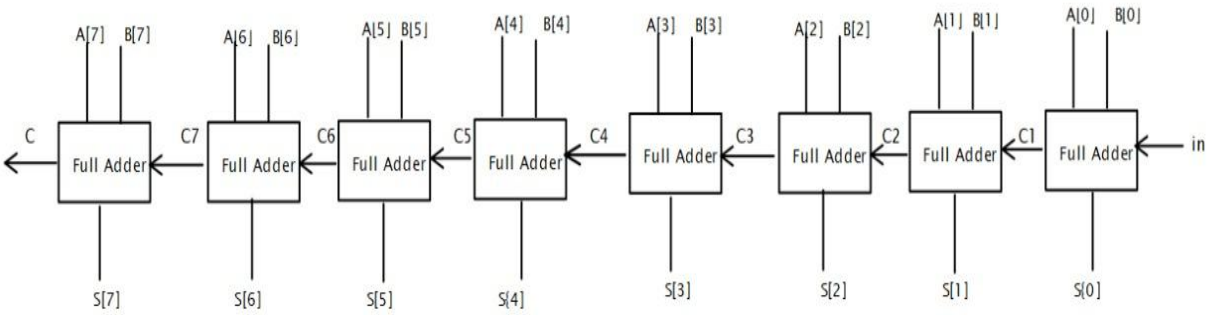
Circuit Diagram:



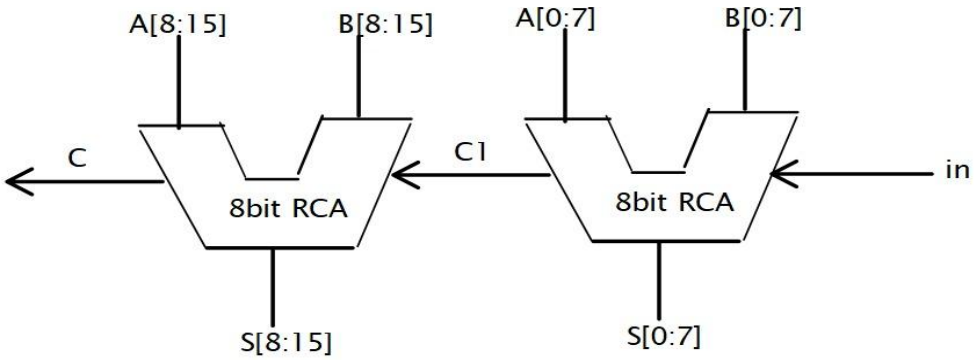
Half adder



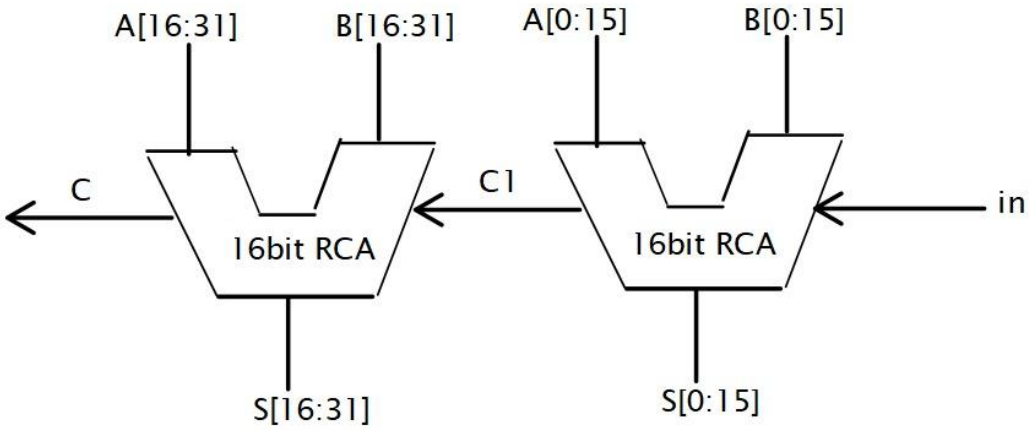




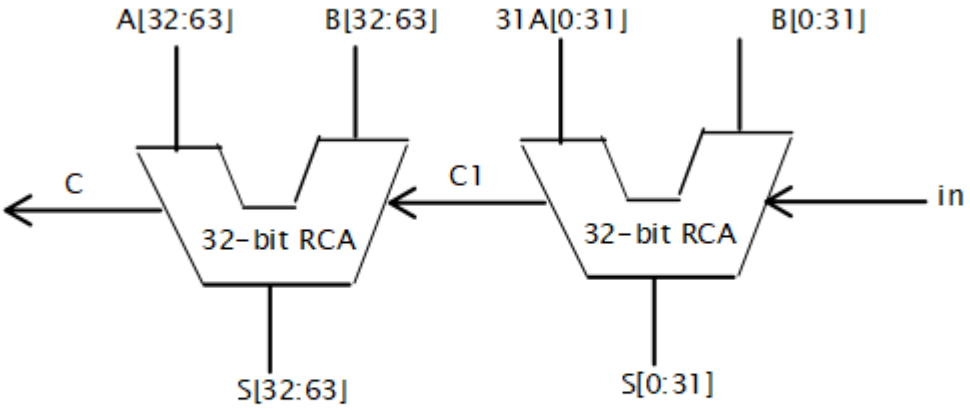
8-bit Ripple Carry Adder



16 bit Ripple Carry Adder(RCA) using two 8-bit RCA



32 bit Ripple Carry Adder(RCA) using two 16-bit RCA



64 bit Ripple Carry Adder(RCA) using two 32-bit RCA

a. Truth Table for half adder:

a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

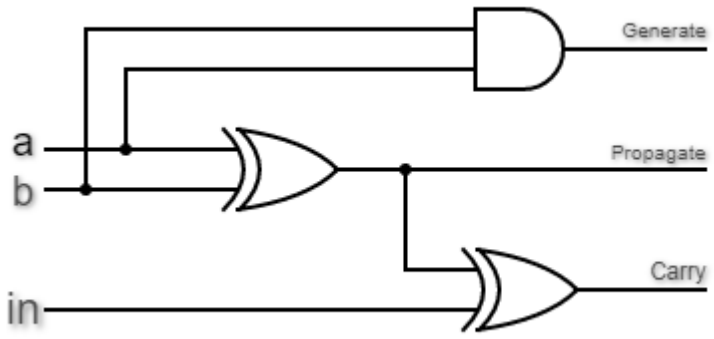
b. Truth Table for full adder

a	b	in	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

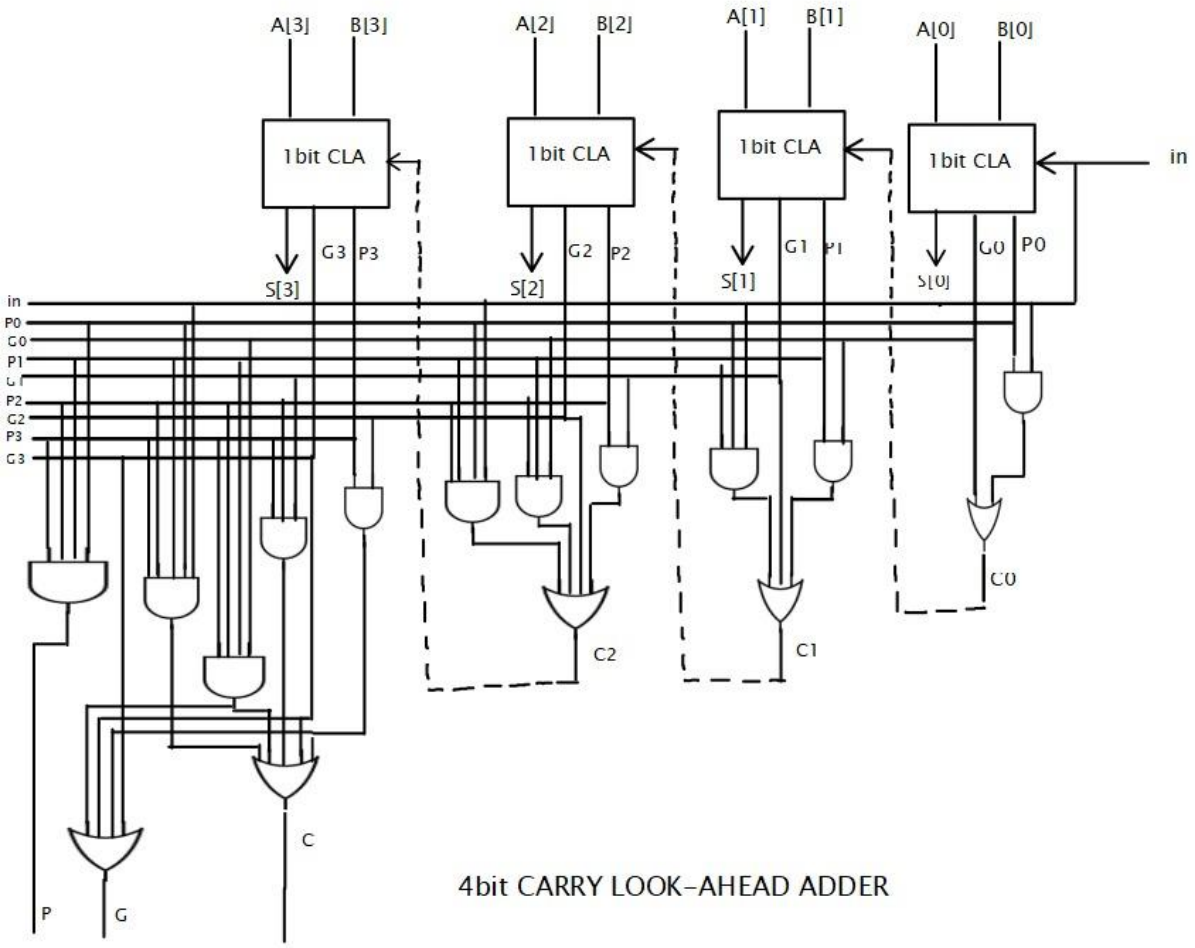
c. **Delays observed after synthesis:**
   4 bit rca : 3.44 ns
   8 bit RCA :5.908 ns
   16 bit RCA :11.236 ns(32 LUTs used)
   32 bit RCA :21.892 ns
   64 bit RCA :43.204 ns

d. **To compute the difference** we will first compute the 2's complement of the number to be subtracted by flipping the bits using NOT gates and then adding 1 to it. Finally the result of 2's complement will be added to the first operand to get the difference of two numbers.This can be efficiently achieved by including an extra XOR gate attached with the each bit of B input(number to be subtracted) and other terminal of XOR connected to a sub input which is 1. If we mean to subtract, the initial Carryin will also be sub to implement addition by 1 after flipping(2's complement).So sub is the boolean input which if 1 it means we are subtracting and if 0 it means normal addition .

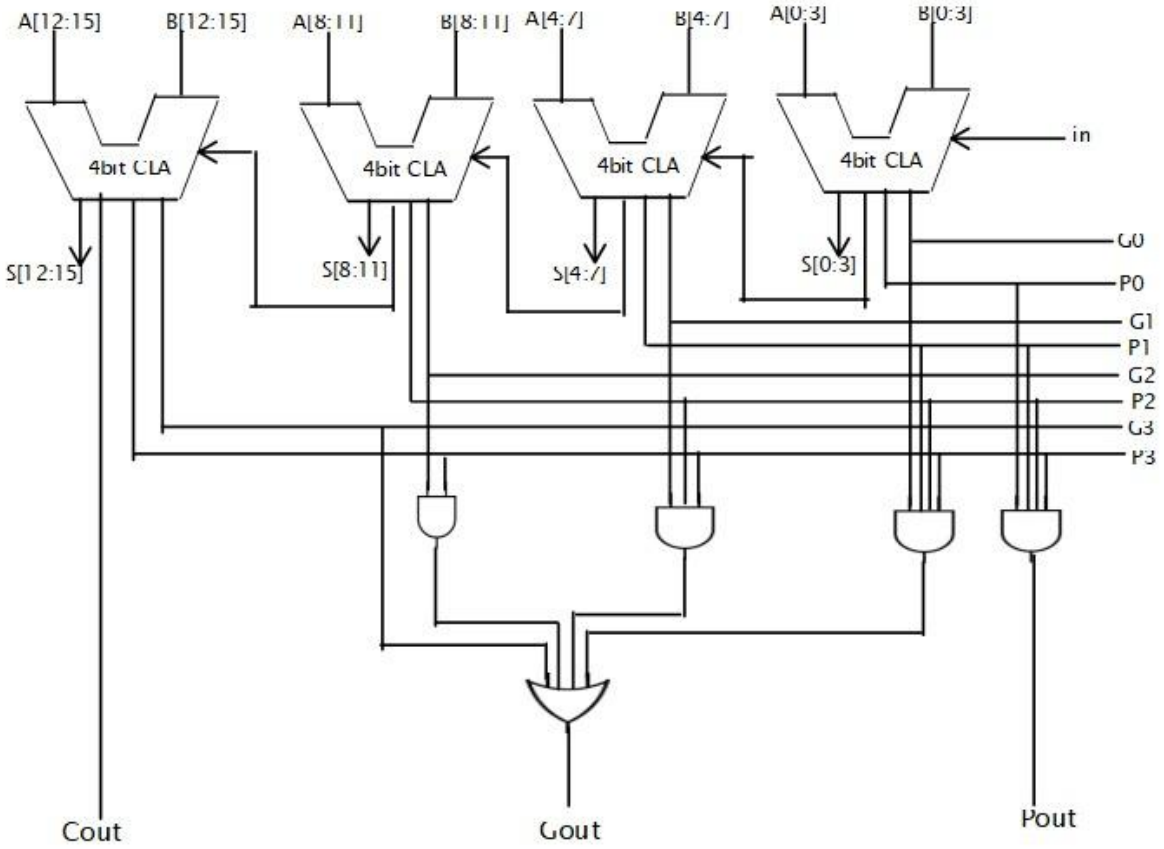
2. Carry Look ahead Adder:



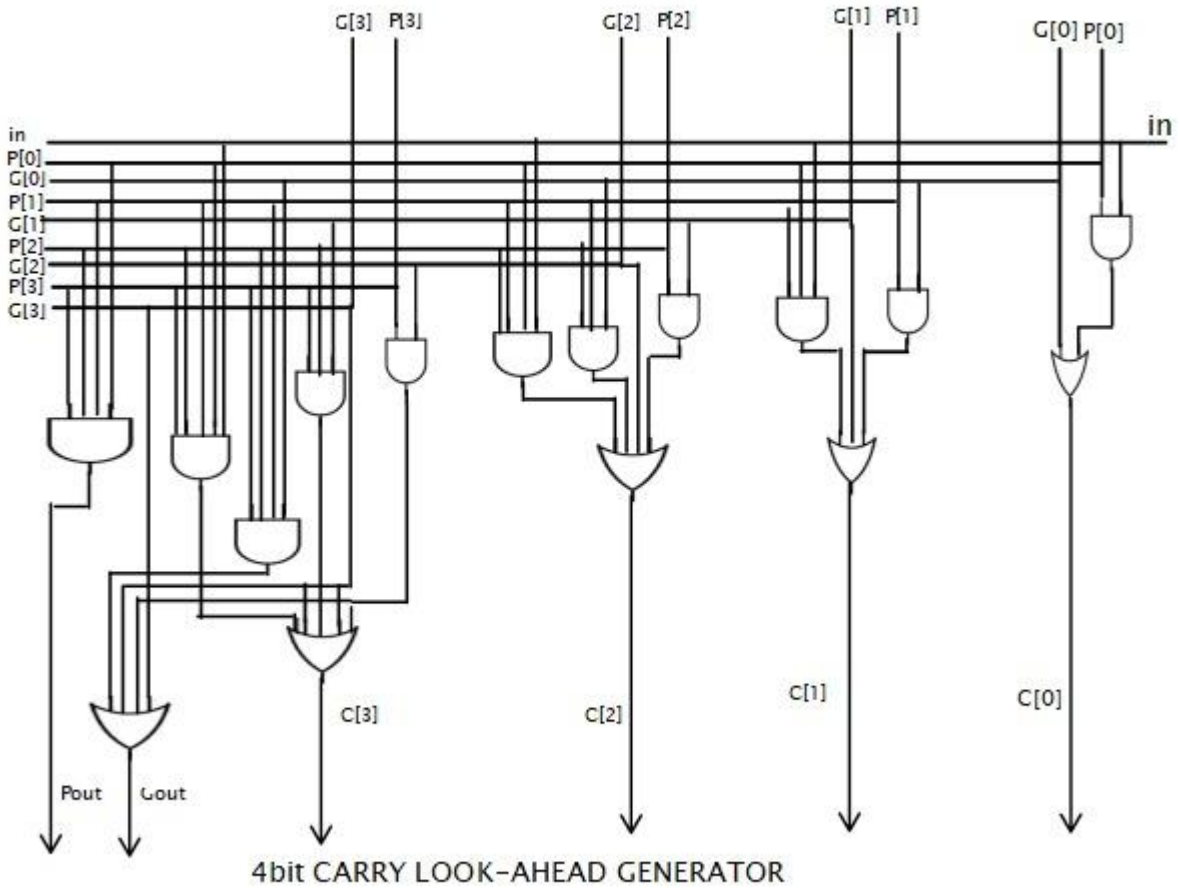
Carry Look-ahead Adder



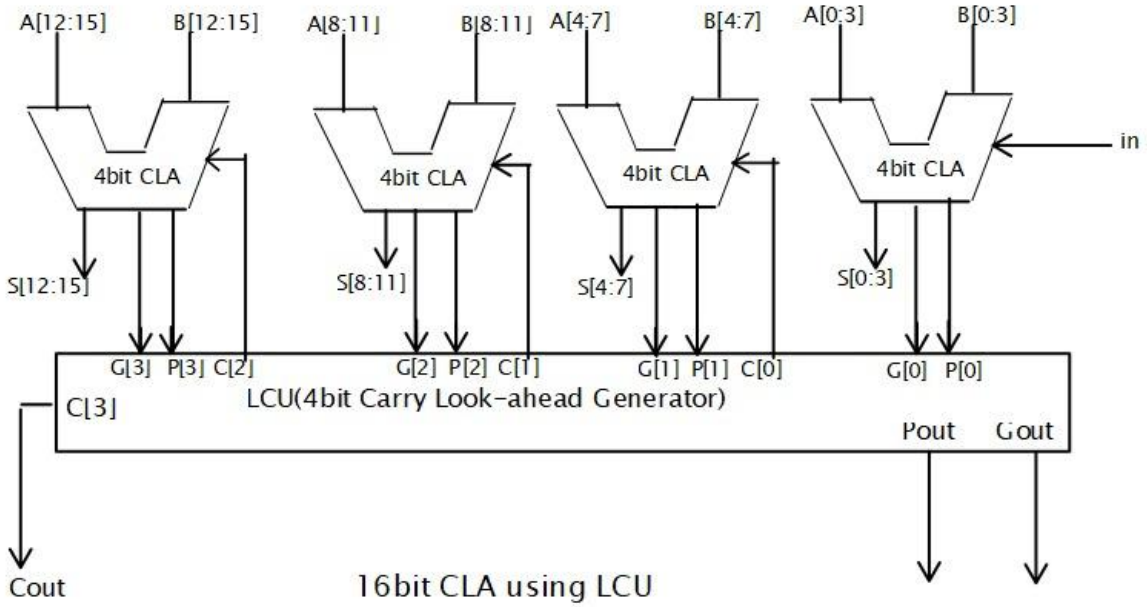
4bit CARRY LOOK-AHEAD ADDER



16 bit Carry Look-Ahead Adder using four 4bit CLA



4bit CARRY LOOK-AHEAD GENERATOR



16bit CLA using LCU

a. Carry bits denoted by C0,C1,C2,C3, and Cin is input carryC0 = G0 + P0.Cin
   C1 = G1+C0P1 = G1 + G0P1 + P1.P0.Cin
   C2 = G2 + G1.P2 + G0.P2.P1 + P2.P1.P0.Cin
   C3 = G3 + G2.P3 + G1.P3.P2 + G0.P3.P2.P1 + P3.P2.P1.P0.Cin
   Equations for generate and propagate:
   For ith Carry Lookahead adder unit
   Pi = Ai xor Bi
   Gi = Ai . Bi , where Ai,Bi denotes ith bits of A and B,
   Block carry propagate P = P3.P2.P1.P0
   Block carry generate G = G3 + G2.P3 + G1.P3.P2+G0.P3.P2.P1
b. Delay of 4 bit CLA : 3.260 ns
   Delay of 4 bit RCA : 3.244 ns
   So the delay values are almost the same .This is because this is for 4 bits only.The efficiency of carry look ahead will be evident when we scale up to higher bits.
c.
   Critical Paths:
   16 bit RCA : Here the critical path should consist of starting from the inputCarry, and going through each of the and and or gates in each full adder, total of 16 full adders ,thus 16*2 = 32 levels for carry.For sum it should be 15*2+3(xor) = 33.
   16 bit CLA with rippling: Here the critical part consists of starting at the least significant input bit(any one of the two), then to the propagate(+3 due to xor) and two logic levels for calculating carry in each of the CLA4 units,passing on to the next unit again 2 levels to get into the next carry,which would be in total 3+2 = 5 for first unit and 2 for rest and in total of 5 + 3*2 = 11 (for carry)due to rippling for the 4 units, and for sum = 5 + 2*2+3(xor to go to sum) = 12.
   16 bit CLA with LCU unit : Here the critical path consists of starting at the least significant input bit,then to propagate(+3 due to xor), and (2(for calculating block generate)+2(LCU unit)) = 4 levels of logic to compute final carry,in total 3+4=7 (for carry),and 3+4+3(xor) = 10 for calculating sum.

   So here we see that CLA complexity depends on number of LCU blocks in the hierarchy which is of the order O(log(n)) for n bits while in case of RCA it is O(n).
d. Delay of 16 bit RCA : 11.236 ns
   Delay of 16 bit Adder with CLA and rippling in second stage : 9.818 ns
   Delay of 16 bit CLA with CLU unit : 6.294 ns

   So it is evident that the carry look ahead unit is more efficient than just rippling the carry.

   LTU cost of 16 bit RCA : 32
   LTU cost of 16 bit Adder with CLA and rippling in second stage : 79
   LTU cost of 16 bit CLA with CLU unit : 79
   So we can see that the CLU adder has higher circuit complexity,compared to RCA,and hence we find a trade off between time efficiency and circuit complexity.