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**Course Name: Digital Circuits Lab**

**Experiment Title: MINI PROJECT**

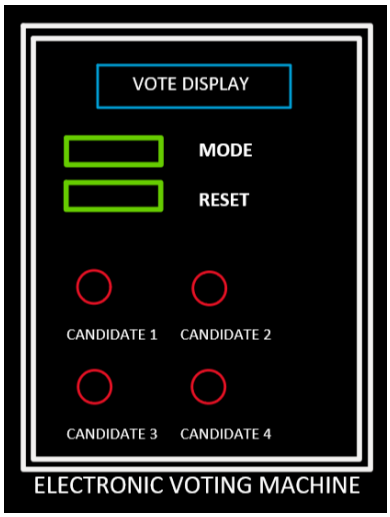
# IMPLEMENTATION OF ELECTRONIC VOTING MACHINE ON ZYBO (USING VERILOG)

**OBJECTIVE:**

The objective this mini project is to implement an electronic voting machine on ZYBO using Verilog code.

**DESCRIPTION:**

Electronic voting machine is a tool used by the Election Committee for the conduction of Voting process. It is used to store the count of votes for each party.




- In our project, we have a **DISPLAY** section, which shows the count of votes for particular candidate.
- We have also a mode button which works accordingly:
  **VOTING MODE** (When voting mode is active, we can vote for a particular candidate and votes are stored.)
  **COUNTING MODE** (When this mode is active, it displays the number of votes casted for a particular candidate in a binary numbered display form)
- We have **4 BUTTONS** on the EVM which refers to 4 candidates and when these buttons are pressed the votes are casted for that particular candidate
- We have **RESET** button which will actually refresh the device vote count, i.e., the all-casted votes so far will be set to 0 when it is activated.

**PROCEDURE:**

1) Here we have implemented 4 modules: button control, mode control, vote logger, voting machine.

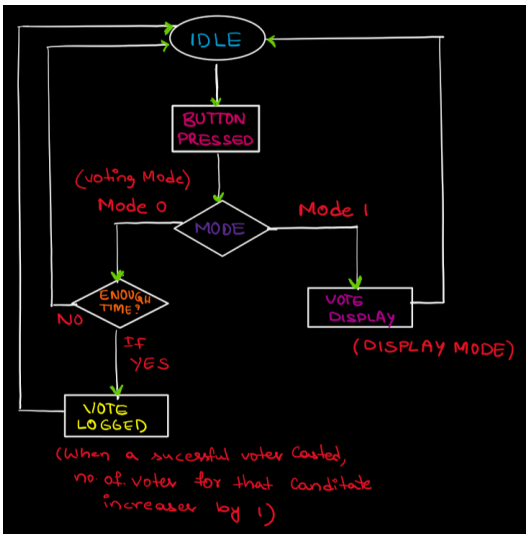
In the button control, the vote will be casted when it is pressed for certain span of time. Even if it is pressed for a large duration, the voted will be casted as a single vote.

In the Vote logger, if the mode is set to 0 (VOTING MODE), then on a single press of candidate button will result in casting a vote to that particular candidate, basically it logs the total number of valid votes for a particular candidate.

In Mode Control, we have a reset button which will refresh the device if it is set to 1 (HIGH) and in the other case it will be count mode. Now, when the mode is 1 (HIGH), on pressing a particular candidate's button we get the count of the votes that were being casted to that particular candidate on ZYBO's LEDs which we have assigned and the display will be in binary form. When the mode is 0, the phase of casting votes is retained and on every successful vote casted, all the LEDs of the ZYBO glows meaning that vote is casted.

In the Voting Machine module, all the above tasks are combinedly performed.

2) The code was implemented by understanding the following Flowchart:



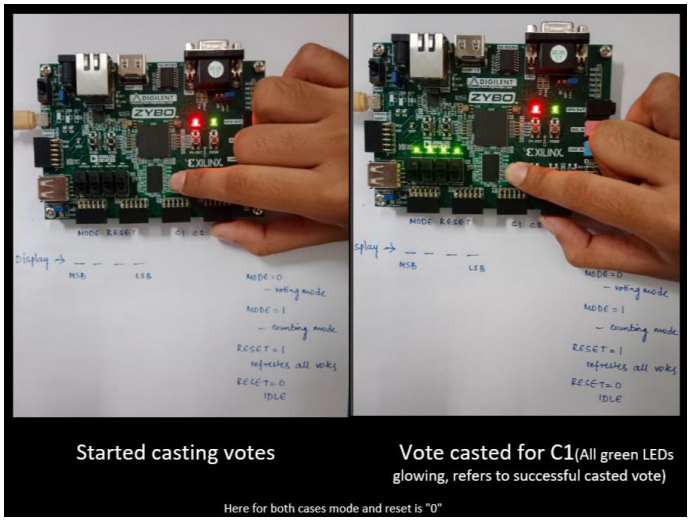

3) The Final Code which we implemented for the mini project is as follows:

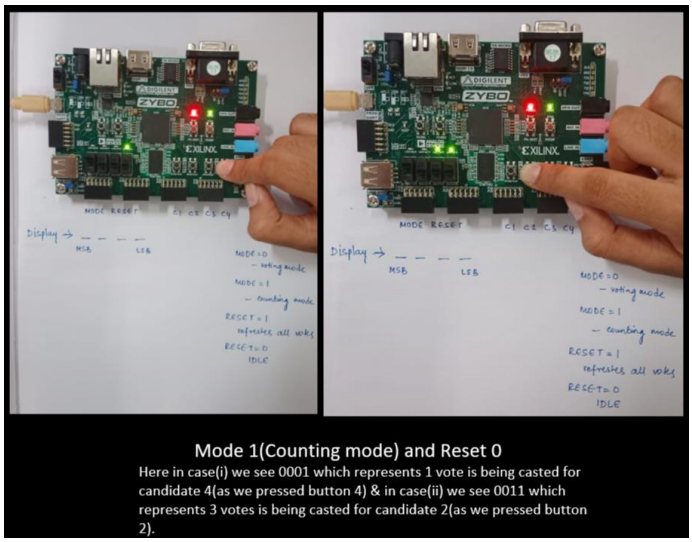
**OBSERVATIONS:**

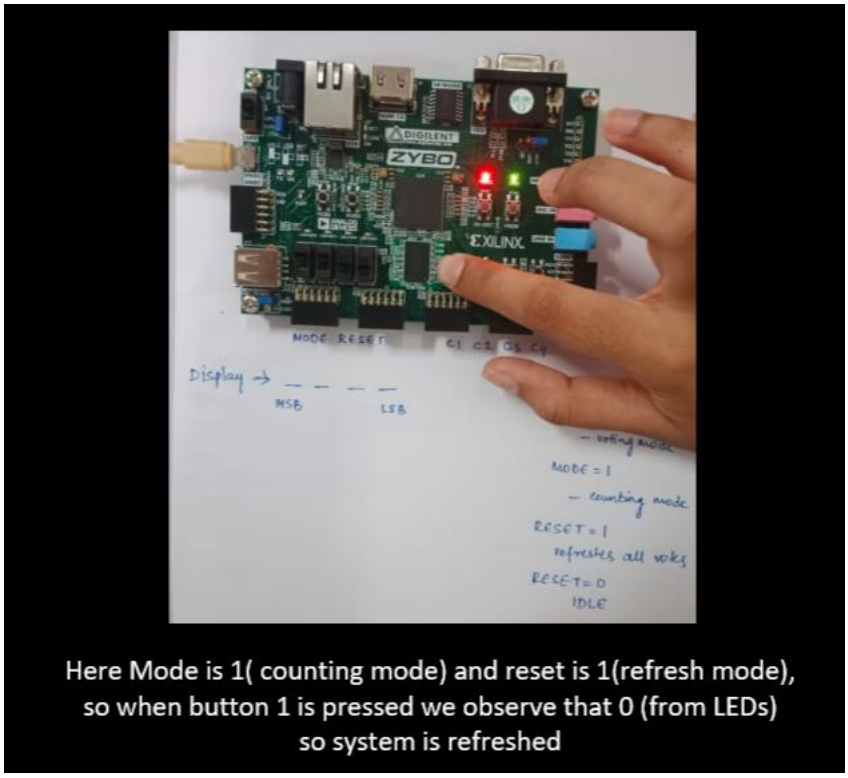
- Here when we have taken mode as “0” and reset as “0”, then we have started casting votes by pressing buttons. When we set the mode as “1” and the reset is “0”, when button 1 is pressed we are able to observe the votes that the candidate 1 has got in binary form on ZYBO(LEDs) with LSB on the rightmost fashion and all others also follows the same fashion i.e., when the respective button is pressed, the respective candidate vote count is displayed.

- Here when we take mode as “1” and reset as “1”, we can observe zero votes are displayed for all the buttons, it means the voting machine’ vote count is refreshed. Again, when the reset is “0” and mode to “0” we can start the re-casting of votes.

- All our observations are observed on ZYBO

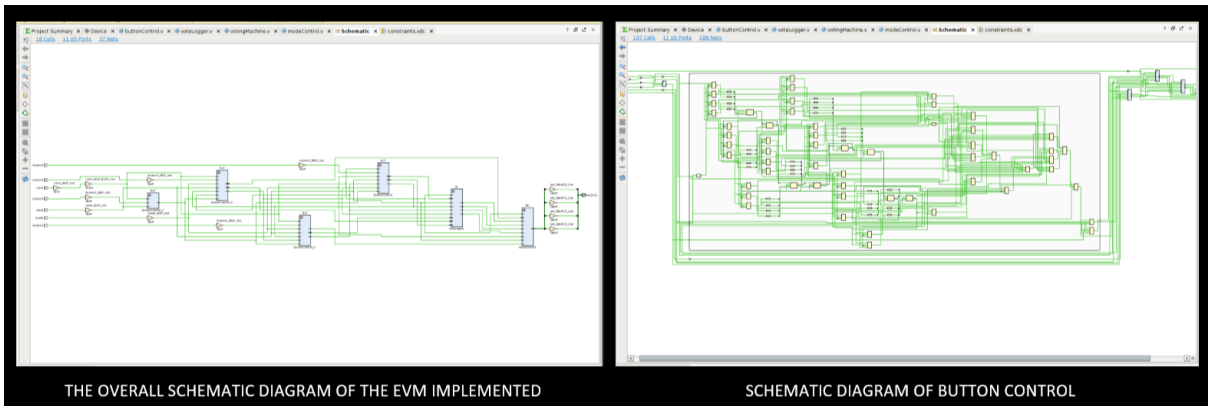




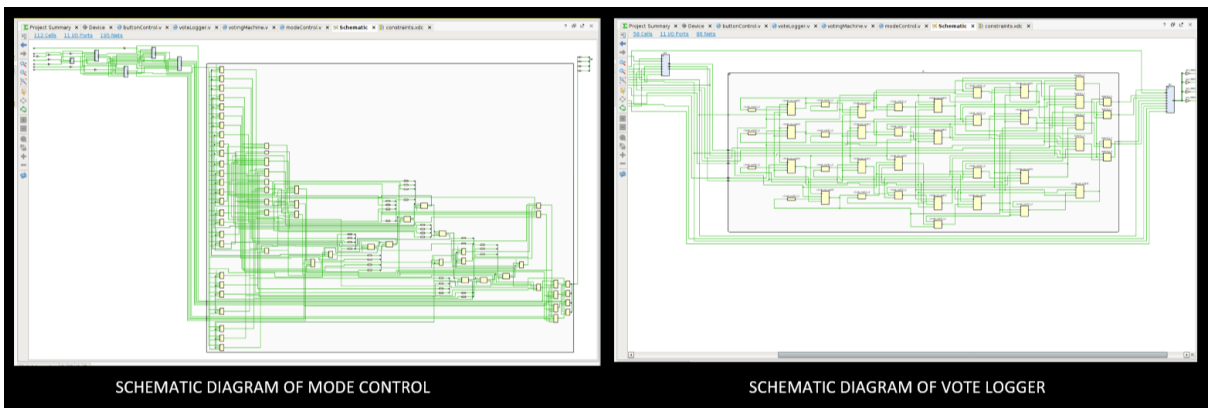

Here Mode is 1( counting mode) and reset is 1(refresh mode), so when button 1 is pressed we observe that 0 (from LEDs) so system is refreshed

**SCHEMATIC DIAGRAMS:**



THE OVERALL SCHEMATIC DIAGRAM OF THE EVM IMPLEMENTED

SCHEMATIC DIAGRAM OF BUTTON CONTROL



SCHEMATIC DIAGRAM OF MODE CONTROL

SCHEMATIC DIAGRAM OF VOTE LOGGER

**RESULTS:**

Here we have successfully created a prototype of electronic voting machine with a casting mode and counting mode and a mode to refresh the device.

We have learnt that L16 pin which is an inbuilt pin of ZYBO can act as a clock with a frequency of 125 MHz

We became much familiar with Verilog coding and ZYBO implementation in a much better way with this project

**CONTRIBUTIONS:**

112101010-CHAPATI ANUSHA: Idea to start, building flow chart for implementing, some part of verilog code.

112101006-BEJJANKI KARTHIKEYA: Gathering information from different sources, rest part of verilog code, implementation on ZYBO.

The both took part together to write the Verilog code, Project Report and both have presented the demonstration of prototype to the faculty.