Comparch Homework 4 Deliverables 1 and 6

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1 Deliverable 1

1.1 Circuit 1

This circuit diagram illustrates the first, more desireable register implementation, which, in behavioral verilog, is

```
module register
(
output reg  q,
input       d,
input       wrenable,
input       clk
);
    always @(posedge clk) begin
        if(wrenable) begin
            q <= d;
        end
    end
endmodule
```

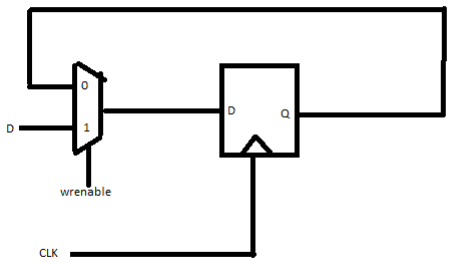

Figure 1: D Flip Flop with enable

1.2 Circuit 2

This circuit illustrates the second, less desirable register implementation, which, in behavioral verilog, is

```
// Gated clock - avoid this style
always @(posedge (clk & wrenable)) begin
        q <= d;
end
```

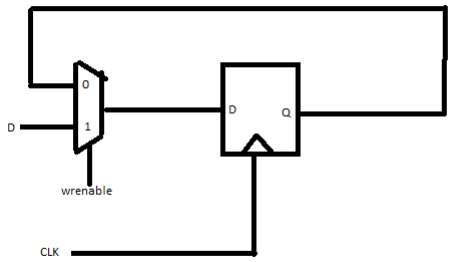

Figure 2: D Flip Flop with enable

2 Deliverable 6

The following behavioral Verilog results in a decoder:

```
module decoder1to32
(
output[31:0]  out,
input         enable,
input[4:0]    address
);
    assign out = enable<<address;
endmodule
```

The way that this module works is by leveraging the addressing associated with the $<<$ (bit shift) operator. Therefore, when the enable pin is set to one, the module will shift the enable bit to the left until it has been stored at the address index in the output bus and set every other value to zero. If the enable pin is set to zero, it should not write directly to the output bus.

This functionality reflects the behavior of a decoder because it sets a single bit on a large output data line based on a specified address value.