ENGR2420 Lab 7 : The MOS Differential Pair

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1 Experiment One : Differential Pair Current–Voltage Characteristics

In this experiment, we measured the current-voltage characteristics of an nMOS differential pair at varying values of the common-mode input voltage and as a function of bias current levels while varying gate voltages for one of the transistors in the pair. We constructed our differential pair out of transistors on the ALD1106 nMOS array.

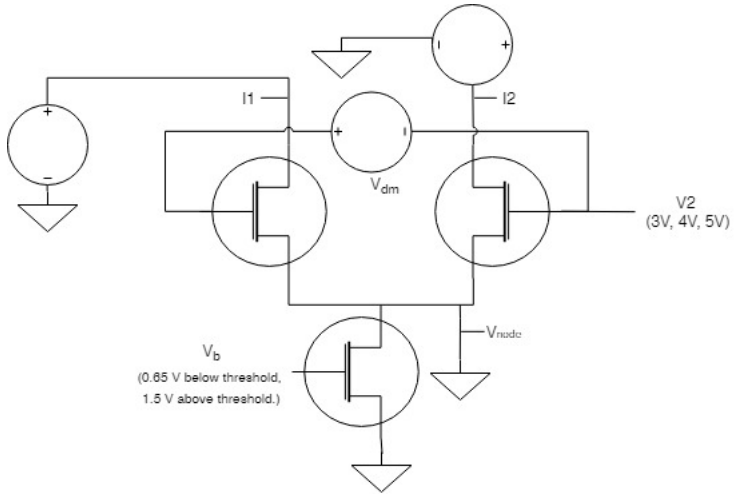

Figure 1: Schematic for the circuit used to characterize the nMOS differential pair.

1.1 Results

We first plotted the values I_1, I_2, I_1+I_2, and I_1-I_2 as a function of V_1-V_2, or V_{dm}, for each value of V_2 when V_b was at the threshold voltage, 0.65 V.

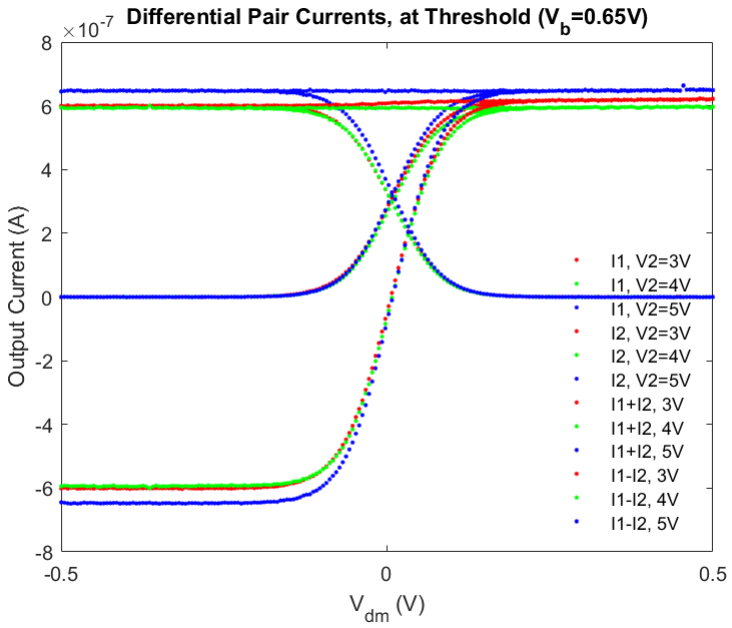

Figure 2: Output current as a function of V_{dm} for nMOS differential pair.

Then, we plotted the voltage at the common source node for each value of V_2.

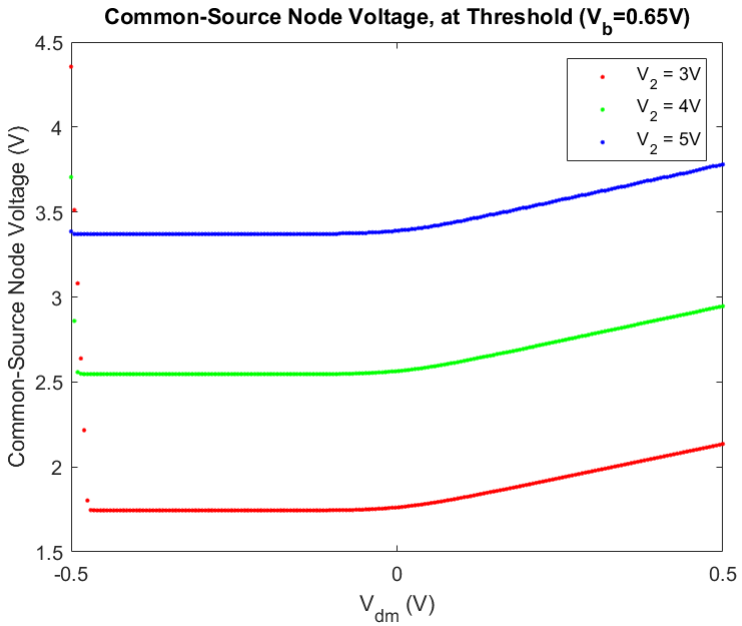

Figure 3: Common-source node voltage as a function of V_{dm} for nMOS differential pair.

We also plotted the incremental differential mode transconductance gain of the differential pair at threshold, as shown in Figure 4.

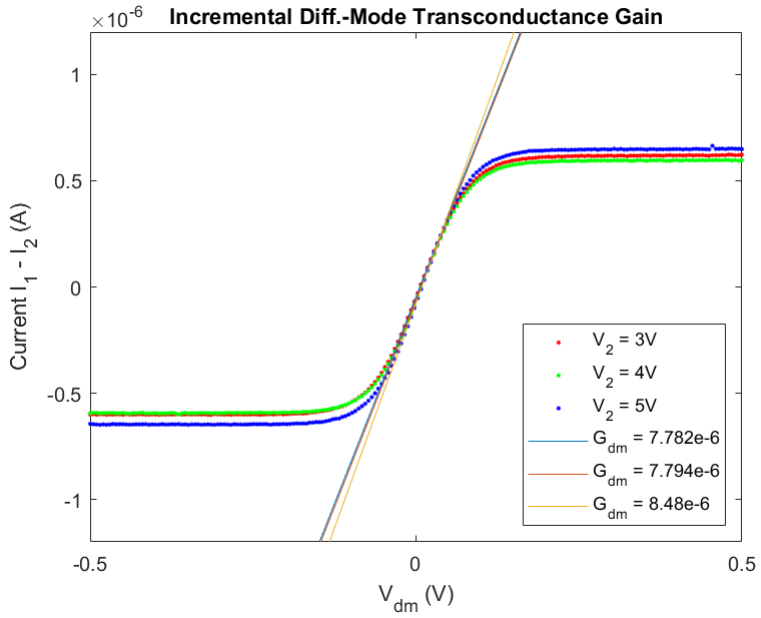

Figure 4: G_{dm} extracted from current-voltage characteristics of nMOS differential pair at threshold.

Next, we set the bias voltage to 1.5 Volts so that the bias current was above the threshold. Then, we set the value of V_2 to 5V. We measured the currents and the common source node voltages for the differential pair. To see the full range of behavior, we swept a range from -1 V to 1 V for voltage at V_{dm}. We plotted output current as a function of V_{dm} for the differential pair above threshold, as seen in Figure 5.

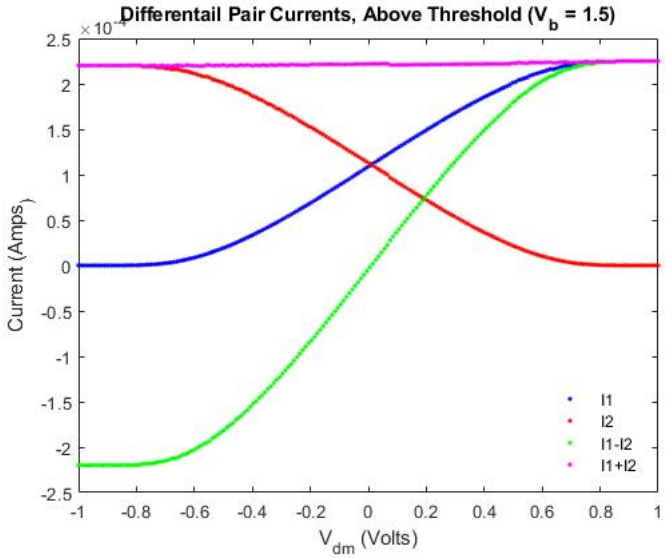

Figure 5: Currents as a function of V_{dm} when bias current is above threshold

We plotted common-source node voltage as a function of V_{dm} on linear axes as seen in Figure 6.

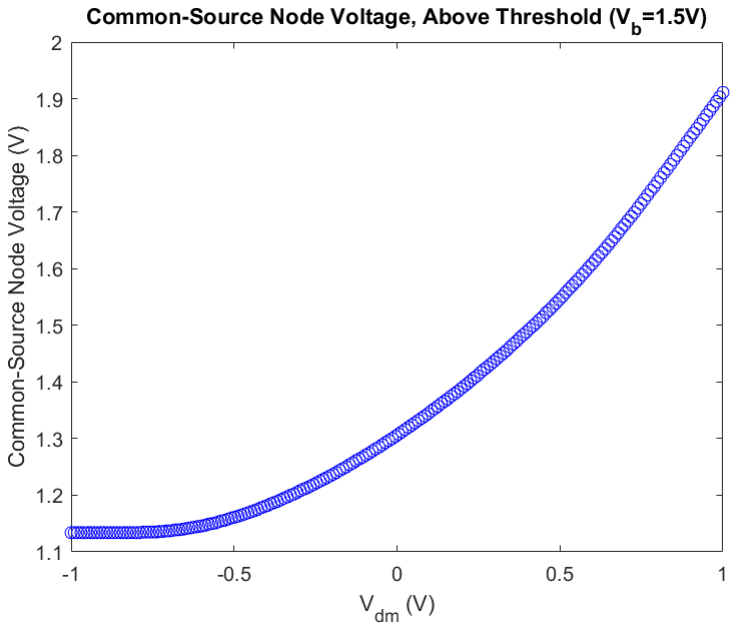

Figure 6: Common-source node voltage as a function V_{dm} when bias current is above threshold.

1.2 Analysis

To start, we studied the differential pair with $V_b = 0.65V$, or at the threshold voltage. Theoretically, a lower V_2 should lead to slightly lower current values for both I_1 and I_2, but the behavior should remain consistent regardless of the value of V_2 - the current should quickly increase from negative to positive around $V_{dm} = 0$ V. Meanwhile, the value of the common source node voltage should increase proportionally as V_2 increases but the behavior should be consistent, with constant voltage when $V_2 < V_1$ and a linear relationship when $V_2 > V_1$. Our experimental results qualitatively reflect this behavior.
The definition of incremental differential-mode transconductance gain is formally given as follows:

$$G_{dm} = \frac{\delta I_{dm}}{\delta V_{dm}}\Big|_{V_{dm}=0} = \frac{\delta(I_1 - I_2)}{\delta(V_1 - V_2)}\Big|_{V_{dm}=0}$$

We fit a line to the linear region of the $I_1 - I_2$ plot, which is the section of the data near the point where $V_1 - V_2 = 0$. By taking the slope of this line, we extracted the incremental differential-mode transconductance gain at each value of V_2, as shown in Figure 4.
Theoretically, in the current-voltage characteristic plot for above threshold, I_1 and I_2 should be mirrors of one another and intersect at 0 V. We expected that the I_1 - I_2 would pass through the point (0,0) on the plot. For the voltage plots, the threshold plot would not follow the soft max function and instead follow an exponential trend.

1.3 Discussion

The current-voltage characteristics change somewhat as V_2 changes, and the most noticeable difference is that when $V_2 = 5V$ the current diverges slightly more, but is still very close in value. Overall, the starting values and slopes are very similar. The current for I_1 and I_2 also rail high to about $6e-7$ amps and rail low to 0 amps. In the case of the common source node voltage, when V_1 goes from below V_2 to above it, the value of V_{dm} as a function of common source node voltage goes from flat lining to having a slope of 0.78, 0.79, and 0.81 for each value of V_2, respectively. Note that these slope values are dimensionless because these are ratios of *volts* over *volts*. In other words, V_{dm} does not change when V_1 is less than V_2, but V_{dm} as a function of common source node voltage has a positive slope when V_1 exceeds V_2.

The value of the differential-mode transconductance gain changes from 7.82e-6 for $V_2 = 3V$ to 7.94e-6 for $V_2 = 4V$ to 8.48e-6 for $V_2 = 5V$. Again, the differential-mode transconductance gain when V_2 is $3V$ and 4V is close together, and when V_2 is $5V$ the value is noticeably larger.

The current-voltage characteristic plot of the circuit below threshold, Figure 2, and the plot above threshold, Figure 6, are similar in many ways. I_1 and I_2 are mirror images of one another and intersect at 0 volts. To be able to see the full current behavior at above threshold, we did have to sweep a wider range for V_{dm} than when the circuit was below threshold. Without the larger range, some of the current behavior would have been cut off. For the below threshold plots, the currents of I_1 and I_2 rail for a longer range of voltages. At above threshold, the transition region is longer because the bias current is higher at strong inversion and it takes longer to saturate.

The distinction between each of the common-source node voltages as a function of V_{dm} for each value of V_b is that the below threshold current plot follows the soft max function and the above threshold plot follows more of an exponential function.