ECE 464 / ECE 520
Homework 5

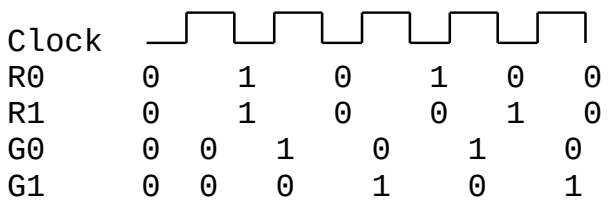
On-line turn-in. Turn in a brief report AND the Verilog file for your design (not your test fixture or synopsys files) using wolfware. These will be checked using Code Comparison tools. If your code is substantially similar to someone else's you will both receive an academic violation for cheating.

Question 1

Please design, code, verify and synthesize the following design:

Simple arbiter.
There are two requesters, that can issue requests to the arbiter on lines R0 and R1. You can grant these requests via the grant lines G0 and G1 on the next clock cycle after the request arrives. If both units make a request on the same cycle then, unit 0 is granted first and then unit 1 on the next cycle. Any unit won't make a new request until after all units have been serviced. Thus you do not have to worry about queuing the requests somehow.

Example of a timing diagram:



The module will have the following IO:

```
input reset, clock;
input R0, R1;  // request lines
output G0, G1; // grant lines
```

Design, verify, synthesize a module that meets these specifications. Use an FSM in your design. You do NOT have to run the post-synthesis flow from the last homework NOR optimize the clock period.

Please turn in the following:

- A drawing of your design (the FSD).
- A fully commented Verilog listing of your design and test fixture.
- Simulation results showing working design
- Final report_timing summary (from Synopsys).
- Final area (from Synopsys) - use report_area

[50 points]

Grading Rubric

Element	**Standard**	**Grade**
Drawing which might just be an FSD	Intelligible, matches code, looks like it would work	**10/10**
	Missing one of the elements above	**5/10**
	Deficient in all elements above	**0/10**
Code	Looks correct in grammer; Looks synthesizable; Matches drawing	**20/20**
	Missing one of the elements above	**10/20**
	Deficient in all elements above	**0/20**
Simulation	Looks correct	**10/10**
	Shows incorrect behavior	**0/10**
Timing	Meets setup and hold	**5/5**
	Meets only one	**3/5**
	Does not meet either setup or hold	**0/5**
Area	Reported	**5/5**
	Not reported	**0/5**
Total		**Out of 50**