ECE 720 – ESL & Physical Design

Lecture 11: Rent's Rule and Donath's Method

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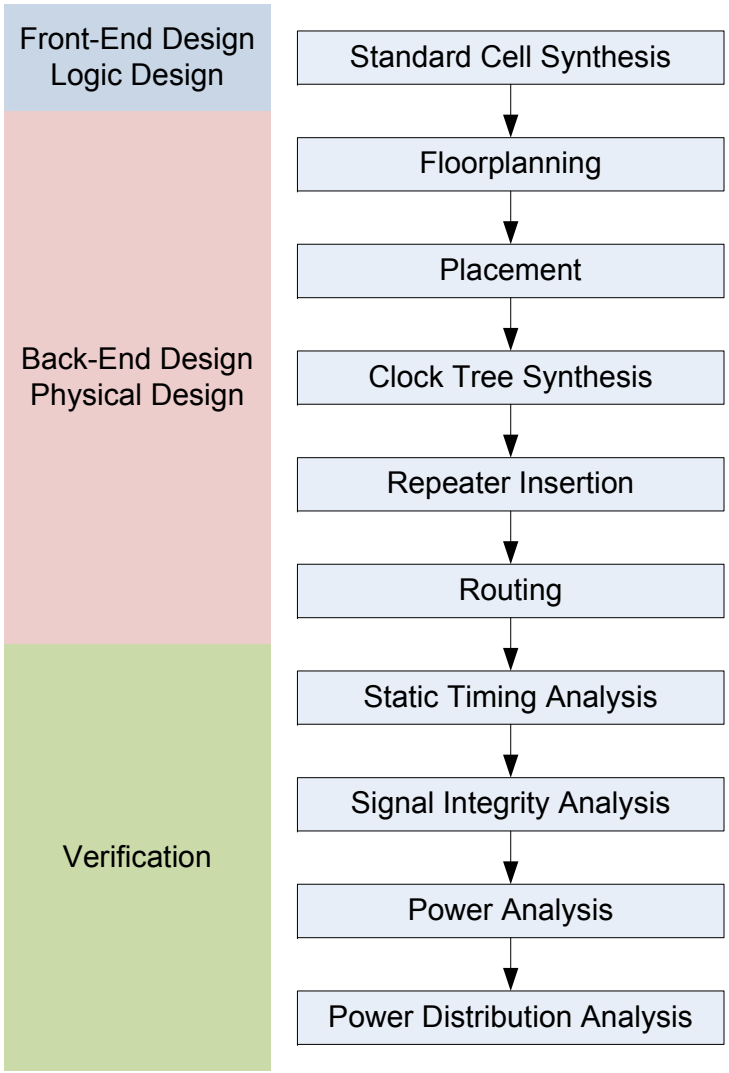
Announcements

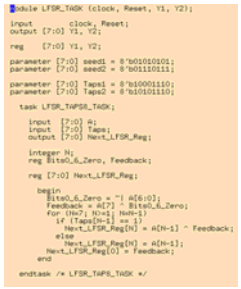
- Homework 5 Due Thursday
  - See updated sc/sgc/setup scripts in cortexm0ds.tar.gz
- Project 2 Due in 2 weeks
- Homework 6 Due in 3 weeks

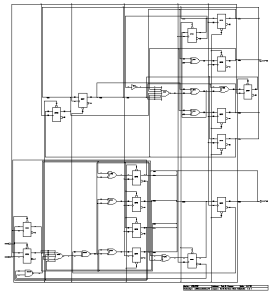
Today's Lecture

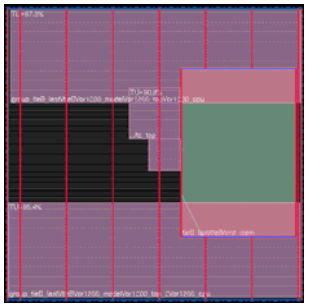
- Wires in Integrated Circuits
- Wire-Length Estimation

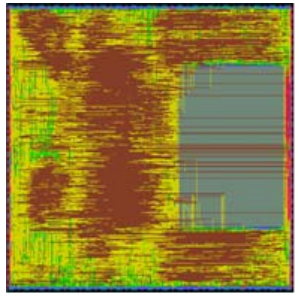
Design Flow





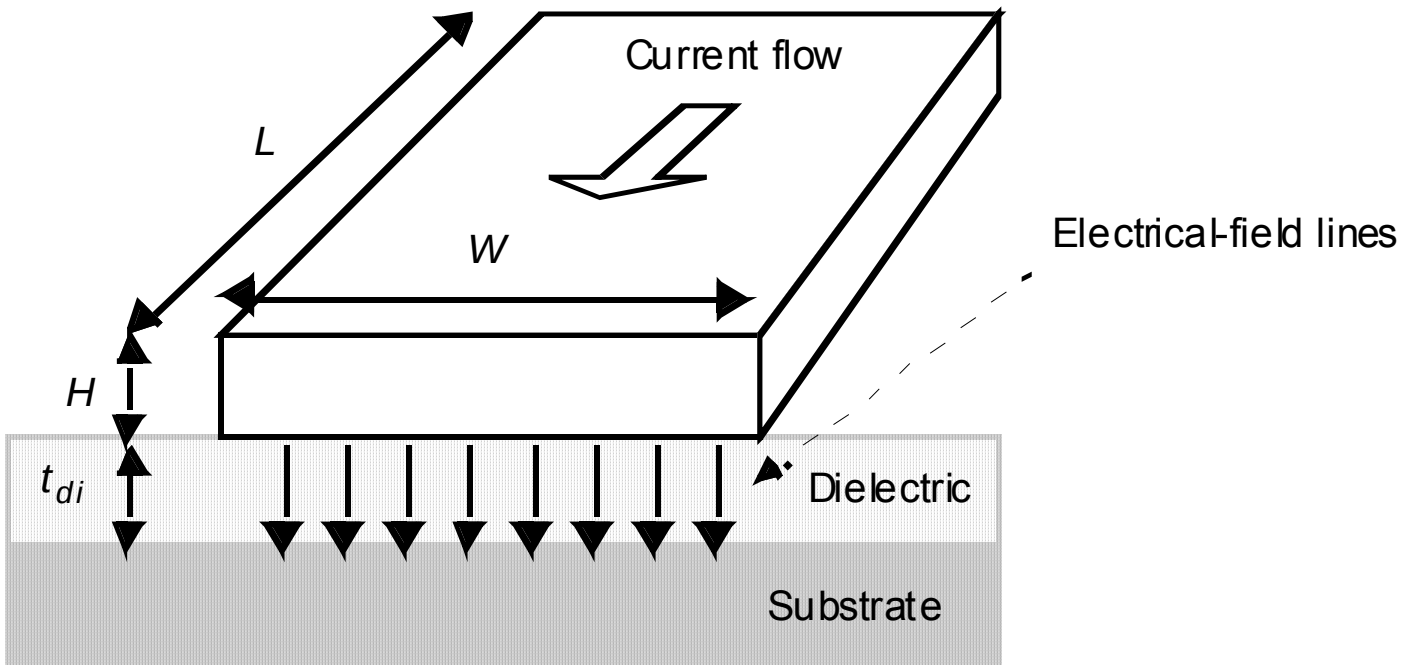






- We will touch all of these, in time
- Today, we begin with the hand-off from front-end to back-end

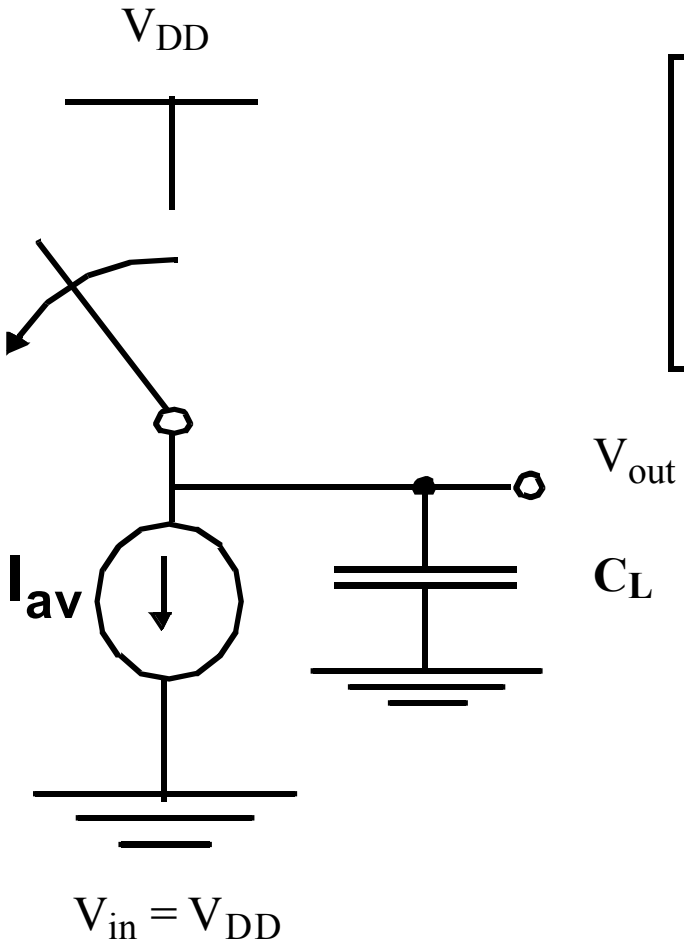
Capacitance: The Parallel Plate Model



$$C_{area} = \frac{\varepsilon_{di}}{t_{di}} WL = c_a WL$$

CMOS Inverter Propagation Delay

Approach 1

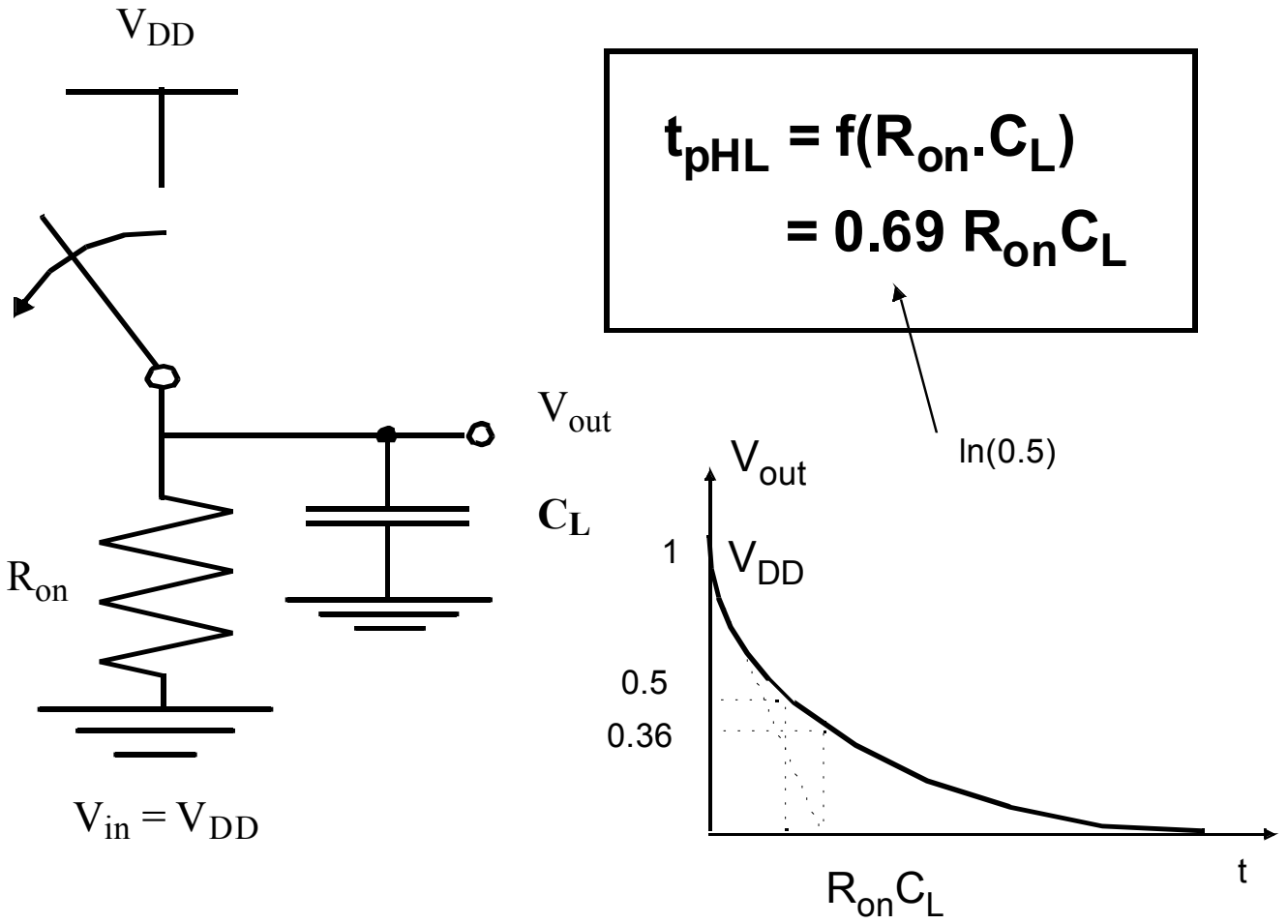


$$t_{pHL} = \frac{C_L \, V_{swing}/2}{I_{av}}$$

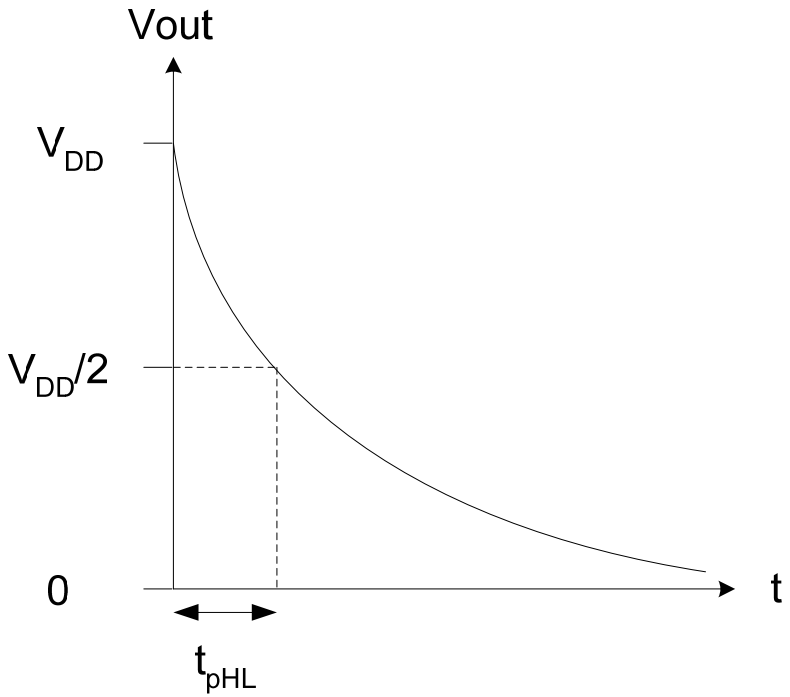
$$\sim \frac{C_L}{k_n \, V_{DD}}$$

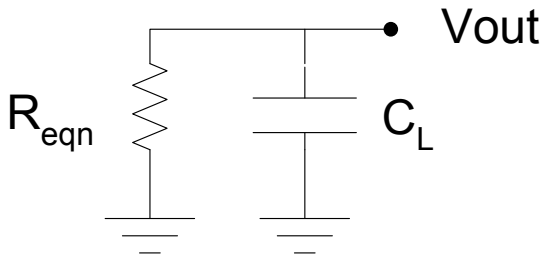
CMOS Inverter Propagation Delay

Approach 2



Propagation Delay





$$V_{out}(t) = V_{DD} e^{-t/R_{eqn}C_L} = V_{DD}/2$$

$$e^{-t/R_{eqn}C_L} = \frac{1}{2}$$

$$t_{p_{HL}} = \ln(2) R_{eq_n} C_L = 0.69 R_{eq_n} C_L$$

$$t_{p_{LH}} = \ln(2) R_{eq_p} C_L$$

$$t_p = \frac{1}{2}\left(t_{p_{HL}} + t_{p_{LH}}\right)$$

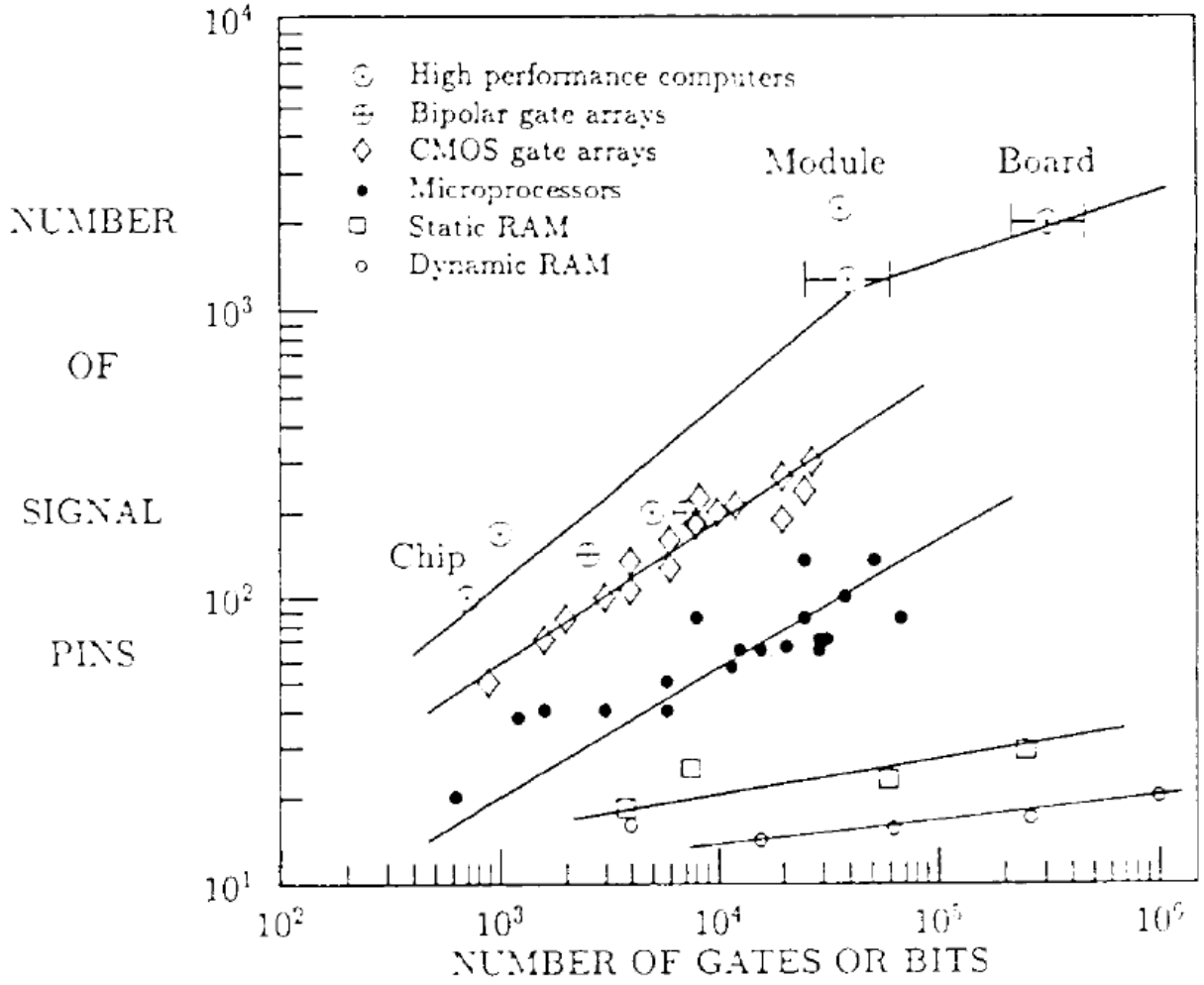
Today's Lecture

- Wires in Integrated Circuits
- Wire-Length Estimation

Rent's Rule

- E. F. Rent 1960 (internal IBM memoranda)
- Relationship between no. of terminals and no. of cell in an IC
- $T=AC^p$
  - T – no. of terminals or pins
  - C – no. of cells or logic gates
  - A – avg. no. of terminals per cell
  - p – Rent's constant
- See document on Rent's Rule posted on web-page

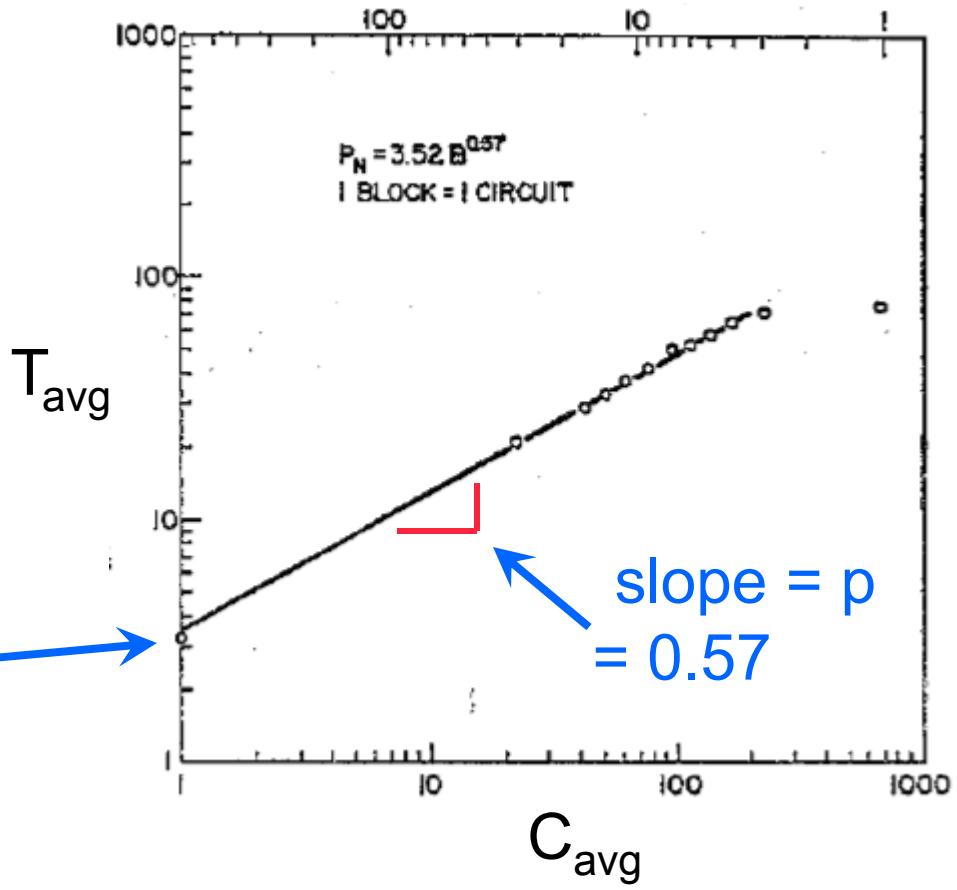
Rent's Curves



Landman and Russo 1971

- Showed that p remains constant throughout hierarchy
  - » Performed a partition throughout all levels of hierarchy
  - » Assumed each partition was a new "block" with a new value of T and C
  - » Found average values of T and C (T_{avg} and C_{avg}) over the blocks in the same level of hierarchy
  - » Plotted the results to find p

Landman & Russo's Results



A = 3.53 pins/cell
NOTE: $T_{avg} = A$ when $C_{avg}=1$

slope = p = 0.57

Donath's Method

$T=AC^p$

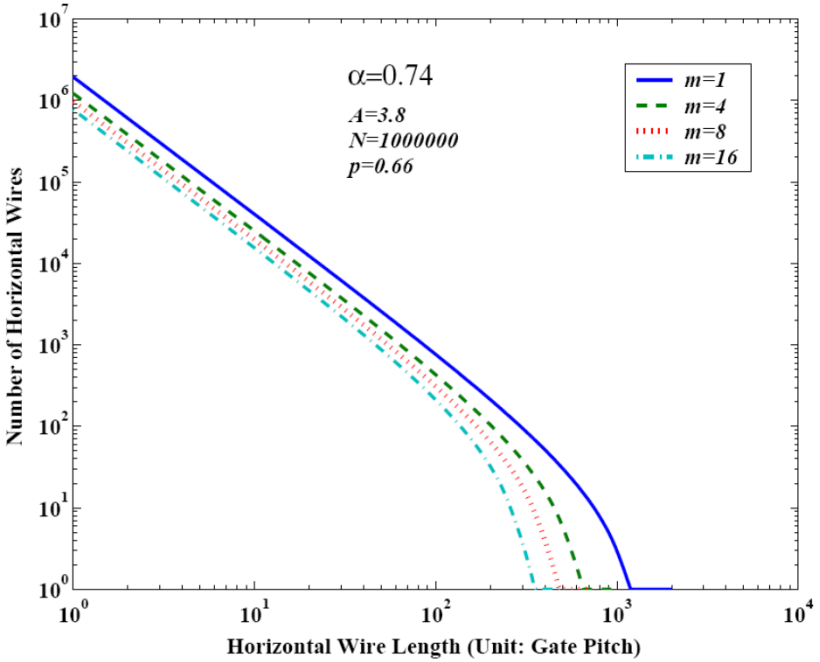
- W. E. Donath, TCAS 1979
- Donath assumes that Landman and Russo's (1971) result holds
  - i.e. that Rent's Rule holds for each level of hierarchy with the same values of A,p
- Assumes that a hierarchy is imposed on the design such that each level contains 4 instances
- Assumes that cells are square and are placed in a larger square such that instances in the same level of hierarchy are placed close to each other
- Allows for estimation of wire length

Average Wire Length

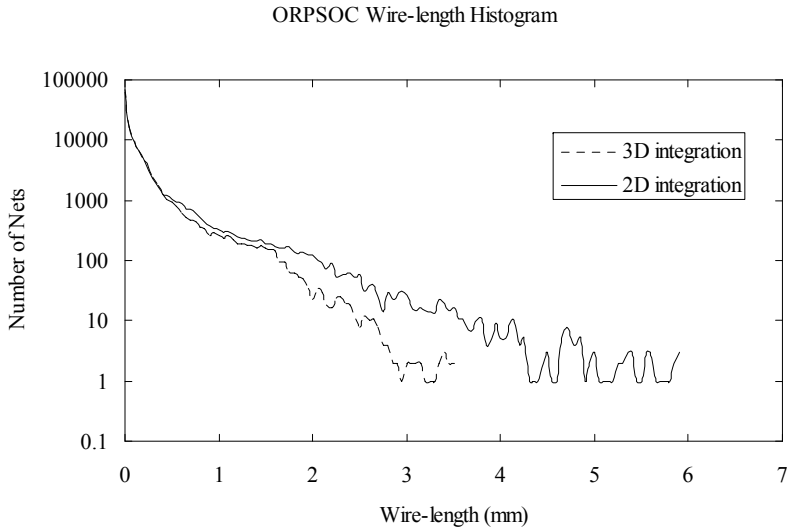
$$L_{avg} = \begin{cases} d_{avg} \cdot \frac{2}{9}\left(7\frac{C^{p-(1/2)}-1}{4^{p-(1/2)}-1} - \frac{1-C^{p-(3/2)}}{1-4^{p-(3/2)}}\right)\cdot\frac{1-4^{p-1}}{1-C^{p-1}} & for\ p \neq \frac{1}{2} \\ d_{avg} \cdot \frac{2}{9}\left(7log_4 C - \frac{1-C^{p-(3/2)}}{1-4^{p-(3/2)}}\right)\cdot\frac{1-4^{p-1}}{1-C^{p-1}} & for\ p = \frac{1}{2} \end{cases}$$

- One of Donath's results was an expression for average wire-length
- Notes
  - d_{avg} = avg. cell dimension
  - independent of A
  - for p>1/2, $\lim_{C\to\infty} L_{avg} = d_{avg} \cdot C^{p-(1/2)}$
  - for most designs, 0.5 < p < 0.75

Wire Length Histograms



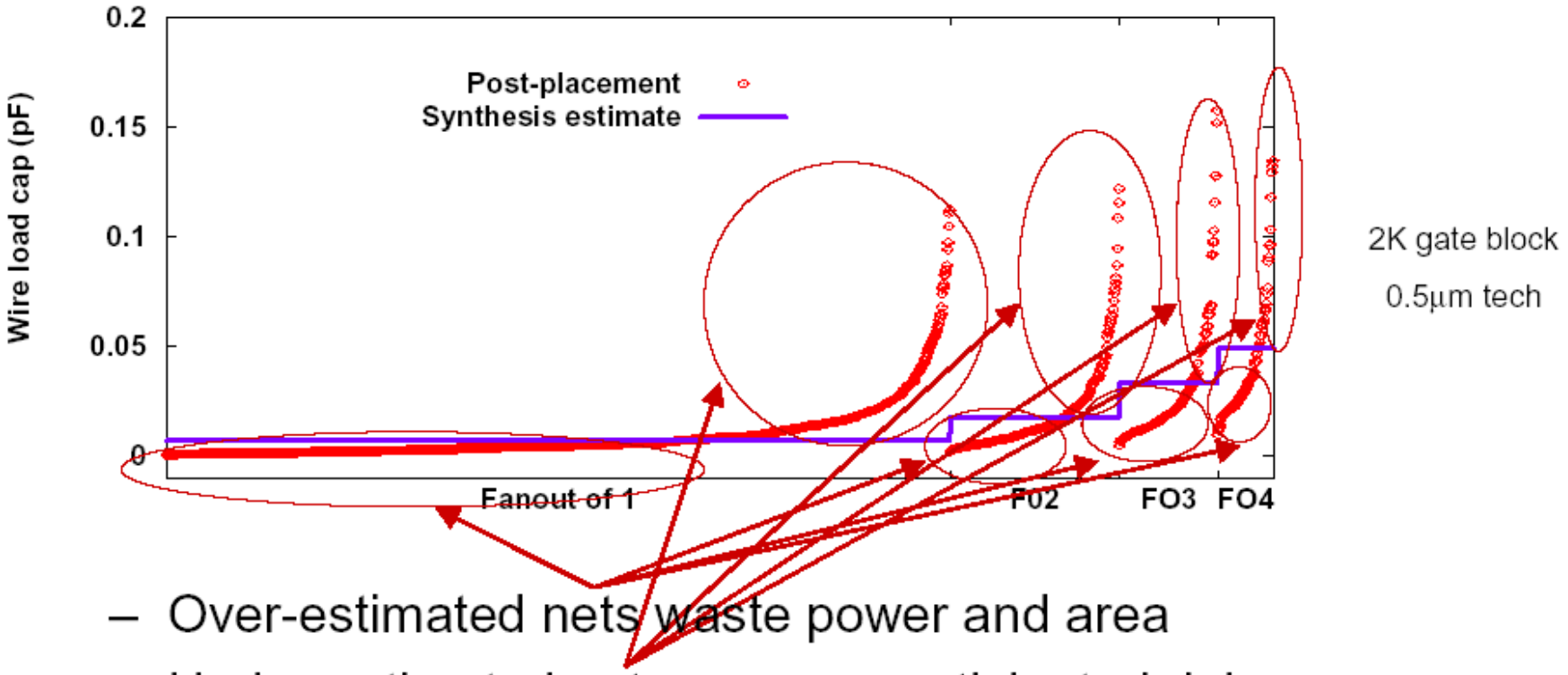
R. Zhang, *et al*, ISQED 2001



H. Hua *PhD Dissertation*, NCSU, 2006

- Donath's method can also be applied to develop histograms of wire-length
- These histograms are similar to what occurs in well-designed circuits

Limitations of Wire-Load Estimation



- Over-estimated nets waste power and area
- Under-estimated nets cause unanticipated delays

- Source: Ho, Mai, & Horowitz 2001
- Wire-Load estimates are all we have during logic-design
- Back-annotation of wire parasitics are necessary to get an accurate idea of performance

Why do we care?

- Wire Load Models Aid Synthesis with Synopsys Design Compiler

```
wire_load(areaunder5K) {
      capacitance:        0.000136
      resistance:         0.000194
      area:               0
      fanout_length(1, … )
      …
      fanout_length(8, … )
      slope:               …
}
wire_load(areaunder80K) {
…
}
```

Donath's method can be used to estimate wire lengths for different synthesized area