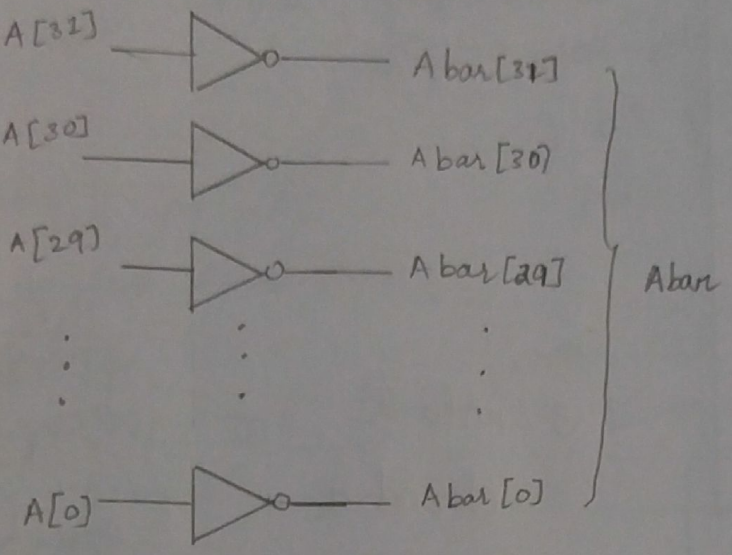
NAME : ANUSHA RAVILLA STUDENTID : 2001/08828 SIGNATURE : Ravilla

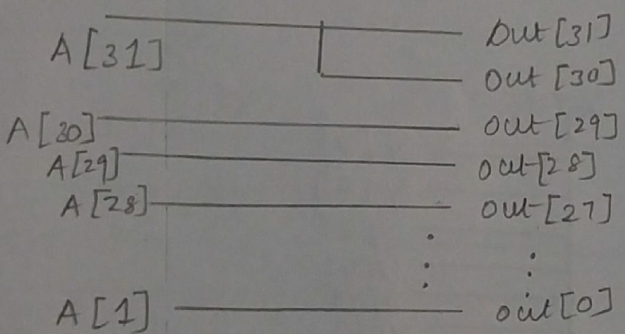
Question 1 :

a.



32 inverters

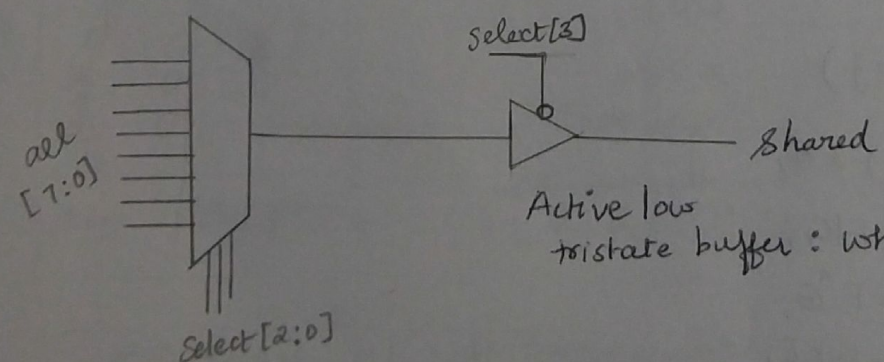
b.



out [31] will be A[31]

out is A shifted right by one bit and the MSB filled by the out[31].

b.



Active low tristate buffer : when shared[3] = 1, shared = 1'bz.

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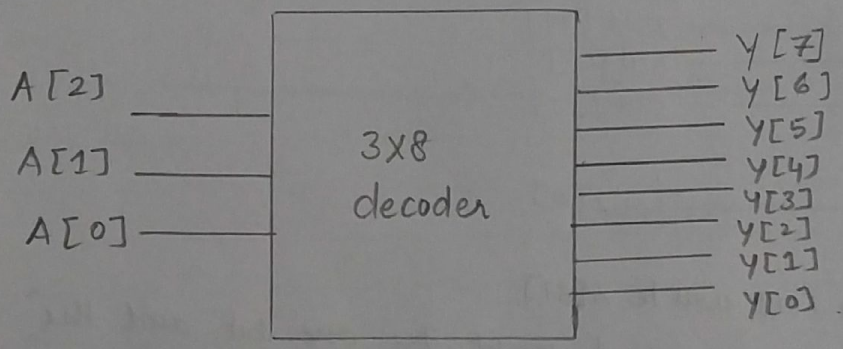
c.

A	Y[7] . . . Y[0]
	Y
	Y[7] . . . Y[1] Y[0]
000	00000001
001	00000010
010	00000100
011	00001000
100	00010000
101	00100000
110	01000000
111	10000000

3 into 8 decoder



(d)

```
always @(C*)
begin
casex({A,B,C})
3'b1xx : H=F&G;
3'b01x : H=F|G;
3'b001 : H=F^G;
default : H=D&E;
endcase
end
```

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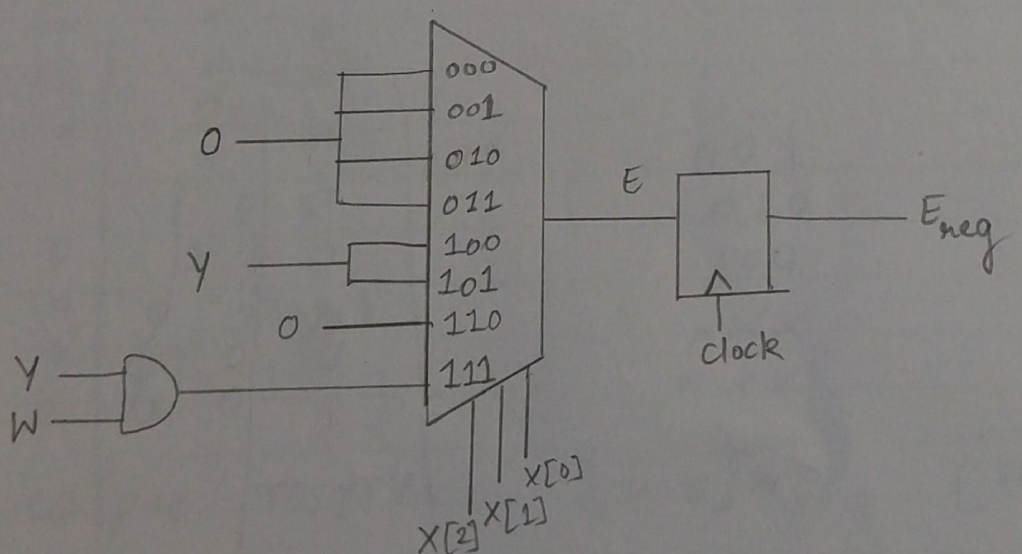
2.

```
reg [7:0] A;
reg parity;
always @(*)
begin
parity = 1'b1;
for (int i=0;i<=7;i++)
if(A[i]==1) parity = ~parity; // Can also be
                              parity = parity ^ A[i];
end
```

3.



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