
ECE 720 – ESL & Physical Design

Project 2 Requirements

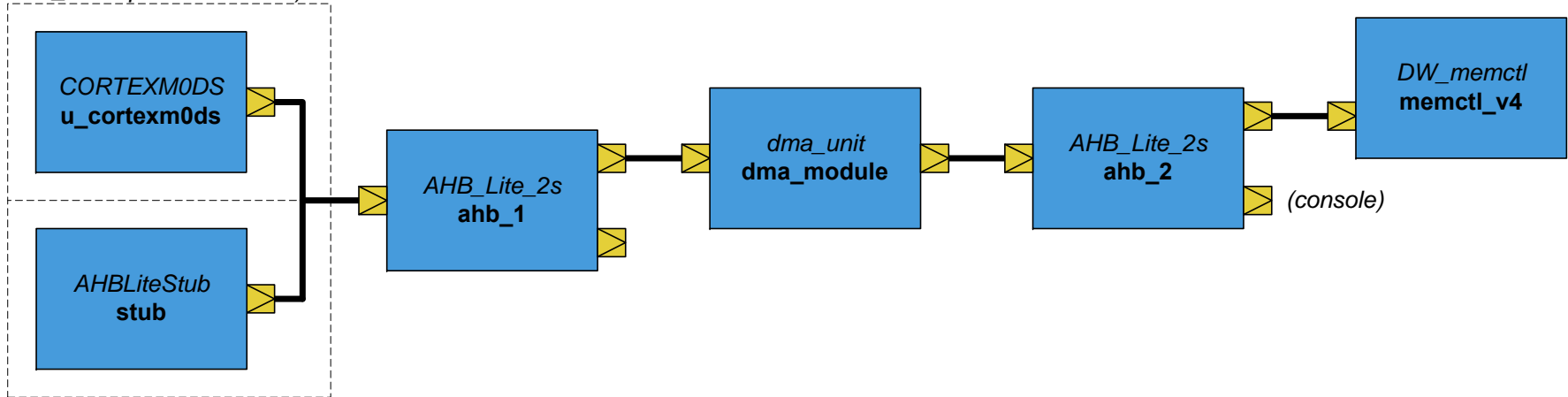
W. Rhett Davis
NC State University

Announcements

- No lecture Thursday (Fall Break)
- Homework 4 due Thursday
- Homework 5 due in 9 days
- Project 2 due in 3 weeks

Project System 2

(swap between cortex_soc & stub_soc top-level modules)



- **v** directory includes RTL and gate-level code for the logic above
- **sc** directory contains SystemC code for basic Cortex-M0DS and some Simple LT 2x2 systems presented in class
- Your project assignment is to complete the TLM simulations

Project Goals

- Demonstrate TLM simulations
 - » of the Cortex-M0DS SoC running *dma.c*
 - *Compute the cycles/sec performance and compare to RTL to show large speedup*
 - *Compare the simulation time to RTL to show small prediction error*

Requirements (1/2)

- Due Tue. Oct. 25 (3 weeks from today)
- TLM Simulation Constraints
 - » TLM 2.0 b_transport calls must be used
 - » DW_memctl & dma_unit must be separate modules
 - » scx_evs_Cortex module must be used, source code for the Cortex image must match RTL Cortex image
 - » Only those aspects needed to represent the RTL simulation behavior must be modeled
 - » Modify sc/sgc/Makefile if needed so that “make” and “make sim” generate the results discussed in your report

Requirements (2/2)

- Documentation Requirement
 - » Document the cycles/sec performance of both TLM and RTL simulations and calculate the speedup
 - » Choose 3 transaction sequences from the TLM/RTL to compare simulations times and calculate the prediction error
 - » Modify the provided compare_tlm_rtl.xlsx file to include the values for each case compared in your report
- Report Requirements
 - » Values claimed in report must match values simulated with submitted code and compare_tlm_rtl.xlsx file
 - » Report should contain an introduction, body, and conclusion. You may use whatever section titles you like for the body.
 - » Report must comment on the speedup and error and state what you might be able to do better.

Project Grading

- (15%) Completeness & Organization – All requirements must be met
- (15%) Writing Quality – Emphasis on Clarity. Good grammar is necessary, but not sufficient
- (15%) Analysis – Graphs and explanation of results
- (15%) Execution – Ability to re-create a data-point
- (40%) Key Outcomes – awarded as follows:
 - » (10%) No successful analysis of behavior, but significant effort
 - » (20%) Limited range of behavior analyzed
 - » (30%) Satisfactory range of behavior analyzed
 - » (40%) Good and bad qualities of the TLM fully analyzed
- Recall that Project 2 is 20% of the total grade