### Digital Integrated Circuit Design

Module BusIntro
On-chip Buses and Interconnects:

Introduction

W. Rhett Davis

# Why do we care?

	What is a Bus?				
	What is an Interconnect?				
Why do we use them?					

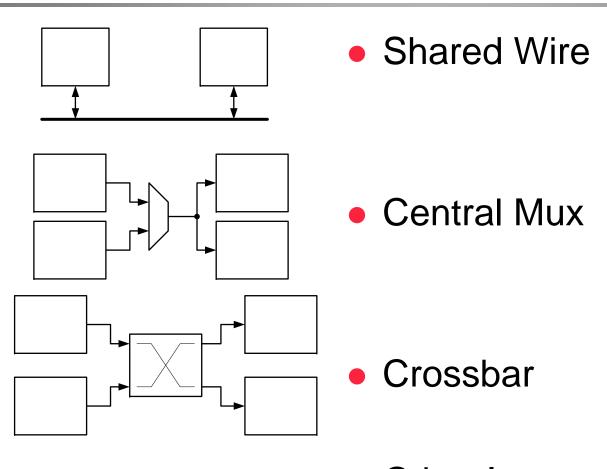
#### Our Question

• Which bus or interconnect should we use?

#### The answer depends on the following:

- » What IP blocks do we have and what do they work with?
- » How many ports do we need?
- » What kind of overhead can we permit?
  - Throughput
  - Area
  - Power

### Types of Interconnects



Other Issues: Queueing, Pipelining

#### **Bus & Interconnect Standards**

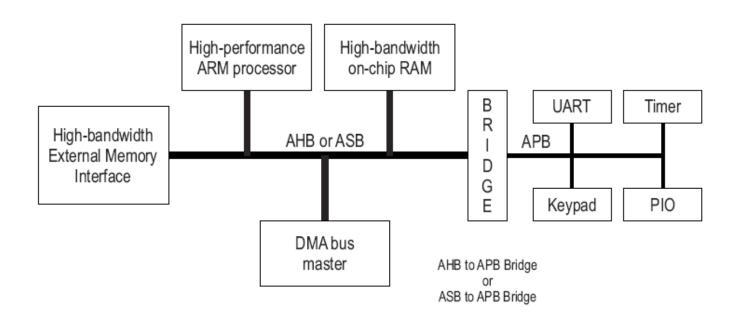
- AMBA from ARM
- Wishbone from OpenCores.org
- CoreConnect from IBM
- Sonics "Silicon Backplane"

We'll focus on AMBA in this class, because it's the most commonly used

#### **AMBA** Introduction

- Advanced Microcontroller Bus Architecture (AMBA), created by ARM as an interface for their microprocessors.
- Easy to obtain documentation (free download) and can be used without royalties.
- Very common in commercial SoC's (e.g. Qualcomm Multimedia Cellphone SoC)
- History:
  - » AMBA 2 released in 1999, includes APB and AHB
  - » AMBA 3 released in 2003, includes AXI and AHB-Lite
  - » AMBA 4 released in 2010, includes AXI4-Stream

# AMBA 2.0 System-Level View



#### AMBA AHB

- \* High performance
- \* Pipelined operation
- \* Multiple bus masters
- \* Burst transfers
- \* Split transactions

#### AMBA ASB

- \* High performance
- \* Pipelined operation
- \* Multiple bus masters

#### **AMBA APB**

- \* Low power
- \* Latched address and control
- \* Simple interface
- \* Suitable for many peripherals

Source: AMBA Specification, Rev. 2.0

## Comparison of AMBA Bus Types

	APB	AHB	AHB-Lite	AXI / PL300
Processors	all	ARM7,9,10	ARM Cortex	ARM11
Control Signals	4	27	12	77
No. of Masters	1	1-15	1	1-16
No. of Slaves	1-15	1-15	1-15	1-16
Interconnect Type	Central MUX	Central MUX	Central MUX	Crossbar w/ 5 channels
Phases	Setup, Enable	Bus request, Address, Data	Address, Data	Address, Data, Response
Xact. Depth	1	2	2	16
Burst Ops.	no	yes	yes	yes
Simultaneous Read & Write	no	no	no	yes

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Thanks for watching