Anusha Ravilla

aravill@ncsu.edu
919-931-9686
www.linkedin.com/in/anusha-ravilla

AREAS OF SPECIALIZATION

|| ***ASIC Verification, ASIC Design, Computer architecture*** ||

EDUCATION

North Carolina State University, Raleigh, NC, USA ***Aug'15 - Dec '16***
Master of Science in Computer Engineering **GPA-3.45/4.00**
National Institute of Technology, Tiruchirapalli, India ***Jul'11 - Jul'15***
Bachelor of Technology in Electrical and Electronics Engineering **CGPA-7.87/10**

PROJECTS

North Carolina State University, Raleigh

- **Verifying a pipelined LC3 Microcontroller: (System Verilog)** **Jan -Mar '16**
  - Designed a layered functional verification environment for a pipelined microcontroller.
  - Performed constrained random testing and directed tests. Ensured maximum coverage using assertions, coverage bins and cover properties.
- **Speeding up GPU warps by Reducing Memory Pitstops: (GPGPU-sim, c++)** **Jan -Mar '16**
  - Prioritized memory requests on detection of saturation to achieve better overlap of compute and memory accesses.
  - Facilitated reuse of data present in the L1 data cache by augmenting re-execution queue with load store unit.
- **Bellman Ford Hardware Accelerator: (Verilog)** **Aug-Dec '15**
  - Designed a hardware accelerator to find the shortest spanning tree between a pair of graph nodes.
  - Synthesized the design in Synopsys Design Compiler and ensured the design met setup and hold requirements.
- **Cache Simulator for Performance Evaluation: (c++)** **Aug-Sep '15**
  - Developed a software simulator for a generic cache with multiple levels of hierarchy.
  - Used the simulator to compare the performance, area, and energy of different memory hierarchy configurations on a subset of SPEC-2000 benchmark suite and for evaluating the effect of addition of victim cache on average access time.
- **Dynamic Branch Prediction Simulator: (c++)** **Sep '15**
  - Developed a simulator configurable for bimodal, gshare and hybrid branch predictor configurations, and used it to design branch predictors well suited to the SPECint95 benchmarks.
  - Evaluated the tradeoff between misprediction rate and cost of the predictor.
- **Dynamic Instruction Scheduler Simulator: (c++)** **Sep-Dec '15**
  - Developed a software simulator for an out-of-order superscalar processor with a 9 stage pipeline that fetches and issues *N* instructions per cycle.
  - Evaluated the effect of Re-order buffer size and Issue Queue size on IPC for different N values.
- **Cache Coherence Protocol Simulator: (c++)** **Aug-Dec '15**
  - Designed a cache coherence protocol software simulator for a multi-core processor system with multiple levels of hierarchy, capable of simulating MSI, MESI and the Dragon protocols.
  - Drew inferences on cache performance for various cache configurations for MSI, MESI and dragon protocols.

National Institute of Technology, Trichy, India **Jan-May '15**

- **Pulse Monitoring System: (embedded c, c++)**
  Developed a system that monitors the driver's blood oxygen level and informs abnormalities to help the driver get out of danger using optical sensor OPT101, GPS and GSM modules.

Indian Institute of Science, Bangalore, India (MATLAB, embedded c) ***Jun - Jul '13***

- Worked on analysis of human gait using inertial sensors which helps in diagnosis of diseases.
- Developed an approximation algorithm for movement of an unmanned surveillance robot.

PATENTS AND PUBLICATIONS

Cost effective Accident Response System for cars using embedded system ***2013***

- Designed a low cost accident response system for vehicles using TI's MSP430.
- Applied for a patent in relation to the above, ***Patent: India 4434/CHE/2013 A,*** filed on September 30, 2013.

SKILL SET

- **Languages**: *Verilog, VHDL, System Verilog, C, C++, Python*
- **Tools**: *ModelSim, Synopsys design compiler, Cadence RTL compiler, Xilinx ISE*
- **Others**: *MATLAB, Pspice, HTML5, Code Composer Studio,* KEIL µVision IDE, AVR Studio IDE, *Linux*

RELEVANT COURSEWORK

ASIC Verification, Digital ASIC Design, GPU Architecture/Data Parallel Processor, Computer Design & Technology, Architecture of Parallel Computers, Electronic System Level & Physical Design, Computer Networks, Embedded System Design