ECE 720 – ESL & Physical Design

Project 3 Requirements (Updated)

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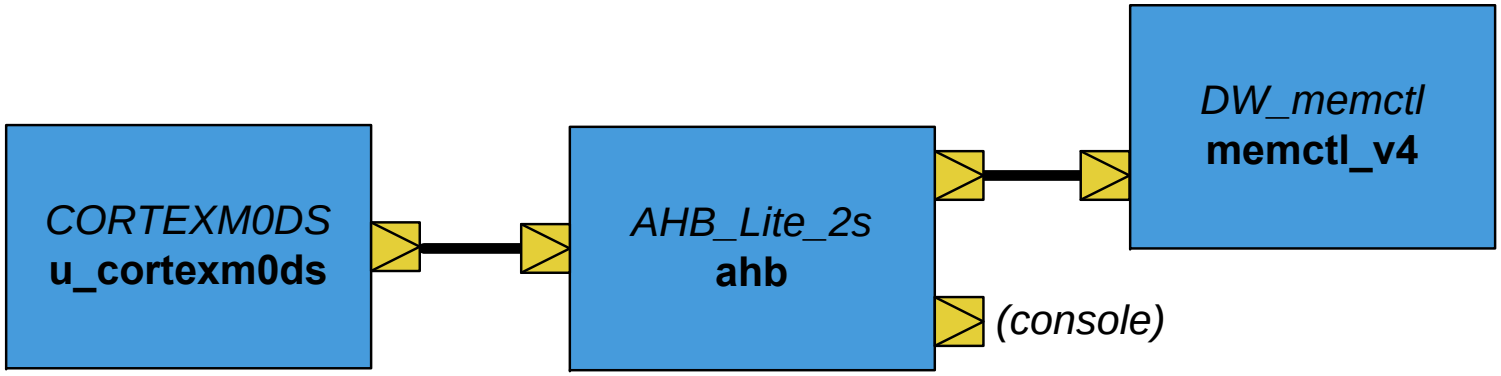
Project System



- ***cortex_soc*** system includes the netlist for this system
- Your project assignment is to execute the physical flow
- "proj3" directories in repositories will be created with files from Project 1 plus Place & Route Tutorial #2
- You will need to modify the files yourself to get the flow working

Project Goals

- Perform the complete physical design flow on the cortex_soc system
- Primary Objective: minimize the metric A^2D
  - A^2 – area of the design squared
  - D – clock period of the design
- Secondary Objective: minimize the number of metal layers

Requirements

- Use ss0p95v125c corner/timing/liberty library
- Keep an iteration record, as in pr_tut2
- Design must meet hold-time constraints (in ICC, no extra margin needed)
- Complete detail routing with no violations

Requirements

- Report Statistics in design_stats.xlsx
  - Area
    - Number of cells (final, not including filler cells)
    - Area (height and width) for both the core and complete design
    - Cell density (target at the beginning of the *init* step)
  - Routing
    - Number of metal layers used
    - Total wire length (“Net Length” from report_qor)
  - Timing and Signal Integrity
    - Target clock rate, setup slack, hold slack (from pr/timing_si_max & _min.rpt)
    - Worst case (by area) noise width and height (from pr/noise.rpt)

Requirements

- Report Statistics in design_stats.xlsx
  - Clock
    - Max skew, max/min transition time, and max/min insertion delay (launch latency) (from timing_si_clock.rpt)
    - Number of stages (i.e. “Levels”) and sinks (from report_clock_tree)
- Images
  - Final Layout
  - Clock Tree Plot

Requirements

- Iteration Report
- Supporting Files (from last iteration only)
  - run_init.log
  - run_place.log
  - run_cts.log
  - run_route.log
  - run_ptsi.log
  - pr/timing_si_max.rpt
  - pr/timing_si_min.rpt
  - pr/timing_si_clock.rpt
  - pr/noise.rpt
  - cortex_soc.def
  - cortex_soc_routed.v
  - your modified versions of all files in the repository
  - pr/work/ (note that you'll need to modify .gitignore to commit this)

Grading

- Satisfying Design Objectives (20%)
- Meeting Design Constraints
  - » No Hold- or Setup-Time Violations w/ ss0p95v125c Corner (15%)
  - » No Routing Violations (15%)
- Report Completeness (50%)

- Due Thu. Dec. 8