Homework - 8

Anusha Ravilla (200108828)

Solution P1:

Place & Route Iteration Record

Iteration	1	2	3	4	5
Period	5 ns	4ns	4ns	4.5ns	4.5ns
Clock Uncertainty	50 ps	50 ps	50 ps	50 ps	50 ps
INIT AspectRatio	1	1	1	1	1
INIT Density	85%	85%	85%	85%	85%
CTS Max Tran	500 ps	500ps	300ps	150ps	100ps
CTS Leaf Max Tran	500 ps	500ps	500ps	500ps	500ps
CTS Target Skew	0	0	0	0	0
ROUTE overflow GRCs	8%H 1%V	8%H 1%V	8%H 1%V	8%H 1%V	8%H 1%V
ROUTE violations	0	0	0	0	0
PT Slow Max Ins Delay	160 ps	143 ps	171 ps	171 ps	113 ps
PT Slow Min Ins Delay	134 ps	113 ps	140 ps	140 ps	96 ps
PT Slow Max Clk Tran	249 ps	211 ps	257 ps	257 ps	103 ps
PT Slow Min Clk Tran	177 ps	134 ps	167 ps	167 ps	50 ps
PT Slow Hold Slack	179 ps	194 ps	196 ps	196 ps	182 ps
PT Slow Setup Slack	170 ps	156 ps	163 ps	163 ps	190 ps
Notes					

The highlighted PT Slow Hold Slack higher than PT Slow Max Clock Transition.

Discarded Iterations:

Iteration	1	2
Period	3.5ns	4ns
Clock Uncertainty	50 ps	50 ps

INIT AspectRatio	1	1
INIT Density	85%	85%
CTS Max Tran	500ps	200ps
CTS Leaf Max Tran	500ps	500ps
CTS Target Skew	0	0
ROUTE overflow GRCs	8%H 1%V	8%H 1%V
ROUTE violations	**21**	**9**
PT Slow Max Ins Delay	175 ps	142 ps
PT Slow Min Ins Delay	448 ps	113 ps
PT Slow Max Clk Tran	284 ps	210 ps
PT Slow Min Clk Tran	129 ps	134 ps
PT Slow Hold Slack	194 ps	195 ps
PT Slow Setup Slack	90 ps	151 ps

Solution P2:

u_logic/n205 was found to have the highest area when the run_ptsi.log was checked after running the Make ptsi.
Victim u_logic/n205 was mapped to *13556 in the CORTEXM0DS_routed.spef file.
Victim u_logic/n17649 was mapped to *5843 in the CORTEXM0DS_routed.spef file.

```
*D_NET *5843 2.855914
….
23 *5843:8 *13556:23 0.2207509
24 *5843:9 *13556:23 0.2207509
```

The above block was obtained from the SPEF file from the information known
Hence the total capacitance connected to victim and the node (C_C)= 0.2207509 + 0.2207509
The capacitance connected to other nodes (C_W) = 2.855914 - 0.4415018 = 2.4144122 pf

$C_W V_1 = (C_W + C_C)\, V_2$

$$\frac{V1}{V2} = \frac{CW}{CW+CC} = \frac{2.4144122}{2.4144122+0.4415018} = 0.845$$

$(1 - 0.845) \times 1.1$ **~ 170 mV**

Solution P3:

The minimum delay can be calculated as:

$$t_{p1} = 0.69 \times R_d \times C_d \times (1+\gamma)$$
$$= 0.69 \times 548 \times 0.61 \times (1 + 1.4)$$
$$= 553.567 \text{ fs}$$
$$\sim 553.57 \text{ fs}$$

Calculating the L critical:

$$Lcr = \frac{L}{mopt} = \sqrt{\frac{tp1}{0.38 \times r \times c}}$$

$$Lcr = \sqrt{\frac{553.57}{0.38 \times 0.18 \times 3}}$$

$$\sim 51.94\ \mu m$$

$$t_{p,crit} = \frac{tp,min}{mopt}$$

$$= 2 \times t_{p1} \times \left(1 + \sqrt{\frac{0.69}{0.38 \times (1+\gamma)}}\right)$$

$$= 2 \times 553.57 \times \left(1 + \sqrt{\frac{0.69}{0.38 \times (1+1.4)}}\right)$$

$$\sim 2.070 \text{ ps}$$

$$t_p(\text{for 1cm}) = \frac{1\ cm}{51.94\ \mu m} \times 2.07 \text{ ps}$$

~ 398.84 ps

The minimum time that is needed to drive a signal across a chip over a distance of 1 cm using repeaters is found to be 398.84 ps.