

ECE 745 PROJECT

BUG REPORT

BY

GROUP 37

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Bug1: The bug is in Controller

Description of the bug : Enable-UpdatePC has the bug in Controller unit. When BR-taken is low, Enable-UpdatePC has to go to Zero but the buggy DUT goes to 1.

We get this Bug for all branch instructions , since Enable-UpdatePC goes to 1 even when BR-taken is Zero.

Instructions in pipeline: For all branch instructions, we detect the bug and Enable_updatePC is 1 without taking BR_taken in to consideration.

The screenshot displays the ModelSim SE 10.3b environment. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, and Help. Below the menu bar is a toolbar with various simulation and editing icons. The main workspace is divided into three panes: a project tree on the left, a source code editor in the center, and a transcript window at the bottom.

The project tree on the left shows a hierarchy of design units. The source code editor in the center displays the Verilog code for the 'writeback_golden_reference' module. The code includes various signals, tasks, and conditional logic. The transcript window at the bottom shows the output of the simulation, including several error messages related to the 'enable updatePC' signal.

The source code in the center pane is as follows:

```
Ln# 84 d2=RegFile[sr2];
85 //d1= fileObj.file[sr1];
86 //d2= fileObj.file[sr2];
87 end
88 end
89 end
90
91 begin
92     forever@(posedge Interface.clock)
93     begin
94         check_async();
95     end
96 end
97 join
98 endtask
99 task check_sync();
100 if(psr!=Probe_writeback.psr)
101 $display($time,"error in WB psr %b,%b",psr,Probe_writeback.psr);
102 endtask
103
104 task check_async();
105
106 //display($time,"d2%d",d2);
107 //display($time,"reg %d",RegFile[sr2]);
108 if(d1!=Probe_writeback.d1)
109 begin
110 $display($time,"error in WB d1 %b,%b",d1,Probe_writeback.d1);
111 //display($time,"probe d1 %d",Probe_writeback.d1);
112 end
113 if(d2!=Probe_writeback.d2)
114 begin
115 $display($time,"error in WB d2 %b,%b",d2,Probe_writeback.d2);
116 //display($time,"reg %d",RegFile[sr2]);
117 end
118 end
```

The transcript window at the bottom shows the following output:

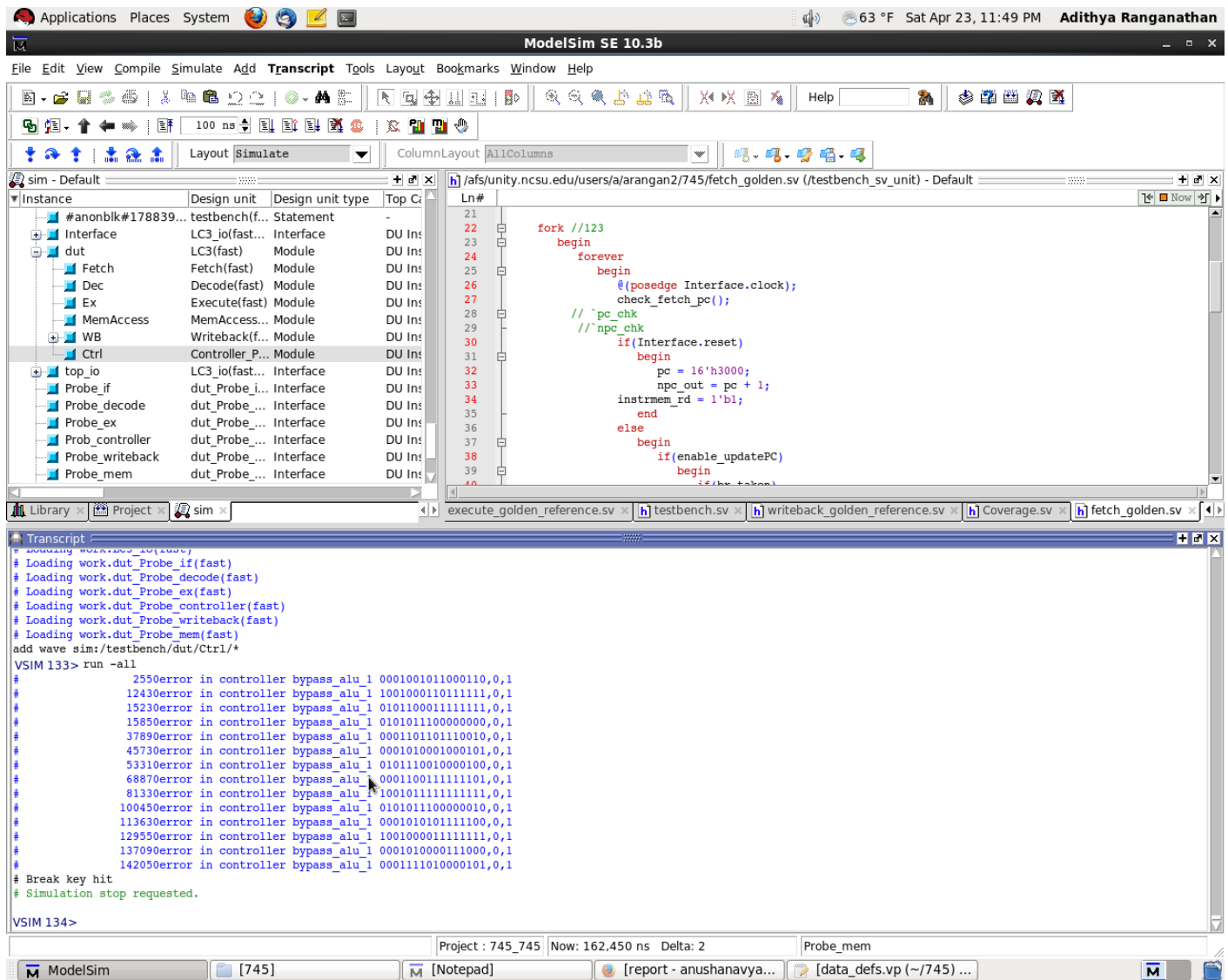
```
VSIM 129> run -all
# 2570error in controller enable updatePC 0000011001100000,0,1
# 10610error in controller enable updatePC 0000010000111110,0,1
# 10890error in controller enable updatePC 0000010111101001,0,1
# 11730error in controller enable updatePC 0000010011100011,0,1
# 15250error in controller enable updatePC 0000010100110000,0,1
# 16070error in controller enable updatePC 0000100111010101,0,1
# 16290error in controller enable updatePC 0000110101000000,0,1
# 18210error in controller enable updatePC 0000100001011110,0,1
# 22510error in controller enable updatePC 0000001101101100,0,1
# Break key hit
# Break in Task testbench_sv_unit/writeback_golden::golden_reference at writeback_golden_reference.v line 84
VSIM 130>
```

The status bar at the bottom of the window shows the current file path, line number, column number, and other simulation parameters.

Bug2: CONTROLLER

When there is a BR instruction, we do not have any source registers for this instruction and there is no data dependency between this instruction in decode stage (IR[8:6]) and another instruction in execute stage whose Destination Register (IR_Exec[11:9]) even if they have the same values. Since there is no data dependency bypass_alu_1 should be 0 but instead it becomes 1.

Instructions in pipeline:



Bug3: CONTROLLER

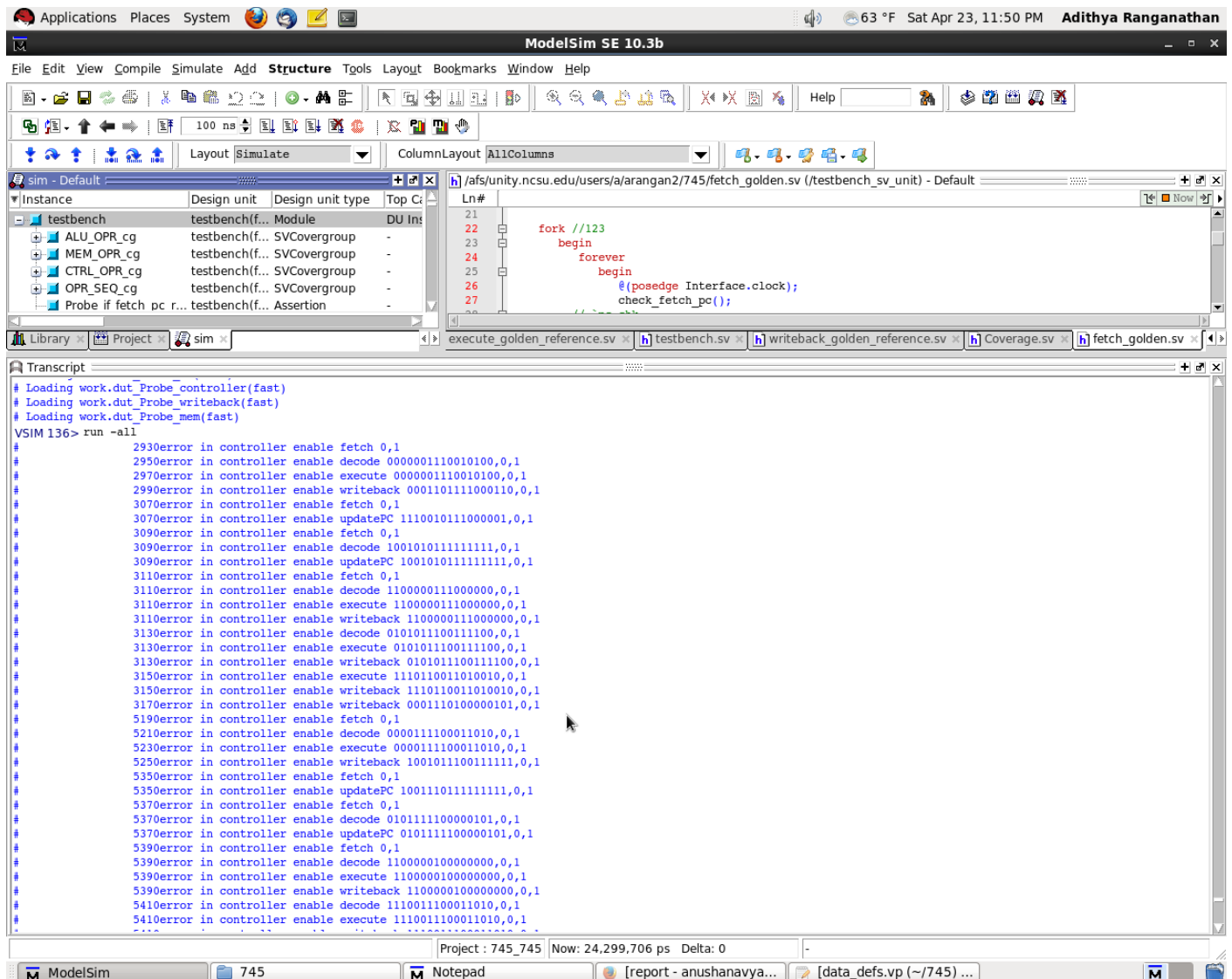
Description of the bug : Enable and Br_taken signals are not matching in the Controller unit

If branch taken, then enable_updatePC and enable fetch should become 1 at the same cycle (enable fetch should only be high in the next cycle) and as a result of this, the pipeline propagates the error

(because enable_decode goes high in the next cycle and so on). Thus resulting in faulty behavior for 4 cycles after a taken-branch.

Example: When 0000111100111011 was driven both the enable_updatePC and enable_fetch went high when the branch is taken

Instructions in pipeline



Bug4: EXECUTE

Description of the Bug : Aluout and PCout outputs of Execute stage are not the same. We get the Bug when Bypass_ALU_2 is 1. The reason is that the second operand of a dependent instruction for an alu-operation takes the Mem_Bypass_Val instead of Aluout.

Instructions in pipeline:

The screenshot shows the ModelSim SE 10.3b interface. The top window displays the testbench code for 'fetch_golden_sv'. The bottom window shows the transcript of the simulation, listing instructions and their corresponding N/Z/P values. The status bar at the bottom indicates the project is '745_745' and the simulation is running at 19.883,594 ps.

Transcript:

```
# Loading work.dut Probe_mem(fast)
VSIM 139> run -all
#
390bug in execute aluout 0001110001000000,1111111111111111,0000110000101000
390bug in execute pcout 0001110001000000,1111111111111111,0000110000101000
990bug in execute aluout 1010011011111000,000000000111111,0010101101011100
990bug in execute pcout 1010011011111000,000000000111111,0010101101011100
1830bug in execute aluout 0101011010100001,0010011111001011,1000011010111101
1830bug in execute pcout 0101011010100001,0010011111001011,1000011010111101
3050bug in execute aluout 010110011101001,1100111100101001,1010101100101111
3050bug in execute pcout 010110011101001,1100111100101001,1010101100101111
3570bug in execute aluout 111011110000111,100001110110111,1011101010100101
3570bug in execute pcout 111011110000111,100001110110111,1011101010100101
3830bug in execute aluout 0010000111001000,0000110110101000,1011001000010010
3830bug in execute pcout 0010000111001000,0000110110101000,1011001000010010
5130bug in execute aluout 1001000101111111,1011111001011100,1010101010101010
5130bug in execute pcout 1001000101111111,1011111001011100,1010101010101010
5150bug in execute aluout 0001011110000101,0100000110100011,0101010101010101
5150bug in execute pcout 0001011110000101,0100000110100011,0101010101010101
9890bug in execute aluout 1011000010010001,1111111111111111,0010001100101111
9890bug in execute pcout 1011000010010001,1111111111111111,0010001100101111
11070bug in execute aluout 0011110100100010,0000000101110001,0010100111111001
11070bug in execute pcout 0011110100100010,0000000101110001,0010100111111001
11530bug in execute aluout 0001010010101110,0111000001001111,0000011001101111
11530bug in execute pcout 0001010010101110,0111000001001111,0000011001101111
11670bug in execute aluout 0001111001100111,0000000101110100,0010000111100110
11670bug in execute pcout 0001111001100111,0000000101110100,0010000111100110
12210bug in execute aluout 1001010001111111,0010000000100010,0000000110000010
12210bug in execute pcout 1001010001111111,0010000000100010,0000000110000010
12590bug in execute aluout 1001000100111111,1000101001010100,0110010001011000
12590bug in execute pcout 1001000100111111,1000101001010100,0110010001011000
15790bug in execute aluout 1110001110110110,1111111010110011,1100011000001011
15790bug in execute pcout 1110001110110110,1111111010110011,1100011000001011
17370bug in execute aluout 0101010111111100,0000000000000000,1111110101100000
17370bug in execute pcout 0101010111111100,0000000000000000,1111110101100000
17710bug in execute aluout 010110110100100,0000000000000000,1000010101011011
17710bug in execute pcout 010110110100100,0000000000000000,1000010101011011
17770bug in execute aluout 1011011100010001,0000000000000000,1010110110000001
17770bug in execute pcout 1011011100010001,0000000000000000,1010110110000001
```

Bug5: EXECUTE

The NZP value in execute stage does not turn out to be the same in Golden Reference and DUT. This is because the middle bit of NZP value for BR instruction always seems to be stuck at 0 ie NZP[1]=0 always. Hence we get an error when the middle bit of NZP goes high in golden reference but instead it stays low in the buggy DUT.

Instruction in pipeline

ModelSim SE 10.3b

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help



100 ns

Layout Simulate ColumnLayout AllColumns

sim - Default

Instance	Design unit	Design unit type	Top C
decode_golden	decode_gol...	SVClass	-
execute_golden	execute_go...	SVClass	-
new	testbench_...	Function	-
golden_referenc...	testbench_...	Task	-
check_execute_...	testbench_...	Task	-
check_execute_...	testbench_...	Task	-

```
Ln#
220
221 begin
222     #0.001;
223
224     /*
225
226         if(Interface.reset)
227             begin
228                 srl = 0;
229                 sr2 = 0;
230             end
231     */
```

Library Project sim

execute_golden_reference.sv testbench.sv writeback_golden_reference.sv Coverage.sv fetch...

Transcript

```
# Loading work.LC3(fast)
# Loading work.Fetch(fast)
# Loading work.Decode(fast)
# Loading work.Execute(fast)
# Loading work.MemAccess(fast)
# Loading work.Writeback(fast)
# Loading work.Controller_Pipeline(fast)
# Loading work.dut_Probe_if(fast_1)
# Loading work.dut_Probe_decode(fast_1)
# Loading work.dut_Probe_ex(fast_1)
# Loading work.dut_Probe_controller(fast_1)
# Loading work.dut_Probe_writeback(fast_1)
# Loading work.dut_Probe_mem(fast_1)
# Loading work.LC3_io(fast)
# Loading work.dut_Probe_if(fast)
# Loading work.dut_Probe_decode(fast)
# Loading work.dut_Probe_ex(fast)
# Loading work.dut_Probe_controller(fast)
# Loading work.dut_Probe_writeback(fast)
# Loading work.dut_Probe_mem(fast)
VSIM 142> run -all
#
# 2570bug in execute Prob_ex.NZP 0000011001100000,011,001
# 5270bug in execute Prob_ex.NZP 0000111100011010,111,101
# 6490bug in execute Prob_ex.NZP 0000011011100101,011,001
# 8310bug in execute Prob_ex.NZP 0000011011000000,011,001
# 10610bug in execute Prob_ex.NZP 0000010000111110,010,000
# 10890bug in execute Prob_ex.NZP 0000010111101001,010,000
# 11730bug in execute Prob_ex.NZP 0000010011100011,010,000
# 15250bug in execute Prob_ex.NZP 0000010100110000,010,000
# 15870bug in execute Prob_ex.NZP 0000011011110101,011,001
# 16290bug in execute Prob_ex.NZP 0000110101000000,110,100
# 18010bug in execute Prob_ex.NZP 0000111111000110,111,101
# 29130bug in execute Prob_ex.NZP 0000110010001011,110,100
# 31710bug in execute Prob_ex.NZP 0000111111011000,111,101
# 37910bug in execute Prob_ex.NZP 0000010101101101,010,000
# Break key hit
# Simulation stop requested.
```

VSIM 143>

Ln: 221 Col: 0 READ Project : 745_745 Now: 44,403,698 ps Delta: 0

ModelSim

[745]

[Notepad]

[report - anushanavya...]

[data_defs.vp (~/745) ...]