Homework #5

Pull the initial files for this homework into your private git repository by changing into that directory and executing the command "git pull". Then complete the problems below, add, commit, and push the results to your GitHub repository.

1. (20 points) Modify the *mem* module from the Simple LT 2x2 TLM example presented in Lecture 9 to model the DW_memctl module as simulated in Homework 2, problem 2. As in that problem, perform 4 read operations, each of 16 bytes. The first and second read should be to the same row and bank, while the third should be to a different row (same bank), and the fourth should be to a different bank. Your simulation should print a message for each read and an increase in the duration of the transaction when the row boundary is crossed. Commit your solution in the *hw05/p1* directory of your *git* repository and push the commit to GitHub. Ensure that you update the *Makefile* if needed so that the code builds and executes properly with the *make* and *make sim* commands, and that unnecessary files are not committed.

2. (20 points) Repeat Homework 2 Problem 1 (parts (a) and (c) only) by analyzing TLM simulation of the Cortex-M0 processor with the ARM Fast Models. Compare your results to your answers from Homework 2 Problem 1(a) and 1(c). Put your answers in a file called *answers.txt* in the *hw05/p2* directory, along with an explanation of how you determined your answer. Commit the simulations needed to determine your answer (along with any scripts you wrote to determine your answer) in the *hw05/p2* directory of your *git* repository and push the commit to GitHub. Ensure that you update the *hw05/p2/sim/Makefile* if needed so that the code builds and executes properly with the *make* and *make sim* commands to repeat the procedure described in *answers.txt*.

3. (30 points) Modify the bus module from the Simple Loosely-Timed 2x2 Transaction-Level Modeling Example discussed in class to model an AHB-Lite central-mux-style interconnect. For full credit, your simulation must show that transactions initiated simultaneously by the stubs are executed sequentially by the memories. Commit your solution in the *hw05/p3* directory of your *git* repository and push the commit to GitHub. Ensure that you update the *Makefile* if needed so that the code builds and executes properly with the *make* and *make sim* commands, and that unnecessary files are not committed.