ECE 720 – ESL & Physical Design

Lecture 12: Base-line Physical Design Flow

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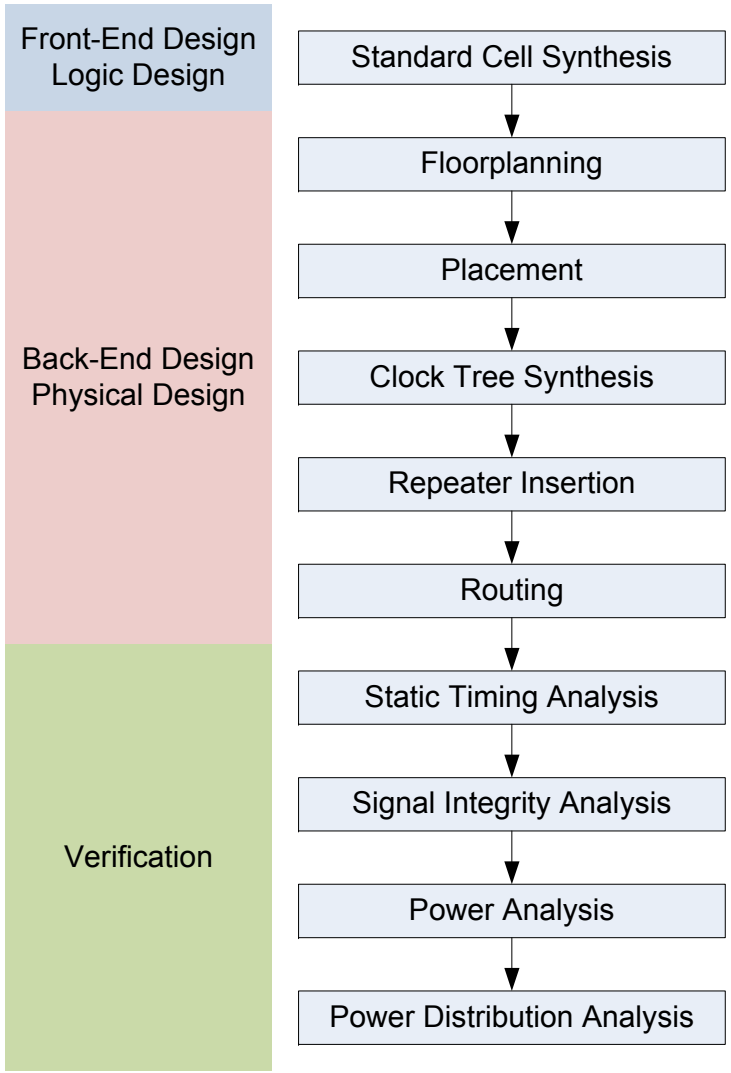
Announcements

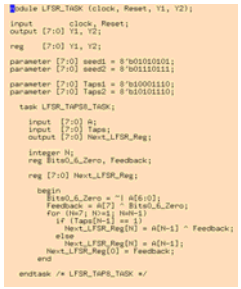
- Homework 5 Due Saturday
- Project 2 Due in 12 days
- Homework 6 Due in 19 days
- Look for “Place & Route Tutorials” Link under Resources Section of course web-page
  - pr_tut1.tar.gz also available in workspace common directory

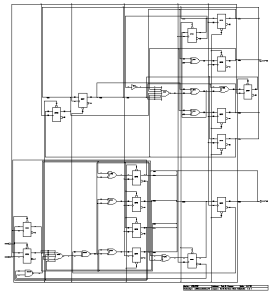
Today's Lecture

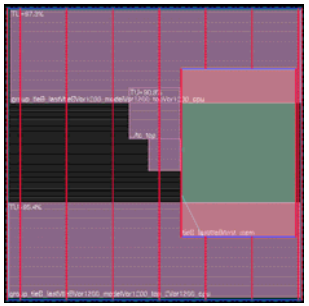
- Baseline Design Flow

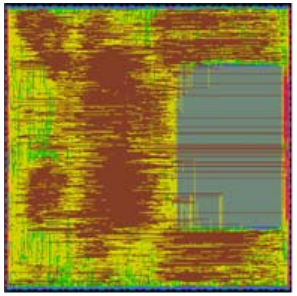
Design Flow





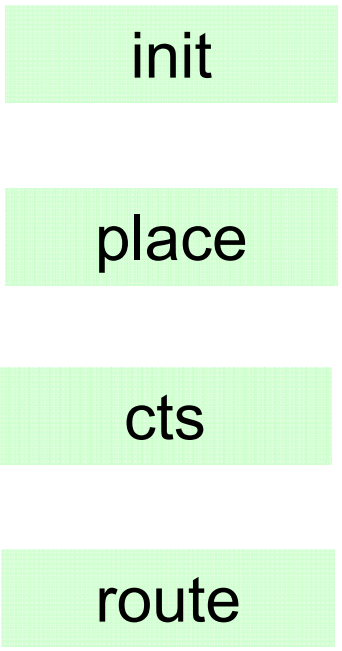






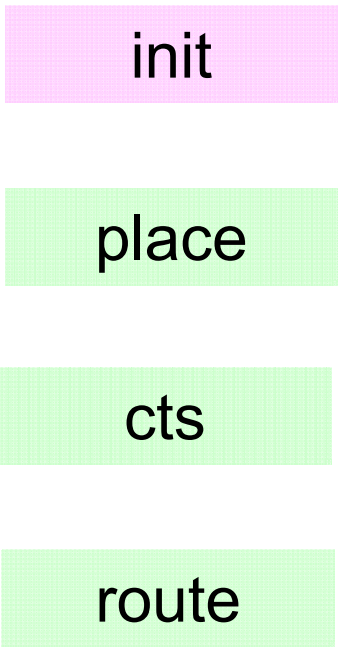
- We will touch all of these (but not necessarily in order!)

Baseline Flow



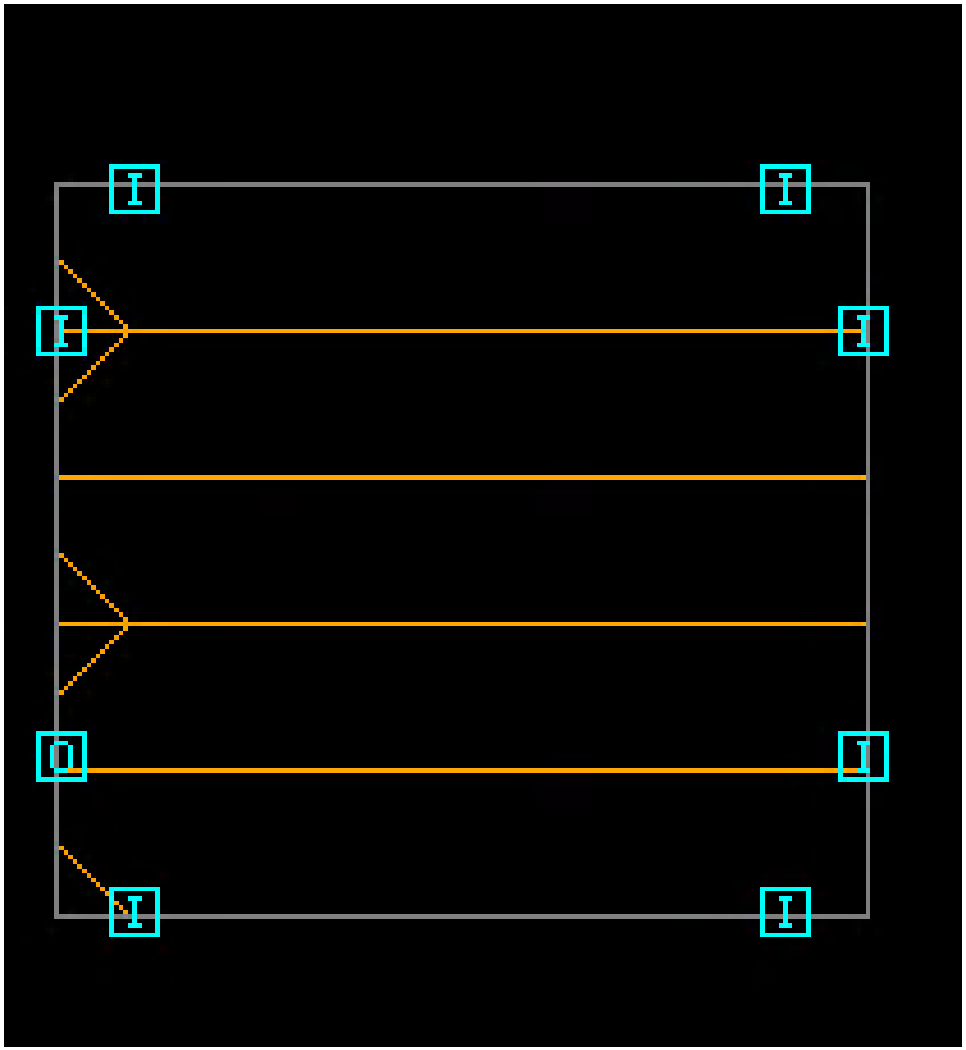
- Four steps
- Each in a separate Tcl script
- Best to run in batch mode
- Checkpoint saved at the end of each step
- dot-files used as targets & pre-requisites (*e.g.* .place, .cts)
  - MilkyWay files have colon in file-names
  - Use “touch .stepname” to re-run subsequent steps

Init Step



- Verilog netlist imported
- Specification of exact floorplan, or aspect ratio & density
- Power routing
- Timing Analysis

Init Step



Place Step

init

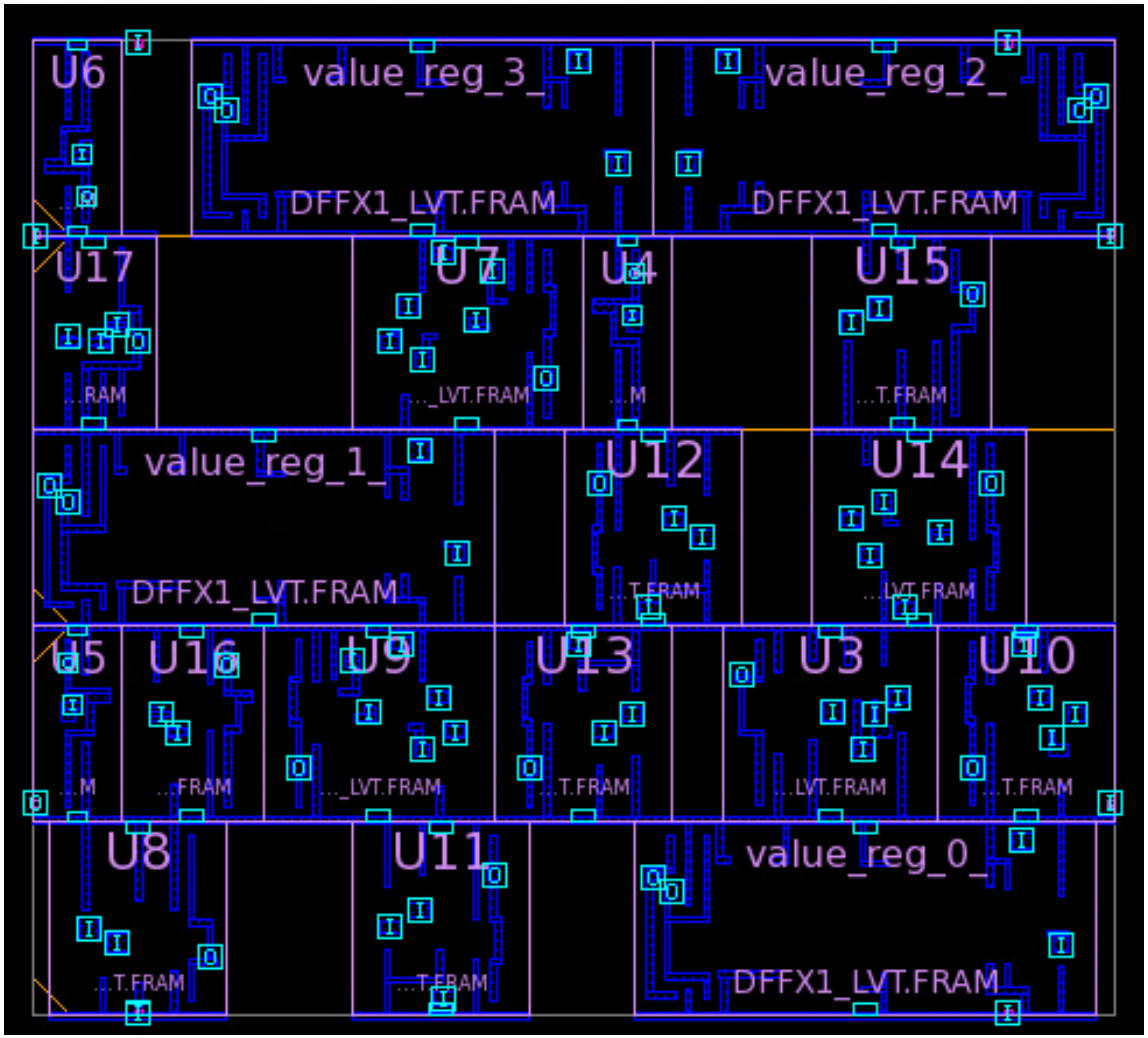
place

cts

route

- Standard-Cells placed

Place Step


U6
value_reg_3_
value_reg_2_
DFFX1_LVT.FRAM
DFFX1_LVT.FRAM
U17
U7
U4
U15
value_reg_1_
U12
U14
DFFX1_LVT.FRAM
U5
U16
U9
U13
U3
U10
U8
U11
value_reg_0_
DFFX1_LVT.FRAM

CTS Step

init

place

cts

route

- Clock-Tree Synthesized

Route Step

init

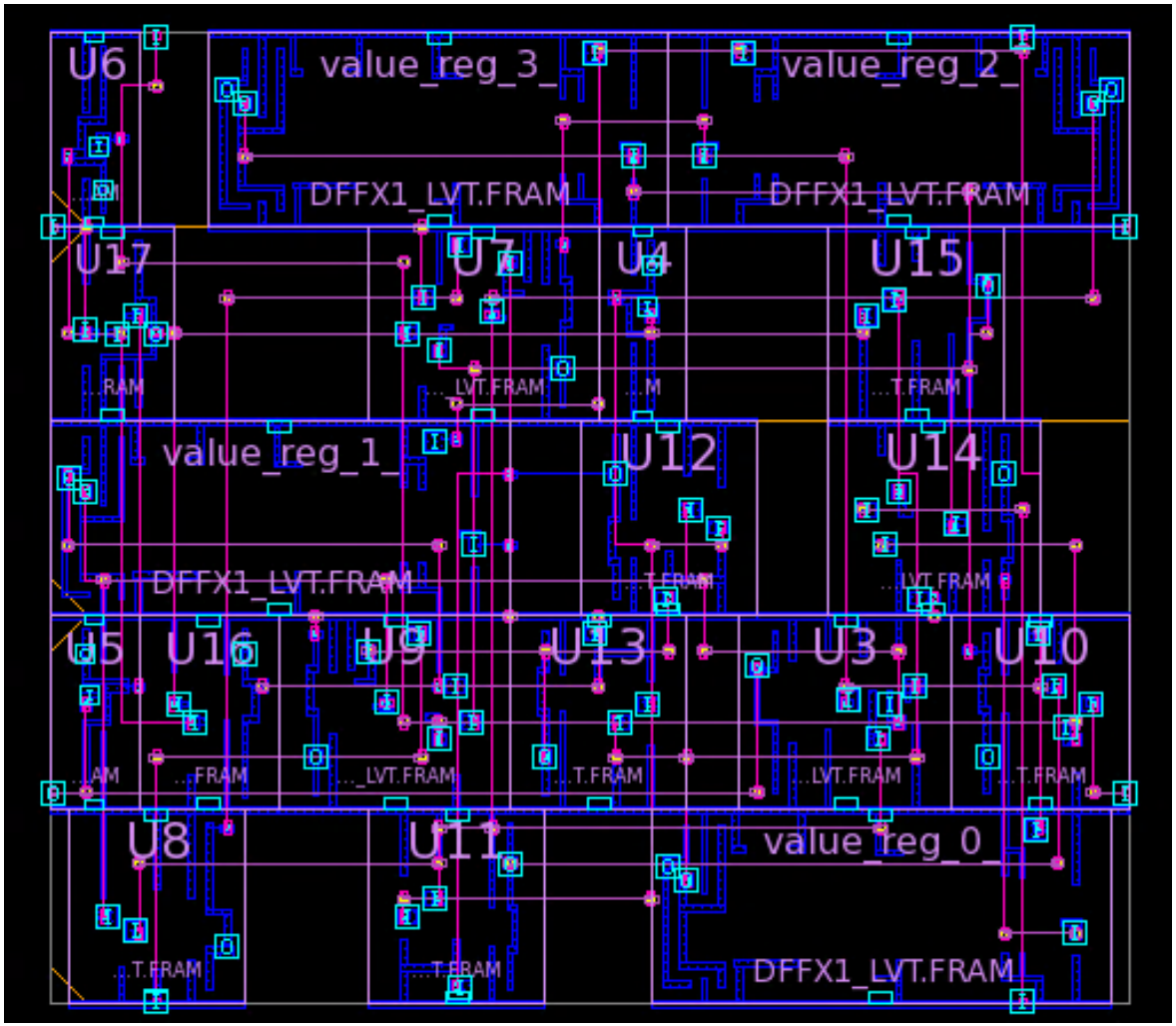
place

cts

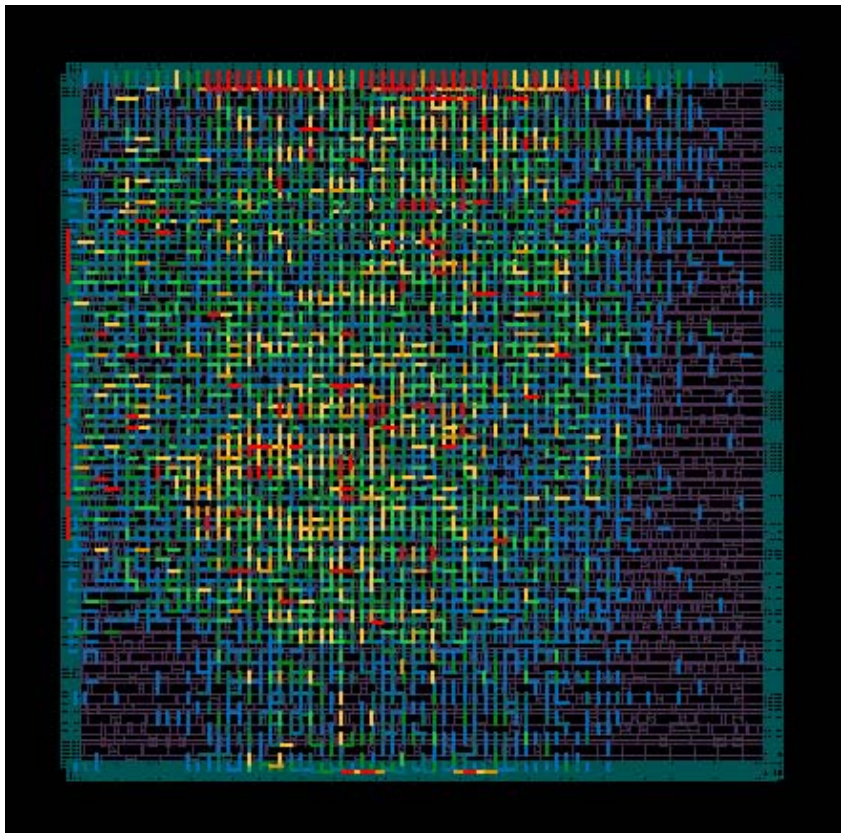
route

- Global Route Performed
- Detail Route Performed
- Power-Rings Connected
- Filler-Cells Inserted
- Parasitics Extracted
- Timing Analyzed
- Verilog Netlist & SPEF Files Created
- DEF File Created

Route Step


U6
value_reg_3_
value_reg_2_
DFFX1_LVT.FRAM
DFFX1_LVT.FRAM
U17
U7
U4
U15
value_reg_1_
U12
U14
DFFX1_LVT.FRAM
U5
U16
U9
U13
U3
U10
U8
U11
value_reg_0_
DFFX1_LVT.FRAM

Global vs. Detail Route



- Global route assigns wires to Global Routing Cells (GRCs)
- Not a final route, but a necessary step along the way
- Congestions markers show numbers of overflows

Counter Design Global Route

- *run_trialroute.log* file (things are going well)

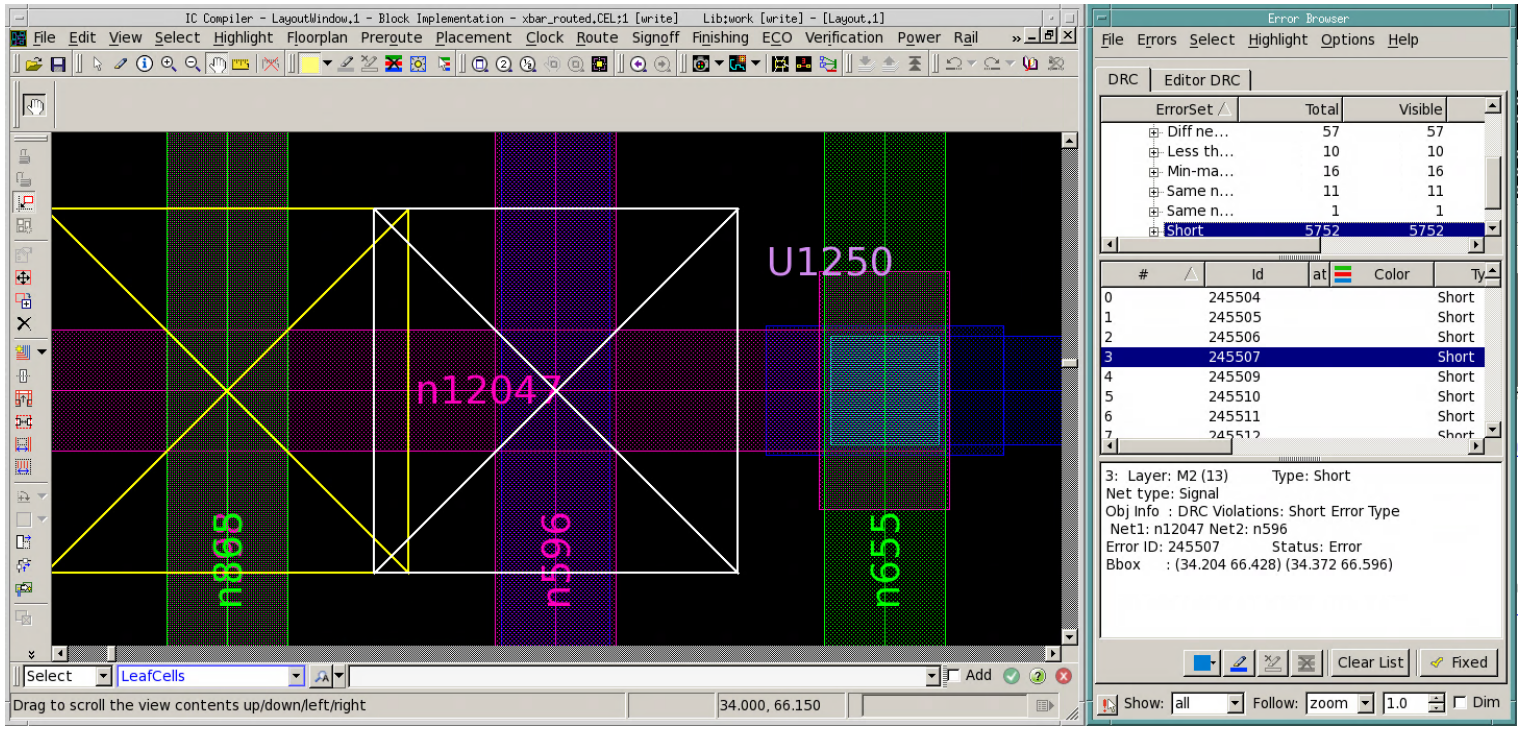
```
phase2. Routing result:
phase2. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
phase2. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M4         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M5         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M6         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M7         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M8         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M9         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. MRDL       Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
```

Crossbar Design Global Route

- *run_trialroute.log* file (things are not going well)

```
phase2. Routing result:
phase2. Both Dirs: Overflow = 14080 Max = 21 GRCs =  7553 (79.32%)
phase2. H routing: Overflow =  8495 Max = 13 (GRCs =  3) GRCs =  4385 (92.10%)
phase2. V routing: Overflow =  5585 Max = 21 (GRCs =  1) GRCs =  3168 (66.54%)
phase2. M1         Overflow =   477 Max = 13 (GRCs =  3) GRCs =   144 (3.02%)
phase2. M2         Overflow =  3367 Max = 21 (GRCs =  1) GRCs =  1702 (35.75%)
phase2. M3         Overflow =  6409 Max =  6 (GRCs = 12) GRCs =  3002 (63.05%)
phase2. M4         Overflow =  2217 Max =  9 (GRCs =  2) GRCs =  1466 (30.79%)
phase2. M5         Overflow =  1608 Max =  4 (GRCs =  4) GRCs =  1239 (26.02%)
phase2. M6         Overflow =     0 Max =  0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M7         Overflow =     0 Max =  0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M8         Overflow =     0 Max =  0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M9         Overflow =     0 Max =  0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. MRDL       Overflow =     0 Max =  0 (GRCs =  0) GRCs =     0 (0.00%)
```

Violations



- Goal of Detail-Route is to get number of design-rule violations to be zero
- Can use the error-browser to be sure

Counter Design Detail Route

- *run_route.log* file (things are going well)

```
Total number of nets = 29, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Information: Using 1 threads for routing. (ZRT-444)
Start DR iteration 0: uniform partition
Routed  1/1 Partitions, Violations =    0

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0
```

Crossbar Design Detail Route

```
Start DR iteration 3: uniform partition
Routed  1/49 Partitions, Violations =   12491
Routed  2/49 Partitions, Violations =   12493
Routed  3/49 Partitions, Violations =   12493
…
Routed  47/49 Partitions, Violations =  12684
Routed  48/49 Partitions, Violations =  12655
Routed  49/49 Partitions, Violations =  12655

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      12655
        Crossing top-cell boundary : 4
        Diff net spacing : 418
        Diff net via-cut spacing : 80
        End of line enclosure : 3
        Less than minimum area : 10
        Min-max layer : 103
        Same net spacing : 21
        Short : 12003
        Internal-only types : 13
```

- Routing a more congested design takes longer, more iterations, and may never complete

How do you solve this problem?

DEF Syntax

```
UNITS DISTANCE MICRONS 2000 ;
...
NETS 31 ;
...

- in[3]
  ( PIN in[3] ) ( U14 A1 )
  + ROUTED metal3 ( 98990 87500 ) ( 180110 * 0 )
    NEW metal3 ( 98990 87500 ) via2_5
    NEW metal2 ( 98990 87500 ) via1_7
 ;
- n35
  ( U5 ZN ) ( U4 A )
  + ROUTED metal3 ( 97090 81340 ) ( 98230 * ) via2_5
    NEW metal1 ( 95570 81340 0 ) ( 97090 * ) via1_7
    NEW metal2 ( 98230 81340 ) via1_4
    NEW metal3 ( 97090 81340 ) via2_5
 ;
...
END NETS
```