## Verilog code for Half Adder

```
module half_adder(
     input a,b
     output sum, carry
     );
assign sum= a^b;
assign carry = a & b;

endmodule
```

## Testbench code for Half Adder

```
module half_adder_tb;
reg a,b;
wire sum,carry;

half_adder_s uut(a,b,sum,carry);

initial begin
a = 0; b = 0;
#10
b = 0; b = 1;
#10
a = 1; b = 0;
#10
b = 1; b = 1;
#10
$finish();
end


endmodule
```

## Decoder Verilog code

```
module decoder

(
  input wire inp,
  output wire zero,
  output wire one
```

```
);

  assign zero = ~inp;   /*when input is 0 zero is 1 and vice
versa*/
  assign one = inp;

endmodule
```

Testbench for Decoder

```
module decoder_tb;
  reg inp;
  wire zero, one;


  decoder uut (
    .inp(inp),
    .zero(zero),
    .one(one)
  );

  // Test input values
  initial begin
    $dumpfile("decoder.vcd");
    $dumpvars(0,decoder_tb);
    inp= 0;
    #10;
    inp = 1;
    #10;
    $finish;


  end
endmodule
```