Ultra Low Power Low Frequency On-Chip Oscillator for Elapsed Time Counter

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***Abstract*— This paper presents a design of CMOS current starved inverter based oscillator which is used to drive the counters that act as a component in the elapsed time counter. A low power temperature independent biasing circuit is designed to enhance the performance meeting the frequency variations. The architecture includes usage of trim bits to shift the frequency at different process corners. Since the oscillator will run on a battery supply, variations in the performance of the oscillator across supply have been compromised. A 32.768 KHz oscillator is implemented in UMC180 CMOS technology, occupying a silicon area of 0.003064 mm². The oscillator consumes as little as 250 nW at room temperature, from 1.8 V power supply. A temperature stability of 454 ppm/ºC from 0ºC to 125ºC and variation of ±12 % with supply voltage from 1.7 V to 1.9 V is achieved.**

Keywords*— *Oscillator, on-chip, low power, temperature compensation, trim bits.

I. Introduction

Low power applications are the major demands of present digital world. Accurate clock generation which is independent of supply and temperature variation has been the main objective. Also in a technology driven world where the devices are shrinking day-by-day, compactness of the device is a major demand. Hence, generation of such low power clocks is a major issue of research.

Oscillators are an integral part of many electronic systems. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameters. Robust, high performance oscillator design in CMOS technology continues to pose interesting challenges [1].

The proposed oscillator design is used in the elapsed time counter product which is used to count seconds when power supply is applied [2]. Typically, an external crystal is used for clock generation, which becomes an input to the counter which continuously keeps the track of time. Increasing demand for on-chip devices motivates to design an on-chip oscillator as a replacement of external crystal to reduce bill of materials cost. Therefore the user has an option to switch between the external crystal and the on-chip clock. The variation in oscillator frequency should be as minimal as possible for all Process Voltage Temperature (PVT) conditions. Since the oscillator has to run on the battery supply, it has to consume very less current for longer battery life.

The objective of this research was to make an ultra-low power oscillator, with product requirements as below:

• A maximum current of 350 nA to be consumed from the battery supply.

• A frequency as close to 32.768 KHz to be obtained.

Organization of rest of the paper is as follows: Section II gives a brief description about a list of various architectures available to implement the idea. Section III discusses the proposed design where the specifications of the design along with the schematics and principles behind each block are explained. Results and discussions are dealt in Section IV with conclusions mentioned the in Section V.

II. Architecture Study

Based on the specifications given in Table II, following architectures of oscillator have been studied and simulated as discussed in further subsections.

A. Ring oscillator

Ring oscillator consists of odd number of CMOS inverters (shown in Figure 1) cascaded in a closed loop as shown in Figure 2. The frequency is very large, from hundreds of MHz to few GHz, for three stages [3]. Since the frequency is inversely proportional to number of stages, large number of stages must be cascaded, hence occupying large area on silicon. Since the architecture cannot limit the variations caused by change in process corners, the circuit is not implemented [4].

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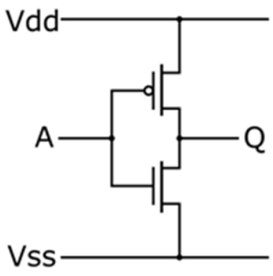

Fig. 1. CMOS inverter

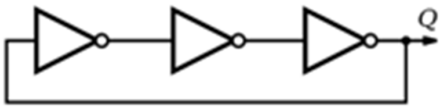

Fig. 2. Ring oscillator

B. CMOS thyristor based oscillator

A single CMOS thyristor element is shown in Figure 3. This element acts as a delay unit. The odd number of such thyristor elements are cascaded, which works as an oscillator as shown in Figure 4. Since the circuit operates on leakage currents, it draws very less power. But the frequency varies enormously as temperature changes. Hence the circuit is not implemented [5].

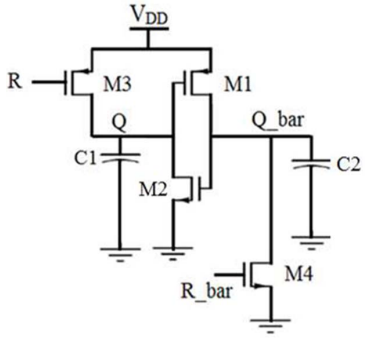

Fig. 3. CMOS thyristor element

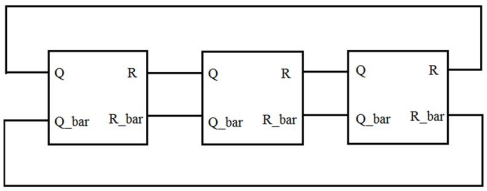

Fig. 4. CMOS thyristor based oscillator

C. Current starved inverter based oscillator

The rate of charging and discharging of output capacitor can be controlled by adjusting the amount of current flowing through it. This can be done by stacking extra MOSFETs biased at a particular voltage, thus working like a current source as shown in Figure 5. Hence the amount of current drawn from the battery supply can be significantly reduced. Also biasing the MOSFETs to allow very low current through them limits the number of stages. Also, the variations caused by change in process corner can be limited by adjusting the bias voltages. Hence this circuit is implemented.

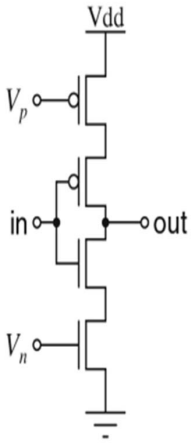

Fig. 5. Current starved inverter

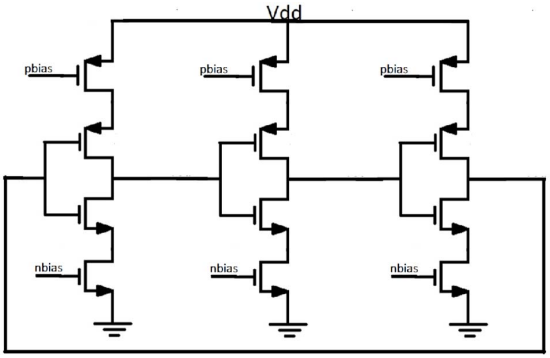

Fig. 6. Current starved inverter based oscillator

Table I summarizes the advantages and disadvantages of different architectures.

TABLE I. COMPARISON OF DIFFERENT ARCHITECTURES

Architecture	Advantages	Disadvantages
Ring oscillator	1. Simple to design.	1. Occupies large silicon area. 2. Large variations caused by temperature and process corners.
CMOS thyristor based oscillator	1. Consumes very less power.	1. Enormous variation in frequency due to temperature.
Current starved inverter based oscillator	1. Consumes less power when compared to ring oscillator. 2. Few stages are sufficient to achieve the required frequency.	1. Need to design a temperature compensated biasing circuit.

III. PROPOSED OSCILLATOR DESIGN

The main objective of the design is that it should consume less power and exhibit minor variations in frequency of oscillation with respect to variations in PVT conditions. This is achieved by making use of current starved inverter based architecture.

Figure 7 reveals the block diagram of on-chip oscillator comprising of temperature compensated biasing circuit, chain of current starved inverters and output buffer as blocks.

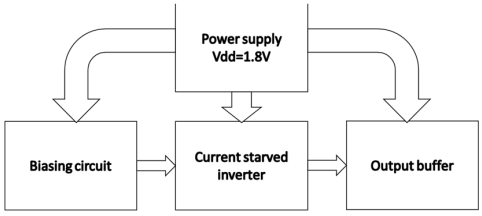

Fig. 7. Block diagram of current starved inverter based oscillator

A. Design Specifications

Table II shows the design specifications of the oscillator to be met.

TABLE II. OSCILLATOR SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Frequency	22.937	32.768	42.598	kHz
Duty cycle	40	50	60	%
Supply Current	---	---	350	nA
Power supply	1.7	1.8	1.9	V
Leakage current	---	---	100	nA
Temperature range	0	27	125	ºC

The oscillator frequency should have a maximum variation of ±30% and consume current less than 350 nA from the battery supply, meeting the variations of temperature ranging from 0ºC to 125ºC, at different process corners (tt, ss, ff, snfp, fnsp) as well.

B. Biasing Circuit

Biasing circuit is the first block of the current starved inverter based oscillator. Biasing circuit is required to control the amount of current flowing through the current starved inverters, which eventually decides the frequency stability of the oscillator. MOSFETs used in diode connected configuration shown in Figure 8 operate in subthreshold region of operation. The current through the subthreshold MOSFETs increases exponentially as temperature increases, this is because threshold voltage V_T decreases linearly with temperature, and the subthreshold current is given as

$$I_D = I_0 e^{\left(\frac{V_{GS}-V_T}{mKT}\right)} \quad \text{(1)}$$

To cancel temperature dependency, stacking of MOSFETs operated in triode region is necessary, where current decreases with temperature.

$$I_D = \mu C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \text{(2)}$$

Therefore, for small V_{DS}, I_D varies linearly with V_{DS}, behaving like a resistor whose resistance is given as

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)} \quad \text{(3)}$$

Even though, in triode region V_T decreases by 2mV/°C rise in temperature, mobility decreases with temperature given by $\mu \propto T^{-1.5}$ due to lattice scattering in the silicon crystal whose effect dominates over that of the V_T, causing R_{on} to increase with temperature [6]. From (1) and (2), it is clear that rate of increase in subthreshold current with respect to temperature is greater than rate of decrease in triode current with respect to temperature, hence large number of triode operated MOSFETs are cascaded when compared to subthreshold operated MOSFETs. Since μ_n is greater than μ_p, R_{on} for PMOS is greater than that of NMOS. Hence less number of triode operated PMOS are enough when compared to triode operated NMOS. Therefore, the increase in subthreshold current is balanced by the decrease in triode current, hence obtaining a temperature independent bias. Large change in V_T across different process corners causes large change in biasing current as shown in Figure 13. This henceforth causes large change in oscillator frequency as shown in Figure 14.

Hence trim bits are designed to control the amount of biasing current. Three trimming MOSFETs with inputs D0, D1 and D2 are designed to shift the frequency closer to 32.768 KHz at different process corners. Sizing of the MOSFETs are decided based on the simulation results as shown in Figure 15. The complete schematic of the biasing circuit is shown in Figure 8.

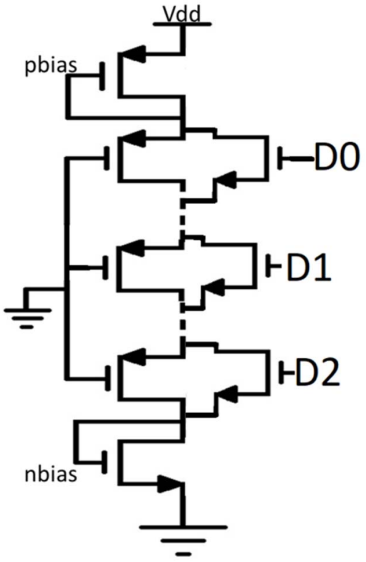

Fig. 8. Biasing circuit

C. Current starved inverter

In conventional CMOS ring oscillator, charging and discharging time of output capacitor is very low. This is because the amount of current is very high, hence ring oscillators produces clock of very high frequencies ranging from hundreds of MHz to few GHz, and also consume high power in the order of few µW. Frequency around 32.768 KHz can be obtained using ring oscillators, but there is no measure to reduce the variations caused by change in process corner.

Hence current starved inverters topology is preferred where the rate of charging and discharging of output capacitor can be controlled by limiting the amount of current flowing through it. The current through biasing circuit is mirrored using PMOS and NMOS current mirrors into the current starved inverters. This limits the rate of charging and discharging of the output of the inverter. Also by limiting

the current drawn from the battery supply the oscillator consumes very less power. Also the number of stages of current starved inverters is very less when compared to ring oscillator.

The frequency of oscillation for the oscillator is calculated using the equation as shown below:

$$f = \frac{1}{2N\tau_D} \text{ ——————————(4)}$$

Where, N is number of delay cells in the ring and τ_D is the delay time of each cell. To obtain a frequency around 32.768 KHz, nineteen stages are sufficient.

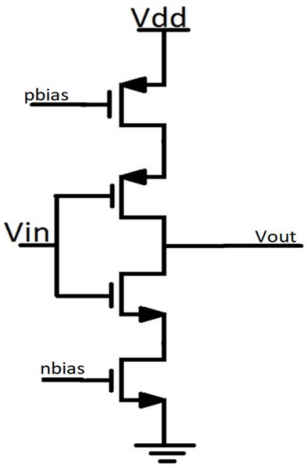

Fig. 9. Current starved inverter

D. Output buffer

The output of current starved inverter chain has large rise and fall delay. This is because the current required to charge and discharge the output capacitor is limited by the starving MOSFETs. The output buffer provides sufficient amount of current, so as to get a steep rise and fall. Hence output buffer is used to get a proper square wave.

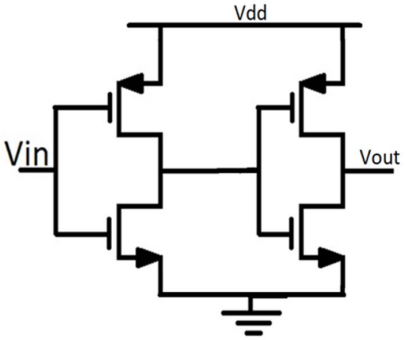

Fig. 10. Output buffer

E. Proposed schematic

The complete schematic of proposed current starved inverter based oscillator is shown in Figure 11. Current through the biasing circuit generates a biasing voltage. This voltage is used to bias the starving MOSFETs of the current starved inverter chain. Here there are nineteen current starved inverters cascaded in a closed loop. The output of the inverter chain goes to the buffer whose output is a clean square wave.

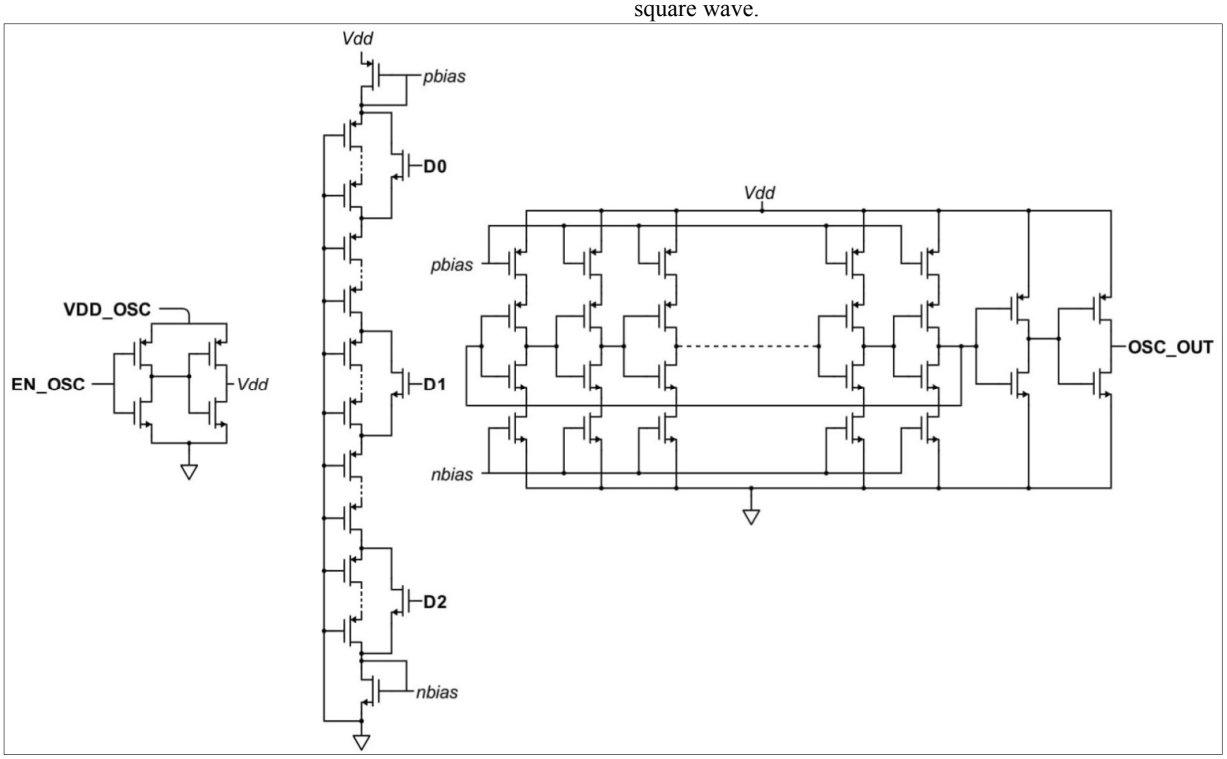

Fig. 11. Proposed schematic of oscillator

IV. Simulation Results

The circuit is simulated using spectre simulator and the output waveforms as shown in Figure 12.

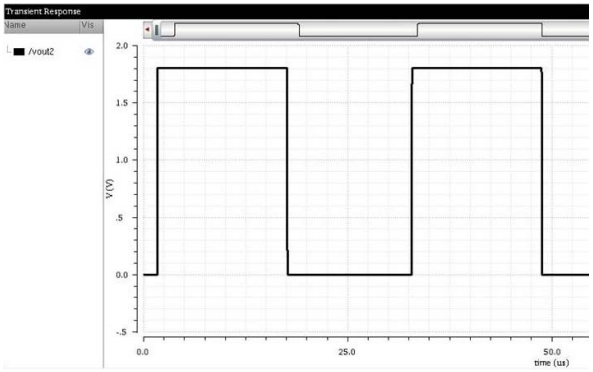

Fig. 12. Oscillator output

The variation in biasing current, after post layout parasitic extraction, without trimming, i.e. D0=D1=D2=0, across temperatures from 0ºC to 125ºC, at 1.8 V supply at different process corners is shown in Figure 13.

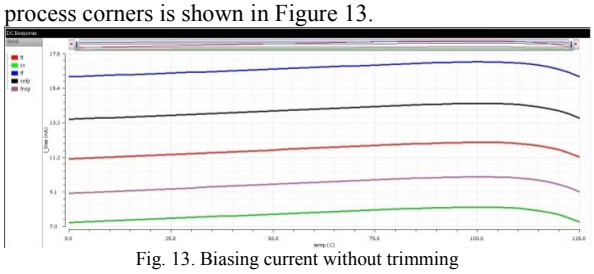

Fig. 13. Biasing current without trimming

The frequency of oscillation is obtained at temperatures from 0ºC to 125ºC, after post layout parasitic extraction, at 1.8V power supply, at different process corners, without trimming the oscillator, i.e. D0=0, D1=0, D2=0, as shown in Figure 14.

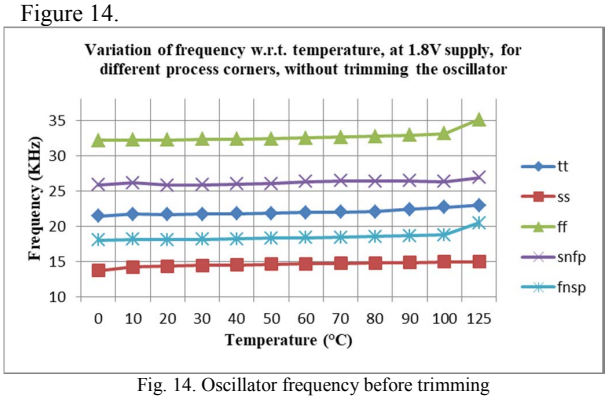

Fig. 14. Oscillator frequency before trimming

The oscillator is later trimmed using trim bits (D0 D1 D2), and the biasing current and the frequency are obtained at temperatures from 0ºC to 125ºC, after post layout parasitic extraction, at 1.8V power supply, at different process corners, as shown in Figure 15 and Figure 16 respectively.

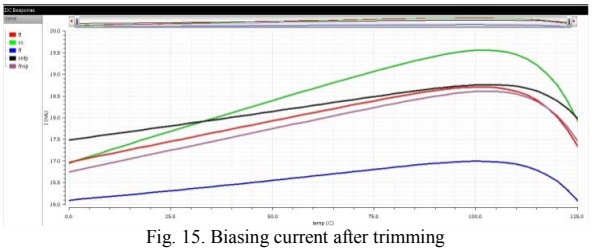

Fig. 15. Biasing current after trimming

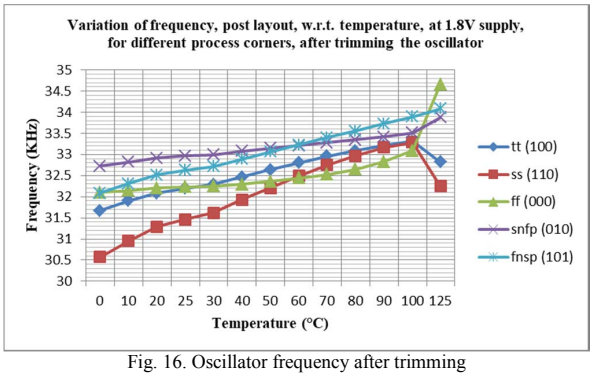

Fig. 16. Oscillator frequency after trimming

Table III summarizes the variation in oscillator frequency across temperatures from 0ºC to 125ºC, at 1.8 V supply, mentioning the trim bit combinations.

Table III. VARIATION IN FREQUENCY ACROSS TEMPERATURES

Sl. no	Process corner	Trim bits D[0]D[1]D[2]	Variation of frequency (in %) w.r.t temperature from 0ºC to 125ºC at 1.8V supply w.r.t 32.768 KHz
1	tt	1 0 0	-3.35% to +1.65%
2	ss	1 1 0	-6.71% to +1.59%
3	ff	0 0 0	-2.04% to +5.77%
4	snfp	0 1 0	-0.12% to +3.39%
5	fnsp	1 0 1	-2.07% to +4.00%

As shown in Figure 17, average current consumed from the battery supply is plotted across temperatures from 0ºC to 125ºC at 1.8 V supply. Even at different trim bit settings, average current is less than 250 nA.

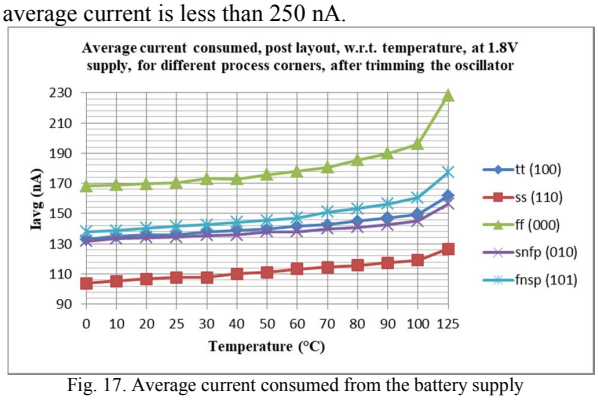

Fig. 17. Average current consumed from the battery supply

The layout of the oscillator is implemented using Cadence Virtuoso Layout Editor. The design consumes an area of 0.003064 mm². The complete layout is shown in Figure 18.

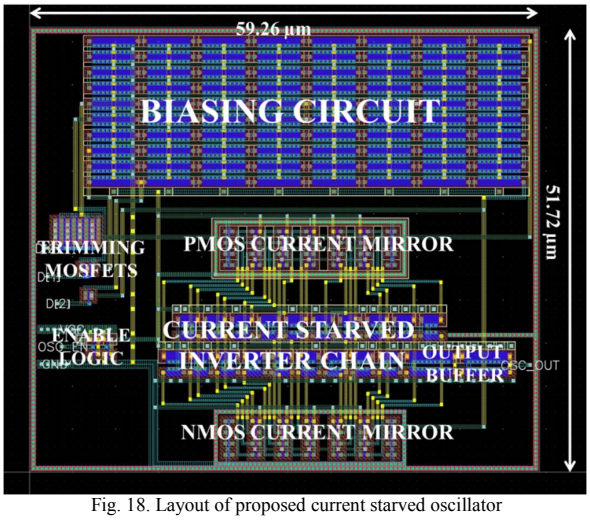

Fig. 18. Layout of proposed current starved oscillator

V. Conclusion

The low power, low frequency on-chip oscillator for elapsed time counter application is implemented in UMC180 CMOS technology. The frequency variation is ±30% without trimming the oscillator. After trimming the oscillator, a temperature stability of 454 ppm/ºC from 0ºC to 125ºC and variation of ±12 % with supply voltage from 1.7 V to 1.9 V is achieved. The average current drawn from the battery supply is less than 350 nA for all conditions. A new low power, temperature compensated biasing circuit has been successfully implemented.

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