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Comparative Study of Analog Matching Structures in 28FDSOI

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Abstract— **Matched devices are extensively used in analog designs, such as differential amplifiers and current mirrors. This paper discusses various competing matching topologies. Paper considers the usage and limitations of SPICE simulations in order to evaluate matching performance. A test structure comprising of several matching structures was developed and fabricated in STMicroelectronics' 28FDSOI technology.**

Keywords— matching, common centroid, current direction, standard deviation

I. Introduction

A lot of efforts have been made to the study of mismatch and layout strategies. Literature studies show that the causes of mismatch can be categorized as systematic and random variations. The random variations are modeled by zero mean Gaussian distribution and tradeoffs can be made between area and matching accuracy while the systematic variations are process dependent and usually modeled as spatial gradients in device parameters.

II. TEST STRUCTURES

In order to study the effects of device orientation, spatial distance and performance of different common centroid structures, 14 NMOS (egnfet) were placed across the test chip in 7 pairs.

Each device pair consists of a pattern of two NMOS devices, each having two fingers of width, W=10µm and length, L=1µm. All devices share their gate terminal which is connected to IO pad.

A. Structure 1

This structure is shown in Fig. 1.a. The NMOS devices are placed in a common-centroid configuration. Each row contains a finger of each device. The source-drain terminals of the devices placed in second row are flipped, so as to have opposite current flow direction through devices placed in second row.

B. Structure 2

This structure is shown in Fig. 1.b. The structure is similar to structure 1, except for the orientation of source and drain of device among both rows. In this structure source-drain terminals of device in both rows were kept in same orientation, so the current through devices in each rows flows in same direction.

C. Structure 3

This structure is shown in Fig. 1.c. In both rows sources of the two devices are merged together. In this structure direction of current flow among devices present in same row is opposite to each other.

D. Structure 4

This structure is shown in Fig. 1.d. As opposed to above three structures, this is not a common centroid structure. In this structure both fingers of one device were placed parallel to each other in one row and that of second device in other row. The source-drain terminals of each device were placed in same orientation.

E. Structure 5

This structure is shown in Fig. 1.e. This structure is similar to structure 4. But the devices in this structure were rotated by 90º.

F. Structure 6/7

These structures are shown in Fig. 2. Here two MOS were placed near to each other having horizontal and vertical gate orientation. Both MOS had two fingers in one row only.

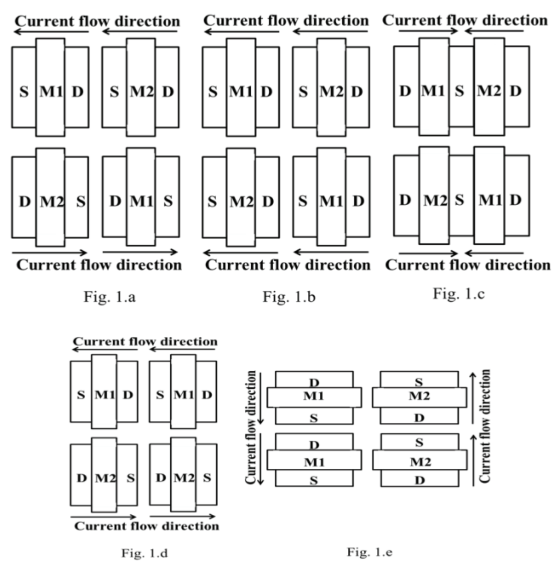

Fig. 1. Test Structures

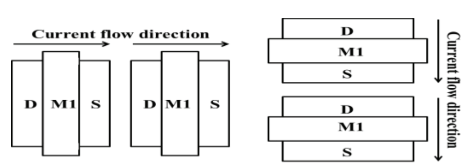

Fig. 2. Corner Structures

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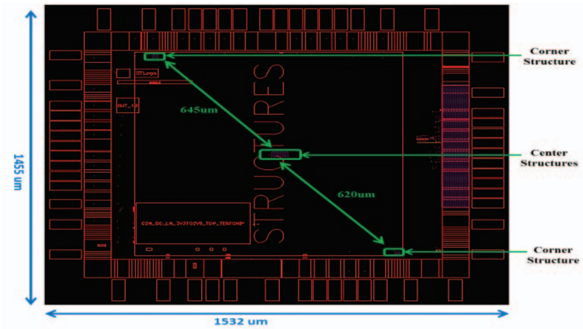

Fig. 3 Chip Overview

III. TEST PROCEDURE

One NMOS out of 14 is selected as the reference NMOS. Its drain terminal is connected to the gate terminal (diode configuration). The gate of reference NMOS is shorted with all other NMOS gates. A current of known value is forced in this diode connected NMOS by the precision tester. The schematic of test pattern is shown in Fig. 4. Table 1 shows the test procedure details.

TABLE 1 TEST PROCEDURE DETAILS

No. of Dies tested	22
No. of structures tested	7
Current range	1nA, 10nA, 100nA, 1uA, 5uA, 10uA, 20uA & 100uA

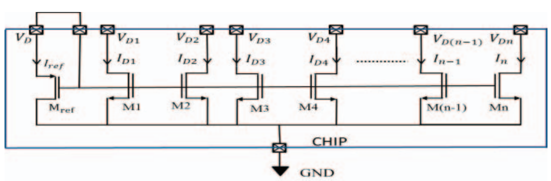

Fig. 4 Schematic of test pattern

IV. MEASUREMENT RESULTS AND DISCUSSION

The analysis and the results are discussed in this section. Monte-Carlo simulations are run on these structures and results are aligned with silicon results.

A. Units Variation with spatial distance

It is observed that matching is good if matching pairs are equidistant from center of die. Variation is not linear. It varies from center of die towards periphery.

B. Variation with device orientation

I. As expected the mismatch in the device with different gate orientation is high. It is observed that mismatch has a directional property. The deviation with different gate orientation is high. The deviation increases diagonally.

TABLE 2 STANDARD DEVIATION OF DIFFERENT ORIENTED DEVICE

Structure	Standard deviation	Average value
Structure 6	0.04785	0.9688
Structure 4	0.05193	0.9956
Structure 5	0.05269	1.008
Structure 7	0.05404	1.014

C. Common centroid verses non-common centroid

Common centroid results were better than any other matching. In common centroid, structures placed is Structure 1, Structure 2 and Structure 3 (shown in Fig.1.a, Fig.1.b and Fig.1.c). Two non-common centroid structures were Structure 4 and Structure 5 (shown in Fig.1.d and Fig.1.e) referring to the table 1 it is clear that common centroid pair (1, 2, 3) have better matching (lower standard deviation) than non-common centroid structures (4 ,5).

TABLE 3 STANDARD DEVIATION OF CENTRE STRUCTURES

Test Structure	**Standard Deviation**
Structure 1	0.03943
Structure 2	0.03427
Structure 3	0.03872
Structure 4	0.05315
Structure 5	0.04894

D. Impact of current direction in Common centroids

Structure 1, Structure 2 and Structure 3 comes under this category. As shown in Table.1, Structure 2 with same current direction has lesser mismatch as compared to structure 1 and 3 which are having different current direction in both rows.

E. Matching with current values

All the 7 structures were tested and it was observed that as the reference drain current increases, whatever be the matching pattern, drain current ratio of two matched devices tends to be 1. With the increase of reference drain current, if current ratio of matched devices was more than 1 at low reference current, its value decreases to reach 1 and if it is less than 1, its value increases to reach the value of 1.

V. CONCLUSION

Standard deviation of current values in matched structures is measured. It is observed that common centroid structure with devices having same current direction has better matching among all the tested structures. Current direction, spatial distance and device gate orientation has expected impact on the matching.