Message from the Steering Committee Chair

Our long-time associate Nagarajan Ranganathan (known to us as Ranga) passed away in Tampa, Florida, USA on October 25, 2018. Wife Radhika, daughter Sheela and son Shiva survive him. *We will miss you, Ranga.*

I first met Ranga in January of 1991 on a flight to USA after attending the *Fourth International Conference on VLSI Design* in New Delhi. He was returning to Tampa where he taught at the University of South Florida (USF). From that day onward, he maintained a close association with the Conference, playing key roles such as those of general chair and program chair. He served on the Steering Committee from 1992. *We feel Ranga's absence.*

The Conference, VLSID as we call it, and Ranga were a perfect match. Everything about Ranga was "VLSI". He graduated from the National Institute of Technology, Tiruchirapalli, India and obtained a PhD from the University of Central Florida, Orlando, USA. In 1988, He joined USF, finally rising to the position of Distinguished University Professor in the Department of Computer Science and Engineering. His areas of research were VLSI circuits and systems design, VLSI design automation, computer architecture, low power design, reversible logic, nano-architectures, hardware algorithms, parallel processing, data compression, and VLSI for vision, video, image processing and pattern recognition. He wrote four books, held ten patents and published over 300 papers. He received a large number of awards, medals and recognitions. He was a member of the VLSI Society of India. In 2002, he was elected a Fellow of the IEEE for contributions to algorithms and architectures for VLSI systems design. He was Editor-In-Chief (2003-2006) of *IEEE Transactions on VLSI Systems*. He chaired the IEEE Computer Society's Technical Committee on VLSI (TCVLSI). His professional contributions are very significant, and too numerous to list here. *The field of VLSI will remember Ranga for years to come.*

After a gap of ten years, the joint conference returns to New Delhi, India, as *32nd International Conference on VLSI Design* and *18th International Conference on Embedded Systems.* It is truly an effort of volunteers from industry and academia. Leading a large team of organizers are Sanjay Gupta of NXP Semiconductors, Preet Yadav of Wipro Limited and Preeti Ranjan Panda of IIT-Delhi. We are thankful to

our sponsor VLSI Society of India (VSI), collaboration partner IESA, technical co-sponsors, IEEE (CAS, CEDA, CPS, CS, TCVLSI and TTTC) and ACM (SIGDA and SIGMICRO), and Industry supporters, NXP, Qualcomm, Intel, Cadence, Mentor and others, for their contributions to the conference.

Following a theme, "Autonomous Intelligence for a Safe, Secure and Smart World," the Conference offers tutorials on January 5 and 6, and keynote and regular papers on January 7, 8 and 9. Additional features are PhD Forum, Startup Forum, Industry Forum, Women in Engineering Forum, Panel Discussions, User/Designer Track, Design Contest, Hackathon, Cultural Evening and not to be missed Industry Exhibits.

The conference venue New Delhi is the capital of India. Once there, you may explore the surrounding area known as NCR (National Capital Region). It consists of Delhi, New Delhi, Faridabad, Gurgaon, Ghaziabad, Noida and a few other neighboring cities. The NCR is going through rapid industrial and urban development. It also contains a number of historical and scenic spots.

Looking into the future, the *Twenty-third International Symposium on VLSI Design and Test* (VDAT) will take place at Indore, Madhya Pradesh, India during July 2019. Next, the *Thirty-third International Conference on VLSI Design* and *19th International Conference on Embedded Systems* will come together at Bengaluru in January 2020.

With warm regards,

Vishwani D. Agrawal

Chair, VLSI Design Conference Steering Committee
December 7, 2018