IIP3 Improvement in Subthreshold LNAs using Modified Derivative Superposition Technique for IoT Applications

Anant Rungta
Department of Electrical & Electronics Engineering
Birla Institute of Technology & Science
Pilani, Rajasthan, India
rungta34@gmail.com

Kavindra Kandpal
Department of Electrical & Electronics Engineering
Birla Institute of Technology & Science
Pilani, Rajasthan, India
kavindra.kandpal@pilani.bits-pilani.ac.in

***Abstract*—This paper proposes a linearization technique for third-order input intercept point (IIP3) improvement in subthreshold low noise amplifiers (LNAs). The proposed LNA is designed for 2.4 GHz radio-frequency wireless receiver front-ends for Internet of Things (IoT) applications. A novel modified derivative superposition technique is presented for the linearization of subthreshold LNAs. In this technique, the main transistors are biased in the weak inversion region, while the auxiliary transistor in the feed-forward path is biased in the strong inversion region, for third-order non-linearity cancellation. With a DC power consumption of 503 µW from a supply voltage of 0.9 V, the LNA delivers an IIP3 of -0.77 dBm, a noise figure of 2.42 dB, and 12.36 dB of power gain. The LNA was designed using UMC 90 nm RF CMOS technology.**

Keywords— Low noise amplifier, subthreshold biasing, nonlinearity, third-order input intercept point (IIP3), derivative superposition.

I. INTRODUCTION

With the advent of the Internet of Things (IoT), there is a demand for sophisticated wireless communication. This requires wireless devices to be extremely energy efficient, while also delivering excellent noise and linearity performance. IoT devices are often battery powered, hence they need to consume minimal power for longer battery lifespan. This necessitates the minimization of power consumption of the individual RF blocks in IoT transmitters and receivers. The communication protocols popularly used in the transmission of data between proximate IoT and wearable devices are Bluetooth, NFC, Zigbee, and Wi-Fi, which typically operate in the 2.4 GHz radio-frequency band [1].

Traditionally, LNAs have been designed with their main transistors operating in the strong inversion region. However, it has been established that transistors operating in the subthreshold region achieve a higher transconductance to current ratio (g_m/I_D) than those biased in the strong inversion region [2]. It has also been reported that moderate to weak inversion region is the optimum region for biasing common source (CS) LNAs for obtaining the best noise and gain performance [3]. Thus in the last decade, many subthreshold LNAs have been designed [3]-[10]. However, in the design of subthreshold LNAs, the biggest design challenge faced is the high nonlinearity, which is measured in terms of its third-order input intercept point (IIP3). Higher IIP3 is desirable in IoT receiver front-ends to ensure that the expected performance is delivered even at high input signal power levels.

Although various linearization techniques for strong inversion LNAs have been reported [11], they cannot be used directly for the linearization of subthreshold LNAs. In these techniques, the main transistor of the LNA operates in the strong inversion region, while the auxiliary transistor, if any, operates in the weak inversion region. The third-order harmonic coefficients of the MOSFETs in the strong inversion and weak inversion regions of operation are opposite in polarity, and therefore the superposition of these two regions minimizes nonlinearity. However, these conventional techniques in [11] need to be modified if the main transistor is operating in the weak inversion region, because of the opposite polarities of the third-order coefficients, as mentioned earlier.

A couple of linearity improvement techniques for subthreshold LNAs have been previously reported. H. S. Jhon et al. [5] have employed the multiple gated transistor technique (MGTR) for subthreshold LNAs, in which the input to the main transistor's gate is also an input to the gate of an auxiliary transistor for nonlinearity cancellation. The active auxiliary path, however, consumes additional DC power. C. H. Chang et al. [4], [6] have proposed a linearization technique in which extra passive components are employed for the cancellation of non-linearity, without the need for a power consuming auxiliary path.

S. Ganesan et al. [12] have proposed a modified derivative superposition technique for the linearization of strong inversion LNAs. In this work, this modified derivative technique is adapted for subthreshold LNAs. In the proposed technique, the main transistor is biased in the weak inversion region and the auxiliary transistor is biased in the strong inversion region. The concept of linearization is the same as in [12]. However, it provides several other advantages like higher g_m/I_D, lower DC power consumption, and better overall performance. Derivative superposition has not been previously employed for the linearization of subthreshold LNAs. The circuit topology that is being used in this work is the inductively-degenerated cascode common source amplifier, which is optimized for superior noise figure and input-matching [13]. An auxiliary feed-forward path is added across the input transistor, which is responsible for the third-order nonlinearity cancellation.

The paper is organized as follows. Section II reviews the modified derivative superposition technique and presents the proposed linearization technique for IIP3 improvement in subthreshold LNAs. Section III presents the results for the linearized subthreshold LNA design and compares its performance with previously reported designs. Section IV concludes the findings of this work.

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00041

II. LINEARIZATION TECHNIQUE

The derivative superposition (DS) linearization technique used in strong inversion LNAs is based on the concept of harmonic cancellation of third-order harmonic terms, exploiting the fact that transistors operating in strong inversion (SI) and weak inversion (WI) have opposite third-order transconductance coefficients (g_3) [11]. In conventional linearization techniques, the main transistors are biased in the SI region, while the auxiliary transistor is biased in the WI region. The transistors are biased such that the positive peak in the third-order nonlinearity of the main transistor and the negative peak in that of the auxiliary transistor get aligned, for maximum harmonic cancellation of the third-order intermodulation (IM3) terms, and thus for the resultant improvement in IIP3.

In Fig. 1, the transfer characteristics of a unit sized MOSFET in a standard CMOS process is shown. I_D is the drain current of the MOSFET. g_1 is the first-order transconductance of the MOSFET measured in A/V, while g_3 is the third-order transconductance of the MOSFET measured in A/V^3. The drain current plot for gate-source voltages (V_{GS}) swept from 0 V to 1 V is differentiated to obtain the g_1 plot. The g_3 plot is obtained by taking the derivative of g_1 twice. As it can be observed from the plot, g_3 goes from a positive value to a negative value as V_{GS} increases. g_3 has a positive peak in the weak-inversion region of operation of the transistor, while it has a negative peak in the strong-inversion region of operation. Therefore, a superposition of signals from transistors in the two regions of operation can possibly lead to cancellation of the third-order non-linearity in the circuit.

In Fig. 2, the circuit topology for the modified derivative superposition technique presented in [12] is shown. The auxiliary transistor (M_B) operates in WI region and is connected in a parallel with the main transistor (M_A). The inductor L_B is employed to tune the third-order

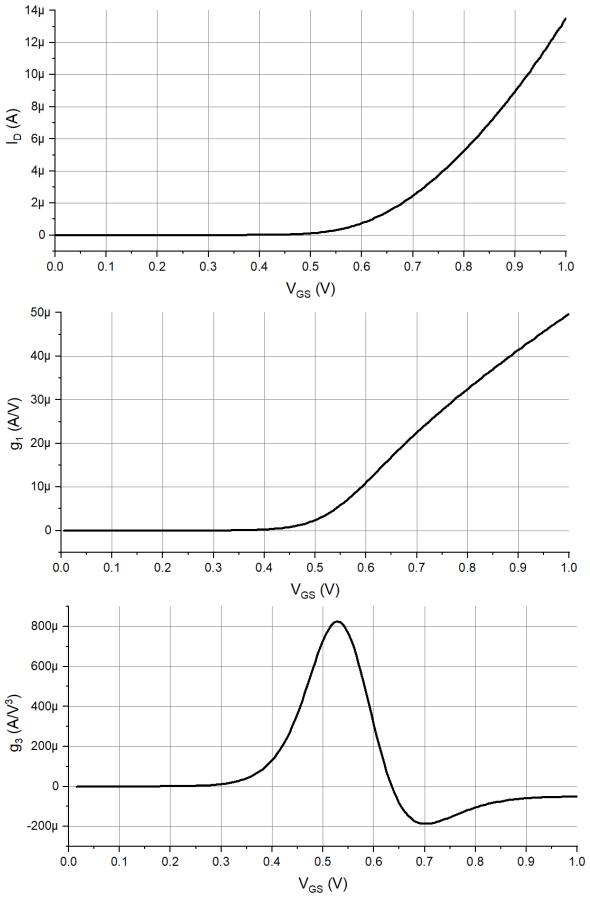

Fig. 1. MOSFET transfer characteristics.

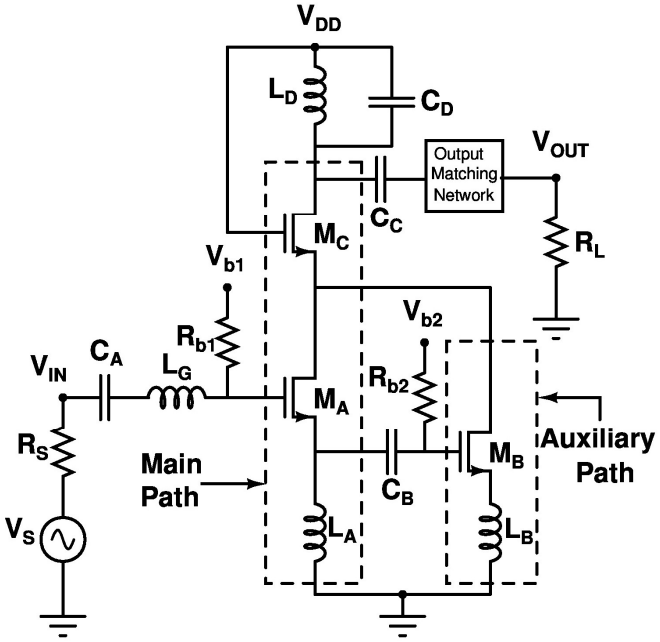

Fig. 2. Proposed LNA Circuit Topology.

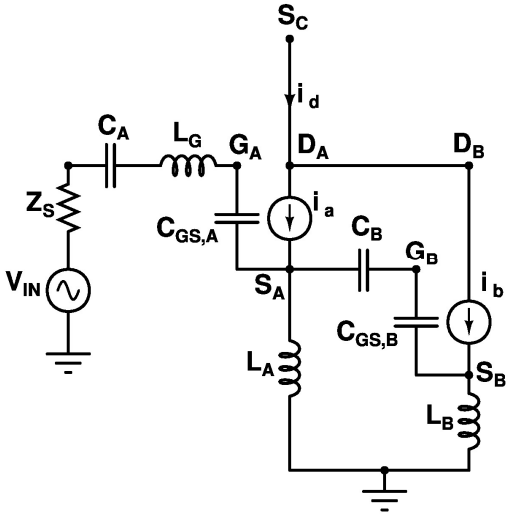

Fig. 3. Small-Signal Model of the proposed LNA.

intermodulation (IM3) terms of the auxiliary path, for achieving the optimum IIP3. V_{b1} and V_{b2} are the DC bias voltages of the main and auxiliary transistors respectively. The capacitor C_B couples the AC signal from the main signal path as an input to the auxiliary transistor. The drain current of the auxiliary transistor superimposes the third-order derivative terms with the main signal.

The voltage to current conversion action of the MOS transistor is responsible for its nonlinearity. The gate-to-source voltage (v_{GS}) to drain current (i_D) transfer function of the two transistors is given by (1). The IIP3 of such a setup is given by (2) [12].

$$i_D = g_1 v_{GS} + g_2 v_{GS}^2 + g_3 v_{GS}^3 \tag{1}$$

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|} \tag{2}$$

Where g_1, g_2, and g_3 are the first, second and third order transconductance coefficients respectively.

The equivalent small-signal model of the circuit is illustrated in Fig. 3. Using Volterra series expansion and two-tone harmonic input analysis [12], the expression of the IIP3 is obtained as follows.

$$IIP3 = \frac{1}{6\mathrm{Re}(Z_S(s))|A_1(s)|^2}\left\{\frac{g_{1a}}{\varepsilon}\right\} \tag{3}$$

$$\varepsilon = g_{3a} - \frac{g_{2a}^2}{3g_{1a}} + g_{3b}n(s)|n(s)|^2\frac{2+s^2L_BC_{GS,B}}{2(1+s^2L_BC_{GS,B})} \tag{4}$$

$$n(s) = \frac{sL_A(g_{1a}+sC_{GS,A})}{1+sC_{GS,B}(sL_A+sL_B)} \tag{5}$$

$$A_1(s) = \frac{1+s^2C_{GS,B}(L_A+L_B)}{2s^2L_AC_{GS,A}(1+s^2L_BC_{GS,B})} \tag{6}$$

From (3), it can be inferred that the term g_{3b} can be adjusted for obtaining a high IIP3 value. The sizing of transistor M_B is tuned to fix the appropriate magnitude of g_{3b}, while the value of L_B is varied to set its argument, to achieve the optimum IIP3.

The entire analysis which has been explained above is also valid if the region of operation of the main and auxiliary transistors are interchanged, that is, if M_A is biased in WI and M_B is biased in SI. This constitutes our proposed design, which permits harmonic cancellation similar to the previously presented case. The circuit diagram and the small-signal model of the proposed technique is also shown in Fig. 1 and Fig. 2 respectively. The mathematical analysis and principle of linearization for the subthreshold LNA is fundamentally similar to the case of the SI LNA linearization explained earlier. Interchanging the regions of operation of the two transistors provides several advantages, which include a higher value of g_m/I_D, lower DC power consumption, and optimum noise and gain performance, as compared to strong inversion LNAs [2], [3].

III. Simulation Results

The LNA depicted in Fig. 1 is designed in UMC 90 nm CMOS technology and is simulated using Cadence Spectre. The inductors L_G and L_S are modelled as off-chip inductors, having a Q-factor of 20 [4]. The effect of bond wire inductances and package capacitances are included to account for the effect of parasitics, ensuring the accuracy of the results. The pins were modelled as quad-flat no-leads (QFN) packages. The equivalent pi -model of the QFN package has a 1 nH inductor in series with a 0.5 Ω resistance, and capacitances 120 fF and 60 fF, which is used for each of the V_{DD}, ground, and input pins [4], [14]. The auxiliary transistor (M_B) is chosen to be a low threshold voltage transistor (LVT) to make sure that it remains in the SI region even for the low drain-to-source voltage due to the lowered supply voltage of 0.9 V. The sizing of M_B and the inductance L_B are appropriately set for optimum linearity. Fig. 4 illustrates the simulated plots for the S-parameters, namely the input and output matching conditions (S_{11} and S_{22}), the power gain (S_{21}) and the reverse isolation (S_{12}). Fig. 5 depicts the IIP3 curves for the conventional and linearized cases. Two input tones

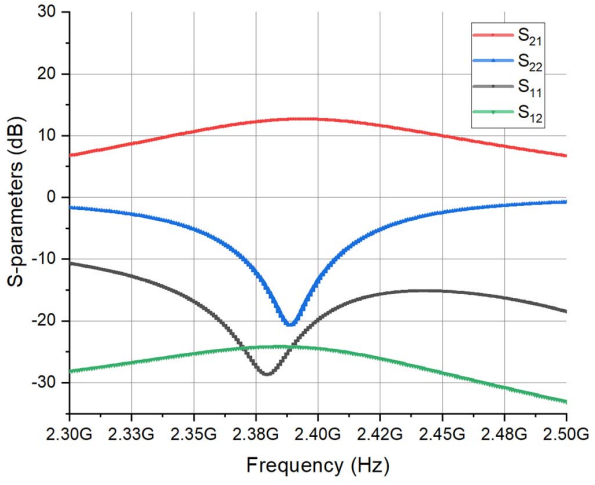

Fig. 4. Scattering Parameters.

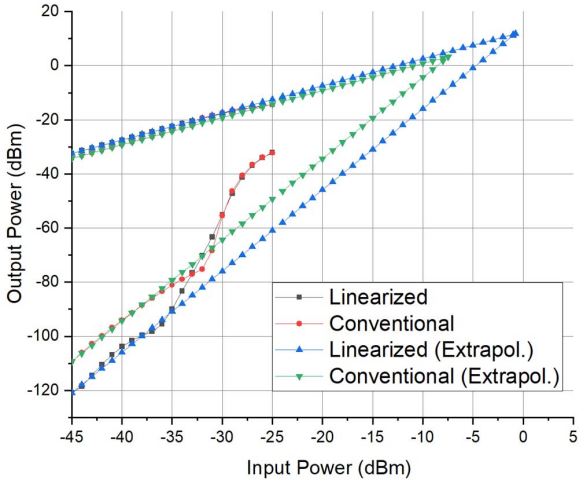

Fig. 5. Third-order Input Intercept Point (IIP3).

with variable amplitudes are injected at 2.4 GHz separated by 1 MHz. An IIP3 of -0.77 dBm is achieved for the linearized case, while that for the conventional circuit is -7.6 dBm. The NF plot is illustrated in Fig. 6.

The design was also simulated across process corners to verify the circuit's robustness to process variations. Table I presents the performance parameters of the LNA across the different process corners (SS, TT, FF), and also for the conventional design (Conv.) in which the linearization circuit is excluded. The effect of the linearization circuit on parameters besides linearity can be observed. Linearity is improved at the cost of additional DC power consumption of the auxiliary path, and a slightly increased noise figure. The power gain can also be observed to improve. Hence the linearization technique is not detrimental to the other performance parameters of the LNA.

Several low-power LNA designs have been reported previously. The design specifications of recent microwatt power subthreshold LNA designs are compared with this work in Table II. A figure of merit is used to draw out a comparison among the designs, given by the following [3].

$$FoM = 10\log\left(\frac{G_{lin} * IIP3 * f_o}{(10^{NF/10} - 1) * P_{DC}}\right) \qquad (7)$$

Where G_{lin} the power is gain in W/W, f_o is the frequency of operation in GHz, the IIP3 is in mW, the NF is in dB, and P_{DC} is the DC power consumption in mW. Gain and NF account for the performance of the LNA in the figure of merit, while IIP3 is included as a measure of the linearity of the LNA. The DC power consumption signifies the power efficiency of the design, which is important for low-power designs. Hence the figure of merit used adequately captures the overall performance of the low-power LNAs.

IV. Conclusion

In this work, a linearization technique for improving the IIP3 in subthreshold LNAs is presented. The modified derivative superposition technique for strong inversion LNAs

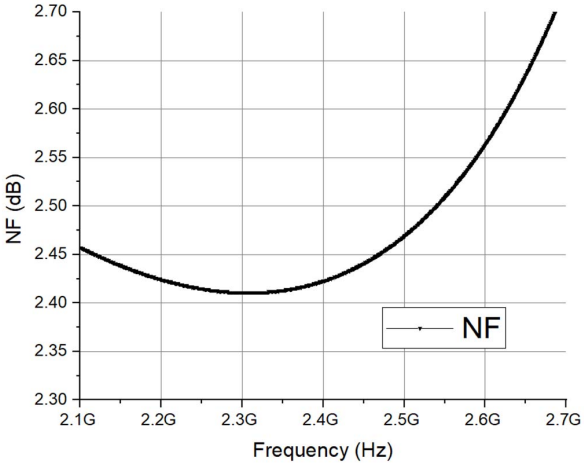

Fig. 6. Noise Figure.

TABLE I. EFFECT OF PROCESS VARIATIONS

Specification	SS	TT	FF	Conv.
P_{DC} (µW)	469.8	503	572.5	302.4
NF (dB)	2.93	2.42	2.03	2.03
S_{21} (dB)	11.4	12.6	13.4	10.4
S_{11} (dB)	- 17.6	-19.9	- 11.6	- 11.2
S_{22} (dB)	- 20.5	- 13.5	- 9	- 14.1
S_{12} (dB)	- 24.8	- 24.5	- 24.6	- 25
IIP3 (dBm)	- 12.5	- 0.77	- 11.8	- 7.6
OIP3 (dBm)	- 1.1	10.8	- 1.5	3.2

TABLE II. COMPARISON OF SUBTHRESHOLD LNAS

Reference	*FoM (dB)*	*P_{DC} (µW)*	*NF (dB)*	*S_{21} (dB)*	*IIP3 (dBm)*	*f_0 (GHz)*	*V_{DD} (V)*	*Tech. (nm)*
This work	**19.88**	**503**	**2.42**	**12.62**	**- 0.77**	**2.4**	**0.9**	**90**
[2]	3.95	400	4.7	9.1	- 11	3	0.6	130
[3]	8.89	680	4.36	9.7	- 4	2.45	1.2	90
[5]	16.04	490	3.8	13.1	- 2.5	2.4	0.7	130
[6]	17.1	336	3.7	14.8	- 3.7	1.8	0.7	110
[7]	2.82	200	4.2	17	- 17.5	0.7	1	180
[8]	10.24	834	3.32	13.92	- 11.5	5.8	0.6	180
[9]	13.14	60	5.3	13.1	- 12.2	2.4	0.4	130
[10]	14.17	475	2.8	17.4	- 10.7	2.4	0.7	65

is briefly explained with the supporting mathematical analysis, which has been adapted for subthreshold LNAs. Simulation results confirm the linearization principle for the proposed low-power, subthreshold LNA designed for IoT applications. The proposed linearization technique can conveniently be integrated with existing subthreshold LNA designs for linearity improvement, as it doesn't degrade the other design parameters. Comparison with previously reported subthreshold LNAs confirms that the LNA presented in this work has the best figure of merit, with a high IIP3 of -0.77 dBm, a low noise figure of 2.42 dB and a low DC power consumption of 503 µW. Therefore, the proposed design is suitable for wireless receivers in low power IoT systems employing 2.4 GHz communication protocols like Bluetooth, Zigbee, and Wi-Fi.

REFERENCES

[1] S. Li, L. Da Xu, and S. Zhao, "The internet of things: a survey," *Information Systems Frontiers*, vol. 17, no. 2, pp. 243-259, 2015.

[2] H. Lee and S. Mohammadi, "A 3GHz subthreshold CMOS low noise amplifier," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006*, San Francisco, CA, 2006, pp. 796–798.

[3] R. Fiorelli, F. Silveira and E. Peralı´as, "MOST Moderate–Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 3, pp. 556-566, March 2014.

[4] C. H. Chang and M. Onabajo, "Linearization of subthreshold low-noise amplifiers," *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, Beijing, 2013, pp. 377-380.

[5] H. S. Jhon, H. Jung, M. Koo, I. Song, and H. Shin. "0.7 V supply highly linear subthreshold low□noise amplifier design for 2.4 GHz wireless sensor network applications," *Microwave and Optical Technology Letters*, vol. 51, no. 5, pp. 1316-1320, May 2009.

[6] C. H. Chang and M. Onabajo, "Analysis and Demonstration of an IIP3 Improvement Technique for Low-Power RF Low-Noise Amplifiers," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 3, pp. 859-869, March 2018.

[7] H. J. Liu and Z. F. Zhang, "An Ultra-Low Power CMOS LNA for WPAN Applications," in *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 2, pp. 174-176, Feb. 2017.

[8] M. T. Lai and H. W. Tsao, "Ultra-Low-Power Cascaded CMOS LNA With Positive Feedback and Bias Optimization," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 1934-1945, May 2013.

[9] T. Taris, J. Begueret and Y. Deval, "A 60µW LNA for 2.4 GHz wireless sensors network applications," *2011 IEEE Radio Frequency Integrated Circuits Symposium*, Baltimore, MD, 2011, pp. 1-4.

[10] M. Rahman and R. Harjani, "A sub-1V, 2.8dB NF, 475µW coupled LNA for internet of things employing dual-path noise and nonlinearity cancellation," *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, 2017, pp. 236-239.

[11] H. Zhang and E. Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 22-36, Jan. 2011.

[12] S. Ganesan, E. Sanchez-Sinencio and J. Silva-Martinez, "A Highly Linear Low-Noise Amplifier," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4079-4085, Dec. 2006.

[13] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[14] Yeong-Lin Lai and Cheng-Yu Ho, "Electrical modeling of quad flat no-lead packages for high-frequency IC applications," *2004 IEEE Region 10 Conference TENCON 2004.*, 2004, pp. 344-347 Vol. 4.