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Analysis and Design of Low Phase Noise LC Oscillator for Sub-mW PLL-Free Biomedical Receivers

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***Abstract*—This work presents the design of a low phase noise LC oscillator (LCO) for a phase locked loop (PLL)-free receiver (RX), which is used for wireless sensor nodes based healthcare applications. A detailed analysis of phase noise of free running LCO has been presented under the influence of off-chip components, which are very often inevitable in biomedical radios. Based on the analysis, a low power cross coupled LCO has been optimally designed for Medical Device Radiocommunication (MedRadio) band, which is a recommended communication band for biomedical applications. The proposed LCO has been fabricated in 180 nm CMOS technology. Measurement results show that the LCO consumes 140 μW power from 1.8 V supply and exhibits a phase noise of -103 dBc/Hz at an offset of 300 kHz, which closely matches with the post layout simulation results. Measurement results also show that the proposed LCO results in significant power reduction in the PLL-free RX while achieving less than 10^{-4} BER at a data rate of 200 kb/s, which is good enough for various biosignal communication.**

***Index Terms*—Phase noise, LCO, Bio-medical, receiver, 400 MHz.**

I. Introduction

Growing demands of healthcare services seek cost effective and time saving solutions. By the virtue of modern sensors and wireless communication technologies, more services can be rendered with limited resources to meet those demands. For example, wearable or implantable devices can be used at the human body to capture and transmit the biosignals such as electro cardiogram, heart rate, respiration rate, temperature, whereas a local receiver can be hosted on base station device such as mobile phone or laptop to receive and record the personal medical data.

Usually, the wireless biomedical portable devices seek very low power consumption for longer operational periods. The main source of power consumption in these devices is the wireless transceiver [1]. In order to reduce power consumption of biomedical transceivers, they are heavily duty cycled ($< 1\%$), i.e., transceiver is turned on for a very brief period during which communication is done and then it go to sleep mode [2]. For this, transceivers require very fast radio frequency (RF) carrier generation, which in turn requires a very low start-up time of RF oscillator, which is the core part of any RF synthesizer.

Traditionally, in a RF synthesizer, RF oscillator is locked in a Phase Locked Loop (PLL) to a stable reference crystal oscillator. This technique filters out the high frequency noise and improves the close-to-carrier phase noise of the RF carrier. However, the price paid is the increased system complexity, increased power consumption and longer settling time of PLL. In view of low power consumption and very low start-up time of oscillators, PLL-less architectures are sought for biomedical transceivers [3]- [7]. However, without PLL, phase noise of oscillators degrade, which eventually affects the performance of the transceiver.

To this point, dedicated communication bands for bio-telemetry comes to rescue, where the spectral requirements are relatively relaxed. For example, 401-406 MHz Medical Device Radiocommunication (MedRadio) band has gained lot of research interests for wireless transmission of biosignals over a short communication range (up to 3 m) [2]. Being a dedicated band, MedRadio has relaxed spectral requirements such as frequency stability of $\pm$100 ppm near 400 MHz. Moreover, it does not have strong interferers as compared to the 2.4 GHz band, where other short range communication protocols such as Bluetooth or Zigbee operate. These points make MedRadio very suitable for bio-telemetry [8]. Moreover, it has attracted attentions for serious medical researches [3] - [12], because it allows only very low output power to be radiated (25 μW effective istropic radiated power), which is harmless for human body. This band is also recommended in various parts of the world for short range (up to 3 m) communication of biosignals [2]. For example, Federal Commission for Communication (FCC) and Wireless Planning Commission (WPC) has recommended it in US and India, respectively.

At 400 MHz, use of off-chip components such as inductors and capacitors are inevitable in the oscillator design due to the requirement of large size components, which are difficult to realize on the chip. Usage of the off-chip components presents more parasitics to the oscillator. This is mainly due to the interaction of the die with the off-chip tank through parasitics caused by IC package and PCB pads and traces. This parasitic loading results in increased power consumption and degraded phase noise of the oscillator. Therefore, at one hand dedicated biomedical bands such as MedRadio gets benefit of relaxed spectral requirements but on the other hand it faces the challenges associated with off-chip components.

In this work, we present a detailed analysis for the degradation in phase noise of a free running LC oscillator in a 400 MHz PLL-less low intermediate frequency (IF) RX under the influence of various off-chip components. The analysis presented in this work is very useful for designing the low

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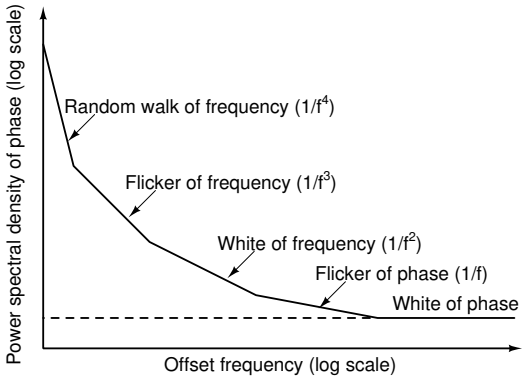

Fig. 1. Power-law noise processes for phase spectral density [13]

phase noise oscillators and was not directly available in the previous literature. Following the analysis, we also present an optimal LCO design for improved performance of the PLL-free RX. The proposed LCO has been designed and fabricated in 180 nm CMOS technology and measurement results of its impact on the performance of a low IF PLL-free RX has been also presented in this work.

The paper is organized as follows. In section II, phase noise analysis for the free running LCO under the influence of off-chip components is presented. Section III explains the design method of the LCO. Section IV presents the simulation and measurement results. Finally, paper is concluded in section V.

II. Phase Noise Analysis

Consider an oscillator, which produces a sinusoidal periodic signal ($v_{osc}(t)$) given below

$$v_{osc}(t) = V_{osc}cos[\omega_0 t + \phi(t)] \tag{1}$$

where, V_{osc} is the oscillation amplitude, ω_0 rad/sec is the nominal frequency of the oscillator, $\phi(t)$ is the zero-mean random quantity, which contains the integrated effects of the variations of frequency and phase from the nominal value. Power spectral density (S_ϕ) of $\phi(t)$ contains the information about the impurity of the oscillator, which is the deviation in frequency or phase from the expected value. S_ϕ is also defined as the phase noise of the oscillator. As shown in Fig. 1, five categories of Power-law noise processes can be used to model S_ϕ of an oscillator [13]. Different oscillators may contain different noise processes. For example, random walk of frequency noise (S_{FM}) is prominent due to the environmental affects such as mechanical shock, vibration or temperature, whereas flicker noise of phase is generally due to the noisy electronics. Typically, phase noise spectrum of high quality oscillators exhibit only $\frac{1}{f^3}$, $\frac{1}{f}$ and flat regions [13].

Leeson proposed a heuristic model for the oscillator noise spectrum, which clearly shows the relationship between the phase noise power spectral density ($S_\phi(\Delta\omega)$) at an offset of $\Delta\omega$ from ω_0 and the known parameters of the oscillator such as carrier power levels, noise of the active devices and tank characteristics [14]. Eq. (2) shows the Leeson's equation,

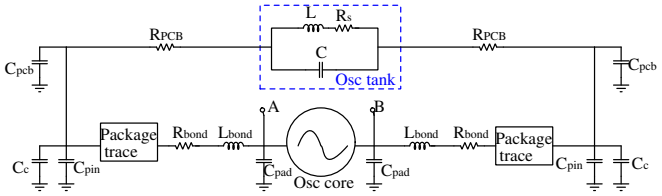

Fig. 2. Detailed electrical model showing different parasitics associated with off-chip tank

where Q is the quality factor of the oscillator tank and S_0 is the effective noise power generated by the active part of the oscillator circuit [14].

$$S_\phi(\Delta\omega) = \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 S_0 \tag{2}$$

As shown in Eq. (2), phase noise of an LC oscillator varies inversely with the square of Q-factor of the tank. In presence of off-chip components, Q-factor reduces, which degrades the oscillator phase noise. Moreover, S_0 also increases due to the involvement of the off-chip components. Therefore, it is important to model the degradation in oscillator phase noise due to the Q-factor reduction and due to the increment of S_0 in the presence of various parasitics, which arise due to the interaction of die with IC package and off-chip components. Following subsections provide the detailed electrical equivalent of LCO tank, analysis of phase noise degradation due to loaded Q-factor and increased S_0 in presence of parasitics, respectively.

A. Detailed electrical equivalent model of LCO tank

Fig. 2 shows the detailed electrical equivalent of the LCO tank in the presence of various parasitics. As shown in the Fig. 2, C_{pad} is the parasitic pad capacitance, C_{pin} is the pin to ground capacitance of the IC package, C_c represents the effective coupling capacitance which arise due to pin-to-pin coupling of IC package, pad-to-pad coupling and substrate coupling. C_{pcb} is the effective parasitic capacitance of the PCB track and PCB pads used to hoist off-chip components. L_{bond} and R_{bond} are the bond wire inductance and capacitance, respectively and package trace corresponds to the resistive losses due to IC packaging. Example values of these parasitics are given at the end of subsection II-B.

B. Analysis of phase noise degradation due to loaded Q-factor

As shown in [15], the Q-factor of a passive network near the frequency of resonance (ω_0) can be defined as follows:

$$Q = \frac{\omega_0}{2}\left|\frac{z'}{z}\right| \tag{3}$$

where, z is the effective impedance of the passive network of the oscillator and $z' = \frac{dz}{d\omega}$.

For ideal situation, i.e. without any parasitics, impedance of the main oscillator tank shown in Fig. 3 can be defined as follows:

$$z = \frac{R_s + j\omega L}{1 - \omega^2 LC + j\omega R_s C} \tag{4}$$

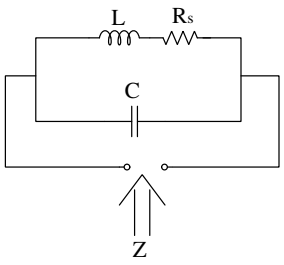

Fig. 3. Simple off-chip tank

and z' can be calculated by using Eq. 5 given below.

$$z' = \frac{dz}{d\omega} = \frac{2\omega R_s LC + jL(1+\omega^2 LC - \frac{{R_s}^2 C}{L})}{\left((1-\omega^2 LC)^2 - \omega^2 {R_s}^2 C^2 + 2j\omega R_s C(1-\omega^2 LC)\right)^2} \quad (5)$$

Resonance frequency of the tank can be defined as shown in Eq. 6.

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{{R_s}^2}{L^2}} \quad (6)$$

At resonance, $|z|$ and $|z'|$ can be found by using equations (4), (5) and (6).

$$|z| = \frac{L}{R_s C} \quad (7)$$

$$|z'| = \frac{2\omega_0 L^3}{{R_s}^2}\frac{1}{\sqrt{LC}} \quad (8)$$

Q-factor of the tank can be derived by using equations (3), (7) and (8):

$$Q = \frac{\omega_0 L}{R_s}\omega_0\sqrt{LC} \quad (9)$$

The effective parallel tank resistance (R_p) at resonance can be given by the following equation :

$$R_p = Q^2 R_s \quad (10)$$

or equivalently,

$$Q = \frac{R_p}{\omega_0 L}\frac{1}{\omega_0\sqrt{LC}} \quad (11)$$

Considering C = 1 pF for the off-chip tank, L = 158 nH will be required for 400 MHz operation. Considering Q-factor of 60 for L [16], the value of R_p of unloaded tank will be about 24 kΩ (Eq. (9) and (10)).

A simplified electrical equivalent of the LCO tank is shown in Fig. 4(a). The effect of all parasitic capacitors shown in Fig. 2 can be approximated as $C_{eq} = (C_{pad} + C_{pin} + C_c + C_{pcb})$. As shown in Fig. 4(b), the effective tank capacitance can be approximately modelled as $C_{eff} = C + C_{par}$, where C_{par} $(= C_{eq}/2)$ is the equivalent parasitic capacitance, which arises due to the series combination of two C_{eq}. Therefore, in the

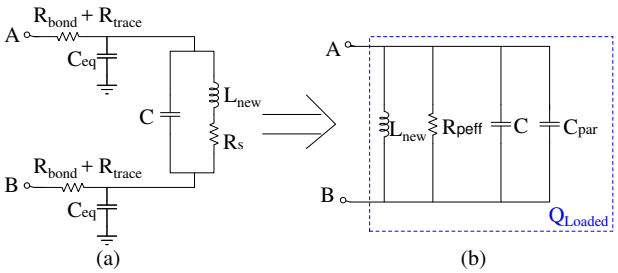

Fig. 4. (a) Simplified tank equivalent with parasitics and (b) equivalent parallel tank model

presence of parasitics, the overall tank capacitance increases from C to a new value given by following equation:

$$C_{eff} = KC \quad (12)$$

where $K = 1 + \frac{C_{par}}{C}$. Parasitic resistance of the IC package trace (R_{trace}) and R_{bond} results into an equivalent parallel parasitic resistance R_{par} at the frequency of resonance, which can be defined by Eq. (13) given below [17].

$$R_{par} = \frac{1}{\omega_0^2 C_{par}^2 (R_{bond} + R_{trace})} \quad (13)$$

The parasitic loss due to R_{par} reduces the effective parallel tank resistance at resonance to a new value $R'_p = (R_p || R_{par})$, which in turn reduces the quality factor (Eq. (11)). Due to the increased tank capacitance, the required tank inductance value will have to be reduced by approximately the same factor (Eq. (6)) to a new value L_{new} given by following expression:

$$L_{new} = \frac{L}{K} \quad (14)$$

Due to the reduction in inductor value, the equivalent parallel resistance of unloaded tank also decreases to a new value ($R_{p_{new}} = \frac{R_p}{K}$) assuming same quality factors for L_{new} and L. Due to these two effects, the overall tank resistance at resonance under the influence of various parasitics reduces from R_p to an effective value R_{peff} defined by the equation given below.

$$R_{peff} = (R_{p_{new}} || R_{par}) \quad (15)$$

From equations (11), (14) and (15), Q factor of loaded tank degrades by a factor of $\frac{R_{peff} \times L}{R_p \times L_{new}} = \frac{K}{M}$, where $M = \frac{R_p}{R_{peff}}$. Therefore, by using equations (2) and (11), degradation in phase noise (ΔS_{ϕ_Q} in dB) due to the Q-factor reduction, can be modelled by the following equation:

$$\Delta S_{\phi_Q} = 20\ log\frac{K}{M} \quad (16)$$

Depending upon the type of package and PCB dielectric, R_{trace} and C_{eq} could be few ohms and few pF, respectively. For example, Quad Flat Packages (QFP) have $R_b + R_{trace}$ of about 2 Ω and $C_{par} = C_{eq}/2$ is about 2-3 pF considering FR4 substrate and 1.6 mm thickness of the PCB [18], [19]. From Eq. (13), value of R_{par} is about 20 kΩ for C_{par} = 2 pF. As calculated above, for C_{par} = 2 pF, K is 3 (Eq. (12))

and unloaded R_p = 24 kΩ, Therefore, $L_{new}(= L/K)$ and $R_{p_{new}}(= R_p/K)$ become about 53 nH and 8 kΩ, respectively. Therefore, the effective parallel resistance of the tank becomes $R_{peff} = R_{p_{new}}||R_{par}$ = 8||20 kΩ = 5.7 kΩ. From these values, $\frac{K}{M} = 0.7$ and ΔS_{ϕ_Q} is about 3 dB (Eq. (16)).

C. Analysis of phase noise degradation due to increased S_0

Typically, the noise sources in the cross-coupled LC oscillator (Fig. 5) are the four transistors and the loss resistance of the tank. Assuming identical NMOS transistors and PMOS transistors, S_0 can be expressed by Eq. 17 given below.

$$S_0 = \frac{1}{2}\left(\frac{\overline{i_n^2}}{\Delta f} + \frac{\overline{i_p^2}}{\Delta f}\right) + \frac{\overline{i_{R_s}^2}}{\Delta f} \tag{17}$$

where, $\frac{\overline{i_{n,p}^2}}{\Delta f}$ is the noise of each MOS device given as follows:

$$\frac{\overline{i_{n,p}^2}}{\Delta f} = 4kT\gamma g_{m_{n,p}} \tag{18}$$

and $\frac{\overline{i_{R_s}^2}}{\Delta f}$ is the noise due to loss resistance of the tank expressed below:

$$\frac{\overline{i_{R_s}^2}}{\Delta f} = \frac{4kT}{R_p} \tag{19}$$

In equations (18) and (19), $g_{m_{n,p}}$ is the transconductance of the transistor (NMOS or PMOS) defined by Eq. 20, and R_p is the equivalent tank resistance at resonance.

$$g_m = \sqrt{\mu C_{ox}\frac{W}{L}I_{tail}} \tag{20}$$

The amplitude of the oscillator voltage can be given as $V_{osc} = I_{tail}R_p$. As discussed in the previous subsection, due to the parasitics effective parallel resistance of tank decreases to a new value R_{peff} , which requires large tail current to achieve a desired voltage swing. If R_p decreases by a factor $M(= \frac{R_p}{R_{peff}})$, I_{tail} will increase by a factor of M and hence g_m will increase by a factor of $\sqrt{M}$. This will result in increase of the noise powers of transistors and resistor by a factor of $\sqrt{M}$ and M, respectively. From Eq. 2, due to the increase in S_0, the phase noise degradation ($\Delta S_{\phi_{S_0}}$ in dB) can be modelled by the following equation

$$\Delta S_{\phi_{S_0}} = 15 \times log(M) \tag{21}$$

As calculated in the previous subsection II-B, in the presence of off-chip parasitics, M was about 4.2, which results in $\Delta S_{\phi_{S_0}}$ of about 10 dB.

By using equations (16) and (21), the overall degradation in phase noise ($\Delta S_{\phi_{Total}}$) (in dB) can be given by Eq. (22) given below.

$$\Delta S_{\phi_{Total}} = 20\ log\frac{K}{M} + 15\ log(M) \tag{22}$$

Eq. (22) is a useful result which models the impact of various parasitics on the phase noise of a packaged LCO with off-chip tank. From Eq. (22), for the example given in above subsections, the overall phase noise degradation is about 13 dB.

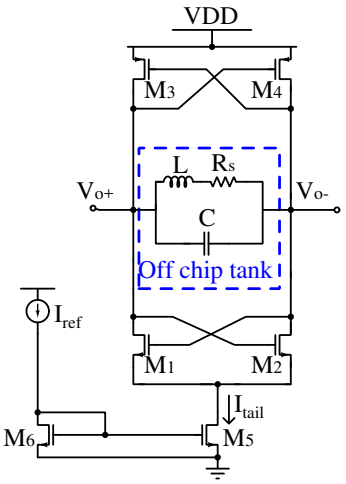

Fig. 5. LCO schematic

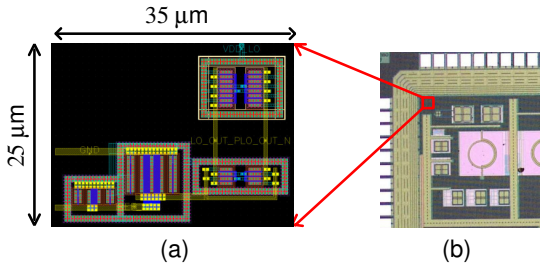

Fig. 6. (a) Layout and (b) die-micrograph of the fabricated LCO

III. Circuit Design

Cross coupled complementary NMOS-PMOS topology (Fig. 5) has been used to design the LCO. As shown in section II, higher R_p is desirable for reduced power consumption. For a given Q-factor inductor, higher R_p requires higher inductor value (L). With higher L, the value of tank capacitance will decrease for a given resonant frequency. The minimum capacitance (C_{min}) for the LCO tank results from the pad, IC package and PCB parasitics. However, if LCO is designed for C_{min}, it might become difficult to tune the LCO at desired frequency after fabrication. Therefore, some margin for tuning should also be kept. For this we also used a tank capacitance C in the design and value of inductor is chosen by considering $C_{min} + C$. The minimum transconductance required for sustained oscillations was calculated as $g_{m_{min}} = 2/R_{peff}$ by considering various parasitic effects [17]. For R_{peff} = 5.7 kΩ calculated in subsection II-B, $g_{m_{min}}$ = 350 μA/V. The tail current required for an oscillation amplitude of V_{osc} was calculated as $I_{tail} = V_{osc}/R_{peff}$ [20]. Transistor sizing was done by considering their transconductance (g_m) 3-4 times of $g_{m_{min}}$ as $(W/L)_{p,n} = (g_{m_{p,n}})^2/(2I_{tail}\mu_{p,n}C_{ox})$ [17]. Fig. 6(a) shows the layout of the LCO.

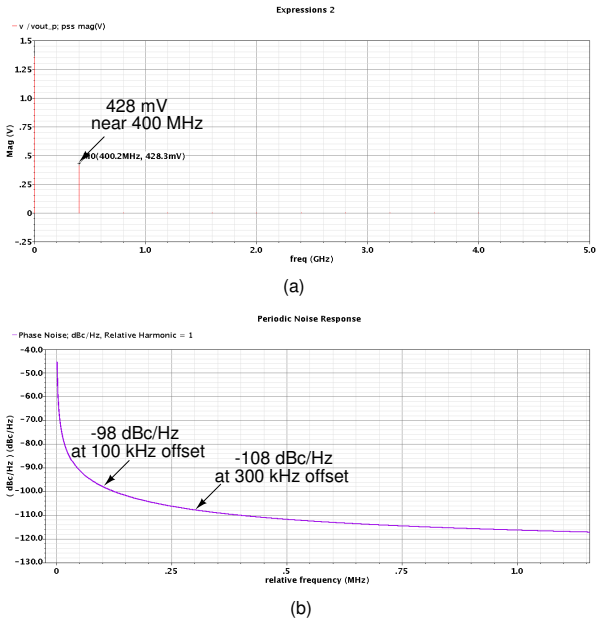

Fig. 7. Post layout simulation results from PSS analysis of the proposed LCO (a) PSS magnitude and (b) Phase noise

IV. Simulation and Measurement Results

The LCO has been designed and fabricated in 180 nm mixed-mode CMOS technology. Fig. 6(b) shows the die-micrograph of the LCO. Fig. 7 shows the post layout simulation results, where the amplitude of oscillation is 428 mV and phase noise of oscillator is about -108 dBc/Hz at an offset of 300 kHz. Usually, RF measurement results are reported from probe testing in a very sophisticated environment, however in real application scenario that is not always the case. ICs are packaged and interfaced with various peripheral components to make a complete system. In this work, measurements of the LCO were done on a packaged IC. Quad flat package with no leads (QFN) has been used for the IC packaging in this work to reduce the IC package parasitics. Measurement results show that the packaged LCO consumes about 140 μW power from 1.8 V power supply.

Inductor value of 56 nH with 0.8 pF off-chip capacitor has been used in the off-chip tank, which are close to the values considered for the analysis in section II-B. Tuning of LCO was done by looking at the IF component of the RX for a known RF input ($f_{LCO} = f_{RF} - f_{IF}$) [6]. As shown in Fig. 8, for f_{RF} of 401 MHz LCO was tuned for f_{IF} of about 1.2 MHz, which shows that f_{LCO} is about 399.8 MHz for the low side injection.

Since LCO was designed to drive a low capacitance input of a mixer in a receiver chain, its phase noise measurements on spectrum analyser (has 50 Ω input impedance) were done using an off-chip buffer [21]. Fig. 9 shows the output spectrum of LCO when it is loaded by the off-chip buffer. The off-chip buffer offers a 2.1 pF extra load to the LCO which causes a frequency deviation from 400 MHz to 369 MHz. The buffer

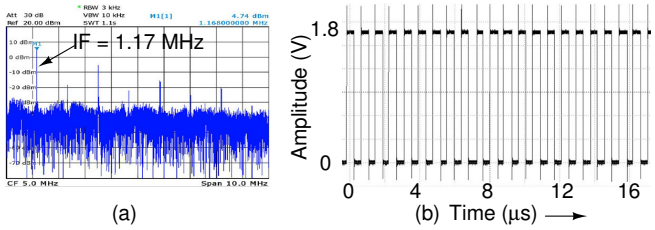

Fig. 8. Measurement results showing (a) spectrum and (b) rail-to-rail transient of IF component

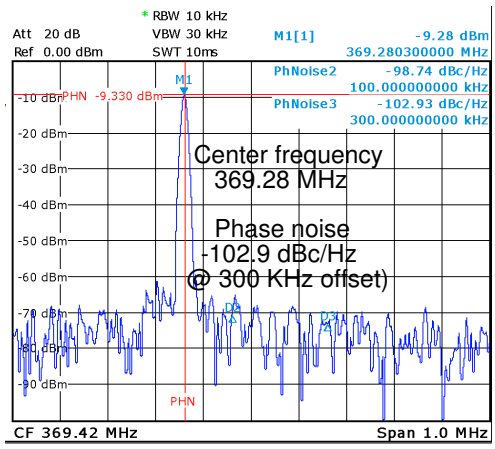

Fig. 9. Spectrum of free running LCO measured with a commercial off-chip buffer [21]

also causes about 3-dB loss in the output power of LCO across a 50 Ω load of spectrum analyzer. The measured phase noise of the RF carrier is better than -100 dBc/Hz at an offset of 300 kHz.

Fig. 10 shows the experimental set up for the measurement of the BER of the low IF RX with the proposed LCO as a local oscillator [22]. RF input to the RX is modulated by using an FPGA and RX output is fed back to the FPGA, where BER is calculated and displayed. Fig. 11 shows the measurement results of RX output at 200 kb/s data rate of operation. The data modulating RF input and data at RX output matches

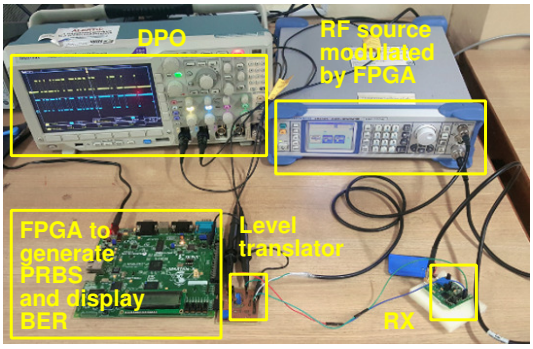

Fig. 10. Setup for the measurement of bit error rate of the RX

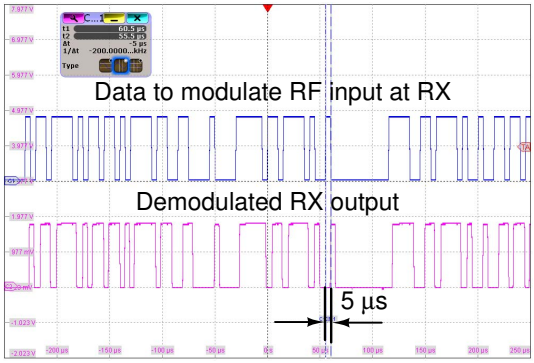

Fig. 11. Measurement results showing (a) data to modulate RF input of RX and demodulated data at output of RX at 200 kb/s

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameters	[9]	[10]	[11]	[12]	This work
Measured/ Simulated	Measured	Measured	Measured	Measured	Measured
PLL-less	Yes	No	Yes	No	Yes
Technology	180 nm CMOS	180 nm CMOS	40 nm CMOS	180 nm CMOS	180 nm CMOS
Oscillator Frequency	400 MHz	400 MHz	400 MHz	400 MHz	369MHz†
Oscillator Phase Noise (Offset)	-105 dBc/Hz ‡ (300 kHz)	-83 dBc/Hz (300 kHz)	-108 dBc/Hz (300 kHz)	-123 dBc/Hz (1 MHz)	-102.9 dBc/Hz (300 kHz)
Frequency Synthesizer Power	900 μW	1.26 mW	-	621 μW	140 μW
RX Data Rate	2 Mb/s	75 kb/s	20 kb/s	187.5 kb/s	200 kb/s
RX BER	10^{-3}	10^{-3}	$< 10^{-3}$	10^{-3}	$<10^{-4}$
RX Power	3.4 mW	2 mW	2.19 mW	1.49 mW	990 μW
Supply	1.8 V	1.8 V	1.2 V	1 V	1.8 V

†Due to off-chip buffer used for phase noise measurements, LCO frequency shifts to 369 MHz from 400 MHz, ‡Estimated from reported phase noise plot

very closely. The measured BER for RX was less than 10^{-4} upto the data rate of 200 kb/s. This result confirms that the LO frequency is quite stable and phase noise of the LCO is extremely low.

Table I shows the performance summary and comparison of the proposed PLL-free RX with other works. As compared to the other works, the proposed RX consumes much less power while having $< 10^{-4}$ BER at a data rate of 200 kb/s, which is a sufficiently high data rate for many bio-telemetry applications. Moreover, phase noise performance is also better than some of the other works mentioned in the table. As compared to the other works, main power reduction in RX has been achieved due to the low power LCO of the proposed PLL-free RX.

V. CONCLUSION

In this work, a useful analysis has been presented to capture the effect of various parasitics on the phase noise performance of a free-running LCO. The analysis also acts like a design guideline to ensure adequate phase noise performance of LCO in a PLL-free RX. Following the analysis, a low power LCO has been designed for 400 MHz PLL-less biomedical receivers. The proposed LCO along with the RX have been fabricated in 180 nm CMOS technology. Measurement results show that the LCO consumes 140 μW power from 1.8 V power supply while having an estimated phase noise better than -100 dBc/Hz at an offset of 300 kHz, which is more than sufficient for MedRadio band biomedical radios. Moreover, measurement results also show that the proposed LCO results in significant power reduction in a PLL-free RX while achieving less than 10^{-4} BER at a data rate of 200 kb/s, which is good enough for various biosignal communication.

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