Energy Efficient Bidirectional Equalized Transceiver with PVT Insensitive Active Termination

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***Abstract*—This paper presents a current-mode bidirectional transceiver for off-chip interconnects, which deploys a feed-forward equalization (FFE) scheme in transmitter for channel-loss compensation. The proposed transmitter makes use of a current-boosting driver (CBD) which boosts the pre-drive current, increasing the current-efficiency of the transmitter compared to the conventional CML driver. Moreover, compared to conventional passive terminated transceivers, the proposed transceiver utilizes an active termination in combination with a special biasing scheme, thereby making the termination impedance insensitive to process-voltage-temperature (PVT) variations. The entire architecture has been designed in 180 nm CMOS technology with a supply voltage of 1.8 V. Simulated power consumption in the transceiver pair is 6.4 mW with an energy efficiency of 1.28 pJ/bit while operating at 5 Gbps over 52-inch FR4 PCB trace having loss of 24.4 dB at one-half the bitrate.**

***Keywords*—Serial link, Feed-forward equalization (FFE), inter - symbol interference (ISI), current-mode logic (CML), active termination, current boosting driver (CBD).**

I. INTRODUCTION

With increasing speed requirement of data communication, chip-to-chip serial links have been pushed to multi-Gbps bit-rates. Different transmitter and receiver architectures are emerging with elevated bandwidth performance. Simultaneously, with the speed advancement in chip-to-chip communication, proper termination for the transmitter and receiver [1-3] finds its role very important for signal integrity and low bit-error rate (BER). Any mismatch between the termination impedance of Tx/Rx and the characteristic impedance of the line can cause reflections and hence degrade the signal integrity. In modern interconnects, diverse impedance standards are used wherein backplane applications 100 Ω differential impedance is preferred [4]. It is a common practice to use passive terminators to match the characteristic impedance of the line. However, passive terminators vary with process [2] and temperature, thereby necessitating the need for proper tuning to match the characteristic impedance of the line [1,3]. In both [1] and [3], driver output impedance is controlled by parallel impedance/passive resistor segments and switches which are digitally controlled. However, use of large number of parallel resistors and big switches increases the output stage area and adds extra parasitic. Moreover, passive resistors can also give rise to high thermal noise. Alleviating all these issues of passive termination, this work proposes an active termination scheme which gives proper impedance matching regardless of process and temperature variations.

The other issue affecting the signal integrity is the channel loss or attenuation in high frequency which primarily occurs due to skin effect and dielectric absorption [5]. Several equalization techniques have been evolved to address this issue. These include Feed-forward equalization (FFE) [1,2,6,7,8], continuous-time linear equalization (CTLE) [5,10,11], decision feedback equalization(DFE) [2,5,6,9,12]. Popularity of FFE Txs are increasing for extending I/O bandwidth because the architecture of a FFE-Tx is simple, easy to implement compared to others and can be designed independently of the Rx. The FFE taps in current-mode Txs are generally realized by parallel CML drivers [1,13,14]. But the CML driver uses 50 Ω passive termination, so the tail current gets equally divided between the terminator and the line which also has a characteristic impedance of 50 Ω. Hence, only half of the tail current gets conveyed to the channel. This work addressed this issue by introducing a current-boosting driver (CBD) which boosts the pre-driver tail current by a factor β before sending to the channel. For the conventional passive terminated CML driver, this factor β is 0.5 and the resulting current-efficiency is also 0.5. Whereas, for the proposed transceiver, the value of β achieved in this work is 1.96 resulting in a current-efficiency of 0.87. Moreover, decoupling the pre-drivers from the channel using the CBD also solves the problem of self-loading [15] associated with the conventional current-mode FFE Txs.

In summary, this work proposes a current-mode FFE transmitter for off-chip interconnects utilizing a CBD, which serves the following purposes: 1) it boosts the pre-driver current while sending to the channel which increases the current-efficiency of the transmitter; 2) it provides an accurate active termination which is insensitive to PVT variations; 3) it prevents the pre-drivers from loading the channel input node and finally 4) the CBD can also act like a receiver, making the link bi-directional.

Remaining part of the paper is organized as follows. Section II describes the entire transceiver architecture along with the circuit implementation. Section III highlights the simulated performance of the transceiver followed by conclusion in section IV.

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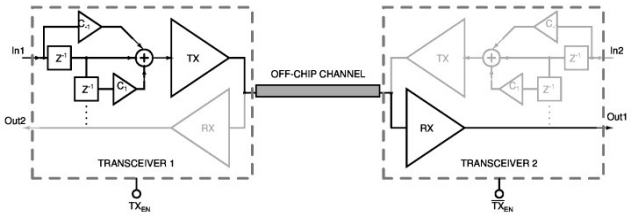
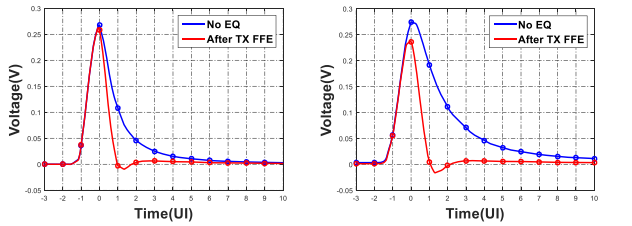
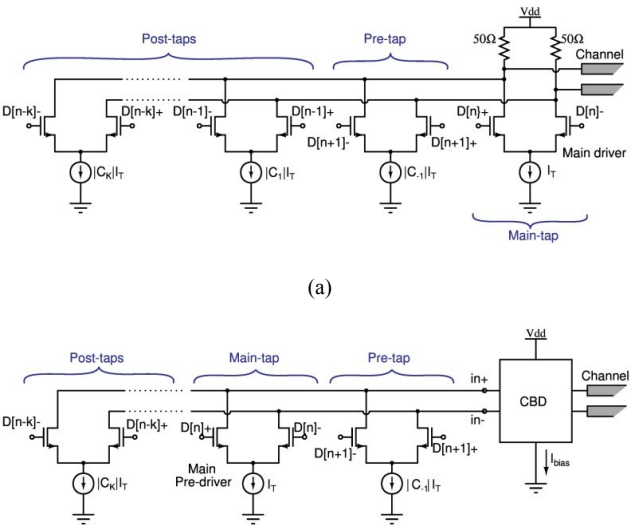


Fig. 1. Architecture of the bi-directional link with transceiver pair



(a) (b)

Fig. 2. Effect of 1st post-tap of FFE on channel pulse response for (a) 29.5-inch PCB trace, (b) 52-inch PCB trace @ 5 Gbps(1UI = 200ps)



(a)

(b)

Fig. 3. (a) conventional current-mode FFE transmitter (b) proposed FFE transmitter with current-boosting driver (CBD)

II. PROPOSED TRANSCEIVER ARCHITECTURE

Fig. 1 shows the architecture of the proposed bi-directional link. The mode of the transceiver pair can be switched between transmitter and receiver by controlling the TX_{EN} pin. In transmitter mode, the pre-drivers realizing the FFE taps are connected to the current-mode driver. In receiver mode, the same current-mode driver acts like a receiver, while the pre-drivers are disconnected from it. The driver output impedance, which is also the receiver's input impedance, is matched to the characteristic impedance of the line and also kept insensitive to PVT variations by biasing it with a constant-g_m bias circuit .

A. Transmitter Feed-forward Equalization

Equalization is needed whenever the shape of the transmitted bit gets distorted due to the channel loss at high frequencies which increases the bit-error-rate (BER) at the receiver side. A feed-forward equalization scheme deploys an FIR filter which pre-distorts the transmitted signal before sending it to the channel. This pre-distortion, though attenuates the transmitted signal by some amount, helps in mitigating the effect of channel distortion by cancelling the pre-cursor and post-cursor ISI of the channel pulse-response (see Fig. 2). Number of FFE taps and the corresponding tap coefficients depends on the channel loss characteristics and determined by the relative heights of the main-cursor, pre-cursors and post-cursors. Fig. 3(a) shows a conventional passive terminated current-mode FFE transmitter with CML drivers. It can be observed that the tail currents of the drivers always get equally divided between the 50 Ω terminator and the 50 Ω line. Hence for a main driver tail current I_T, always $I_T/2$ is conveyed to the channel as signaling current. The total current in the transmitter can be given by

$$I_{total,C} = I_T + |C_{-1}|I_T + |C_1|I_T + |C_2|I_T + \cdots . + |C_k|I_T \quad (1)$$

Where I_T is the main driver current and C_i's are the FFE tap coefficients which can be positive, negative or zero. Now, given these tap coefficients, the maximum signaling current that can be achieved is

$$I_{s,max,C} = \frac{1}{2}\left(I_T + |C_{-1}|I_T + |C_1|I_T + |C_2|I_T + \cdots . + |C_k|I_T\right) \quad (2)$$

Hence, defining current efficiency E_C for the conventional FFE Tx, as the ratio of the maximum signaling current to the total current in the transmitter, gives a current efficiency of 0.5 for the conventional FFE Tx. On the other hand, the proposed FFE Tx in Fig. 3(b) deploys a CBD to boost the tail currents of the CML pre-drivers by a factor β. In other words, if I_T be the tail current of the main pre-driver, the corresponding signaling current would be given by β I_T .The total current of this Tx can be written as

$$I_{total,P} = I_{bias} + I_T + |C_{-1}|I_T + |C_1|I_T + |C_2|I_T + \cdots . + |C_k|I_T \quad (3)$$

Where I_{bias} is the quiescent current in the CBD required for its operation. Also, the maximum signaling current can be given by

$$I_{s,max,P} = \beta\left(I_T + |C_{-1}|I_T + |C_1|I_T + |C_2|I_T + \cdots . + |C_k|I_T\right) = \beta(I_{total,P} - I_{bias}) \quad (4)$$

Hence, the current efficiency becomes

$$E_P = \frac{I_{s,max,P}}{I_{total,P}} = \beta\left(1 - \frac{I_{bias}}{I_{total,P}}\right) \quad (5)$$

Implementation of the proposed transceiver with 3-taps shows a β value of 1.96 and $I_{bias}/I_{total,P}$ ratio of 0.55 yielding in a current efficiency, $E_P = 0.87$, in comparison with $E_C = 0.5$ of conventional current-mode FFE Tx.

Another important drawback of the Tx in Fig. 3(a) is the self-loading [15] due to parasitic capacitances of the driver transistors. It is to be noted that the drains of all the driver transistors constituting the FFE taps are directly connected to the channel input. Hence, the equivalent drain capacitance (c_d) coming from all the transistors are directly interfering with the termination resistor to change the termination impedance. This change in termination impedance causes mismatch and degrades the return loss. Also, the self-loading increases linearly with the total number of FFE taps. However, the proposed Tx alleviates the issue of self-loading by decoupling the FFE taps from the channel input node by means of the CBD. As the channel always sees the CBD output impedance as the termination impedance, it is not susceptible to the drain parasitic capacitances of the pre-drivers and hence there is no degradation in return loss.

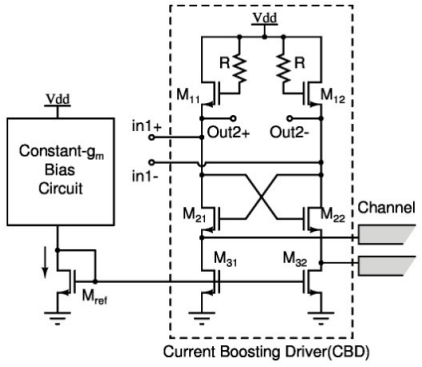
B. Current-Boosting driver(CBD)

Fig. 4(a) shows the current-boosting driver [16,17] which becomes a receiver when the input node is disconnected from the pre-drivers by MOSFET switches. The input and output nodes of CBD reverse their roles in transmitting and receiving modes. It utilizes a cross-coupled pair of transistors M_{21} and M_{22} along with diode connected inductive peaking loads M_{11} and M_{12}. The inductive peaking load acts like an active inductor in series with a resistor enhancing the bandwidth of operation [16]. There are two important features of this driver circuit. First one, a very low output impedance can be achieved burning a nominal static current. From the analysis in [16] at low frequencies, the small signal output impedance of this driver is given by

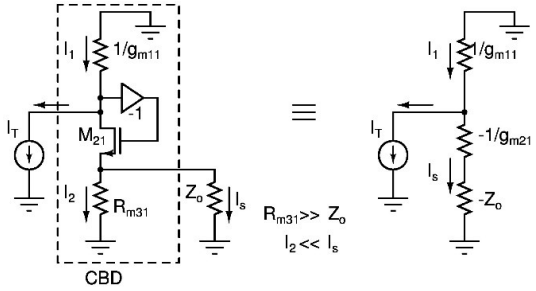
$$Z_{out} = {}^{1}\!/_{g_{m21}} - {}^{1}\!/_{g_{m11}} \quad (6)$$

Where g_{m21} and g_{m11} are transconductance of transistors M_{21} and M_{11}. As Z_{out} is obtained as a difference between $1/g_{m21}$ and $1/g_{m11}$, it can be made very low with low static power to match the characteristic impedance of the channel for avoiding reflection. Also, transconductance of a transistor can be given by

$$g_m = 2\sqrt{kI_{quiescent}} \quad (7); \qquad k = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) \quad (8)$$



(a)



(b)

Fig. 4. (a) Current Boosting Driver circuit and its biasing scheme to make the output impedance PVT insensitive (b) small-signal analysis of half-circuit equivalent of the CBD

Where, $I_{quiescent}$ is the quiescent current through the transistor. Hence, as g_m depends on the quiescent current, electron-mobility and sizes of the transistor, the value of Z_{out} is sensitive to the process, supply-voltage and temperature (PVT) which is an inherent drawback of [16] and [17]. To address this issue, this work utilizes a constant-g_m biasing circuit which makes the g_m of the concerned transistors PVT insensitive resulting in an accurate output impedance of the CBD.

The second important feature is that this driver can act as a current boosting stage, which utilizes the negative small-signal impedance offered by the cross-coupled pair [18] to inject boosted signal-current into the channel. The half-circuit small-signal equivalent and the simplified half-circuit equivalent [18] of the CBD is shown in Fig. 4(b). If I_T be the pre-drive current and I_s be the signaling current being conveyed into the channel with characteristic impedance z_o (=50Ω), then a simple analysis of Fig. 4(b) shows that I_s can be given by

$$I_s = \frac{{}^{1}\!/_{g_{m11}}}{Z_o + \left({}^{1}\!/_{g_{m21}} - {}^{1}\!/_{g_{m11}}\right)} . I_T \quad (9)$$

which after substitution by (6) gives

$$I_s = \frac{1/g_{m11}}{Z_o + Z_{out}} . I_T = \frac{1/g_{m11}}{100} . I_T = \beta I_T \qquad (10)$$

Where β is the current-boosting factor. It is to be noted that the value of β is 0.5 for a conventional FFE Tx as explained in section II(A), whereas for the proposed Tx, β can be designed to be greater than 1 by making the small-signal resistance, $1/g_{m11}$ of the inductive peaking load M_{11} greater that 100 Ω, as it is evident from (10). Implementation shows a β of 1.96 with a quiescent current of 300μA in both the branches of the CBD.

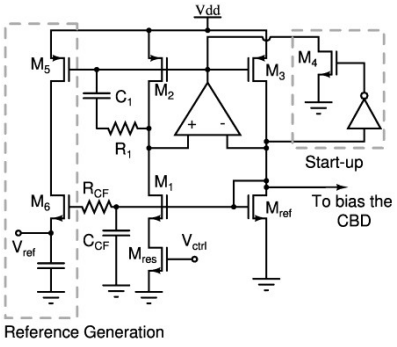
C. Constant-g_m bias circuit

From (6) it can be seen, that the output impedance of the CBD depends only on the transconductance of the transistors. Hence, to make the output impedance insensitive to process, voltage and temperature, the quiescent current in the CBD is mirrored from M_{ref} (see Fig. 4(a)) whose g_m is kept fixed and does not change with PVT variations. The circuit [19] producing the bias current of M_{ref} is shown in Fig. 5. It can be shown that the current I_{bias} through M_{ref} and the transconductance (g_m) of M_{ref} is given by

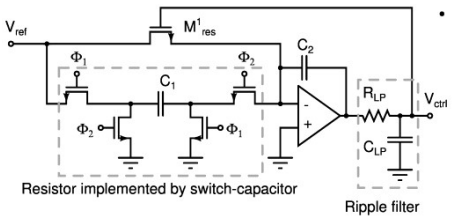
$$I_{bias} = \frac{2}{\mu_n C_{ox}(\frac{W}{L})} . \frac{1}{R^2} . \left(1 - \frac{1}{\sqrt{p}}\right)^2 \qquad (11)$$

$$g_m = 2\sqrt{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) I_{bias}} = \frac{2}{R} . \left(1 - \frac{1}{\sqrt{p}}\right) \qquad (12)$$

Where p is the size ratio of M_1 and M_{ref} and R is the equivalent resistance of M_{res} working in triode region. R is matched to a switch-capacitor resistor using the control loop shown in Fig. 5(b). From (12) it is observed that g_m of M_{ref} depends only on R and p and no other parameters pertaining to process, voltage or temperature. Hence, the circuit adjusts the current through M_{ref} to make its g_m constant if there is a variation in electron mobility (μ_n) due to temperature variation or other properties of the transistors due to process variation. Moreover, as same bias current is flowing in both the branches of the CBD, according to equation (6), the output impedance of the CBD also becomes PVT insensitive.



(a)



(b)

Fig. 5 (a) Implementation of the constant-g_m bias circuit (b) tuning circuit for generating the control voltage [19]

III. SIMULATION RESULTS

The entire architecture has been designed and simulated in 1.8 V-supply, 180 nm CMOS technology using cadence virtuoso and Hspice simulator. S-parameter models [20] of different FR4 PCB traces, having vast usage in backplane applications, have been used for testing the performance of FFE transmitter along-with 1nH series inductance and 1 pF shunt capacitance to account for the package parasitics (Fig. 6). A data stream of bit-rate of 5 Gbps has been used for validating the performance of the transceiver. Fig. 7 shows the channel frequency response for different FR4 PCB traces. The channel losses at Nyquist frequency (2.5 GHz) are 3.76 dB, 13.17 dB and 24.4 dB for 7.5", 29.5" and 52" FR4 PCB traces respectively. Hence there is no requirement of equalization for 7.5" trace, whereas significant amount of equalization is needed for other two lossy traces.

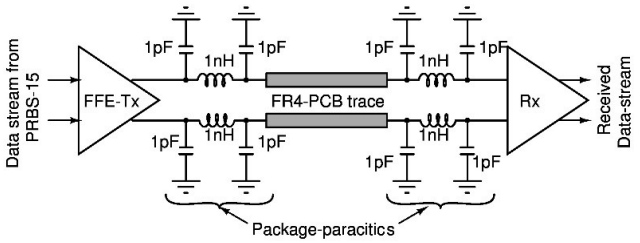


Fig. 6. Simulation set-up for the FFE-Tx including package paracitics

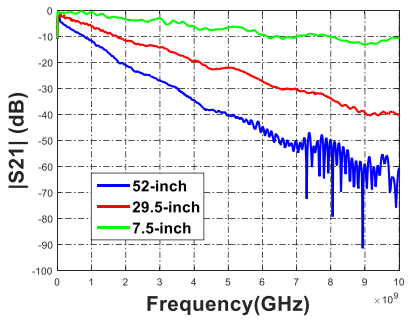


Fig. 7. Frequency response ($|S_{21}|$) for different FR4 PCB traces

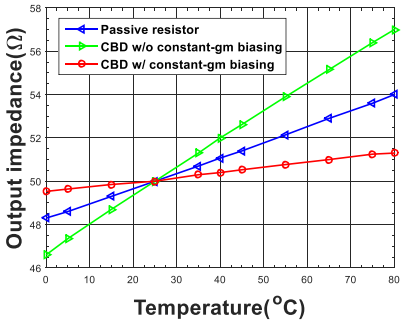


Fig.8. Variation of transmitter output impedance with temperature for different termination schemes

Fig. 9 shows the eye-diagram of received data, with and without equalization for the two lossy channels as mentioned above. A 2-tap FFE gives an 80% eye-opening for the 29.5" trace whereas, 3-taps have been used with proper tap-coefficients for the more lossy 52" trace to get the same eye-opening. Also, in the later-case, the total quiescent current in the CBD is 600 µA giving a β value of 1.96 and the pre-driver currents are chosen to be 250 µA, 170 µA and 60 µA for the main-tap, post-tap and pre-tap respectively. Using the above values of currents in (5), gives a current efficiency (E_P) of 0.87, compared to the current-efficiency (E_C) of 0.5 in conventional current-mode FFE Tx.

TABLE I

Variation of transmitter output impedance with process

Termination type	Lowest	Highest
Passive resistor*	32.9 Ω	72.5 Ω
CBD w/o constant-g_m biasing	42.26 Ω	53.58
CBD w/ constant-g_m biasing	42.6 Ω	54.6 Ω

*in SCL 180-nm CMOS process technology

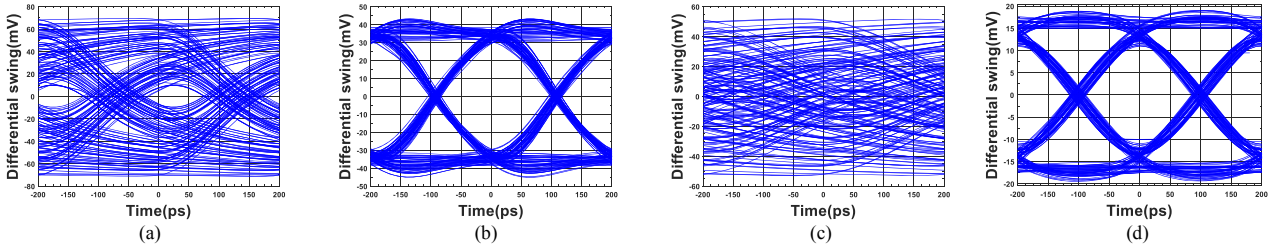


Fig 9. Eye-diagrams of received data @5 Gbps for (a) 29.5" PCB trace w/o equalization (b) 29.5" PCB trace w/ equalization (c) 52" PCB trace w/o equalization (d) 52" PCB trace w/ equalization

TABLE II

Comparison of the proposed bi-directional link with recent literatures

References	Tech (nm)	Suppply (V)	Link Type	Loss @ Nyquist (dB)	Equalization	Data rate (Gbps)	Power (mW)	Efficiency (pJ/b)
[1]	65	1	Uni-directional	15.3	4-tap FFE	12	19	1.6*
[2]	65	1.2 TX, 1 RX	Uni-directional	27.6	4-tap TX FFE, 1-tap FIR, 2-tap IIR RX DFE	16	173.7	10.9
[14]	180	1.8	Uni-directional	-	-	10	450	45
[21]	180	1.8/3.3	Uni-directional	-	-	3.125	48	15.36
This work$	180	1.8	Bi-directional	13.2	2-tap FFE	5	3 (TX+RX) 3.4 (Biasing circuit)	1.28#
				24.4	3-tap FFE			

*only TX power #both TX+RX power, including power in biasing circuits $ simulation

Simulated performance of the Tx with temperature variation is shown in Fig. 8. It is evident from Fig. 8 that, the constant-g_m bias circuit improves the temperature variation characteristic of the output impedance of the CBD and limits its variation within $\pm$ 2.6% for a 0-80°C temperature variation. Whereas, with normal biasing, the CBD shows a 12.8% variation in output impedance and a 50 Ω passive resistor shows around 8% variation, given the same temperature range. Also, the voltage variation of the output impedance for the proposed transceiver for 1.5 V to 2.1 V is limited within $\pm$ 4%, i.e. 48 Ω to 52 Ω. Table-I compares the worst-case variation of the termination impedance, on varying the process, for different termination schemes, where the typical value of the termination impedance is taken to be 50 Ω. Table-II compares the performance of this transceiver with that of some other existing literatures.

IV. CONCLUSIONS

Alleviating the drawbacks of a conventional current-mode FFE Tx, this work presents a new current-mode FFE Tx with enhanced current-efficiency by means of the current-boosting property of the CBD. While implemented in a 1.8 V, 180 nm CMOS process, the Tx shows a current-efficiency of 0.87 and energy-efficiency of 1.28 pJ/b, while transmitting data through a 52-inch FR4 PCB trace at a data rate of 5 Gbps. Also, the design is area efficient as there is no need of large switch for tuning the terminating passive resistor. Biasing the CBD using the constant-g_m bias circuit limits the temperature variation of the output impedance to $\pm$ 2.6%.

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