Exploiting Negative Control Lines and Nearest Neighbor for Improved Comparator Design

Tathagato Bose
India Systems Development Lab
IBM Corporation, Bengaluru, India
tathbose@in.ibm.com

Kamalika Datta
Dept. of Computer Sc. & Engineering
NIT Meghalaya, Meghalaya, India
kdatta@nitm.ac.in

Indranil Sengupta
Dept. of Computer Sc. & Engineering
IIT Kharagpur, Kharagpur, India
isg@iitkgp.ac.in

***Abstract*—In this paper, improved reversible comparator designs are investigated using Multiple Control Toffoli(MCT) gates, improving Quantum Cost(QC) and also Nearest Neighbor Cost(NNC) metrics of circuits. The proposed designs are compared with recent works and found to be efficient in terms of cost by making these nearest neighbor compliant using Swap gate insertions.**

***Keywords*-Reversible logic; Quantum computing; Negative control; Nearest neighbor Architecture;**

I. Introduction

Reversible logic [12] has gained importance due to applications in low-power design methods [2], quantum computing [5], etc. Most of the researchers prefer to use Multiple Control Toffoli (MCT) as the standard gate library which may derive NOT, CNOT [3] and Toffoli [9] gate. As a cost metric, NNC have been considered along with QC [1]. We have exploited swap gates and mixed polarity MCT gates to decrease NNC of respective circuits. Three comparator designs have been investigated in this work.

II. Background

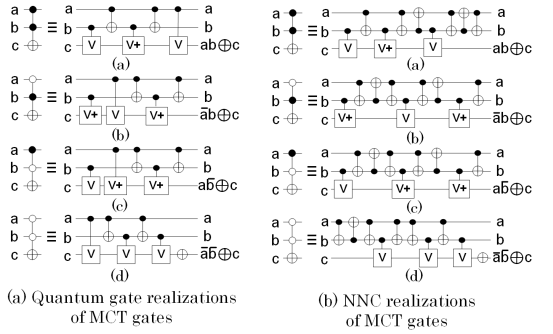
An n-input, n-output logic function is said to be reversible if it implements a bijective function. Quantum computer uses qubits representing state superposition where unitary operations are performed by quantum gates. An n-bit MCT gate reverses the target line if the product of the control-set evaluates to true and passes all other inputs. Additionally, negative-control Toffoli gate has at least one negative control which inverts its target bit. Swap gates are inserted to make the control and target lines adjacent, thereby making the gate Nearest Neighbor compliant (see Fig. 1).

III. Proposed comparator Designs using Negative Control and Nearest neighbor

A. Basic comparator function

Let us consider $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$. The various comparator functions can be expressed in terms of the following conditions, where $X_i = A_iB_i + \overline{A_i}\ \overline{B_i}$.

$A = B$	$X_3X_2X_1X_0$
$A > B$	$A_3\overline{B_3} + X_3A_2\overline{B_2} + X_3X_2A_1\overline{B_1} + X_3X_2X_1A_0\overline{B_0}$
$A < B$	$\overline{A_3}B_3 + X_3\overline{A_2}B_2 + X_3X_2\overline{A_1}B_1 + X_3X_2X_1\overline{A_0}B_0$



(a) Quantum gate realizations of MCT gates

(b) NNC realizations of MCT gates

Fig. 1. Quantum gate realization of MCT gates

B. Reversible serial comparator design

Thapliyal et al. [8] used cascade of cells using Toffoli/AND gates:

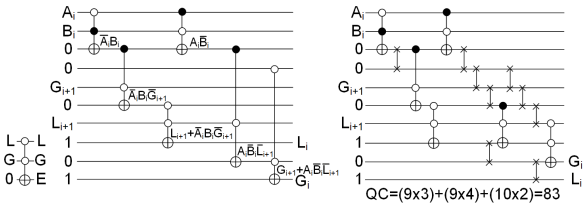
$$L_i = L_{i+1} + \overline{A_i}B_i\overline{G_{i+1}} \quad (1)$$

$$G_i = G_{i+1} + A_i\overline{B_i}\overline{L_{i+1}} \quad (2)$$

$$E_i = \overline{L_i + G_i} \quad (3)$$

Proposed serial comparator design: Fig. 2 uses negative control Toffoli gates that reduce cost. In [8], calculated NNC is $19N+1$ whereas proposed design reduces it to $14N+1$. A comparison is shown in the following for N-bit comparator.

Cost parameter	Design of [8]	Proposed Design
Quantum cost	$39N + 9$	$32N + 6$
Quantum delay	$(35N + 7)\Delta$	$(27N + 6)\Delta$



(a) Proposed 1-bit serial comparator cell

(b) Nearest Neighbor compliant 1-bit serial comparator cell

Fig. 2. 1-bit serial comparator cell

C. Reversible tree based comparator design

Binary tree based comparator [7] contains nodes built in 2-bit comparator cells to combine children's result and forwards

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it to the parent. The root node generates 2-bit comparison result of n-bit numbers and an *Output Circuit* generates *equality* signal. To implement a 2-bit comparator cell [8] we use two *R-Bcomp* (Reversible Binary Comparator) modules made of 2 TR-gates & 1 CNOT gate (QC=9).

Proposed tree based comparator design: Negative control in first TR gate optimizes *R-Bcomp* module (QC=6). From [7], QC (2-bit comparator) = 2 * QC (*R-Bcomp*) + QC (Outside circuitry) = 2 * 9 + 9 = 27. On the other hand, QC (Proposed 2-bit comparator design) = 2 * 8 + 9 = 25.

From the binary tree design of [7], QC = $(N-1)$ * QC (2-bit comp.) + QC (Outside circuitry).

Original design [8]	$(N-1)*27+9 = 27N-18$
Proposed design	$(N-1)*25+6 = 25N-19$

From [8], we calculate NNC(*R-Bcomp* module) is 3 and NNC(outside circuitry) is 15. We insert Swap gates to make the circuitry NN compliant.

TABLE I
COMPARISON OF TREE-BASED N-BIT COMPARATOR

Parameters	Design of [8]	Proposed design
Nearest Neighbor Cost	$(N-1)*23+1$ $= 23N-22$	$(N-1)*13+1$ $= 13N-12$
QC of NN Compliant circuit	$(N-1)*87+13$ $= 87N-74$	$(N-1)*73+10$ $= 73N-63$

D. Reversible prefix based comparator design

In [10], an N-bit comparator contains 3 stages (see Fig. 6 of [7]). Input stage generates *Equal* and *Greater than* signals for a bit pair. The second stage is made of cells with the prefix tree grouping method. It takes inputs from the N first stage cells and generates *Equal* and *Greater than* signals. The final stage generates the *Less than* signal.

Proposed prefix based comparator design: Proposed design optimizes all the three stages.

a) **Stage 1:** Computes *equal* and *greater than* signal:

$$E_i = A_i \oplus \overline{B_i}$$
$$G_i = A_i.\overline{B_i}$$

The design in [10] uses Peres and NOT gate(QC (cell) =5). The NNC of the original design is 1, and to make it 0 the QC incurred will be 9 (i.e. QC (NNC-optimized Peres gate) =8 & QC (NNC Optimized NOT gate) =1). Further, using a combination of NNC-optimized TR and NOT gate (see Fig. 3(a)) reduces the QC to 8.

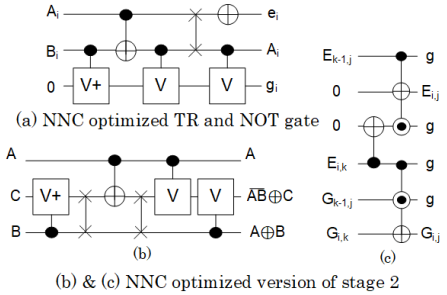

Fig. 3. NNC optimized TR & NOT gate and stage 2

b) **Stage 2:** Groups the *greater* and *equal* signals using black cells. Here, QC (black cell) = 2 * QC (Peres gate) + QC (CNOT gate) = 9. The NNC of this design is 3 where Fig. 3(b) shows the NNC-optimized design. As Fig. 3(c), QC (stage 2) = QC (Swap gate) + QC (3-input NNC-optimized Peres gate with target in the middle) + QC (3-input NNC-optimized Peres gate) = 1 + 10 + 8 = 19.

c) **Stage 3:** Generates *Less than* signal using one Toffoli gate and four NOT gates (total QC =9). Addition of negative controls increases the QC by 6. Reducing NNC of the original design from 1 to 0, leads to incurring a QC of 10.

TABLE II
COMPARISON OF REVERSIBLE PREFIX BASED COMPARATOR DESIGN

Design of [10]	Proposed design
N * QC (First stage cell) + $(N-1)$ * QC (Black cell) + QC (Output circuitry)	N * QC (First stage cell) + $(N-1)$ * QC (Black cell) + QC (Output circuitry)
$N * 5 + (N-1) * 9 + 9$	$N * 5 + (N-1) * 9 + 6$
$14N$	$14N-3$

IV. CONCLUSION

In this paper, the nearest neighbor constraint has improved various comparator designs, namely, serial, tree-based and prefix-based comparators. We have shown the cost reduction methods using mixed-control MCT gates. Later we have exploited Swap gates to make the designs nearest neighbor compliant which aid implementation using ion traps [4] or superconduction transmons qubits [11]. Other additional topological constraints are currently examined by the IBM Q Experience [6].

REFERENCES

[1] A. Barenco, H. Bennett, R. Cleve, D. DiVinchenzo, N. Margolus, P. Shor, T. Sleator, J. Smolin, and H. Weinfurter. Elementary gates for quantum computation. *Physical Review A (Atomic, Molecular, and Optical Physics)*, 52(5):3457–3467, 1995.

[2] C. Bennett. Logical reversibility of computation. *Journal of IBM Research and Development*, 17:525–532, 1973.

[3] R. Feynman. Quantum mechanical computers. *Optic News*, 11:11–20, 1985.

[4] B. Lekitsch, S. Weidt, and A. G. Fowler. Blueprint for a microwave trapped ion quantum computer. *Science Advances*, 3(2), 2017.

[5] M. Nielsen and I. Chuang. *Quantum Computation and Quantum Information*. Cambridge University Press, 2000.

[6] P. Nikolov and V. Galabov. Experimental realization of controlled square root of z gate using ibm's cloud quantum experience platform. *FDIBA Conference*.

[7] P. S. Phaneendra, C. Vudadha, V. Sreehari, and M. Srinivas. An optimized design of reversible quantum comparator. In *27th International Conference on VLSI Design*, pages 557–562, 2014.

[8] H. Thapliyal, N. Ranganathan, and R. Ferreira. Design of a comparator tree based on reversible logic. In *10th IEEE Conference on Nanotechnology (IEEE-NANO)*, pages 1113–1116, 2010.

[9] T. Toffoli. Reversible computing. *Automata, Languages and Programming. Springer, Tech. Memo-MIT/LCS/TM-151, MIT Lab for Comp. Sci*, 1980.

[10] C. Vudadha, P. S. Phaneendra, V. Sreehari, S. E. Ahmed, N. Muthukrishnan, and M. Srinivas. Design of prefix-based optimal reversible comparator. In *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 201–206, 2012.

[11] J. Wang, D. R. Legrain, and L. Bretheau. Gate-tunable transmon qubit made with graphene/hbn heterostructures. *Bulletin of the American Physical Society*, 2018.

[12] R. Wille and R. Drechsler. *Towards a Design Flow for Reversible Logic*. Springer-Verlag, 2010.