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Power and Area Efficient Approximate Heterogeneous 8T SRAM for Multimedia Applications

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***Abstract*— Approximate computing paradigm has emerged as one of the key research fields in area and energy efficient CMOS circuit design for error-tolerant applications like data mining, scientific computing, multimedia applications, etc. Multimedia applications (such as H.264) which use SRAM as storage consume a significant amount of power. In this paper, we propose heterogeneous 8T SRAM memory architectures without and with truncation (2-bit) as storage for low power multimedia applications in smartphones. To the best of our knowledge, this is the first work where both heterogeneous SRAM design and bit-truncation techniques have been simultaneously used to obtain low power memory design for multimedia applications. We show that the proposed techniques provide high image quality even at low power and low area budget of 0.3 μW/pixel and 5.2 μm^2/pixel at 0.5 V and 20 MHz in UMC 28nm. The proposed memory architecture is compared with existing heterogeneous 6T, hybrid 8T/6T, all-identical 6T, and all-identical 8T SRAM memory. The results show that proposed memory architectures perform cumulatively better than existing techniques in terms of dynamic power, leakage power & area. The use of proposed memory for storage of an image has much higher Peak Signal to Noise Ratio (PSNR) and Structural Similarity Index Metric (SSIM) than existing SRAM techniques. The results are verified by Spice simulation performed in UMC 28 nm CMOS technology.**

***Index Terms*: 8T SRAM cell, multimedia applications, approximate computing, bit-truncation, PSNR, BER, SSIM, memory.**

I. INTRODUCTION

Wide-spread availability of the 4G data network has tremendously increased the viewing and sharing of on-line videos in hand-held devices. These video applications are, in general, computationally intensive and require large memory storage and access [1]. The video compression circuits like H.264/H.265/MPEG consume a significant amount of power for storage of frame (image) in SRAM [2]. In fact, it is reported that in H.264 video processor, almost 30% of the total power is consumed in SRAM alone [3]. Video compression circuit generally operates at low-frequency range, from 1-20 MHz [4], which gives an opportunity to a designer to apply VDD scaling method in SRAM. VDD scaling helps in reducing dynamic and leakage power of the SRAM [5]. However, at low voltage, conventional 6T SRAM cell suffers from high bit error rate (BER) [5] which degrades the image/video quality significantly [5]. To resolve this issue, approximate computing method is proposed for multimedia applications, as these applications are inherently tolerant to some amount of errors [1], [3], [4], [6]–[10].

A. Related Work

Owing to the conflicting read and write stability, the 6T SRAM cell shows very high BER [5] at low voltage under the large local and global process variations. To counter this, an 8T SRAM cell has been proposed [11]. It has a read-decoupled structure which enhances the read and write stability. Though 8T SRAM shows better stability as compared to 6T SRAM, 8T SRAM cell requires 20% more area than 6T SRAM.

Considering the fact that errors in higher order bits (HOBs) degrades the visual quality of an image much more than error in order bits (LOBs) [4]. In [4], the authors have made use of hybrid 8T/6T SRAM memory to optimize both stability and area specifically for multimedia applications. As 8T SRAM has low BER, it has been used for 3 HOBs and despite 6T SRAM has high BER, it is used for 5 LOBs to save area. In this way, in [4] memory design is optimized to provide better PSNR for a given area. However, the issue with hybrid 8T/6T SRAM memory is the alignment of 8T and 6T in the same row, as 8T has an additional read-decoupled circuit which needs different pre-charge, read and write circuit as compared to 6T SRAM. This issue has been addressed in [6] where a heterogeneous 6T SRAM memory has been proposed, where the HOBs SRAM cells are designed with a relatively larger area as compared to the LOBs SRAM cells. While this approach is definitely better than homogeneous SRAM design, the sizes required for reducing BER in HOBs demand large area, thereby contributing more to dynamic and leakage power. The requirement of large area in [6] has been addressed and circumvented in [7] where a triple supply voltage technique is used to design the SRAM cell for different bits of a pixel with same sized SRAM to reduce BER. However, it would require multiple level shifters and DC-DC converters which, in turn, would increase the design complexity. Work done in [8] shows the significant power reduction by using hybrid 10T/8T SRAM for multimedia application, but 10T/8T SRAM has very large area penalty.

In summary of the above proposed work, the SRAMs designed for multimedia applications either have large area penalty or design complexing. In this paper, we propose an approximate memory built from heterogeneous 8T SRAM and heterogeneous 8T SRAM with 2-bit (LOBs) truncation,

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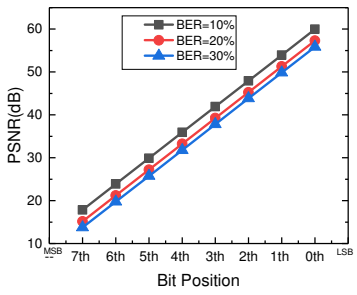


Fig. 1. PSNR Vs. Error Position (The error in MSB are more sensitive to video quality than LSB).

with comparable areas as 6T SRAM but which can operate at 0.5 V in UMC 28nm.

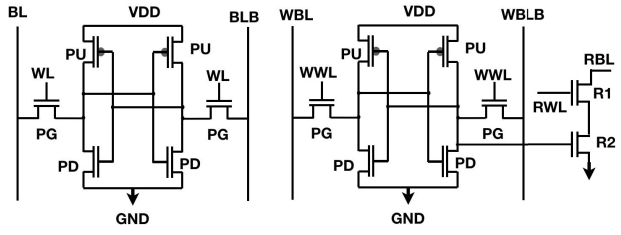
B. Our Contributions

In this work, a 32×32 (1Kb) approximate memory is designed for multimedia applications built from heterogeneous 8T SRAM and heterogeneous 8T SRAM with 2-bit truncation. We have shown that truncation of the 2 LOBs of *chroma* and *luma* pixels do not change the human visual experience of an image, but reduces the leakage power, dynamic power, and area all by 25%. This is because one has now to store only 6-bit out of 8-bit. Apart from this, we also show that under iso-area (equal area) constraint, all-identical (homogeneous) 8T SRAM memory is more suitable for multimedia application in terms of leakage power, dynamic power, and PSNR as compared to all-identical (homogeneous) 6T SRAM. Further, we show that, under iso-area and iso-power constraint, the proposed heterogeneous 8T memory has better performance (PSNR and SSIM) as compared to the other existing schemes. To the best of our knowledge, this is the first paper which uses both heterogeneous (8T) SRAM memory and truncation for multimedia applications. All the Spice simulations are done in UMC 28nm CMOS technology at 0.5 V.

The rest of the paper is arranged as follows. In Section II we present the comparison of 8T SRAM and 6T SRAM memory and its utility for multimedia applications. In Section III we show the effect of truncation on image quality. In section IV, we design the heterogeneous 8T SRAM and heterogeneous 8T SRAM with 2-bit truncation memories for multimedia applications and compare them with existing techniques. We conclude the paper in Section V.

II. Utility of 8T versus 6T SRAM Cell for Multimedia Applications

In this section, we compare the area of 8T and 6T SRAM cells in terms of BER, PSNR, leakage power, and dynamic power. Since multimedia applications generally run at low-frequency ranges from 1-20 MHz [4], and since both 8T and 6T SRAM cells can operate at this frequency range at 0.5 V under worst-case slow nMOS and slow pMOS (SNSP) corner, the supply voltage is fixed at 0.5 V for the rest of analysis.



6-T	W(nm)	L(nm)
PG	160	30
PU	100	30
PD	250	30

(a)

8-T	W(nm)	L(nm)
PG	100	30
PU	100	30
PD	100	30
R1-R2	100	45

(b)

Fig. 2. Schematic of (a) 6T SRAM cell (b) 8T SRAM cell and their sizes.

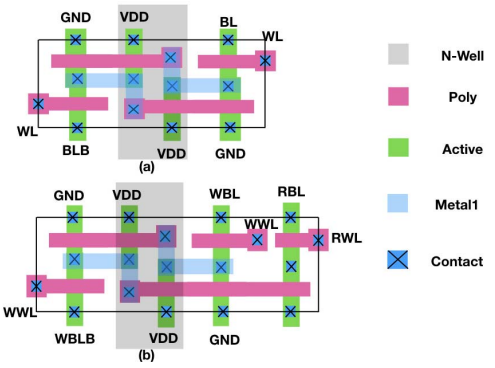


Fig. 3. Layout representation of (a) minimum sized 6T SRAM cell (b) minimum sized 8T SRAM cell.

A. Bit Error Rate Analysis

Fig. 1 shows the effect on PSNR of an image when errors are introduced in different bits of a pixel. PSNR is the metric which gives the quantitative measure to determine the quality of an image with respect to the reference image [6]. High PSNR suggests a better resemblance to the reference image. As demonstrated in Fig. 1, errors injected into the HOBs degrades the PSNR significantly, whereas errors in LOBs do not have any significant effect on the PSNR value [4] [1]. This observation has motivated many researchers to design memory differently for multimedia applications.

Fig. 2(a) and Fig. 2(b) show the schematic of 6T and 8T SRAM cell respectively. The size of the transistors used for a minimum-area 6T and 8T SRAM cell are tabulated and shown with their respective figures. The layouts of the minimum sized 6T and 8T SRAM cell are shown in Fig. 3(a) and Fig. 3(b) respectively. The minimum cell area of the 6T and 8T SRAM are 0.64 μm^2 and 0.76 μm^2 respectively, which shows that minimum sized 8T SRAM cell is 18.75% larger than minimum sized 6T SRAM cell. Although 8T SRAM cell takes higher area, it provides better cell stability than 6T SRAM.

The issue with 6T SRAM cell is that it has conflicting

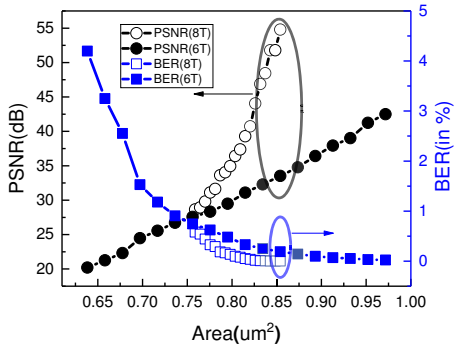


Fig. 4. PSNR and BER versus area for 8T and 6T SRAM cells.

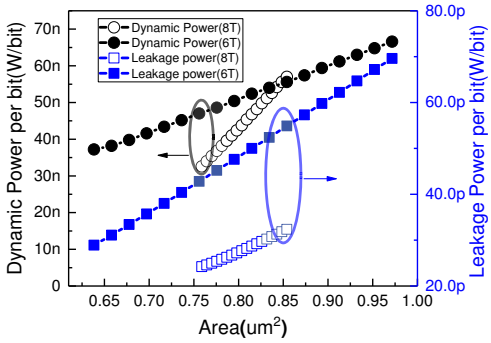


Fig. 5. Dynamic and leakage power per bit versus cell area for 8T and 6T SRAM cell.

read and write stability (improving one degrades the other). In order to improve both read and write margin, all the transistors of the 6T SRAM cell need to be increased simultaneously [6] [1]. On the other hand, 8T SRAM cell has read-decoupled structure and has a sufficiently high read margin. In order to improve the cell stability of 8T SRAM cell, only write stability of the 8T SRAM cell has to be improved [11]. To improve the write stability only pass gate (PG) (shown in Fig. 2(b)) of the cell needs to be increased. Therefore, in order to improve cell stability, all transistors of 6T SRAM cell are increased simultaneously whereas, in the case of the 8T SRAM cell, only the size of PG is increased. Hence, although the minimum-sized 6T SRAM occupies lesser area than minimum-sized 8T SRAM, when 6T and 8T SRAM both sized for reducing failure, the area of 8T SRAM turns out to be smaller than 6T SRAM cell. To find the BER, we have performed 100,000 transient Monte-Carlo (MC) simulations of a cell in 1Kb memory under all the process corners: slow nMOS slow pMOS (SS), fast nMOS slow pMOS (FNSP), slow nMOS fast pMOS (SNFP) and fast nMOS and fast pMOS (FF) at 0.5 V, 20 MHz. We found that in 6T SRAM cell, read BER is high at FNSP corner and write BER is high at SNFP corner. We also observed that read BER is significantly higher than write BER, and hence only read BER is taken into account for 6T SRAM cell. Similar results are reported in earlier works as well [4] [6]. In case of 8T SRAM, write error is found to be high at SNFP. As read is decoupled, there are no read errors at 0.5 V.

1) BER and PSNR versus Area: Fig. 4 shows the BER (right Y-axis) and PSNR (left Y-axis) versus cell area for 8T and 6T SRAM cells. As shown in Fig. 4, as cell area increases, BER reduces for both 6T and 8T SRAM cell. We have increased the area up to a point where BER is reduced to 0.01%. As shown in Fig. 4, to get similar BER, the cell area of 6T SRAM needs to be increased from 0.64 μm^2 to 1.01 μm^2, whereas in 8T SRAM cell, the area needs to be increased from 0.74 μm^2 to 0.83 μm^2. Thus to reduce the BER to 0.01%, area increment required for 8T SRAM cell is mere 12% with respect to minimum sized 8T SRAM cell area, whereas in case of 6T SRAM cell, area increment required is 57% with respect to minimum sized 6T SRAM cell area. It can also be seen from Fig. 4 that, under the same area, PSNR (left Y-axis) obtained in case of 8T SRAM is higher than 6T SRAM as BER of 8T SRAM is lower than 6T SRAM. Hence, it is motivating to use 8T SRAM cell in place of 6T SRAM cell for multimedia applications.

2) Dynamic and Leakage Power versus Area: Fig. 5 shows the dynamic power (read+write) (Left Y-axis) and leakage power (Right Y-axis) per bit versus area (area is increased to reduce BER) in a 1 Kb memory operated at 0.5 V and 20 MHz. As shown in Fig. 5, to reduce the BER to 0.01% in 6T SRAM cell, the cell area needs to be increased due to which dynamic power and leakage power increases by 88% and 158%, respectively, with respect to its minimum sized 6T cell. Whereas, in 8T SRAM cell, the increase in dynamic power and leakage power required are 57% and 24% with respect to its minimum sized 8T cell. The low power penalty required in case of 8T SRAM as compared to 6T SRAM is attributed to the fact that only PG transistor size needs to be increased in 8T SRAM cell, whereas all transistor sizes need to be increased simultaneously in a 6T SRAM cell.

B. Applicability for multimedia applications

To test the applicability of SRAM in multimedia applications, the images are taken in 4:2:0 YCbCr format. Y contains the brightness property of the pixel and Cb, Cr contain the color difference. The images (frames) are extracted from videos (in CIF format) recommended for testing by Joint Collaboration team on video coding [12]. First, we find the BER by performing 100,000 MC Spice simulations in 28nm at 0.5 V. To find the degradation in the quality of an image, the BERs are injected at their respective positions of the pixel using MATLAB. Degradation in image quality is measured using PSNR. Fig. 6 shows the degradation in image quality due to errors in 6T and 8T SRAM cells for iso-area. As shown in Fig. 6, for area constraints of 0.79 μm^2/cell and 0.854 μm^2/cell, the conventional all-identical 8T SRAM based memory provides 2.19 dB and 21.3 dB higher PSNR respectively as compared to the conventional all-identical 6T SRAM. Along with better image quality, 8T SRAM memory has less leakage and consumes less dynamic power for an area of 0.79 μm^2/cell,

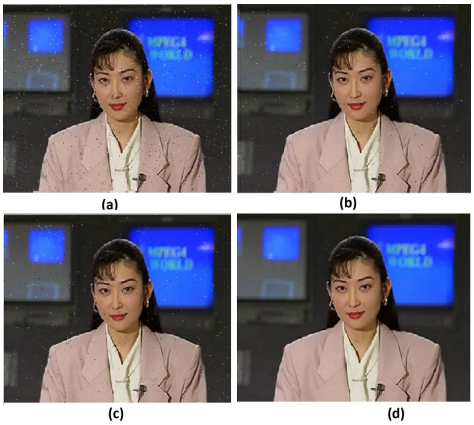


Fig. 6. For an iso-area of 0.79 μm^2/cell (a) 6T SRAM (PNSR= 29.45dB, Dynamic power=403 nW, Leakage power=380 pW) (b) 8T SRAM (PNSR= 31.64dB, Dynamic power=328 nW, Leakage power=213.6 pW), For iso-area 0f 0.854 μm^2/cell(c) 6T SRAM (PNSR= 33.49dB, Dynamic power=444.8 nW, Leakage power=439.2 pW) (d) 8T SRAM (PNSR= 54.8dB, Dynamic power=456 nW, Leakage power=259.2 pW).

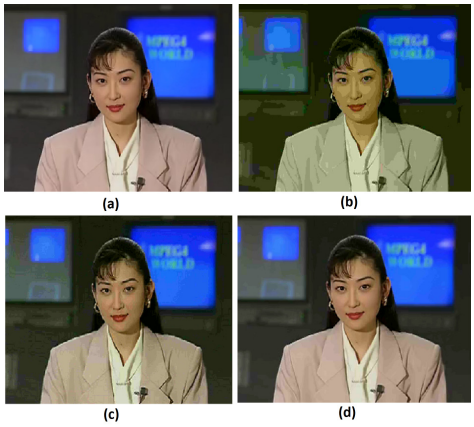


Fig. 7. (a) original (b) 4-bit truncation in the LSB of each Y, C_B,& C_R, (PNSR= 21.8dB) (c) 3-bit truncation in the LSB of each Y, Cb, & Cr (PNSR= 28dB) (d) 2-bit truncation in the LSB of each Y, Cb, & Cr (PNSR= 35.3dB).

and has less leakage power with slightly higher dynamic power for an area of 0.854 μm^2/cell as compared to 6T SRAM. However, for an area of 0.854 μm^2/cell, there is a large benefit in PSNR (by 21dB).

III. Truncation Technique for Multimedia Applications

Bit-truncation is one of the most widely used approximation technique for multimedia applications owing to its simplicity. In the truncation method, some LOBs of pixels are neither stored nor processed as LOBs are not expected to affect the image quality [9]. In our work, we have used 2-bit truncation to design an approximate memory. Fig. 7 shows the effect of truncation on image quality. Fig. 7(a) is the original image while Fig. 7(b), Fig. 7(c) and Fig. 7(d) show the effect on image quality due to truncation of 4, 3 and 2 LOBs in each of Y, Cb and Cr components, respectively. As shown in Fig. 7(b) and Fig. 7(c), the degradation in image quality is noticeable and changes the visual experience as the PSNR is 21.81 dB and 28 dB, respectively. However, Fig. 7(d) shows high resemblance to the original image with PSNR 35.5 dB, where 2-bit truncation is used. Hence, in this paper, we have proposed 2-bit truncation in heterogeneous 8T SRAM memory architecture to reduce power in multimedia applications.

IV. Bit-truncated Heterogeneous 8T Memory for Multimedia Applications

In this section, we discuss the design of our proposed heterogeneous 8T SRAM and heterogeneous 8T SRAM with bit-truncation to store an image for low power multimedia applications. Heterogeneous memory is designed in such a way that for HOBs, larger sized SRAM cells are used, and for LOBs, smaller sized SRAM cells are used. Since we have already noted that image quality is more sensitive to HOBs of an image pixel than LOBs, we have assigned a larger size to HOBs than LOBs to reduce BER in HOBs.

Algorithm 1: Maximize PSNR under Given Power Budget

Input: Power Budget: P_{MAX}, Supply Voltage
Output: Optimal sizing of SRAM cell, C_{opt}

Set MSE_{MAX} =255
Find all combinations, C_k under given power budget P_{MAX}
// C_k is area required for each SRAM cell, where,
// k=0,1,2...,7
Arrange combination of cells in decreasing order of area
// Larger area cells are allocated for HOBs,
// (C_7- maximum area, C_0- minimum area)
For all C_k, do
$MSE_k \leftarrow \sum_{i=0}^{7}(2^i \times BER_i)$
if $MSE_k < MSE_{MAX}$ then
$MSE_{MAX} \leftarrow MSE_k$
// C_k corresponds to minimum MSE_{MAX} provides the
// optimal area
$C_{opt} \leftarrow C_k$

Output: c_{opt} corresponds to minimum MSE

A. Algorithm for designing heterogeneous memory

In this section, we explain the algorithm used for optimal area selection for a given power budget. To design optimized heterogeneous memory, the algorithm works for the following two cases: (1) fixed power budget and (b) fixed area budget. The outcome of the algorithm is a set of SRAM cells of different sizes which provides minimum mean square error(MSE) or maximum PSNR, under a given power or area budget. Algorithm 1 is used to maximize the PSNR under given power budget where the area of SRAM for luma/chroma pixel of 8-bit is represented as $C = (< C_7, C_6, ...C_0 >)$ and for 6 bit, $C = (< C_7, C_6, ...C_2 >)$ (for heterogeneous 8T with 2-bit truncation). Here C_7 and C_0 corresponds to the area of MSB and LSB bit of a pixel

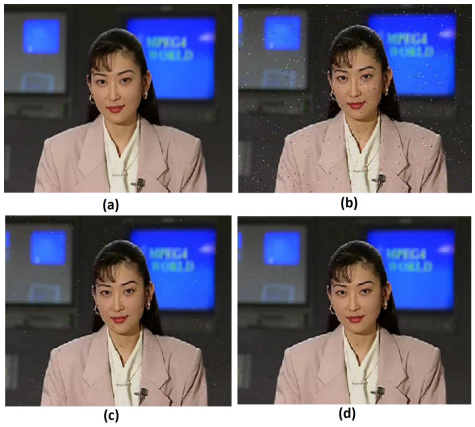


Fig. 8. For a Power Budget of 0.3μW (a) original (b) Identical 8T (PNSR= 31.1dB, SSIM=0.84) (c) Heterogeneous 8T (PNSR= 38.5dB, SSIM=0.99) & (d) Heterogeneous 8T with truncation of 2-bit in each LSB of luma and chroma pixel (PSNR= 35.3, SSIM=0.983).

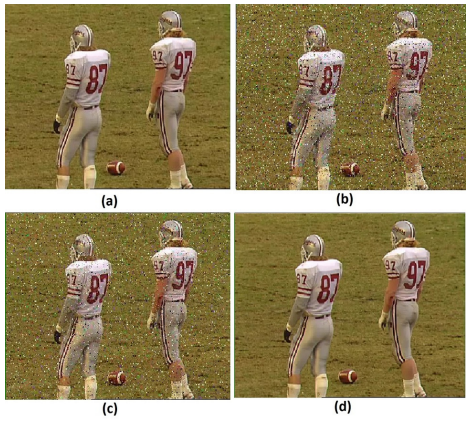


Fig. 9. For an Area Budget of 5.2 μm^2(a) original (b) Identical 6T (PNSR= 20.2dB, SSIM= 0.63) (c) Heterogeneous 6T (PNSR= 22.2dB, SSIM= 0.727) &(d) Heterogeneous 8T with truncation of 2-bit in each LSB of luma and chroma pixel (PSNR= 35.5, SSIM= 0.99).

respectively. We chose 20 different cell areas and found all the possible 8-bit combinations of area C under the given power budget, using MATLAB. These are then arranged in decreasing order so that the highest area is provided for MSB, in the decreasing order of area from MSB to LSB. MSE is calculated for each of these combinations. The sizes correspond to *minimum* MSE are considered as the optimal sizes for 8 bit. A similar algorithm is also applied for a fixed area budget, where the inputs are area budget and voltage, instead of power budget, and voltage.

Using this algorithm, heterogeneous memory is designed using 8T SRAM (for 8-bit) and 8T SRAM with 2-bit truncation. The existing heterogeneous 6T SRAM cell [6] is also designed using a similar algorithm by taking 20 different SRAM sizes in 28nm at 0.5 V. Under the same power budget all-identical 6T SRAM, all-identical 8T SRAM and hybrid 8T/6T SRAM [4] memories are also designed. Fig. 8(b), Fig. 8(c) and Fig. 8(d) show the images obtained after the image was processed through the all-identical 8T SRAM, heterogeneous 8T SRAM & heterogeneous 8T SRAM with 2-bit truncation. From Fig. 8(b), we observe that errors in MSBs cause dots to appear in an image when such memory is used for storage and quality of an image is degraded.

As shown in Fig. 8, image quality for heterogeneous 8T SRAM is much better as compared to all-identical (homogeneous) 8T SRAM. This is because of low BER in HOBs in heterogeneous 8T SRAM due to the larger area. We also note from Fig. 8(d), that the image stored in heterogeneous 8T SRAM with 2-bit truncation has a better resemblance to the original image as compared to the heterogeneous 8T SRAM memory. This is because since the two LOBs are removed, the HOBs can be further increased in sizes for a given power budget. These further reduce BERs in HOBs leading to better image quality. It can be concluded that even though heterogeneous 8T SRAM with 2-bit truncation has lesser PSNR than heterogeneous 8T SRAM cell, it has better image quality. This is because two LOBs has a very little impact on the visual appearance of the image.

We have, therefore, used another relevant metric, the structural similarity index metric (SSIM), for quality comparison of images. Ideally, SSIM=1. In [13], authors claim that SSIM metric provides a better quantitative measure for quality of image than PSNR metric. As shown in Fig. 8, the use of heterogeneous 8T SRAM for storage of an image has SSIM=0.99 and heterogeneous 8T SRAM with 2-bit truncation has SSIM=0.98, which are sufficiently high, which shows that the proposed technique does not visually deteriorate the image quality during storage. In contrast, for Fig. 8(b), SSIM=0.84, which also shows degradation in image quality.

Table I shows the comparison results of our proposed SRAM architecture with other existing ones for a power budget of 0.3 μW (Fig. 8). As shown in Table I, heterogeneous 8T SRAM (proposed-1) has an enhancement in PSNR by 7 dB, 19 dB, 17 dB, and 7.5 dB as compared to the all-identical 8T, all-identical 6T, Heterogeneous 6T, and hybrid 8T/6T SRAM memory, respectively and heterogeneous 8T SRAM with 2-bit truncation shows the improvement in PSNR by 4.18 dB, 15.5 dB, 14.1 dB, and 4.47 dB as compared to all-identical 8T, all-identical 6T, heterogeneous 6T, and hybrid 8T/6T SRAM memory architecture, respectively. It can also be observed that heterogeneous 8T SRAM with 2-bit truncation has better (0.983) SSIM as compared to the other existing techniques.

We also performed the experiment with the minimum area constraint. For this, we have considered hybrid 8T/6T SRAM implementation where MSB uses 8T SRAM cell and all other bits use 6T SRAM cell. We found that the minimum area required for implementing all-identical (homogeneous) 6T SRAM is 5.1 $\mu m^2/pixel$ and for 8T/6T hybrid SRAM (with only MSB implemented as 8T) design it is 5.2 $\mu m^2/pixel$. But under these tight area constraints, we could not be able to implement all-identical 8T and heterogeneous 8T SRAM memory, as all-identical 8T SRAM requires a minimum area budget of 6.07 μm^2/pixel. However, we could design heterogeneous 8T SRAM with 2-bit truncation. From Fig. 9(d), it

TABLE I

FOR A POWER BUDGET OF 0.3 μW FOR FIG. 8 (AKIYO IMAGE)

	8T(Identical)	6T(Identical)	6T(Heterogeneous) [6]	Hybrid 8T +6T [4]	**Proposed – 1** Het-8T	**Proposed – 2** Het-8T with 2-bit Trunc
PSNR	31.12	19.76	21.20	30.83	**38.51**	**35.3**
SSIM	0.84	0.38	0.42	0.78	**0.99**	**0.983**
Area (μm^2/pixel)	6.24	5.10	5.14	5.53	**6.22**	**5.00**
Leakage Power (pW/pixel)	203	231	236	221	**205**	**179**

TABLE II

FOR AN AREA CONSTRAINT OF 5.2 μm^2/PIXEL FOR FIG. 9(RUGBY GAME)

	8T(Identical)	6T(Identical)	6T(Heterogeneous) [6]	Hybrid 8T +6T [4]	**Proposed – 1** Het-8T	**Proposed – 2** Het-8T with 2-bit Trunc
PSNR	N/A	20.2	22.2	24.6	**N/A**	**35.5**
SSIM	N/A	0.63	0.72	0.82	**N/A**	**0.99**
Dynamic Power(nW/pixel)	N/A	297	302	293	**N/A**	**350**
Leakage Power(pW/pixel)	N/A	231	240	226.5	**N/A**	**197**

can be seen that image obtained by using heterogeneous 8T with 2-bit truncation has very good resemblance with the original image, whereas in all-identical 6T (Fig. 9(b)) and heterogeneous 6T SRAM architectures (Fig. 9(c)) the image quality degrades significantly. The same can be confirmed by the PSNR and SSIM values. Table II shows the comparison results with the existing techniques under the area budget of 5.2 μm^2/pixel for an image shown in Fig. 9(a). When compared with all-identical 6T SRAM, 6T heterogeneous and hybrid 8T/6T, our proposed heterogeneous 8T with 2-bit truncation improves the PSNR by 15.2 dB, 13.3dB, and 10.9 dB respectively but has slightly more dynamic power/pixel than existing techniques. Further, the proposed technique has very high SSIM value (0.99). To conclude, the proposed heterogeneous 8T SRAM with 2-bit truncation memory architecture provides high image quality even at low power and area budget of 0.3 μW/pixel and 5.2 μm^2/pixel. The proposed technique also has a significant reduction in leakage power compared to other designs.

V. CONCLUSIONS AND FUTURE EXTENSIONS

Multimedia applications are being widely used in the battery operated hand-held devices like smartphones, i-pads etc., which consume significant power. In this paper, we have proposed heterogeneous 8T SRAM design and *heterogeneous 8T SRAM with 2-bit truncation* that are highly suitable for multimedia applications as they consume very low power and require less area. Bit-truncation and heterogeneous SRAM design have been combined together to obtain a significant reduction in area and power requirements of SRAM designs, without degrading image quality. We have shown that the proposed memory architectures provide good image quality even at low power and area budgets of 0.3 μW and 5.2 $\mu m^2/pixel$, respectively. The applicability of the proposed technique is shown for multimedia applications and can be extended to the other data-intensive applications.

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