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Adaptive Fractional Open Circuit Voltage Method for Maximum Power Point Tracking in a Photovoltaic Panel

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***Abstract*— The output power of a Photovoltaic (PV) panel changes with solar insolation and temperature. Also the P-V (Power-Voltage) and I-V (Current-Voltage) characteristics of a PV cell is highly non-linear. Hence the maximum output power from the PV panel is achieved at a particular voltage (V_{MPP}) and current (I_{MPP}). To improve the overall efficiency, it is important to keep the PV panel to work at Maximum Power Point (MPP). This paper presents an Adaptive Fractional Open Circuit Voltage (AFOCV) method to track the MPP. It does not require the PV panel characteristics to be known in advance. In the proposed circuit, the fraction (k) is estimated adaptively i.e. k is estimated once and then used for a certain period of time to determine the MPP. Again after sometime a new k (that might change due to change in solar insolation) is estimated. In the proposed circuit, for different values of k the output power from the PV panel is calculated and the power levels at two consecutive points on the PV panel is compared. When the MPP is reached that value of k is locked in the fractional voltage generator block and all other blocks are turned off so as to reduce the power consumption. The proposed circuit is designed in a 180 nm CMOS process.**

Keywords: Energy harvesting, maximum power point, adaptive fractional open circuit voltage, fractional open circuit voltage, photovoltaic panel.

I. INTRODUCTION

ENERGY charge batteries. It can also be deployed to provide scavenging is becoming a popular alternative to the supply voltage to the sensors installed in remote places where replacing or charging a battery is not so easy [1]. The ambient light source can be used for low power consuming indoor remote sensors by using amorphous silicon PV cells to convert the light into electrical energy [2]. Among many different energy harvesting sources, solar cells provide the higher amount of energy per unit area

Photovoltaic cells are used to convert solar energy into electrical energy. The P-V and I-V characteristics of a PV panel are shown in Fig. 1 and these characteristics are non-linear. The maximum power from the PV panel is achieved only at a particular voltage (VMPP) and current (IMPP). Further, the characteristics of the PV panel changes with the level of insolation. The process of tracking this MPP is known as Maximum Power Point Tracking (MPPT). Usually, DC-DC converters are used to set the output voltage of the PV panel to the MPP, this gives the maximum output power [3].

Different topologies have been proposed for MPPT such as Fractional Open Circuit Voltage (FOCV), Perturb and Observe (P&O) and Incremental Conductance method [4]. A 3-points based hill climbing method was used in [5]. This circuit is quite novel though the power consumption is quite high (25 uW). In [6], a new method for MPPT is proposed the architecture is quite complex and also only a Verilog-A block design is presented. In [7], a classic hill climbing based MPPT method is used. But in this circuit, there is a limit on the load i.e. the load should have a constant voltage. A novel low power MPPT is proposed in [8] which is used for low light intensities for the indoor conditions. A universal energy harvesting system is proposed in [9]. This system is adaptable to various energy sources.

According to the FOCV method the MPP voltage is fraction of the open circuit voltage i.e.

$$V_{MPP}=k*V_{OC} \text{ - - - (1)}$$

where k (0.7-0.8) is a constant of proportionality depending on the PV panel characteristics [4]. So the variation in the value of k with PV panel characteristics is one of the disadvantage of the FOCV method [7]. In this paper, we are proposing a novel method called Adaptive Fractional Open Circuit Voltage (AFOCV) method where the proportionality constant k is determined adaptively. The AFOCV algorithm is discussed in Section II. The system and circuit design for the AFOCV is presented in Section III. Section IV discusses the results verifying the proposed method. Finally Section V concludes the work with the future scope.

II. ADAPTIVE FRACTIONAL OPEN CIRCUIT VOLTAGE ALGORITHM

The flowchart showing the algorithm for the adaptive fractional open circuit method is shown in Fig. 2. In the proposed algorithm the PV panel characteristics need not be known in advance. This is an iterative algorithm, where k is estimated adaptively. The algorithm consists of two sessions namely "Estimate k" and "Wait session". In the "Estimate k" session, the algorithm carries out a certain number of power comparisons corresponding to different values of k and once the MPP is reached that k value is stored. In the Wait session,

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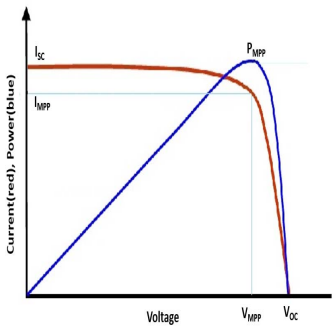


Fig. 1: PV panel I-V and P-V characteristics

the value of k is locked and used for a certain period. The above steps are repeated after a certain time.

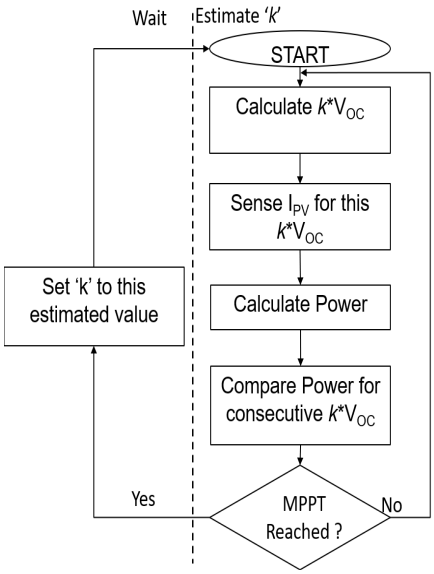
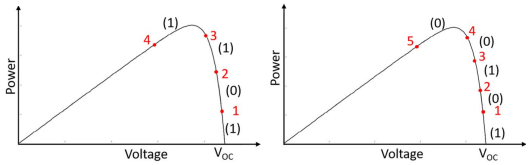


Fig. 2: AFOCV Algorithm Flow Chart

The indication for the MPP is given by the power (output power from the PV panel) comparison results. These power values are stored on capacitors. Let's take an example for a PV panel characteristics for a particular solar insolation as shown in Fig. 3. If the first value of k chosen is corresponding to point 1 and the next value of k is corresponding to point 2 in Fig. 3a, so the power comparison result (with power corresponding to point 1 as input to positive terminal and corresponding to point 2 to the negative terminal of comparator) for these two points from the comparator will give output to be 0 (as shown by (0) between 1 and 2 in Fig. 3a). Now the capacitor where power corresponding to point 1 was stored is charged with power corresponding to point 3 (the power at the capacitor for point 1 is updated because it had the least power between points 1 and 2) and again the comparison between the power for points 2 and 3 is made and the output from the comparator will be 1 (as shown by (1) between 2 and 3 in Fig. 3a). Similar power comparison is done until MPP is reached.

If to reach the MPP an even number of comparisons was done as shown in Fig. 3a then the instance when the output from the comparator is '1' (high) for two consecutive cycles indicates that MPP is reached. Similarly, for the odd number of comparisons, the output from the comparator will be '0' (low) for two consecutive cycles as shown in Fig. 3b.



(a) with even no. of comparisons (b) with odd no. of comparisons

Fig. 3: PV panel P-V characteristics (1, 0 (red) inside the bracket is the output of the comparator for two consecutive power comparison)

III. System and Circuit Design of the AFOCV MPPT Circuit

The block diagram for the proposed AFOCV is shown in Fig. 4. F_{CLK} is the clock for the converter and F_{MPPT} is a very low frequency MPPT clock that starts the "Estimate k" Block to start estimating a value of k. The two integral part of the AFOCV are Power Stage and "Estimate k" Block. The sub blocks of the AFOCV architecture are explained below:

A. Power Stage

The power stage is a boost converter as shown in Fig. 4. At the input of the converter, a capacitor is used to supply the instantaneous current to the boost converter. Boost converter is used between the source and the load to step up the input voltage. During ON time, M1 switch becomes ON and inductor (L) will store the energy and during OFF time the stored energy of the inductor will be transferred to the output through the diode (D). The load resistance R_L is connected at V_{out}.

B. Fractional Voltage Generator

A resistive voltage divider is used to get the fraction of the V_{OC}. The control signal for the switches S_1,S_2,S_3,S_4 is generated using UP/DWN counter. By controlling these switches different values of V_F (fraction of V_{OC}) are generated. The resistance are selected such that R_5>R_4>R_3>R_2>R_1. The value of k generated by voltage divider lies between 0.7-0.9. The state machine for UP/DWN counter is shown in Fig. 5. When a positive edge of SAMPLE arises and DISABLE=0 then a new sequence will be generated resulting in the operating point moving towards the MPP point. If DISABLE=1 and a positive edge of SAMPLE arise then the UP/DWN counter will be locked to the previous state since after that all the control blocks will be switched off resulting in NO sample signal generated from pulse generator block. Now again UP/DWN counter will be turned on when the positive edge of CLK_{MPPT} arises. Finally,

$$V_F = \frac{V_{OC} * R_5}{R_5 + \overline{S_4} * R_4 + \overline{S_3} * R_3 + \overline{S_2} * R_2 + \overline{S_1} * R_1}$$

C. Pulse Generator Block

The input to the pulse generator block is CLK_{MPPT}, V_{hys}, TG_{sel} and its output is SAMPLE, TG and CLK_{comp}. The pulses to be generated are shown in Fig. 6. When a negative edge of MPPT clock arise, the pulse generator block generates the SAMPLE, TG and clock for the power comparison comparator in a sequence shown in Fig. 6. These pulses are generated using a digital circuit which is designed using D-Flip Flops, logic gates and delay units.

D. Power Comparison Block

The power comparison block consists of two capacitors (C_4 and C_5) for storing the output power from PV panel for two consecutive points and a latched comparator for comparing these two powers for two values of k. The circuit for the latched comparator [10] is shown in Fig. 7. When the clock is low then M3 and M4 are ON (Di+, Di- nodes charged to Vdd) and due to this M8 and M11 will be ON and output is low. When CLK is high then Di+ and Di- nodes will be discharged and the rate of discharge of these two nodes will depend on the sign of In+ - In- and hence output

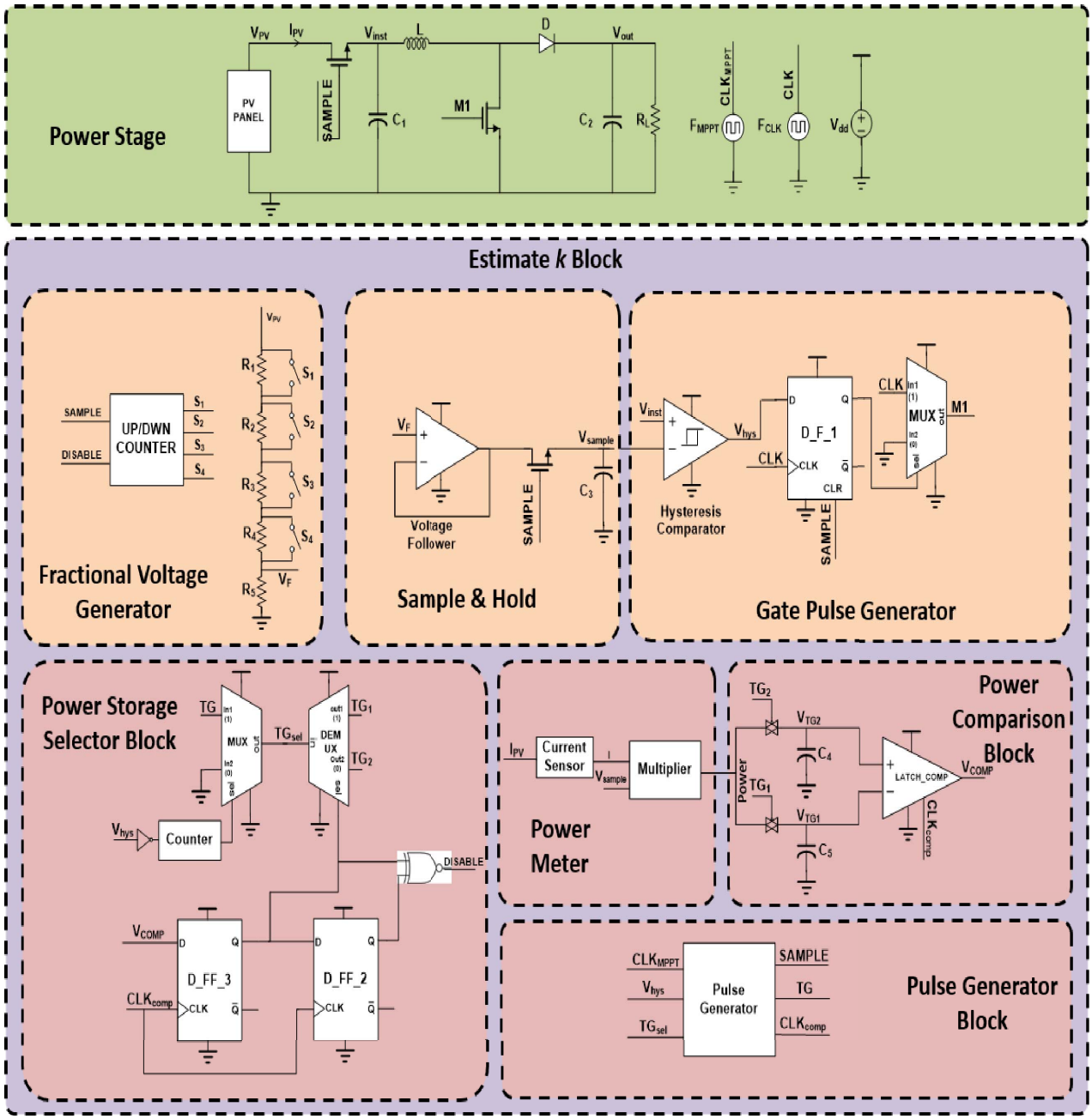


Fig. 4: Block Level Design for Adaptive Fractional Open Circuit Voltage

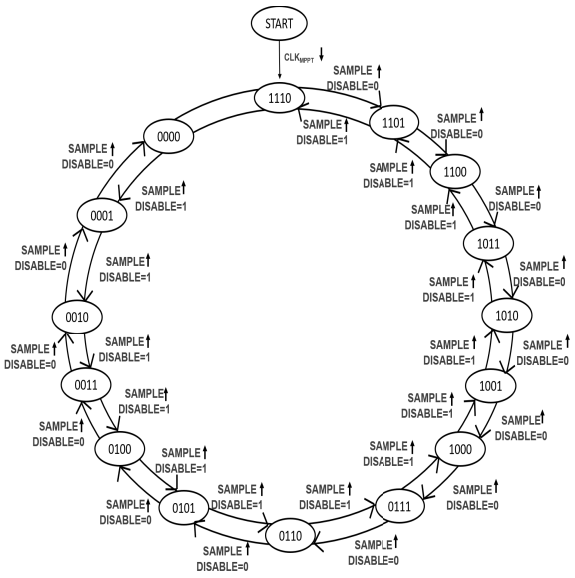


Fig. 5: State Machine for UP/DWN Counter

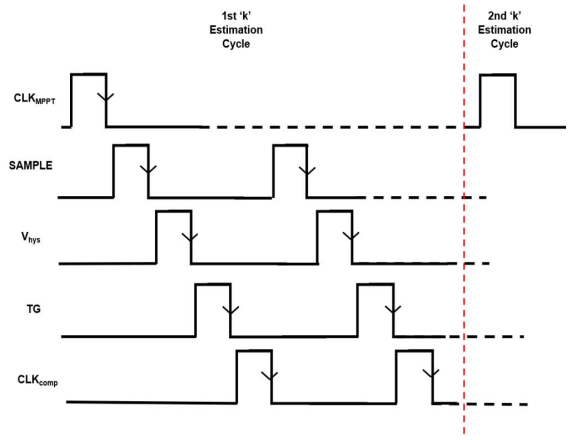


Fig. 6: Series of pulses generated from the Pulse Generator Block

will become high (In+>In-) or low (In+<In-).

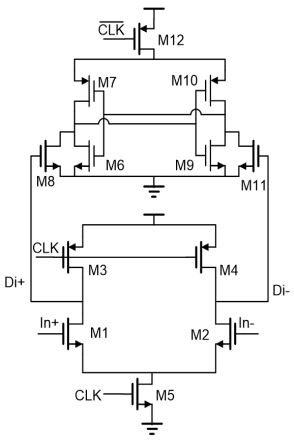


Fig. 7: Double Tail Latch Comparator Circuit

E. Power Storage Selector Block

This block gives the information about which capacitor (C_4 or C_5) stores the power corresponding to the particular value of k. Since the power corresponding to k will be stored either on C_4 or C_5 so TG will be selected by a multiplexer and passed to TG_1 or TG_2 on the basis of previous comparator outputs which is stored in D_FF_3. D_FF_3 and D_FF_2 form a shift register where two consecutive comparator outputs are stored and the XNOR of these two outputs of the shift registers decides whether the MPP point is reached (DISABLE=1) or not (DISABLE=0).

F. Power Meter

This block calculates the output power from the PV panel. It consists of a current sensor to sense the PV panel output current and a Multiplier to multiply the current(I_{PV}) to voltage(V_F) to calculate the power. For the verification of the idea, we have used Verilog-A blocks for the current sensor and multiplier to calculate the power.

G. Gate Pulse Generator Block

The gate pulse generator circuit is used to give the gate pulse to transistor M1. The circuit for the hysteresis comparator [11] is shown in Fig. 8. The hysteresis comparator is used to control the PV panel within a certain band of the MPP voltage. The input to the hysteresis comparator is the PV panel instantaneous voltage (V_{inst}) and V_{sample}. When the V_{inst} tries to go above the upper threshold $V_{sample}+\Delta V$ the hysteresis comparator output (V_{hys}) becomes high (1.8 V) and when V_{sample} tries to go below lower threshold $V_{sample}-\Delta V$, V_{hys} becomes low (0 V). There is an internal positive feedback in the hysteresis comparator. For this positive feedback to sustain the ratio $\frac{(W/L)_6}{(W/L)_3}$ and $\frac{(W/L)_7}{(W/L)_4}$ should be greater than 1. In the present circuit, $\frac{(W/L)_{6,7}}{(W/L)_{3,4}}$=2.2. Let's assume initially V_{inst} is very less compared to V_{sample} hence all of I_5 will flow through M1 and I_2 will be very less. Now V_{sample} will increase and the point at which I_6 becomes equal to I_2 is the point of the upper threshold. Now at certain point whole I_5 will flow through M2 and now PV panel will be connected to the load hence its voltage will decrease making current I_2 to decrease and I_1 to increase, the point at which I_1 becomes equal to I_7 is the point of lower threshold. The second stage formed by transistors M11, M12, M9, M10 is used to get the full swing in the output. The two CMOS inverters placed at the output act as a buffer state and reduce the propagation delay.

Now the output of the hysteresis comparator is used to give the gate pulse to M1. The voltage V_{hys} is connected to the input of the edge triggered D flip-flop. When V_{hys} is high and the positive edge of the CLK arrives then the output of the D flip-flop will also be high and hence CLK will be selected by the multiplexer and it will be given as the input to the gate of M1. When V_{hys} is low then the ground will be selected at the output of the multiplexer and no gate pulse will be given to M1.

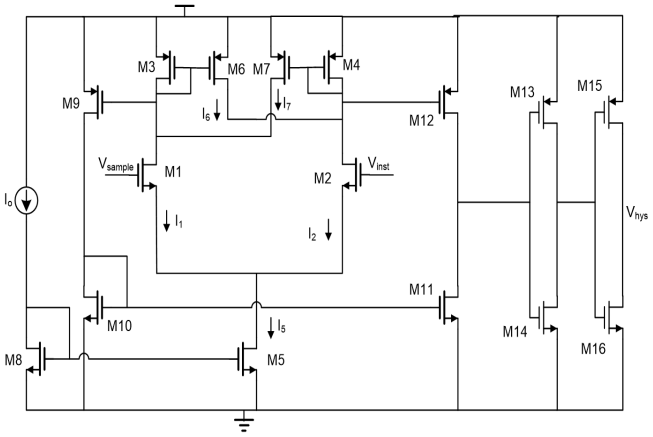


Fig. 8: Circuit for Hysteresis Comparator

IV. Simulation Results

Fig. 9 shows the one diode model for a single PV cell [12]. Fifty of such cells are used in parallel to get the PV panel used in the simulation. The specification for the PV panel is shown in Table. I.

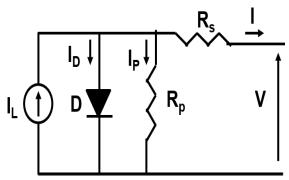


Fig. 9: PV Cell equivalent circuit

The parameters/specifications for the circuit in Fig. 4 is shown in Table. II. For verification of the algorithm we have used two switches in the fractional voltage generator, so four values of k will be taken and one of them will correspond to the MPP.

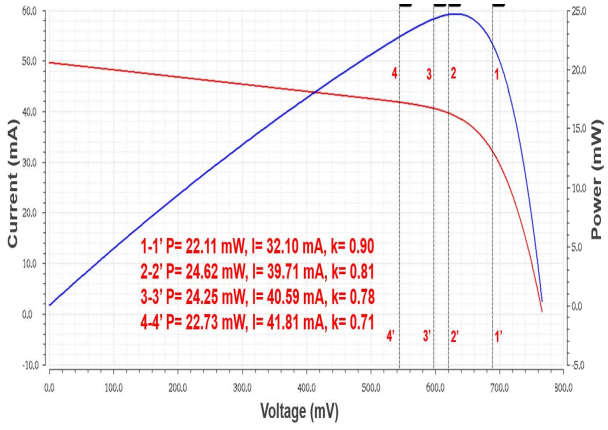


Fig. 10: P-V (blue) and I-V (red) curve for photovoltaic panel with the power, current, voltage and k values labelled

Fig. 10 shows the P-V and I-V curve for the PV panel used in the proposed circuit. The resistances in the fractional voltage generator (R_1, R_2, R_3) are selected such that four values

TABLE I: PV Panel specifications

Parameter	Value
R_S	3.49 kΩ
R_P	3.49 kΩ
V_{MPP}	0.638 V
V_{OC}	0.766 V
I_L	50 mA
I_{MPP}	37 mA

TABLE II: Specifications for the AFOCV circuit

Parameter	Value
C_1	10 uF
C_2	10 uF
C_3	333 pF
$C_{4,5}$	10 pF
R_L	10 kΩ
R_1	1.786 MΩ
R_2	1.389 MΩ
R_3	1 MΩ
R_5	2.113 MΩ
V_{dd}	1.8 V
F_{MPPT}	0.5 mHz
F_{CLK}	1 MHz
L	600 nH
I_o	100 nA
ΔV	5 mV

for k are 0.9(S_1=1,S_2=1), 0.81(S_1=1,S_2=0), 0.78(S_1=0,S_2=1), 0.71(S_1=0,S_2=0) marked by dashed line 1-1', 2-2', 3-3', 4-4' in Fig. 10.

Fig. 11 shows the waveform for the whole system. It can be seen that whenever V_{PV} is within the set band (by the hysteresis comparator) the output of the hysteresis comparator becomes high, thus enabling the gate pulse for the converter. At the negative edge of the V_{hys} TG becomes high and the power is stored on either one of C_4 or C_5 depending on the algorithm explained in Section III for the power storage selector block. When the output from the comparator is same for two cycles (marked by line 2-2' and 3-3' in Fig. 11) the MPP is reached i.e. the value of k for the previous cycle (k corresponding to 2-2') is the k corresponding to MPP. In Fig. 11 DISABLE becomes high after 3-3' indicating that k corresponding to MPP is the k in the previous cycle. Hence the UP/DWN counter will go in down mode and will be locked in that state. Therefore from these four k values k=0.81 is the k corresponding to MPP.

V. Conclusion

In this work, we have proposed a novel Adaptive Fractional Open Circuit Voltage method for MPPT for a PV panel. The circuit is designed in a 180 nm CMOS process. The proposed method has resolved one of the disadvantage (k changing with PV panel characteristics) of the fractional open circuit voltage MPPT method by adaptively estimating k. One more advantage of the proposed circuit is that as soon as k is estimated all the high power consuming blocks are switched OFF and only the power stage, sample & hold and gate pulse generator blocks are ON which consume much less power, hence reducing the total power consumption of the circuit. The future work involves the circuit design for the power meter and then finally the layout of the design.

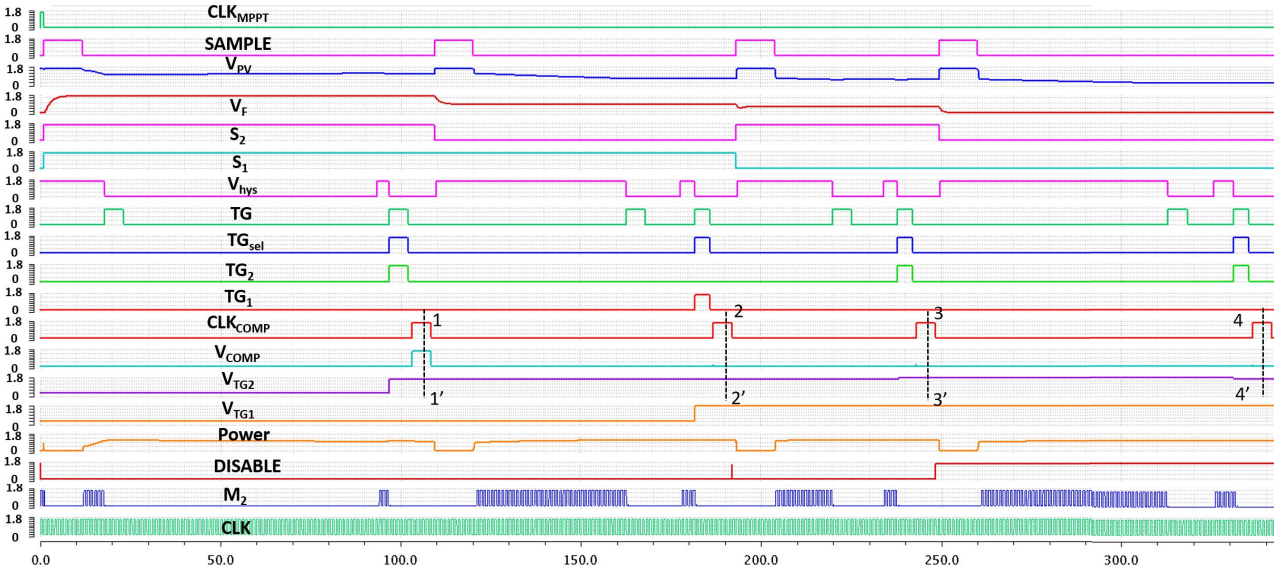


Fig. 11: Waveforms for the Improved FOCV circuit(for 2 switches in fractional voltage generator, y-axis is in Volts(V))

VI. Acknowledgement

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