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Delay Skew Reduction in IO Glitch Filter

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***Abstract*— Glitch filtering is an integral part of digital input signal conditioning. Filtering introduces delays in the system. Mismatches in rise and fall delay of the filter causes duty cycle distortion in the input resulting in system failure. A timing failure occurred in a product fabricated in CMOS 140nm TSMC process due to delay mismatch in IO glitch filter. A failure analysis is done and capacitor asymmetry at low voltage is found to be the root cause of delay mismatch. Drive transistor DC mismatch and output inverter threshold asymmetry were also contributing factors. The reasons of delay mismatch are analyzed and the steps taken to solve them are described in this paper**

Keywords— glitch filter, signal integrity, capacitor asymmetry, DC mismatch

I. INTRODUCTION

With the advent of IoT, cloud computing and the like, new age technology has assumed a hitherto non-existent dominant position in the lives of everyone. From automated cars to unmanned jets, the people of today increasingly rely on these devices to perform as expected. This relies on the ability of different devices to establish reliable and accurate communication leading up to a network in which each member is required to interpret and act on signals originating from a different type of device. Every device in a network is expected to follow the protocol and any flaw in signal integrity has the potential to cascade through all devices in communication [1].

Although many models exist to accurately predict signal propagation in communication channels, they fall short of modelling glitches which occur in digital systems. [2] provides an account of how no existing continuous-time, binary value-domain model for digital circuits can correctly capture glitch propagation. The paper discusses the near impossibility of analysing circuitry with glitches assumed to be present.

Hence, it is of paramount importance to ensure that the signals so involved are free from 'glitches', guaranteeing characteristics that would result in proper switching of every device in the system. At the signal input of a digital system, glitches can occur due to switch bounce, slow switching signals, noise etc. Therefore, it is prescient to account for glitches before and during system design than to make systems without adequate mechanisms to counter the glitch phenomenon.

The only way to counter the action of glitches is to eliminate glitches before they make their presence felt. There are many methods to achieve this purpose as detailed in [3]. But the premium on silicon real estate preclude such solutions, prompting the need for a solution possessing as small a footprint as possible. Spurious glitches not only increase the power consumption [4][5], but also can create false switching resulting in system failure. A good input signal conditioning system should remove spurious glitches without affecting the signal input.

A glitch filter is a circuit designed to stop pulses of narrow width, while allowing the passage of pulses of larger width. The circuit removes chatter and extraneous noise in digital systems. Communication protocols such as SWP, IIC, SLIMbus, I2C etc. necessitate the presence of glitch filters as an important component of most Input/Output circuits [5].

Glitch filter invariably adds a delay to the input signal. Theoretically this delay should be more than or equal to the maximum width of pulses removed by the filter. Since the filter does not have future prediction capabilities, the filter must wait for at least the stop band amount of time to ensure that the input signal is stable. This introduces a necessary delay in the system by the glitch filter. Most glitch filters, utilize an RC circuit to introduce this delay [1]. Ideally this delay should be equal in both directions, however rise and fall delays can differ. This can introduce duty cycle distortion in the input signal. This paper attempts to list the reasons for a delay mismatch and present the steps taken to reduce the same in a digital input glitch filter present in a multi-function IO cell implemented in 140nm TSMC process.

II. IO GLITCH FILTER ANALYSIS

The filter used as a starting point for the analysis is shown in Fig. 1. The switching transient after an input inverter is applied to the RC circuit, comprising of the resistor R0 and NMOS capacitor MN4. The RC circuit delays the rise of the signal across the capacitor. Since this voltage is fed to the output inverter, the inverter switches later than the input as the signal across it is delayed by the capacitor. For signals with pulse width less than a certain value, the voltage across the capacitor does not reach the threshold voltage of the output inverter before the input signal switches back, and this ability is used in filtering out high frequency glitches [1].

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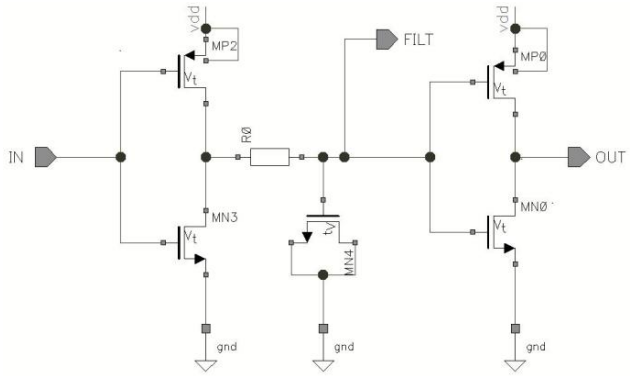


Fig. 1. Initial glitch filter circuit.

The input signal and the resulting waveform at node FILT resembles the curves in a low-pass RC circuit and is given in Fig. 2.

The propagation delays from node IN to node OUT are seen to be skewed by 85%. This skew in delays propagates along the channel, altering the duty cycle of waveforms, with the potential of false triggering along the signal path, as the devices have pre-defined threshold voltages. The objective of this paper is to equalize the rise and fall delays, with the intention of reducing the skew to less than 2.5% in the typical case and less than 10% in the worst-case corner.

Circuit analysis of the filter leads to three sources of the skew:

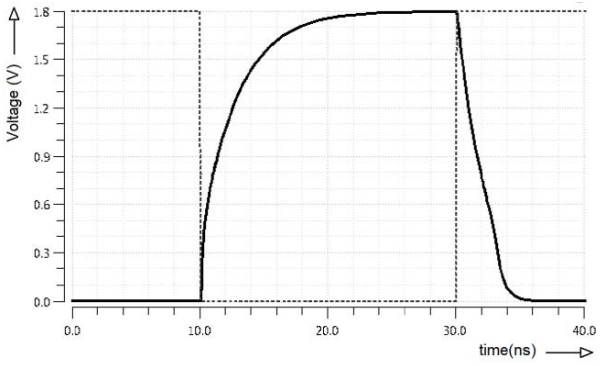
1) Capacitor asymmetry at low voltage,
2) Transistor DC mismatch, and
3) Output inverter threshold offset.

The following sections address each of the above issues.

III. Skew Resolution

A. Transistor mismatch

The transistors present a voltage dependent resistance to the signal at FILT, hence controlling the rise of potential at the node. The transistors are said to be mismatched when the resistance at the node when one of the transistors is switched on is different from the resistance when the other transistor is switched on.



4)
5) Fig 2. Input signal (dash) and signal at node FILT (solid).

In the glitch filter circuit, the transistors are mismatched as the resistance of the charging path (MP2) and discharging path (MN3) are different as shown in Fig. 3. This occurs primarily due to transistors being sized for speed and not resistance.

To reduce the mismatch between the NMOS and PMOS transistors, a resistor is added in series to both the transistors. The resistors are tuned to achieve equal resistance in PMOS and NMOS paths. This rather than resizing the transistors helps in reducing across the process corner mismatch and is easier to retune in post layout tuning phase. The on resistances of both the transistors after adding the series resistors are shown in Fig. 4.

B. Capacitor asymmetry

The skew related to the capacitor occurs primarily due to the non-uniform capacitance value of the NMOS transistor (MN4) gate capacitance with respect to gate source voltage. When the applied gate source voltage is lower than the threshold voltage the channel is not formed. From MOS capacitor theory, the gate capacitance before the creation of the channel is lesser when compared to that when the channel is present.

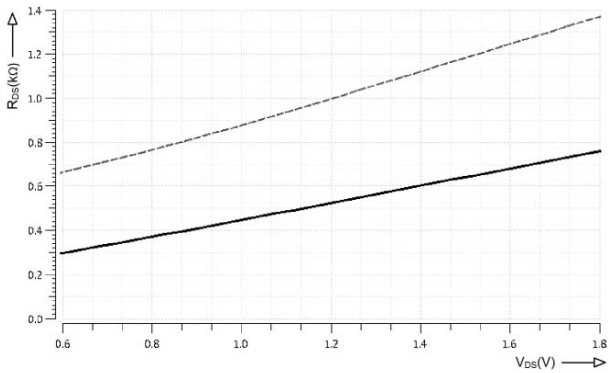


Fig 3. On resistances of NMOS (solid) and PMOS (dash) vs. drain-source voltage.

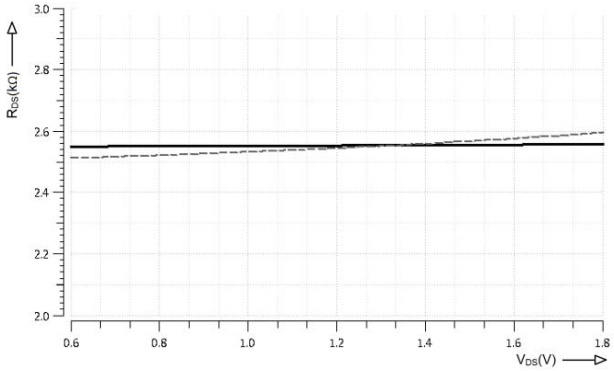


Fig 4. Path resistances of NMOS (solid) and PMOS (dash) after connecting resistors.

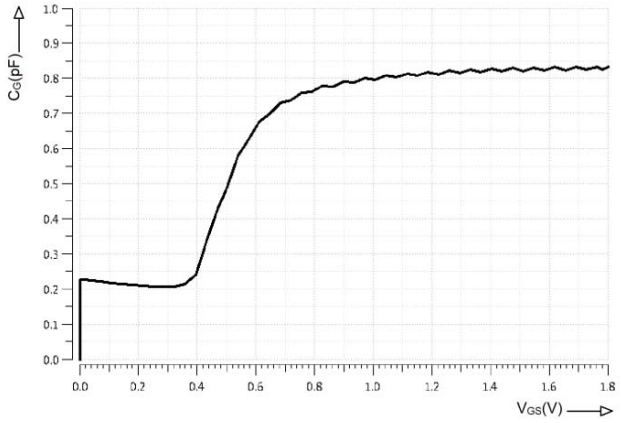


Fig 5. Capacitance presented to the signal at increasing gate voltages.

At lower capacitance values, the rate of change in voltage is greater. This is clearly visible in Fig. 2, where the signal at node FILT rises and falls much faster at voltages less than 0.5 V. Fig 5. depicts the capacitance of the NMOS capacitor as the gate voltage is swept. The value of capacitance is lesser at low voltages, specifically near and below the transistor threshold voltage of approximately 0.5 V.

Since Fig. 5 is the capacitance vs voltage, area under the curve from a certain voltage to other is equal to value of capacitor multiplied by the difference in voltage or *CdV*, which is the amount of charge required to charge the capacitor trough that voltage difference.

Assuming the final inverter has a threshold of 50% of VDD, the charge required to charge the capacitor from 0 V to 50% of VDD (0.9 V) is the area under the curve from 0 to 0.9 V. The time taken by PMOS transistor MP2 to charge the MOS capacitor MN4 is the primarily contributing factor offered by the system on an input signal fall cycle. FILT node will be charging from 0 V to 0.9 V in this cycle till the final inverter starts to fall. This charge is represented by the lightly shaded region in Fig. 6.

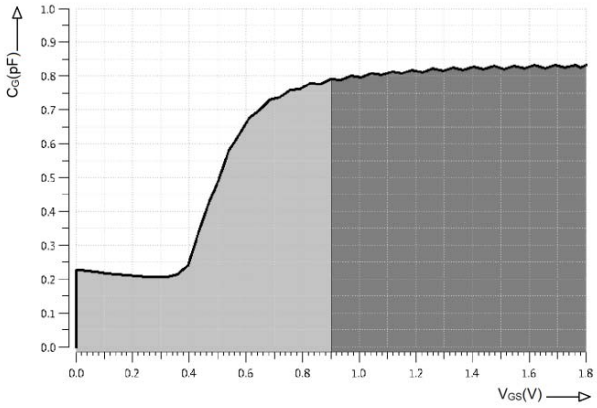


Fig 6. The area covered by the lighter region depicts the charge required to charge the capacitor from 0 to 50% of VDD. The darker area depicts the charge required to discharge the capacitor from VDD to 50% of VDD.

Similarly, the darker shaded region represents charge required to be discharged by MN3 before the final output can rise. It is clearly visible from the figure that there is a mismatch in both the charges causing the system to be inherently delay skewed. This mismatch is clearly visible when considering the FILT node waveform in Fig. 2.

Even though this could be solved by mismatching the initial inverter, the solution will work only for one set of PVT conditions. As the operating voltage rises, the threshold of the transistor does not change causing this difference to be less pronounced. A PMOS transistor can also be used as a capacitor, but that will have the same problem when gate voltage approaches supply voltage. To systematically solve this problem at the root cause, a combination of PMOS and NMOS is found to be the best solution since they compensate each other. Both the devices are tuned to match and capacitance of each are given in Fig. 7. The combined capacitance of both the devices on FILT is given in Fig. 8.

Unlike the original capacitance given in Fig. 6, it is easily seen from Fig. 8 that both the lightly shaded and darkly shaded region are roughly the same charge. This goes a long way in reducing capacitor asymmetry in the glitch filter delay.

The total capacitance at the node FILT (C_G) due to both PMOS (C_P) and NMOS (C_N) transistors is the sum of the capacitances of the individual capacitances.

$$C_G = C_N + C_P \quad (1)$$

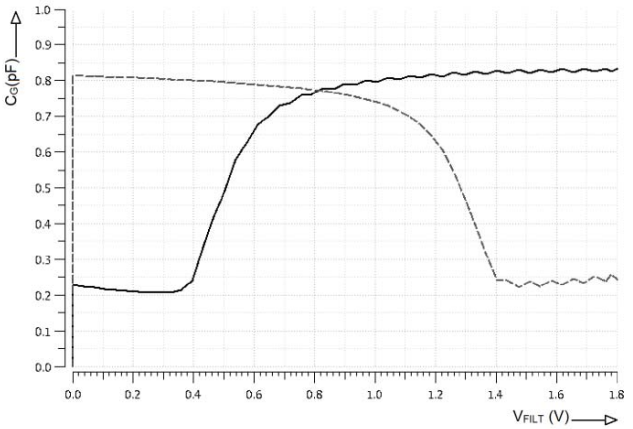


Fig 7. Capacitances of NMOS transistor (solid) and PMOS (dash) against FILT node voltage (V_{FILT}).

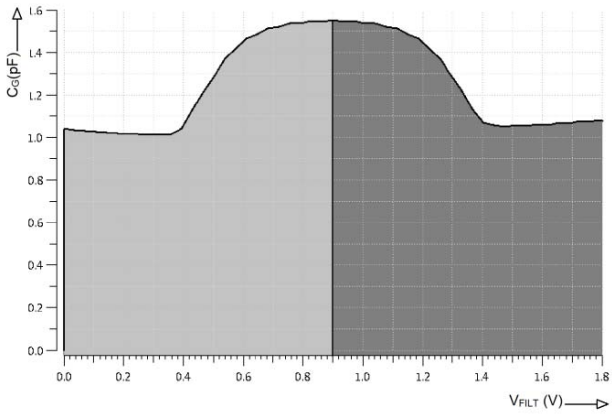


Fig 8. Total capacitance of FILT node vs voltage.

C. *Output inverter threshold offset*

The inverter is tuned to set the threshold voltage of the output inverter at VDD/2.

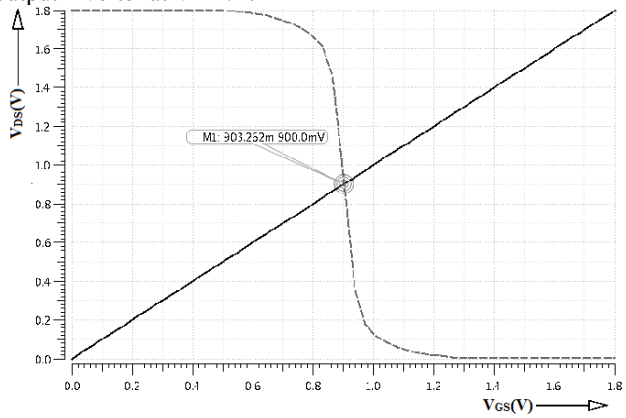


Fig 9. Transfer curve of tuned inverter, V_{OUT} (dash) vs V_{FILT} (solid).

IV. Simulation Results

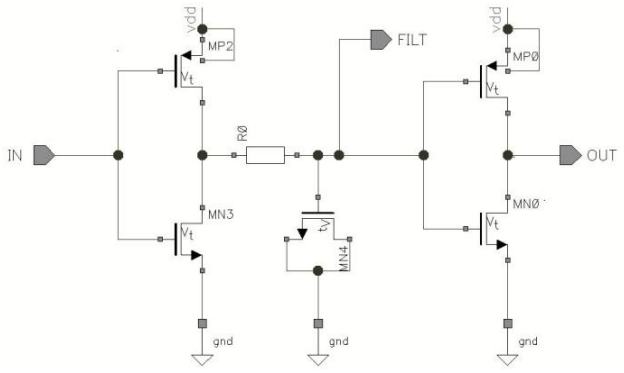


Fig 10. Optimized glitch filter circuit.

The circuit after modifying as indicated in the previous section, is given in Fig. 10. The maximum rise delay, fall delay and the relative skews of the final circuit when compared to the initial circuit (shown in Fig. 1), for all PVT corners is given in Table I.

TABLE I. Relative Skew Comparison

Parameter	Initial circuit	Final circuit	Units
Rise delay	2.521	2.942	ns
Fall delay	1.274	2.831	ns
Relative skew	85.15%	8.67%	

In the final circuit, the typical skew is less than 1% with worst case values varying between -5% and +8%, across all PVT corner. A Monte Carlo simulation of 200 samples is run to find the real-life variation. The results are given in Table II.

TABLE II. Monte Carlo Results

Parameter	Mean (μ)	Std. dev. (σ)	Units
Rise delay	2.445	0.109	ns
Fall delay	2.421	0.103	ns
Relative skew (absolute value)	0.024	0.085	ns
Relative skew (%)	0.974	3.469	

Considering the mean and standard deviation values for the relative skew, the maximum variation of the skew between the rise and fall delays for a Six Sigma process which is the standard in the automotive industry, $\mu \pm 6\sigma$ is $0.024 \pm 6*0.085$, i.e. between -0.481 ns and 0.527 ns. The power consumed in the delay skew optimized circuit is found to be marginally lesser (~7%) less than the original glitch filter circuit.

V. Conclusion

The IO glitch filter was modified to reduce the skew to an acceptable level. This was achieved by identifying the three key contributors to the offset and negating their effect. In the case of the transistor mismatch, the resistances of the PMOS and NMOS transistors were made equal by a mismatched resistor. To overcome capacitor asymmetry, a PMOS capacitor was added in addition to the esisting capacitor at the node FILT. The output inverter was tuned to negate the inverter threshold offset.

The Six Sigma skew variation of the tuned filter is within ±0.5 ns while stopping 2.5 ns glitches.

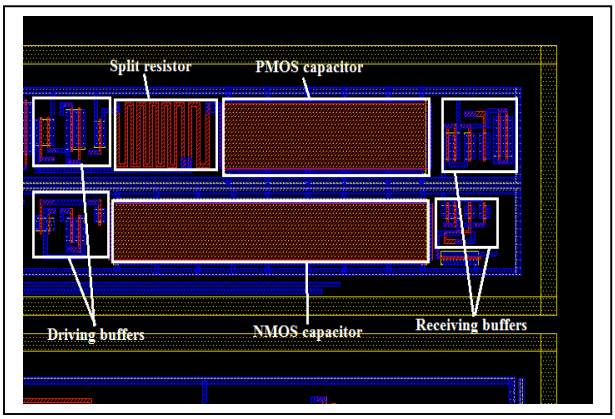


Fig 11. GDSII capture of the filter implemented in a product.

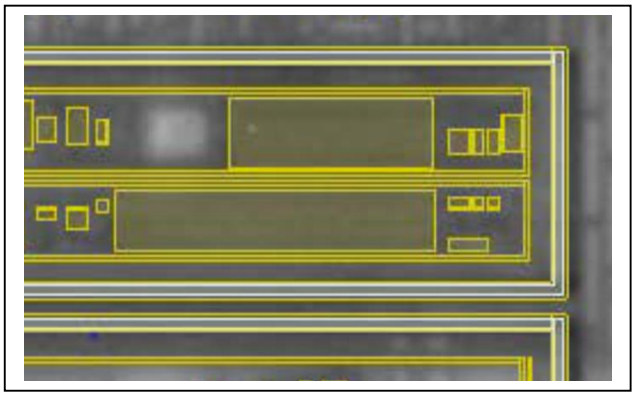


Fig 12. Photon Emission Microscope image with STI overlay.

Fig. 11. gives a screen capture of the glitch filter architecture expounded in the paper applied to a real-world design. The updated circuit is implemented in silicon and avoided the timing failure from the original circuit. Fig. 12 is a Photo Emission Microscope image of the fabricated silicon with STI overlay. The implemented silicon contains additional circuitry compared to Fig. 10, however, the basic filter concept is identical to the one presented in this paper.

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