Design and Implementation of Threshold Logic Functions using Memristors

Y. K. Y. Danaboina* Pravanjan Samanta* Kamalika Datta† Indrajit Chakrabarti* Indranil Sengupta*
* Indian Institute of Technology, Kharagpur, India
Email: yaswanthkrishna93@gmail.com, pravanjan2008@gmail.com, indrajit@ece.iitkgp.ac.in, isg@iitkgp.ac.in
† National Institute of Technology, Meghalaya, India
Email: kdatta@nitm.ac.in

***Abstract*—In this paper, a new design to implement programmable Threshold Logic Gate (TLG) using memristors as weights combined with CMOS circuits for threshold control and comparison has been reported. In this design it is possible to program both weights and threshold of the gate that gives greater flexibility in implementing logic functions with minimum gate count. The operation of the gate has been experimentally verified through simulation by implementing some linear threshold logic functions.**

***Index Terms*—Threshold logic gate, memristor, logic design**

I. Introduction

With the emergence of various nanotechnologies, researchers have again focussed on Threshold Logic Gate (TLG) as an alternate design paradigm for implementing digital logic functions in the last two decades. A Threshold Logic Function (TLF) can be loosely defined as a Boolean function in which the output is evaluated in terms of the input weights and a given threshold value. In this paper we propose a new memristor-based TLG design. The variable resistance property of the memristor has been utilized to program the weights in the proposed design.

II. Background

We now present a brief review of threshold logic. A Threshold Logic gate (TLG) has n digital inputs $X = (x_1, x_2, \ldots, x_n)$ and a single digital output Y. Its internal parameters are a threshold value T, and weights $W = (w_1, w_2, \ldots, w_n)$ where each weight w_i is associated with the input variable x_i as shown in Figure 1. The values of T and W may be real, finite, positive or negative. The input-output relationship of the gate can be expressed as follows:

$$Y = \begin{cases} 1, & \text{if} \quad \sum_{i=1}^{n} w_i x_i \geq T \\ 0, & \text{otherwise} \end{cases} \tag{1}$$

A team from HP Labs [1] announced the fabrication of a memristor in 2008. A TiO_{2-x} layer with oxygen vacancies is placed on a perfect TiO_2 layer and these layers are sandwiched between platinum electrodes. Let R_{off} and R_{on} denote the resistances of the undoped and doped regions of respectively. The total resistance of the device is determined

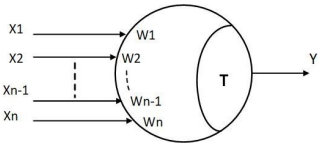

Fig. 1: Threshold logic gate

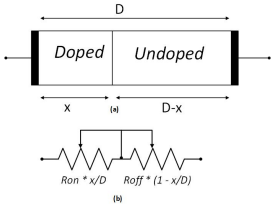

Fig. 2: (a) Physical structure of memristor, (b) Equivalent circuit

by the sum of the resistances of doped and undoped regions, as shown in Figure 2.

The variable resistance of memristor can be modelled as

$$M(x) = R_{on}.\frac{x}{D} + R_{off}.(1 - \frac{x}{D}) \tag{2}$$

Rajendran et al. [2] have proposed a simple memristor threshold circuit by using a pMOS current mirror as a current comparator with a fixed threshold value.

In this paper we propose a new design of threshold gate that does not use any current mirrors in input terminals and hence to prevent backward flow of current, it uses pass transistors that are more area efficient. Also, threshold value has been made programmable. For current comparison, we have used Traff's comparator [3] that is faster than the current mirror comparator used in [2] because of regenerative feedback.

III. Proposed Threshold Gate Design using Memristors

This section describes the design implementation of the proposed threshold logic gate with memristive weights and programmable threshold. In the proposed design memristor resistances act as weights, and a reference current is used as

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00115

the threshold. If V_i and Mem_i are the input voltage and and memristance at input X_i, then output Y is given by

$$Y = \begin{cases} 1, & \text{if} \quad \sum_{i=1}^{n} \frac{V_i}{Mem_i} \geq I_{ref} \\ 0, & \text{otherwise} \end{cases} \tag{3}$$

There are mainly three parts in the proposed threshold logic gate design, viz. input weights, programmable threshold, and current comparator as shown in Figure 3. We shall discuss each part in detail.

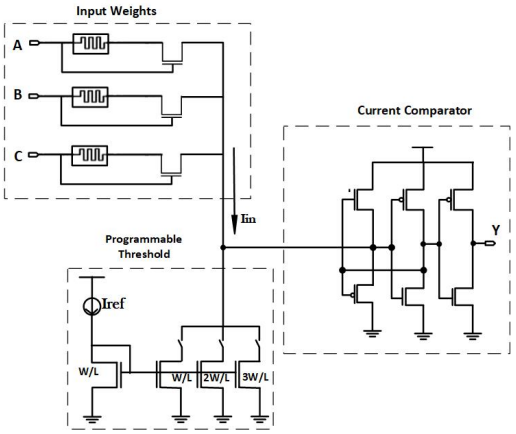

Fig. 3: Schematic diagram of the proposed 3-input MTL gate

A. Input Weights

At each input we have a memristor as the corresponding weight followed by a pass transistor having its gate connected to the input as shown in Figure 3. The main purpose of the pass transistor is to block the backward flow of current towards the input terminal when the input at that terminal is at logic 0 (i.e. low voltage). In the absence of the pass transistors, if input voltage at a particular terminal is zero then current will be flowing into the input terminal.

B. Programmable Threshold

The main advantage of the proposed threshold gate design is that the threshold value is programmable, which provides the flexibility of changing the gate functionality dynamically as per the requirement. We have used the current mirror concept to generate integer multiples of the reference current I_{ref}. Also, there are controllable switches above each transistor. Depending on the requirement, closing the required switches can provide threshold values in the range I_{ref} to $6I_{ref}$.

C. Current Comparator

We have used a Traff's comparator [3] in the proposed design, which has a buffer and an inverter connected in feedback as shown in Figure 3, followed by another inverter stage to bring back the voltage levels to rail-to-rail. As there is a regenerative feedback connection we expect this comparator to be faster than the conventional current mirror comparator that was used in [2].

IV. Experimental Evaluation

The proposed design of TLG has been simulated using SPICE, results for which are presented and discussed in this section. Device modeling and circuit-level performance analysis has been carried out using Cadence Spectre using Berkeley Predictive Technology Models (PTM) [4] for 45nm CMOS transistors. The memristors are modelled in Verilog-A using the linear drift velocity model proposed in [1], [5]. The physical parameters used in our analysis such as R_{on}, R_{off}, thickness, etc. have been obtained from [1], [2]. The voltage applied is 1V for logic-1 and 0V for logic-0 and power supply voltage is 1V.

Table I shows the weights, threshold, corresponding memristive weights and reference current. The memristive weights and reference current for 3-input OR gate are taken as mentioned in [2], and for the remaining logic functions the weights and threshold are adjusted accordingly.

TABLE I: Weights and threshold values for 3-input functions

Functions	Weights			Threshold	Memristance (KΩ)			I_{ref}
	A	B	C		A	B	C	(μA)
A+B+C	1	1	1	1	400	400	400	0.8
ABC	1	1	1	3	400	400	400	0.24
AB+BC+CA	1	1	1	2	400	400	400	0.16
AB+AC	2	1	1	3	200	400	400	0.24

We compare the delay and energy of the proposed memristor-based TLG with the memristor-based TLG implementation of [2] in Table II.

TABLE II: Delay and energy comparison with respect to [2]

Functions	Delay (ns)			Energy (fJ)		
	[2]	Proposed	% Impr.	[2]	Proposed	% Impr.
A+B+C	0.637	0.372	41.60	7.29	0.77	89.47
ABC	1.920	0.558	70.93	6.80	1.82	73.19
AB+BC+CA	1.190	0.432	63.69	6.65	1.23	81.45
AB+AC	0.928	0.478	48.49	6.93	1.54	77.72

V. Conclusion

A memristor-based implementation of threshold logic gate has been proposed in this paper, that allows reconfiguration of both weights and threshold. Also the proposed TLG is more energy efficient with improved delay as compared to [2].

References

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams. The missing memristor found. *Nature*, 453:80–83, May 2008.

[2] J. Rajendran, H. Manem, Ramesh Karri, and Garrett S. Rose. An energy-efficient memristive threshold logic circuit. *IEEE Transactions on Computers*, 61(4):474–487, April 2012.

[3] H. Traff. Novel approach to high speed CMOS current comparators. *Electronics Letters*, 28(3):310–312, January 1992.

[4] Berkeley predictive technology model (ptm). http://ptm.asu.edu/.

[5] Y. N. Joglekar and S. J. Wolf. The elusive memristor: Properties of basic electrical circuits. *European J. Physics*, 30(4):661–675, 2009.