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Ultra Low Energy Reduced Switching DAC for SAR ADC

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***Abstract*—This paper presents a novel architecture for a low-energy Digital-to-Analog converter (DAC) used in Successive Approximation Register Analog-to-Digital converters (SAR ADCs). The proposed ultra low-energy reduced switching (RS) architecture for DAC employs a new charge sharing and restoration technique for generating the desired voltage. Using its unique capacitor array and switching technique, it reduces the energy consumption for capacitor charging by 99.85% (for 10-bit) as compared to conventional SAR ADC. The proposed architecture requires a fewer number of switches as compared to other low-energy architectures and efficiently reduces the switching energy as well.**

***Index Terms*—SAR, ADC, MSB, DAC, J-S, RS.**

I. Introduction

Analog to Digital Converters (ADC) are required for a variety of real-world applications. They provide a measure of the physical analog quantities by translating them to digital domain, which simplifies the processing and storing of data. Due to their extensive use, the power required by the ADC block becomes a major design concern, especially in the battery operated devices. In critical applications, such as, in bio-medical devices, where power consumption is a hard constraint, ultra low power circuits with moderate resolution and sampling rate are required. Low-power architectures of SAR ADCs have been a popular choice for such applications [1-10]. SAR ADCs converge to the output digital code by determining one bit at a time, starting with the Most Significant Bit (MSB). Due to this evaluation scheme, the sampling rate of the SAR ADCs range around low KS/s.

SAR ADCs generally comprise of a DAC block, a comparator and a control block with a shift register. However, the DAC block consumes a large fraction of the total energy consumed by the SAR ADC. Over the past years, many energy-efficient architectures have been designed to reduce the energy required by the DAC block, such as, capacitor-splitting, junction-splitting, two-step junction-splitting, ultra low-energy and C-2C switch-capacitor technique [1-5]. The ultra low-energy [4] brought down the capacitor charging energy in the DAC block to its bare minimum. In this paper, we present a new architecture for the DAC block of the SAR ADC. The proposed DAC block uses binary weighted capacitors to take away a specific amount of charge from the unit capacitors. The unit capacitors are then recharged to generate the desired voltage, thus, eliminating the need to charge larger capacitors.

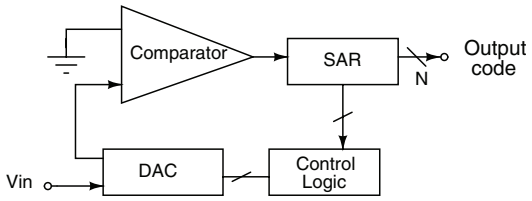

Fig. 1: Block diagram of a conventional SAR ADC

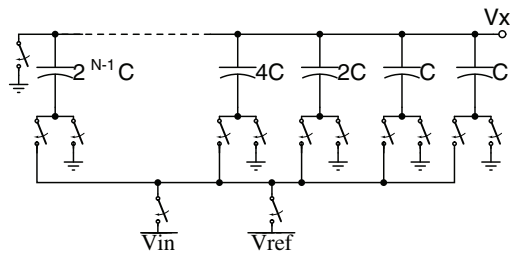

Fig. 2: DAC block of a conventional SAR ADC

This paper is organized as follows. The conventional, two-step junction-splitting and ultra low-energy SAR ADCs are reviewed in section II. The proposed reduced switching (RS) DAC architecture is discussed in section III. Section IV provides the calculations and simulation results for justifying the efficiency of the proposed architecture. The comparisons and discussions are provided in section V. The conclusions are discussed in section VI.

II. SAR Algorithm and Exisiting Low Power Architectures

An N-bit SAR ADC works by determining the Most Significant Bit (MSB) bit in the undetermined bits in each step and continuing till all the bits of the N-bit digital code are determined. The block diagram of a typical SAR ADC is shown in Fig. 1.

The DAC block of the SAR ADC produces an approximation to the input signal based on the already determined

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bits. The output of DAC is then compared to the input signal to determine the next MSB, which is then fed back to the DAC using the SAR and control logic, and the process is repeated until the entire digital code is determined. The DAC block of the conventional SAR ADC [11] uses binary weighted capacitors as shown in Fig. 2. An N-bit conventional DAC block requires using larger capacitors till 2^{N-1}C, where C represents the smallest unit capacitor in the circuit, whose charging and 'down' transition requires a large amount of charge and energy.

This problem of energy waste during 'down' transitions and charging of larger capacitors was reduced by energy-efficient two-step junction-splitting method [3]. The two step junction-splitting method reduces the energy dissipated by 98% as compared to the conventional method.

Using two smaller binary weighted capacitor arrays, two step J-S also limits the total capacitance of the circuit to $2^{(\frac{N}{2}+1)}C$ F for even N and $2^{(\frac{N+1}{2}+1)}C$ F for odd N, which helps reducing the area required by capacitor array by a large fraction.

The energy consumption was reduced by 99.85% by Ultra low-energy SAR ADC [4], which using a unit capacitor array brought down the total capacitor area required to the area required by $(N+1)$ C. The Ultra low-energy SAR ADC [4], however, employed passive charge sharing between unit capacitors at every bit determination. For an N-bit ADC, N capacitors are charged passively. Any charge lost during switching and charge sharing is not compensated which produces an error in the voltage generated by the DAC block. This limits the resolution of the Ultra low-energy SAR ADC [4].

III. Proposed Ultra Low-Energy Reduced Switching (RS) DAC for SAR ADC

The proposed SAR ADC is shown in Fig. 3 (A). It contains the ultra low-energy RS DAC block, an SAR, control logic block, a unit capacitor for sampling and holding Vin and a comparator.

The DAC block shown is illustrated in Fig. 3 (B), for a 4-bit resolution for simplicity. It contains two unit capacitors connected between Vref and ground via switches and a series of charge discarding capacitors which are used to take a specific amount of charge from the unit capacitor. The binary weighted capacitor $\frac{C}{2^x}$ F is realized by connecting 2^x unit capacitors in series. The circuit can be extended by extending the series of charge discarding capacitors and respectively added switches to any N-bit model.

The circuit uses three configurations during the conversion process:

1) Reset: All capacitors are shorted to remove any unwanted or leftover charge from previous conversions.
2) Charge Dumping: A specific set of capacitors are connected in parallel with one of the unit capacitors while V_{ref} is disconnected from the circuit. By doing so, the set of capacitors take a specific amount of charge from the said unit capacitor and are disconnected in the next step. This allows the shared charge to be dumped. After determining i^{th} bit, b_i, switches are controlled by the logic:

$$S1 = b_i$$
$$S2 = \sim b_i$$
$$S(j+2) = (\sim b_i \wedge b_{i-j}) \qquad \forall j \in [1, i-1],$$
$$S(j+2) = 1 \qquad \forall j \in [i, n-2],$$

where $\wedge$ represents 'exclusive or' and logic '1' represents a closed switch

By using the above switching method, one of the unit capacitors loses $\frac{C.V_{ref}}{2^i}$C charge by depositing it on charge discarding capacitors.
3) Recharging: The two unit capacitors are connected between Vref and ground while the rest of the capacitors are disconnected from this circuit and shorted. The charge lost during charge discarding phase is equally restored on both capacitors, i.e, both unit capacitors gain $\frac{C.V_{ref}}{2^{i+1}}$C amount of charge. This effectively introduces a change of $\frac{V_{ref}}{2^{i+1}}$V across the unit capacitors and in the output voltage, Vx, which is the desired change after i^{th} bit determination.

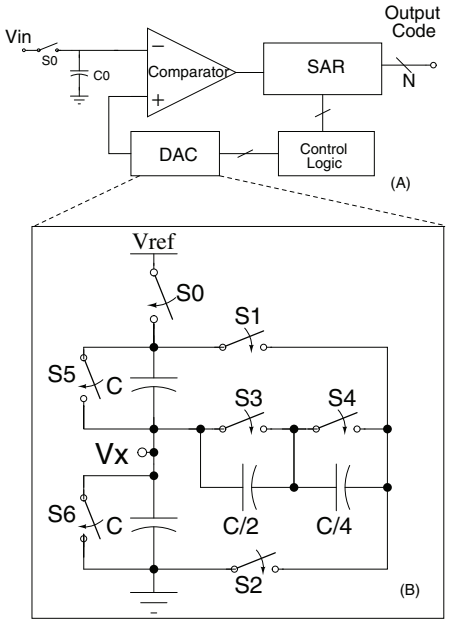

Fig. 3: Proposed SAR ADC with expanded view of DAC block

The proposed mechanism is illustrated for a 4-bit case in this paper, for simplicity. Let the input voltage be such that the input digital word to the DAC is (b_1,b_2,b_3,b_4) = (1,0,0,1). Steps for the same are given as follows:

1) To remove any initial charge present on the capacitors, all capacitors are first shorted in the reset phase, as shown in step 1 of fig. 4.

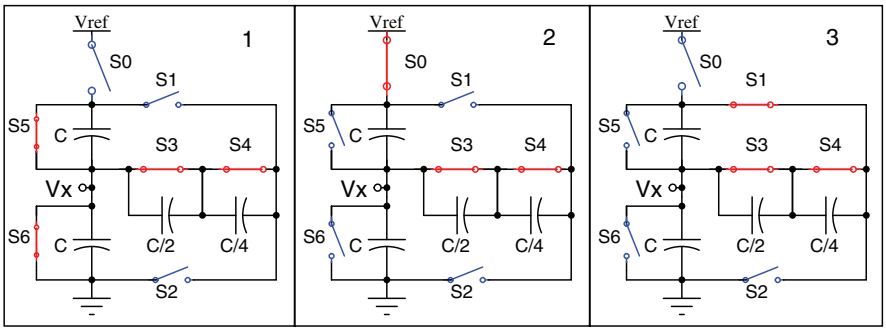

Fig. 4: Step 1: Reset Phase, Step 2: Recharging Phase and Step 3: Charge Dumping Phase

2) The two unit capacitors are then charged as shown in step 2 of fig. 4. After charging of capacitors,

$$Vx[1] = \frac{V_{ref}}{2}V \tag{1}$$

The first bit can now be determined by comparing V_x with V_{sample}. Energy consumed in 1^{st} bit determination,

$$E[1] = \frac{1}{2}CV_{ref}^2J \tag{2}$$

Sampled input voltage is now compared with DAC output.

3) After recharging, the circuit shifts to charge discarding phase. Since the bit obtained after first comparison, (b_1) is 1, top unit capacitor is shorted. This is realized by logic:

$$\begin{aligned} S1 &= 1 \\ S2 &= 0 \\ S(j+2) &= 1 \qquad \forall j \in [1, i-1], \\ S(j+2) &= 1 \qquad \forall j \in [i, n-2], \end{aligned}$$

This transition is shown in step 3 of Fig. 4. In this phase, $\frac{C.V_{ref}}{2}$C charge is taken away from the top unit capacitor.

4) After charge discarding, circuit shifts to recharging phase as shown in step 2 of fig. 4. Now,

$$Vx[2] = \frac{3V_{ref}}{4}V \tag{3}$$

Energy consumed in 2^{nd} bit determination,

$$E[2] = \frac{1}{4}C.V_{ref}^2J \tag{4}$$

Since $\frac{C.V_{ref}}{4}$C charge is supplied by V_{ref} in this step. Sampled input voltage is now compared with DAC output.

5) Since the next bit (b_2) obtained after second comparison is 0, capacitor $\frac{C}{2}$ is connected in parallel with bottom unit capacitor. This is achieved by logic:

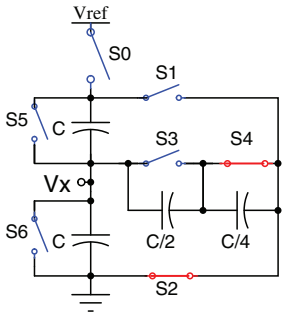

Fig. 5: Step 5

$$\begin{aligned} S1 &= 0 \\ S2 &= 1 \\ S3 &= 0 \\ S4 &= 1, \end{aligned}$$

This transition is shown in Fig. 5. In this phase, $\frac{C.V_{ref}}{4}$C charge is taken away from the top unit capacitor.

6) After charge discarding, circuit shifts to recharging phase as shown in step 2 of fig. 4. Now,

$$Vx[3] = \frac{5V_{ref}}{8}V \tag{5}$$

Energy consumed in 3^{rd} bit determination,

$$E[3] = \frac{1}{8}C.V_{ref}^2J \tag{6}$$

Since $\frac{C.V_{ref}}{8}$C charge is supplied by V_{ref} in this step. Sampled input voltage is now compared with DAC output.

7) Since the next bit (b_3) obtained after third comparison is 0, capacitor $\frac{C}{4}$ is connected in parallel with bottom unit capacitor. This is achieved by logic:

$$\begin{aligned} S1 &= 0 \\ S2 &= 1 \\ S3 &= 1 \\ S4 &= 0, \end{aligned}$$

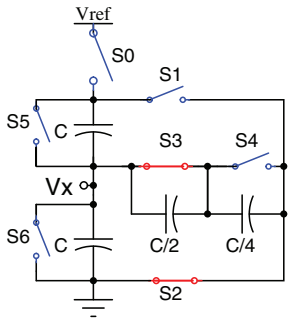

Fig. 6: Step 7

This transition is shown in Fig. 6. In this phase, $\frac{C.V_{ref}}{8}$C charge is taken away from the top unit capacitor.

8) After charge discarding, circuit shifts to recharging phase as shown in step 2 of fig. 4. Now,

$$Vx[4] = \frac{9Vref}{16}V \tag{7}$$

Energy consumed in 4^{th} bit determination,

$$E[4] = \frac{1}{16}C.V_{ref}^2.J \tag{8}$$

Since $\frac{C.V_{ref}}{16}$C charge is supplied by V_{ref} in this step. Sampled input voltage is now compared with DAC output.

9) After this, the LSB (b_4) can be determined and will be obtained as 1. This completes the conversion process.

Total energy required $= (1 - 2^{-n}).C.V_{ref}^2$J
for n-bit conversion

For a 10-bit conversion, total energy required is approximately $C.V_{ref}^2$ J.

IV. Simulation Results

The proposed reduced switching DAC requires approximately $C.V_{ref}^2$ J energy for 10-bit conversion irrespective of the output code. The results of this model are applied to 10-bit model and compared with DAC block of conventional SAR ADC [11], two-step junction-splitting SAR ADC [3] and ULE SAR ADC. Simulations for energy consumption for the above mentioned methods were performed for all digital output codes. Normalized energy plots for these methods are shown in Fig. 7 and Fig. 8.

The proposed architecture was tested for non-linearity for 10-bit resolution using 45nm transistors for switching. For an n-bit DAC block, 2^{n-1} distinct outputs are possible at the last step of conversion. Fig. 9 and Fig. 10 show the differential and integral non-linearity analysis of the proposed DAC block respectively on the output voltage obtained after complete conversion.

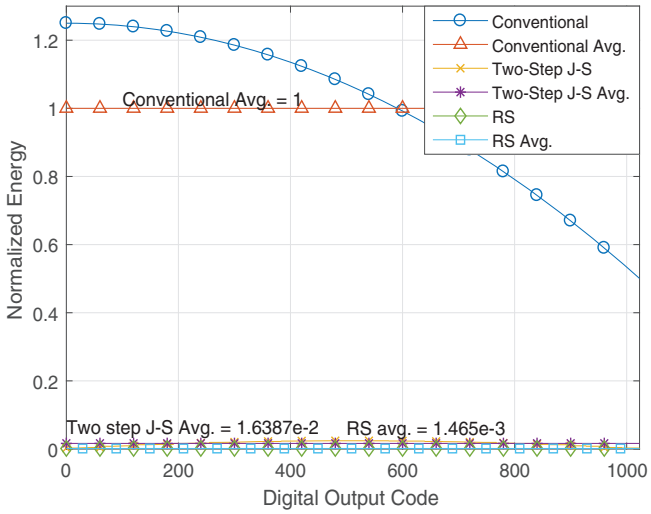

Fig. 7: Normalized Energy comparison of discussed DAC methods

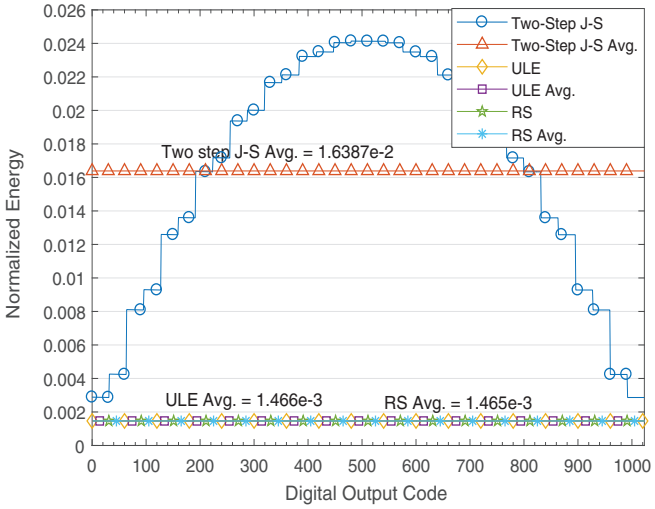

Fig. 8: Expanded view of Normalized Energy consumption comparison of two step J-S, ULE and proposed RS method

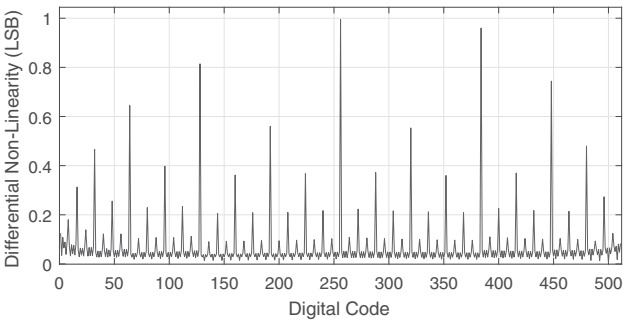

Fig. 9: Differential Non-Linearity plot

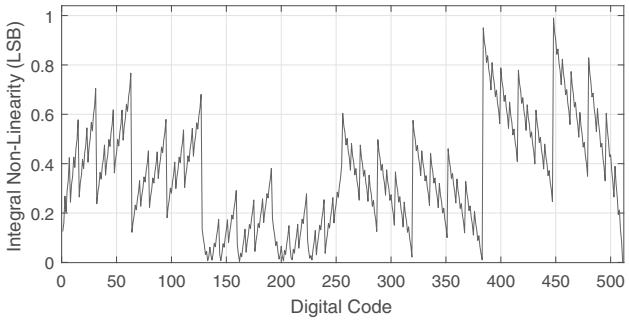

Fig. 10: Integral Non-Linearity plot

TABLE I: Comparison of discussed DAC methods

DAC type	Throughput (words/cycle)	Total Capacitor Area (C)	Number of Switches	Avg. Normalized Energy for 10-bit DAC(%)
Conventional Cap. [11]	$\frac{1}{N}$	2^N	2N+5	100
Two step J-S [3]	$\frac{1}{N+1}$	$2^{(\frac{N}{2}+1)}$, for even N $2^{(\frac{N+1}{2}+1)}$, for odd N	$\frac{N^2}{4}+\frac{5N}{2}+4$, for even N $\frac{N^2}{4}+3N+\frac{27}{4}$, for odd N	1.64
ULE [4]	$\frac{1}{2N}$	N+2	4N+1	0.1466
RS (Proposed)	$\frac{1}{2N}$	2^{N-1}	N+3	0.1465

The dnl and inl values were calculated using the following formulas:

$$DNL = \left| \frac{V_{i+1} - Vi}{V_{LSB\_ideal}} - 1 \right| \tag{9}$$

$$INL = \left| \frac{V_i - V_0}{V_{LSB\_ideal}} - i \right|, \tag{10}$$

where V_{LSB_ideal} represents the ideal gap between the voltage level of two consecutive codes during last bit determination. Both dnl and inl are obtained within 1 LSB limit with $V_{ref} = 1V$, unit capacitance $C = 8.2$ pF and a sampling frequency of 47.6 kS/s. The architecture performed best with the smallest size transistor available indicating that there is a possibility of increasing the sampling frequency as well as decreasing the unit capacitance by using an even smaller technology node.

V. Comparison and discussion

The above mentioned four methods were compared in terms of throughput, total capacitance, number of switches and the normalized average energy dissipated for 10-bit resolution. The comparison is shown in Table 1.

The proposed method requires fewer switches as compared to conventional [11], two step junction-splitting [3] and ULE [4] methods. The capacitor charging energy was brought down to its minimum by ULE architecture [4]. The proposed architecture while keeping the capacitor charging energy to its minimum, significantly reduces the switching energy. Also, the charge lost while charge sharing in the DAC block of ULE architecture [4] is never compensated and introduces an error in the output voltage, thus, limiting its resolution to 7-bits . The proposed circuit has a recharging phase in which any erroneous charge lost while charge sharing phase is partially restored. This allows the proposed circuit to be successfully scaled to a resolution of 10-bits with 45nm technology node switches. The capacitor area required is reduced to $2^{(n-1)}$ C from 2^nC as compared to conventional architecture [11]. Also, although the number of cycles per conversion increases to 2N cycles from N cycles required in conventional method [11], the duration of cycles can be reduced since the maximum capacitance of the charging circuit is reduced by a factor of $2^{(N+1)}$, as compared to conventional architecture [11], by using the proposed method. This allows the proposed DAC block to charge and discharge approximately $2^{(N+1)}$ times faster as compared to conventional circuit.

VI. Conclusion

We have proposed a new DAC block for SAR ADCs which generates the desired voltage by discarding a specific amount of charge from unit capacitors on a series binary weighted capacitor array and recharging the unit capacitors using V_{ref}. It eliminates the need to charge larger binary weighted capacitors, hence reducing the energy required for capacitor charging by 99.85% as compared to conventional architecture [11], 92.5% as compared to two step junction-splitting architecture [3] and the same as ULE architecture [4] (for 10-bit architecture) . In comparison to all discussed architectures, the proposed architecture uses fewer number of switches and significantly brings down the switching energy as well.

Acknowledgement

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