# *Low Power Design Technique in Passive Tag to Reduce the EMD Noise for Reliable Communication with Reader*

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***Abstract* - This paper describes the digital design technique to reduce electromagnetic disturbance (EMD) noise generated by a passive tag, Proximity Integrated Circuit Card (PICC) while processing commands issued by a reader, Proximity Coupling Device (PCD). The higher EMD noise reduces reliability of communication if its frequency falls close to the sub-carrier modulation frequency of 848KHz, which is generally observed at low field strengths. The proposal uses voltage sensor to detect the higher EMD noise and adjusts the clock-gating of the digital design. The voltage sensor output is monitored to detect a pattern, which eventually scales to an EMD noise. Based on the pattern, a pre-defined clock-gating is applied to shift the EMD noise frequency from 848KHz to 3.39MHzThe mixed-signal simulation shows 4mV peak EMD noise reduced to 1mV with the solution and the same has been confirmed by silicon validation. The clock-gating impacts the command processing time, which is increased at low field strengths.**

***Keywords – ISO 14443, Frame Delay Time, EMD, clock-stop***

## I. INTRODUCTION

Radio Frequency Identifier (RFID) tag is a contactless identification technology, which identifies the object by radio frequency and allows access to the relevant data without human intervention. It supports features like secure data storage, secure communication, good reading speed, long service life and good environment adaptability. Earlier RFID integrated circuits were mainly targeted at traditional market like ticketing, loyalty cards, access management, micropayment etc. Near Field Communication (NFC) Tags are specialized subset within the family of RFID technology. In smartphones NFC connectivity is growing ubiquitous to facilitate the Internet of Things (IoT). NFC Tags are interesting proposition in establishing secure communication between physical and virtual world in IoT space. Connecting these billions of familiar physical devices (NFC tags), the IoT promises to improve how we live, work, and play by turning our homes, cars, offices, and cities into smart, interactive environments. These NFC Tags can be configured as Smart Media for convenience, speed and security or even for Smart Sportswear for appropriate usage. They can also be effectively used for Proximity marketing, Smart Packaging, Bluetooth pairing, brand protection and even tamper management. These NFC tags normally adhere to ISO/IEC 14443 and are compliant to NFC standard. There are mainly two types of tags, viz. active and passive, based on source of voltage supply. The proposed solution mainly targets passive tags/devices (PICC).

PICC being a contactless device with proximity range, the main requirement is to have a reasonable reading range for rich user experience. One of the challenge here, is establishing reliable communication over the distance to overcome EMD generated by the PICC digital circuit during processing of PCD command. The passive contactless devices (PICC) generates supply voltage using RF field based on electromagnetic induction principle. Hence, the power consumption by the PICC digital circuit during command processing can load the RF field, which is the source of EMD disturbance. As the PICC distance from PCD increases the field strength reduces. The variation in power consumption from digital circuit can severely impact communication due to these EMD disturbances (noise) at low field strengths. These EMD disturbances or noise generated during command processing time (referred as Frame Delay Time in ISO/IEC 14443 specification) can be misinterpreted by the sensitive readers as response, which can cause communication failure. With this, either user can face delayed transactions because of repeated trials or in worst case denial of service, which inherently means bad user experience.

### *A. Alternate Methods*

There are various methods available to reduce EMD noise during digital processing time.

- Simplest method is to lower the System clock, though this can reduce EMD during processing it negatively impacts processing time even during higher field strength.
- Another method is to detect lower field strength using field sensor and appropriately scaling down the clock. It

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costs significant area overhead to design a good field sensor in silicon.

- Alternate method is to isolate input field and digital supply; with this technique noise generated by digital activity would have minimum impact on field. Method can cost significant area overhead and overall complexity.
- Additional flavor of above method could be isolation itself, which can be indirectly achieved by having different voltage domains. Even this method has similar limitation from area or complexity perspective.

All above methods impact either silicon area or performance significantly.

## II. Implementation

Section A introduces the Frame Delay Time (FDT), Section B describes Electromagnetic disturbance (EMD) and Section C explains Clock-stop. Impact on EMD due to clock-stop is discussed in Section D. Section E provides the proposed solution.

### A. *Frame Delay Time (FDT)*

As per the ISO/IEC 14443-3[2], the frame delay time is defined as the time between two frames transmitted in opposite directions. This is the time between the end of the last pause transmitted by the PCD and the first modulation edge within the start bit transmitted by the PICC. Illustrated in Figure 1.

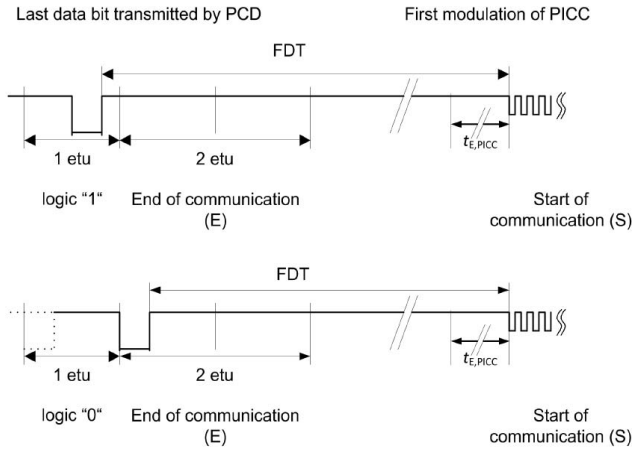


Fig. 1 Frame delay time PCD to PICC for bit rates up to fc/16

### B. *Electromagnetic disturbance (EMD)*

As per the ISO/IEC 14443-3[2], while the PCD is waiting for the PICC response, the PICC is processing the requested command. The dynamic current consumption of PICC during execution time may cause an arbitrary load (which may not be purely resistive) modulation effect on the magnetic field. In some cases, the PCD may misinterpret EMD as data sent by the PICC and this may negatively impact proper reception of the PICC response.

The effect of the EMD on the PCD reception may depend on

- PICC operation and speed,
- PCD and PICC antenna geometries [4] and relative distance (coupling factor), and
- Sensitivity of PCD receiver channel.

The EMD specification on the limits are described in ISO/IEC 14443-2[1], section 10. Electromagnetic disturbance levels.

### C. *Clock-stop and its purpose*

During communication with a PCD, once a command is received by the PICC, it shall be decoded, processed and response is transmitted back to the PCD. During command processing (FDT) there shall be a drop in the voltage due to active digital logic. A voltage sensor based mechanism is used to reduce the power consumption by controlling the clock-gating of active digital logic. This is necessary to avoid reset due to low voltage, particularly at lower field strengths. This is referred as clock-stop in this paper and this feature is necessary to achieve higher distance of operation of PICC from PCD (Lower Hmin).

Waveform in Figure 2, shows that the clock-stop triggers (vsens_clkstop_a_o) whenever voltage drops below predefined threshold voltage (vdda_int). Here voltage sensor threshold is set to 1.8v. Digital logic clocks shall be gated using vsens_clkstop_a_o.

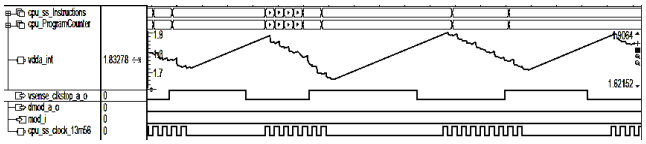


Fig. 2 shows an example of a clock-stop sensor operation

### D. *Impact on EMD due to clock-stop*

At a certain field strength based on the clock-stop threshold voltage, there is a possibility that clock-stop triggers repeatedly at a certain frequency and could fall in range of 848KHz, which is sub-carrier modulation frequency. Due to this, a voltage swing is visible as Noise at ~848KHz from the PICC. It is observed that the PCD starts understanding this Noise (~848 KHz) as a response to its command, leading to command failure.

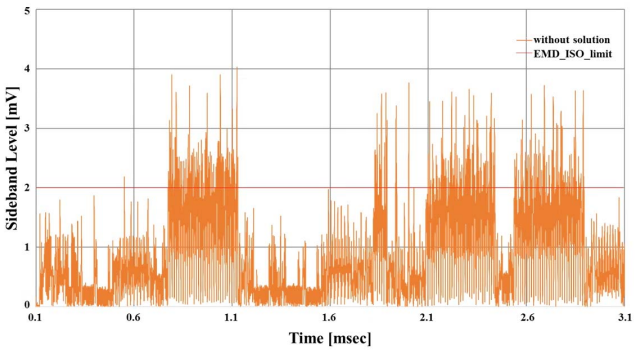


Fig. 3 LMA vs Time during FDT showing EMD levels

Figure 3 shows load modulation amplitudes (LMA) versus time of a PICC for evaluation of EMD levels as per program defined in Annex J of ISO/IEC 10373-6[3].

*E. Proposed solution*

The PCD is sensitive to EMD Noise from the PICC because, frequency of the Noise is in the range of 848KHz. Therefore, the proposed solution is to shift the EMD Noise Frequency to outside (~3.39MHz) of the PCD's response detection frequency (~848KHz), which is sub-carrier frequency of PICC response. Thus, PICC EMD noise would be undetectable to the PCD. The proposed solution is implemented using clock-stop frequency adjustment system which is configurable via non-volatile memory and has two subcomponents as shown in Figure 4,

- Clock-stop frequency detector: Detection of EMD noise frequency (clock-stop frequency) that might result as an invalid response to PCD.
- Clock-stop frequency shifter: Shifting of the EMD noise frequency to outside (~3.39MHz) of the PCD response detection frequency (~848KHz).

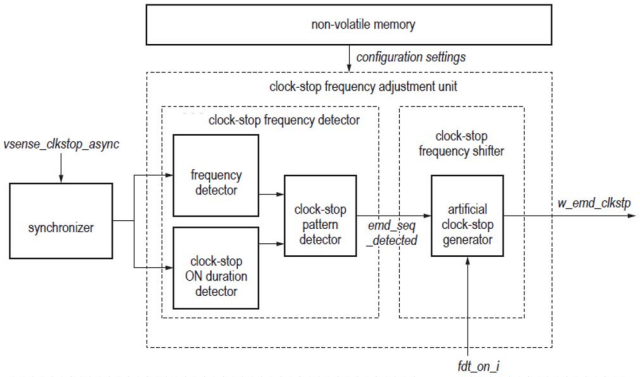


Fig. 4 Clock-stop frequency adjustment system block diagram

Function of the synchronizer, in Figure 4 is to remove glitches and to synchronize the clock-stop sensor output signal, which is an asynchronous signal from the analog domain, to the digital clock domain.

The frequency detector, in Figure 4 is configured to measure the clock-stop sensor output from the analog domain. It is configured to measure the period of the clock-stop sensor output.

The clock-stop ON duration detector in Figure 4 is configured to measure the high (logic 1) duration of the clock-stop sensor output. In other words, it is configured to measure the clock-stop sensor output duty cycle.

The clock-stop pattern detector in Figure 4 is configured to check if the frequency measured by detector falls within the configured frequency range, and to check if the ON duration measured by detector falls within the configured ON duration range. If both frequency and ON duration of the clock-sensor output fall within the configured ranges, it is concluded that a pattern has been detected. If this pattern repeats for the configured number of times, the signal *emd_seq_detected* is asserted, which indicates that unacceptable EMD noise has been detected.

The artificial clock-stop generator in Figure 4 is configured to override, once the pattern has been detected, the clock-stop sensor output with a predefined, shifted frequency and duty cycle, referred to as an artificial clock-stop (*w_emd_clkstp*). Thus, the term "artificial" is used to indicate that the shifted clock-stop signal overrides the clock-stop sensor output, which is used to gate the digital logic. The input signal *fdt_on_i* indicates a command processing duration as explained in section III. Unacceptable EMD noise is particularly harmful during the processing of a command. Thus, the signal *fdt_on_i* is used to activate the artificial clock-stop generation module during processing of the command.

*a. Clock-stop frequency detector*

It monitors the clock-stop frequency and its duty cycle. For example, identify if the clock-stop frequency is in the range of ~600KHz to 1MHz and Duty cycle is in the range of 20% to 80% (ON duration). This range would be treated as PCD detectable EMD Noise.

Figure 5 shows that clock-stop (*vsense_clkstop_a_o*) at a frequency of around 848KHz and hence is detected, seen on signal, *emd_seq_detected*.

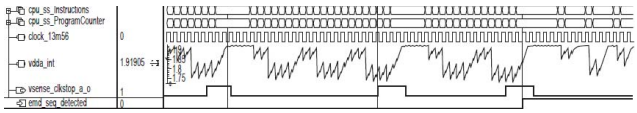


Fig. 5 Mixed signal simulation showing EMD Noise frequency detection

The pattern detection parameters and its number of occurrence are configurable via NV memory.

*b. Clock-stop frequency shifter*

On detection of the PCD detectable EMD Noise frequency, generate an artificial clock-stop at frequency of 3.39MHz.

Figure 6 shows that an artificial clock-stop signal (*w_emd_clkstp*) is generated at 3.39MHz frequency after detecting the clock-stop frequency of around 848KHz (*emd_seq_detected*)

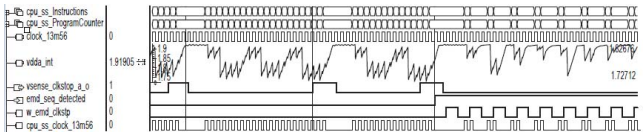


Fig. 6 Mixed signal simulation showing artificial clock-stop generation

The resulting artificial clock-stop frequency and duty cycle can be configured via NV memory.

Separate set of parameters can be chosen for different set of commands, say one set for layer 3 commands and another set for layer 4 commands as per ISO14443.

For example, the artificial clock-stop duty cycle could be 50% for layer 3 commands, whereas 75% for layer 4

commands, etc. An illustration of 75% (3:1) and 50% (2:2) duty cycle of clock-stop generation as shown in Figure 7.

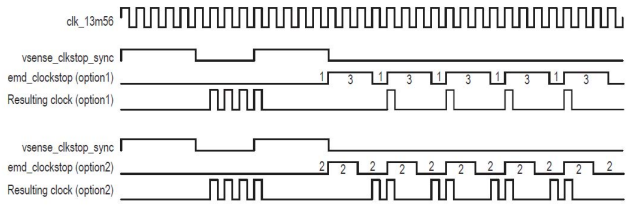


Fig. 7 Illustration of artificial clock-stop duty cycle, 75% and 50%

## III. Measurements & Results

Simulation and Silicon results have been measured and a comparative analysis has been made in this section to understand the EMD improvements of the proposed solution. Section A compares the EMD level vs Time, Section B compares EMDpeak vs field strength and the impact on the FDT by the solution with respect to field strength is compared in Section C. Section D has the area details.

### *A. EMD level vs Time*

The EMD level vs Time comparison is done from simulation data and silicon measurements.

#### *a. EMD vs Time simulation results*

Figure 8, shows EMD levels during FDT with the proposed solution (dark blue) against without solution (orange) at a field strength of 0.3A/m from the digital power trace and Analog simulation data. It is evident from the results that the proposed solution is showing lower EMD noise level of 1mV peak compared to 4mV peak.

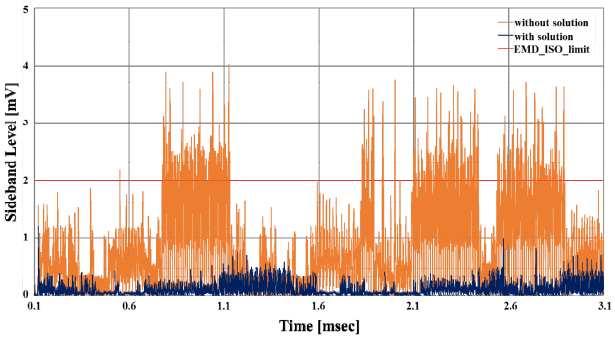


Fig. 8 EMD vs Time using simulation data comparing solutions

#### *b. EMD vs Time silicon results*

The EMD level measurement on silicon were performed and compared as shown in Figure 9, at a field strength 0.3A/m. A similar trend of EMD noise reduction as in simulation result is observed. It can be noted from the Figure 9 that the EMD level without solution is at least 2mV and above throughout the FDT, which is a major cause for false interpretation of response by a PCD. It is also noted that though FDT with the solution is approximately doubled at this field strength, however it is accepted as the communication is reliable and stable without misinterpretation of processing as response. At this field strength, we can observe at approximately 20usec, a first high EMD peak of 1.5mV is visible (* marker). This high EMD peak is required by the detection logic to inject artificial clock-stop as described in Sub-Section E of Implementation Section II. This first peak would occur anytime during FDT whenever the EMD noise is detected. This EMDpeak would not occur at low EMD time as specified in [2], Section 8.2 EMD handling timing constraints.

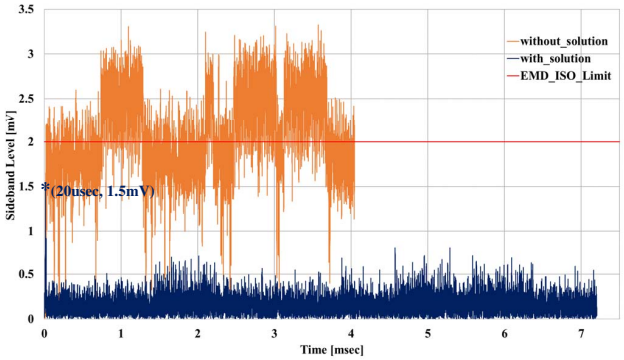


Fig. 9 Silicon EMD result comparison for complete FDT

### *B. EMDpeak vs Field Strength silicon results*

The maximum EMD level during FDT at a given field strength is referred as EMDpeak. Figure 10, shows silicon results of EMDpeak versus field strength. The proposed solution is showing clear advantage till 0.7A/m field strength where EMD is high and might create false response. It is also observed that the solution is not introducing the artificial clock-stop from 0.75A/m onwards as the pattern detector allowed the clock-stop pattern that is not creating the high EMD levels. Thus both the curves follow each other above 0.75A/m. The EMD level specification in [1] is used for the limits as depicted in curve "EMD_ISO_limit". Even though [1] specification defines from 1.5A/m, for analysis 2mV is used as limit for field strength less than 1.5A/m.

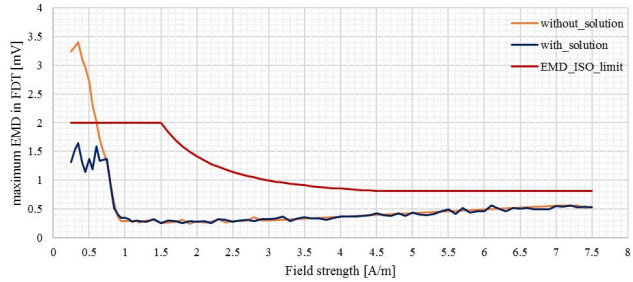


Fig. 10 EMDpeak vs field strength comparison

### *C. Impact on FDT vs Field Strength silicon results*

Figure 11, shows FDT vs field strength comparison between clock-stop only (or without solution) to the proposed solution from silicon measurements. It is observed that the processing time is slowed down at low field strengths till 0.75A/m for proposed solution and has same FDT from

0.8A/m onwards. At 0.75A/m even though artificial clock-stop is not triggered, the FDT is higher with solution as the EMD detection logic consumes additional power and delays the charging time of clock-stop sensor compared to without logic.

The scale down factor (green) is a ratio of FDT with solution to without solution and is incorporated in the same figure 11 for simplicity. The highest scale down factor of 2.46 is observed at 0.45A/m and average of 1.76 is observed, indicating the performance degradation in the low field strengths.

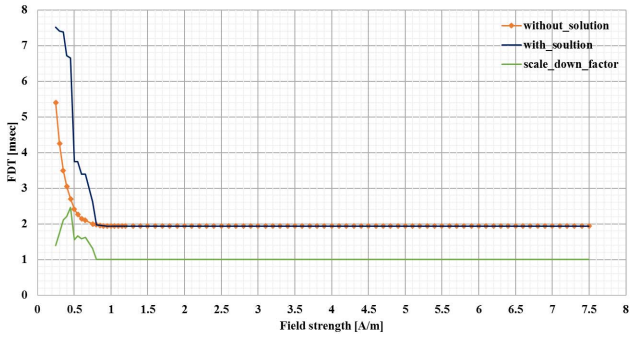


Fig. 11 FDT vs field strength comparison

### D. *Impact on Area*

The implemented solution has an area overhead of approximately 400 NAND equivalent gates, including the clock-stop sensor.

## IV. Conclusion

In PICC application, EMD noise is a challenge and creates instability in the communication with PCD. The proposed solution shows a clear advantage from the simulation results and been validated on silicon. Since an existing clock-stop sensor has been re-used to derive this solution, this is a simple and cost-effective approach compared to other solutions.

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