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Stability Analysis of SRAM Designed Using $In_{0.53}Ga_{0.47}As$ nFinFET with Underlap Region

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***Abstract*—In this paper, the static noise margin (SNM) performance of 6T-static random access memory (SRAM) cell has been demonstrated by utilizing sub-14 nm $In_{0.53}Ga_{0.47}As$ nFinFET devices with underlap fin length (L_{un}) for low-voltage operation. The quantum corrected drift-diffusion model along with density gradient approach is used to perform the simulation for$In_{0.53}Ga_{0.47}As$ nFinFET with 14 nm channel length. We have assessed the impact on the SRAM stability with the help of SPICE simulations using the BSIM-CMG model. Simulations have been carried out with different L_{un} values such as 0, 3, 6, 9 nm to extract SRAM stability parameters. The device with L_{un}= 9 nm has reported the Static Voltage Noise Margin (SVNM) and Write Trip Voltage (WTV) of 6T-SRAM with 281 mV and 251 mV, respectively using an N-curve technique.**

***Index Terms*—$In_{0.53}Ga_{0.47}As$ nFinFET, N-curve, SRAM and Underlap Fin Length**

I. Introduction

Beyond 16 nm technology, III-V channel materials FETs has been contemplated as better candidate to expand the scaling trend for increasing device switching speed [1]. The solution to this problem is III-V semiconductor compound materials, having high injection velocity and electron mobility i.e about 10 times higher than that of silicon devices [2], [3]. In high speed processors, SRAM caches the performance are vital for storing the data. When SRAM integration is done with InGaAs FinFETs it gets affected due various short channel effects (SCEs) parameters and deteriorate the performance of it. Especially leakage current affects the SRAM stability during read/write operation.

In sub-14 nm region suppression SCEs can be achieved through techniques like incorporating the underlap region [4], [5]. This technique significantly helps in reducing SCEs, but at the cost of I_{on} [6]. In general, devices with higher underlap fin length causes lower I_{on} but nFinFETs with $In_{0.53}Ga_{0.47}As$ tries to compensate its effect due to higher mobility as compared to Silicon nFinFETs. Effect of underlap fin length on 6T-SRAM cells are carried out using N-curve and SNM. The analysis is performed using BSIM-CMG spice model which is calibrated according to TCAD simulated devices. It has been observed that the better control of underlap fin length in $In_{0.53}Ga_{0.47}As$ nFinFETs results in good stability of SRAM during read/write operation. L_{un}= 9 nm shows the enhancement of 8.9% and 5.9% in SVNM and WTV respectively compared to L_{un}= 0 nm. Apart from N-curve parameters the SNM of L_{un}= 9 nm is 9.3% more compared to L_{un}= 0 nm. The rest of the paper has been organized as follows: The device structure and simulation methodology adopted to carry out the investigation is discussed in Section 2. Section 3 describes about the significance of underlap region in SRAM with detailed discussion on its stability parameters and the paper concludes with Section 4.

II. Device Formation and Simulation Framework

The cross section view of 14 nm channel length $In_{0.53}Ga_{0.47}As$ nFinFET device is shown in Fig. 1(a). 3-D TCAD Synopsys tool is used to design and simulate the device. The framework of device physics used for the simulating 14 nm channel length FinFETs have been incorporated by various physics models adopted in [7], [5]. The Verilog-A model of BSIM-CMG was used and calibrated according to the simulated devices of TCAD tools via Spectre circuit simulator. The various material parameters and process parameters are incorporated in verilog A file. Using Verilog-A file of BSIM-CMG a simple nFinFET was characterized and was compared with TCAD characterized devices. The parameters are then optimized to obtain the similar characterization as that of TCAD simulated devices. The parameters associate with I_{ds}-V_{gs} and C_{gg}-V_{gs} are optimized according to the desired characteristics. The tuning of various parameters were done apart from the material parameters to obtain the BSIM-CMG model file for 14 nm channel length $In_{0.53}Ga_{0.47}As$ nFinFETs [8]. The parameters used for simulating the device are mentioned in table of Fig.1(b). Silicon based PTM 14 nm FinFET model [9] is used for pmos device in 6T-SRAM. The 6T-SRAM cell schematic is shown in Fig.1(c). The calibration of TCAD simulated device and BSIM-CMG spice model is shown in Fig.1(b). The low power application of all the underlap devices were carried out using spice model generated by BSIM-CMG model file. SRAM performance for different L_{un} was carried out using BSIM-CMG model.

The performance parameters of sub 14 nm for the underlap $In_{0.53}Ga_{0.47}As$ FinFETs devices are extracted using 3-D TCAD SDEVICE Synopsys tool [10]. The characteristics of devices are simulated using the quantum corrected drift-diffusion and density gradient transport models. I_{off} of 100 nA/μm is adjusted to obtain other parameters of the $In_{0.53}Ga_{0.47}As$ FinFETs according to ITRS [11]. The major effect of the traps are observed in SS which plays an important role in defining the SCEs. SS for L_{un} = 3 nm, 6 nm and 9 nm 97.35, 88.21 and 87.96 mV/decade respectively. The

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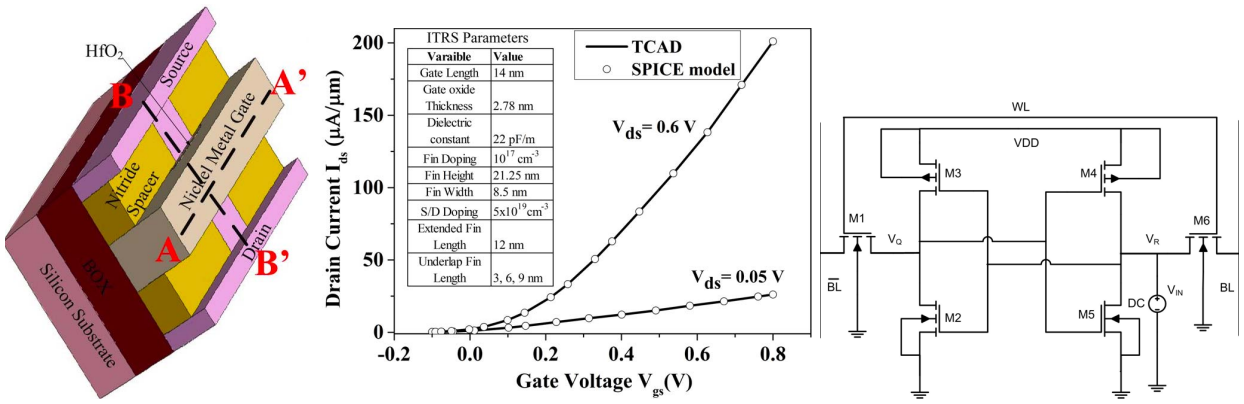

(a) (b) (c)

Fig. 1. FinFET structure (a) 3-D view (b) Calibration of I_{ds}-V_{gs} TCAD result with BSIM-CMG spice model (c) 6T-SRAM Cell

improvement in SS suggests the predominance of underlap fin length over conventional devices.

III. Results and Discussions

Figure.1(c) shows the schematic for calculating the read and write stability of conventional 6T-SRAM. The various parameters which are obtained from N-curve are related to 6T-SRAM stability factors. SVNM, Static current noise margin (SINM), Write Trip Current (WTI) and Write Trip Voltage (WTV) Figure.2 reflects both WTV and WTI for all the cells. Better read stability, is obtained when the values of SVNM, and the magnitude of SINM higher which relates to low static power. However, for preferable write ability WTV and WTI must be less.

TABLE I
N-Curve Parameters of 6T-SRAM cell

L_{un}(nm)	A(mV)	B(mV)	SINM(uA)	WTI(uA)	C(mV)	SVNM(mV)	WTV(mV)
0	71	329	1.04	2.19	596	258(0%)	267(0%)
3	70	334	1.1873	2.25	597	264(2%↑)	263(1.4%↓)
6	67	340	1.30	2.32	598	273(5.8%↑)	257(3.7%↓)
9	65	347	1.53	2.44	598	281(8.9%↑)	251(5.9%↓)

SVNM obtained for L_{un}= 9 nm is 281 mV. The improvement of 8.9% is observed in SVNM as compared to non underlap device SRAM. Table.I display all the stability parameters of 6T-SRAM. The dominant of L_{un} is observed in stability parameters for during read operations. For L_{un}= 9 nm WTV is 5.9% lower compared to non underlap device SRAM. WTI for L_{un}= 9 nm is 2.44 μA which is higher compared to other devices.

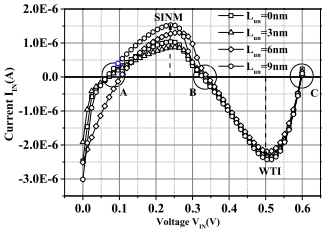

Fig. 2. N-Curve of SRAM cell for L_{un}= 0, 3 nm, 6 nm and 9 nm

SNM of 6T-SRAM is acquired by read and write operation. In read operation, initially V_R= 0 V and V_Q= V_{dd} are assumed. The presence of underlap help to provide better SNM as it restricts the flipping of node voltage during any of the operation. L_{un}= 9 nm has the SNM of 140 mV. SNM of L_{un}= 9 nm is 9.3% higher compared to L_{un}= 0 nm. SNM of higher underlap region produces the good stability of SRAM.

IV. Conclusion

Analysis of sub-14 nm $In_{0.53}Ga_{0.47}As$ nFinFETs devices with different L_{un} has been carried out for 6T-SRAM. The parameters like SINM, SVNM, WTI and WTV are analysed for the L_{un}= 0, 3, 6 and 9 nm. VAlues for SVNM and WTV are observed as 281 mV and 251 mV respectively for L_{un}= 9 nm, while SNM is 140 mV. The electrical characteristics of higher L_{un} shows better control over gate and results into improved SS but at the cost of low current. Better control of L_{un} on gate of nFinFETs implies the good read/write stability of SRAM. However, this current degradation is compensated due to higher mobility of $In_{0.53}Ga_{0.47}As$ nFinFETs as compared to Silicon nFinFETs for same L_{un}.

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