Investigation of Unified emerging-NVM SoC Architecture for IoT-WSN Applications

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***Abstract*—In this paper, we discuss the application of emerging NVM (Non-Volatile Memory) devices such as Phase Change Memory (PCM), OxRAM (oxide based), and magneto resisitive STT-MRAM memory in System-on-Chip (SoC) used for IoT-WSN (Wireless Sensor Node) applications. We validate the concept of a unified memory architecture relying on all NVM implementation, in particular for IoT-WSN applications. Simulation and analysis for NVM based unified memory architecture are presented on MSP430 platform with Contiki, benchmarked for the Sky-Collect application. Performance parameters such as-area, write hits, write hit rate/evolution, power and latency are considered.**

***Index Terms*—IoT, Wireless Sensor Nodes, Non-Volatile Memory, unified memory, OxRAM, PCM, STT-MRAM.**

I. Introduction

Ubiquitous sensing enabled by Wireless Sensor Network (WSN) technologies cuts across many areas of modern day living. This offers the ability to measure, infer and understand environmental indicators, from delicate ecologies, natural resources to urban environments. The proliferation of these devices in a communicating-actuating network creates the Internet of Things (IoT). Fueled by the recent adaptation of a variety of enabling wireless technologies such as RFID tags, embedded sensor and actuator nodes, the IoT has stepped out of its infancy and is the next revolutionary technology in transforming the Internet into a fully integrated Future Internet [1]. In a typical application scenario, IoT-WSN (Wireless Sensor Nodes) must autonomously acquire, record and wirelessly transmit signals (from sensors) over extended periods of time, while relying on small batteries or energy harvesters. Thus, power efficiency of the entire system, from acquisition to transmission, is essential for such systems. [2]

A major cause of energy dissipation in such systems is typically the main memory and the extra memory operations needed to perform wake-up from sleep by loading boot code back from ROM to RAM. The advent of emerging NVM technologies presents us with an opportunity to further optimize these systems. Owing to their inherent non-volatility use of emerging NVM devices will solve the need for a dedicated backup mode/ROM.

In this paper, we discuss the design of an IoT-WSN SoC which exploits the characteristics of emerging NVM devices when used as unified memory using some standard architectural research tools. We analyze the application performance profiles on a standard IoT sensor node. Additional analysis shows how these limitations of the NVM devices in terms of endurance and write energy don't pose any challenges to their applicability for IoT applications or degrade the expected improvements in performance.

TABLE I
BENCHMARKING EMERGING RESISTIVE NVM AND SRAM [8]

	SRAM	**STT-MRAM**	**PCM**	**OxRAM**
Area (F^2)	>100	6-50	4-30	4-12
Voltage	1	1	2	2
Read Time	∼1 ns	<10 ns	<10 ns	<10 ns
Write/Erase Time	∼1 ns	<10 ns	∼50 ns	<10 ns
Retention	NA	>10 years	>10 years	>10 years
Endurance	$> 10^{16}$	$> 10^{15}$	$> 10^{9}$	$> 10^{6} - 10^{12}$
Write Energy/bit	∼fJ	∼0.1 pJ	∼10 pJ	∼0.1 pJ

II. Background

A. Wireless Sensor Nodes

A variety of wireless sensor node platforms (Motes) are available in the market. Prominent ones include micro-controllers based on ARM Cortex-M series, TI MSP430, and Atmels ATMEGA series. Most network oriented IoT realizations involve simple micro-controllers with wireless-interface, and multiple interfaces for connecting a variety of sensors. Almost all realizations include an on-chip RAM and EEPROM. These micro-controllers are typically ultra-low power so that they can ensure a longer battery life during operation. This also enables use of energy harvesting in certain cases.

B. Emerging NVM devices

Emerging NVM devices like STT-MRAM, PCM, and OxRAM have been widely proposed for IoT applications [3], [4], [5], [2], [6], owing to their inherent advantages such as-high density, low power, high endurance, non-volatility, 3D integration, etc. Table I shows a benchmarking of various NVM devices with that of SRAM. While latency/write-speeds of emerging NVM stands as the main bottleneck preventing them from directly replacing conventional SRAM, the NVM devices fare better for several other parameters. Recent developments have reported STT-MRAM with speeds as low as ∼200 ps [7].

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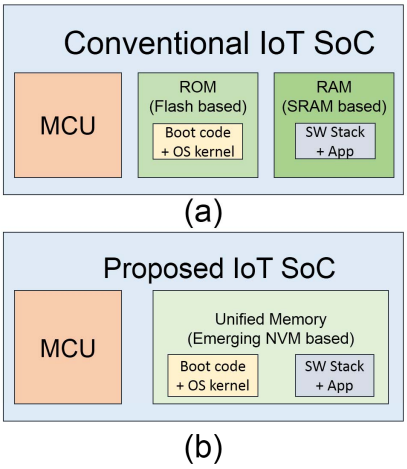

Fig. 1. IoT SoC Architectures : (a) Conventional IoT SoC (b) Proposed IoT SoC (unified memory design)

III. Proposed Unified Memory Architecture

Conventional IoT-WSN SoC architecture (Fig. 1(a)) uses two separate memories: (i) RAM and (ii) ROM for separate applications resulting in more area and power consumption. We propose a novel IoT-WSN SoC architecture (Fig. 1(b)) wherein the ROM and RAM are combined as a single unified memory block based on emerging NVM devices. The unified memory will store the OS and also serve as the main memory for the micro-controller. Unified memory would lead to near instantaneous wake-up from sleep mode, reduced power consumption, and low on-chip area requirement. To validate the applicability of the unified NVM IoT-WSN SoC concept we performed extensive custom simulations described in the subsequent sections.

A. Simulation Setup

The device under consideration for this work is a TI MSP430 micro-controller based WSN (Mote). We used the following applications for simulations:

- MSPSIM [9]: A java based simulator for cycle accurate simulation of various MSP430 based platforms for IoT-WSN applications. It is an event simulator with instruction level simulation capability.
- Contiki [10] : An open-source OS for WSN.
- NVSIM [11] : An architectural research tool for estimating performance parameters for emerging NVM devices. It comprises circuit-level models for estimating NVM device performance, energy, and area. It supports various NVM technologies such as- STT-RAM, PCM and OxRAM.

B. Simulated Platform

The simulated platform used for this work is Tmote Sky. It is an ultra low-power wireless module used for- sensor networks, monitoring and rapid prototyping applications. Tmote Sky uses TI MSP430F1611 (block diagram shown in Fig. 3).

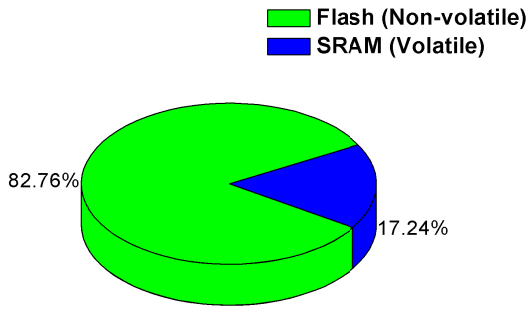

Fig. 2. Memory breakdown based on type of memory for MSP430F1611.

TABLE II
Memory organization of MSP430F1611 [12]

Technology	Description	Parameter	Value
Flash	Memory	Size	48kB
	Interrupt vector	Address	0FFFFh-0FFE0h
	Code memory	Address	0FFFFh-04000h
SRAM	RAM	Size	10kB
		Address	038FFh-01100h
Flash	Information memory	Size	256 Byte
		Address	010FFh-01000h
EEPROM	Boot Memory	Size	1kB

Detailed memory organization of the simulated controller is shown in Table II. The controller includes 10 kB SRAM and 48 kB Flash. Fig. 2 we can observe that majority of the on-chip memory is non-volatile (Flash). However, Flash is slow and has low endurance. Therefore, several new emerging NVM technologies are being developed [13]–[16]; such as STT-MRAM, RRAM and PCM, which have higher endurance, high scalability and are fast. Hence replacing the current memory with emerging NVM would improve performance and area for this partition of the memory. The challenge would be to meet the performance of the SRAM partition. Memory profiling results shown in Section III-D consider the SRAM part of the microcontroller.

C. Simulated IoT WSN Application

Table III shows the estimated memory footprint (RAM/ROM requirements) of some typical micro-controller + IoT sensor applications. The Sky-collect application [10] in particular, was used for benchmarking as it collects data from multiple sensors and transmits over wireless network to a central receiver, thus making it a typical case study for IoT-WSN.

D. Memory profiling results

IoT-WSN application specific memory requirement estimates as obtained from the MSP430 compiler for the Contiki OS are shown in Table III. It can be seen from the table that all applications require a relatively larger ROM compared to RAM for the application execution.

As the RAM of the micro-controller is responsible for performing most of the memory operations (i.e. read/write), we

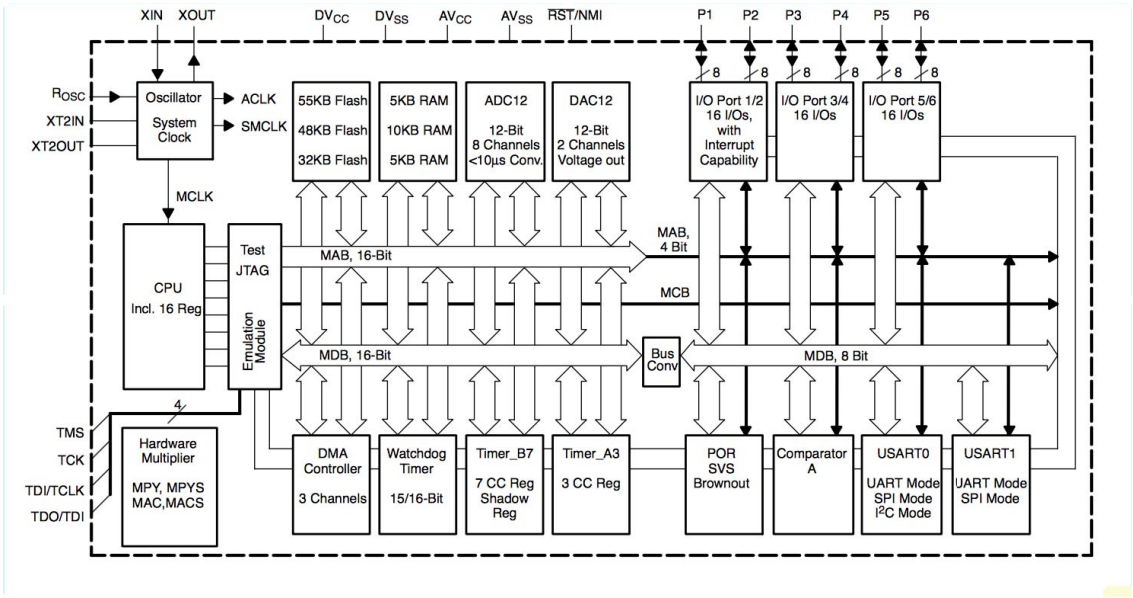

Fig. 3. Functional block diagram of TI MSP430F1611 [12]

TABLE III
MEMORY FOOTPRINT OF TYPICAL CONTIKI IOT WSN APPLICATIONS

Application	RAM size (B)	ROM size (B)	Description of application
test-adxl345	3596	31742	Accelerometer (Motion)
test-reed-sensor	2984	20280	Proximity
test-tlc59116	2958	20156	LED Driver
test-tmp102	2958	20144	Temperature sensor
sky-collect	7504	36719	Collect sensor data from 4 wireless sensors and transmit

are required to obtain a memory profile showing the number of read/write during the entire application execution. In order to profile the memory operations performed on the on-chip RAM of the simulated micro-controller we altered the MSPSIM simulator code (adding lines of code providing a statistical summary of the memory profile (Table IV)). It was observed that a majority of RAM operations performed were of read-type. Important parameters for evaluating the use of NVM devices in the system are: write-hit rate for single NVM bit-cell, ratio of processor operating speed and maximum write speed supported by the NVM memory type. In the ideal case we would want both these parameters to have a small value; i.e. smaller write-hit rate/per NVM bit-cell, and ratio <1.

Number of write hits over the entire RAM for Sky-Collect is shown in Fig. 4. Note that most of the write hits are concentrated in a small localized area of the memory. The evolution of write hits and write hit rate with time is shown in Fig. 5. Number of write operations were found to increase

TABLE IV
RAM USAGE STATISTICS FOR SKY-COLLECT APPLICATION (12S EMULATED TIME)

	Read	Write
Total operations	5.77E+05	3.12E+05
Unique addresses	6.91E+02	7.52E+03
Max hits	3.54E+04	2.10E+04

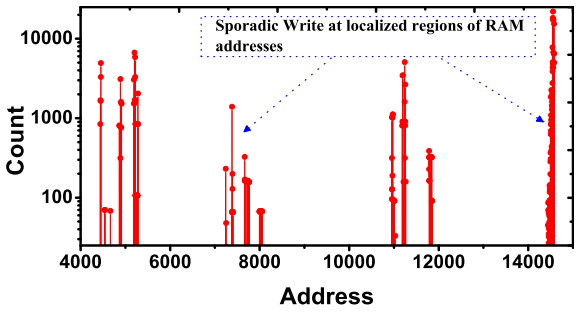

Fig. 4. Memory write hit profile for IoT application Sky-collect. It can be observed that the writes are concentrated in localized RAM address rather than being uniformly distributed. Thus, the write profile is fairly sporadic in nature.

linearly with time resulting in a nearly constant rate of write.

IV. DISCUSSION AND ANALYSIS

There are three major limitations of emerging NVM devices which can limit their applicability. They are listed as follows:

- Write-latency
- Write-energy
- Endurance

TABLE V
MEMORY WRITE STATISTICS FOR SKY-COLLECT APPLICATION

Emulated time (s)	Max write hit	Max writes per cycle	Max write per ms
2.65	4.34E+03	1.63E-06	1.63
5.18	9.14E+03	1.76E-06	1.76
7.28	1.31E+04	1.79E-06	1.79
12.15	2.20E+04	1.81E-06	1.81

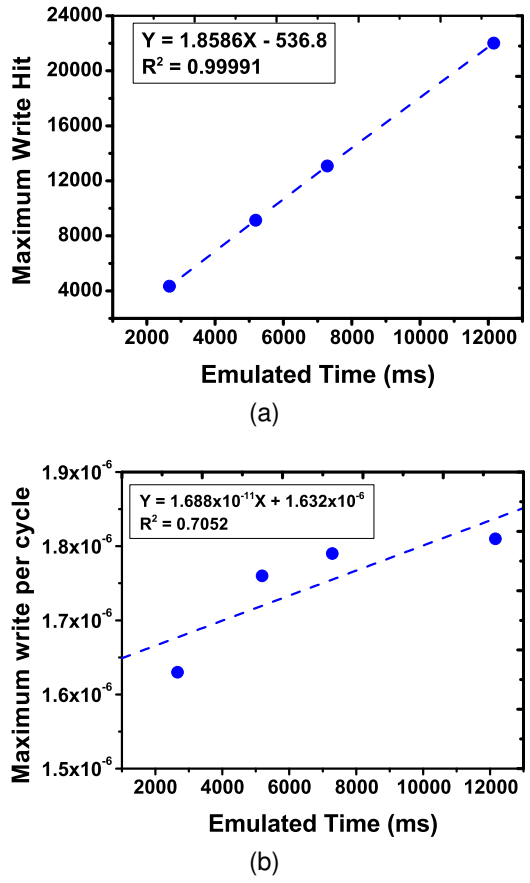

Fig. 5. Variation of (a) maximum write hits and (b) total max writes/cycle with time for Sky-collect application over the entire RAM.

In this section we discuss ways to overcome each limitation separately as a result of the application constraints. Then we discuss implications of replacing SRAM with NVM through a detailed analysis using parameters like area, power and EDP.

A. Solutions to limitations of NVM for unified-memory architectures in context of IoT-WSN

1) Memory write latency: : Most IoT WSN applications require intermittent operations which consist of sensor reading and data transmission with long sleep cycles. As a result developing support for normally-off computing in these systems would lead to better energy utilization as they are primarily powered using batteries. Moreover, since the most time critical part of the IoT WSN application is sensor data recording using a micro-controller, the memory-write latency of NVM based memories is not a major bottleneck in the implementation since most sensors of interest don't have a very high sampling rate. After this sensor read, the memory will achieve stable state due to the use of NVM as main memory before the IoT WSN goes into sleep mode and transmits the sensor data on the next wake up interrupt. This facilitates a fault-tolerant operation, faster wake-up time due to persistent memory state, and lower energy requirements overall.

2) Memory write energy: : As can be seen from Table IV, the number of read operations dominate the number of write operations for most IoT-WSN applications. Hence higher write energy observed in case of certain emerging NVM devices is not as detrimental for their application as main memory.

3) Endurance: : Certain emerging NVM devices (PCM, OxRAM) have limited endurance compared to SRAM, which makes them more suitable for ROM-type applications. From Fig. 4 and Table V, it is evident that write operations are sporadic and concentrated only in localized regions of the RAM. Hence, the endurance limitations can be overcome to some extent by distributing accesses across the memory space, rather than overwriting the same cells repeatedly. For this purpose, the high density offered by emerging NVM can also be exploited by introducing redundancy. This strategy can lead to a better memory write-hit profile as compared to the one shown in in Fig. 4 thus making even low-endurance device technologies (PCM,OxRAM) more applicable for main memory applications.

B. Performance analysis of NVM devices for unified-memory in IoT-WSN

To further support the case for emerging NVM in the proposed unified concept architecture, we compared the performance of SRAM and various NVM technologies using the NVSim [11] tool for a 16 kB RAM memory with a 16-bit wide data-bus at 65 nm technology node. The said configuration is chosen such that it is closest to the case of the simulated micro-controller for IoT-WSN applications. Table VI shows the read/write dynamic energy, leakage power, area, read/write latency, and estimated application specific total power for- PCM, STT-MRAM, OxRAM and SRAM for the above mentioned configuration.

1) Power and Energy Analysis: The power and energy performance of the system is analyzed considering both the dynamic energy and the leakage power. Dynamic energy estimate includes both transient dynamic energy of the peripheral circuit and the NVM device bit-cell. Dynamic energy presented in Table VI is at the level of a single memory operation. From Fig. 6 it can be seen that both the read and the write dynamic energy for STT-MRAM and OxRAM are very much comparable to SRAM's dynamic energy values giving us a fair advantage of replacing SRAM type of RAM with NVM type RAM with the same dynamic energy performance. Leakage power for all three types of NVM devices for the WSN application was found to be less than that of SRAM based implementation. It can also be observed from the figure that the percentage contribution of the leakage power is more for NVM

TABLE VI
PERFORMANCE BENCHMARKING OF EMERGING NVM AND SRAM FOR SIMULATED APPLICATION USING NVSIM.

Device	Dynamic energy (pJ)		Leakage Power (mW)	Area (mm^2)	Latency (ns)		Skycollect simulation statistics	
	Read	Write			Read	Write	Total Power (mW)	Delay(ms)
SRAM	14.54	14.22	148.94	1.12	0.35	0.33	190.71	0.31
STT-MRAM	17.54	18.15	99.38	1.09	1.26	5.62	105.74	2.48
OxRAM	9.84	17.91	98.25	0.55	0.31	150.26	98.48	47.13
PCM	10.23	80	108.36	0.35	0.77	20.13	112.94	6.74

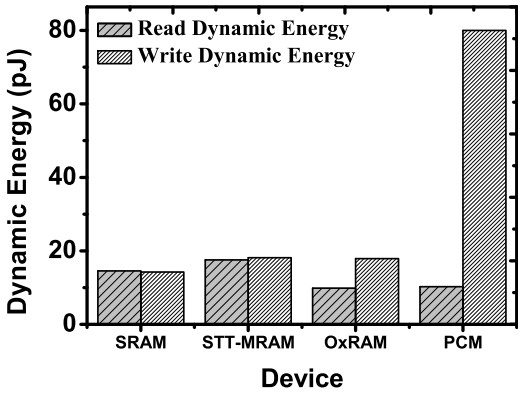

Fig. 6. Dynamic Energy for Read and Write Operations with SRAM and different NVM devices. While the read dynamic energy for all NVM devices are comparable to that of SRAM, the write dynamic energy is quiet high for PCM devices, while STT-MRAM and OxRAM shows comparable values to SRAM.

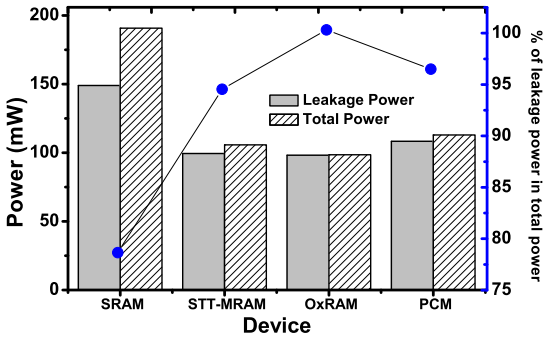

Fig. 7. Leakage power and total power consumption of the system for IoT WSN application for SRAM and different NVM devices. The blue dots in the plot shows the % contribution of the leakage power in the total power of the system.

device based RAM as compared to SRAM based RAM. Since the leakage current in NVM devices are negligible/almost zero [17], the leakage power is mostly contributed by the peripheral circuit associated with it as compared to the memory array. We also observe from Fig. 7 that all NVM devices save about $\sim$ 50% in power budget which may have a large impact on the battery life.

2) Timing Analysis: Delay estimates from Fig. 8 indicates that both STT-MRAM and PCM latencies are compatible with MSP430 processor frequency of 80 MHz. As MSP430

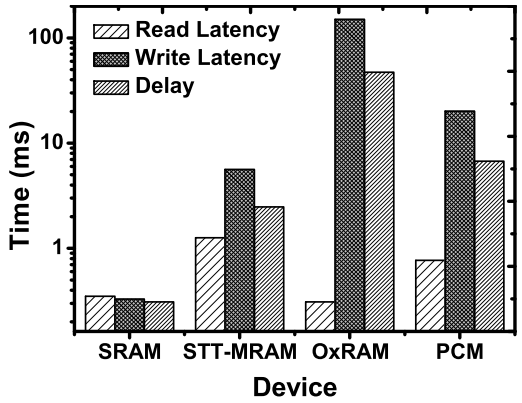

Fig. 8. Latency and Delay estimates for the MSP430 processor for SRAM based RAM and different NVM devices based RAM. The processor is operating at a frequency of 80 MHz.

instructions referencing data from RAM require a minimum of 4 cycles [18] for execution, the minimum required latency is approximately $\sim$ 64 ns. As a result of this application execution time will not be affected. Fig. 8 also gives an insight to the read and the write latencies of SRAM and NVM based RAM in the MSP430 processor. It can be observed that the write latencies for the NVM devices are higher than that of SRAM. But since the write profile for the WSN application is largely sporadic, the overall effect on the performance is not an issue. It can also be observed that the read latencies of STT-MRAM and PCM are comparable to that of SRAM, thus, will not affect the performance of the processor seriously.

3) Area Analysis: Area advantage is best in case of PCM as can be seen in Table VI. PCM gives an area advantage of $\sim$69% as compared to SRAM. This means that in same on-chip area at 65 nm technology node, the PCM based RAM can have more than double the capacity as compared to SRAM. While OxRAM based RAM gives an area advantage of $\sim$50%, STT-MRAM based RAM gives an area advantage of only $\sim$3%.

4) Energy Delay Product: From Fig. 9 we can see that although the EDP for all NVM device based RAM is higher than that of SRAM based RAM, the closest performance in terms of EDP is given by STT-MRAM based RAM. The EDP for STT-MRAM is 36x that of SRAM. This is due to higher latencies pertaining to STT-MRAM operations.

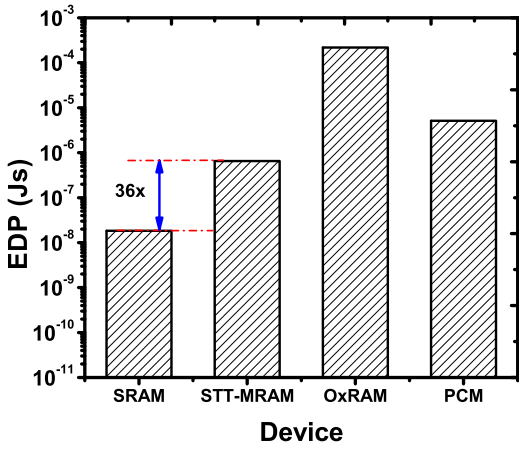

Fig. 9. Energy-Delay Product (EDP) for SRAM and different NVM based RAM

C. Implications of technology evolution

An important point to consider is that the emerging NVM devices discussed in this study are evolving by the day. Application centric benefits for the proposed unified architectures will become more visible and strengthen with time as the respective NVM device technologies mature with time in terms of write/erase speeds and switching energy.

V. Conclusion

While emerging NVM technologies such as PCM, OxRAM, STT-MRAM offer promising alternatives to flash based storage systems, they also have the potential for embedded contenders in future hybrid unified RAM-ROM architectures. While none of the emerging technologies can directly replace SRAM in terms of speed, however, interestingly purely NVM driven memory architectures can be tried for applications such as IoT-WSN as shown in this study. The NVM based unified memory architecture offers advantages in terms of area and power while incurring a tolerable penalty for operational speed and endurance/life cycle. The speed/latency limitation of the technology doesn't affect functionality of IoT-WSNs due to the lower operational frequency requirements.

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References

[1] J. Gubbi, R. Buyya, S. Marusic, and M. Palaniswami, "Internet of things (iot): A vision, architectural elements, and future directions," *Future generation computer systems*, vol. 29, no. 7, pp. 1645–1660, 2013.

[2] R. Braojos, D. Atienza, M. M. S. Aly, T. F. Wu, H.-S. P. Wong, S. Mitra, and G. Ansaloni, "Nano-engineered architectures for ultra-low power wireless body sensor nodes," in *Hardware/Software Codesign and System Synthesis (CODES+ ISSS), 2016 International Conference on*. IEEE, 2016, pp. 1–10.

[3] Y. Lu, T. Zhong, W. Hsu, S. Kim, X. Lu, J. Kan, C. Park, W. Chen, X. Li, X. Zhu *et al.*, "Fully functional perpendicular stt-mram macro embedded in 40 nm logic for energy-efficient iot applications," in *Electron Devices Meeting (IEDM), 2015 IEEE International*. IEEE, 2015, pp. 26–1.

[4] K. Lee, J. J. Kan, and S. H. Kang, "Unified embedded non-volatile memory for emerging mobile markets," in *Low Power Electronics and Design (ISLPED), 2014 IEEE/ACM International Symposium on*. IEEE, 2014, pp. 131–136.

[5] T. Nakada, T. Shimizu, and H. Nakamura, "Normally-off computing for iot systems," in *SoC Design Conference (ISOCC), 2015 International*. IEEE, 2015, pp. 147–148.

[6] T.-K. Chien, L.-Y. Chiou, S.-S. Sheu, J.-C. Lin, C.-C. Lee, T.-K. Ku, M.-J. Tsai, and C.-I. Wu, "Low-power mcu with embedded reram buffers as sensor hub for iot applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 6, no. 2, pp. 247–257, 2016.

[7] W. Zhao, E. Belhaire, C. Chappert, and P. Mazoyer, "Spin transfer torque (stt)-mram–based runtime reconfiguration fpga circuit," *ACM Trans. Embed. Comput. Syst.*, vol. 9, no. 2, pp. 14:1–14:16, Oct. 2009. [Online]. Available: http://doi.acm.org/10.1145/1596543.1596548

[8] S. Yu and P. Y. Chen, "Emerging memory technologies: Recent trends and prospects," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 43–56, Spring 2016.

[9] J. Eriksson, A. Dunkels, N. Finne, F. Osterlind, and T. Voigt, "MSPSIM–an extensible simulator for msp430-equipped sensor boards," in *Proceedings of the European Conference on Wireless Sensor Networks (EWSN), Poster/Demo session*, 2007, p. 27.

[10] A. Dunkels, B. Gronvall, and T. Voigt, "Contiki-a lightweight and flexible operating system for tiny networked sensors," in *Local Computer Networks, 2004. 29th Annual IEEE International Conference on*. IEEE, 2004, pp. 455–462.

[11] X. Dong, C. Xu, Y. Xie, and N. P. Jouppi, "Nvsim: A circuit-level performance, energy, and area model for emerging nonvolatile memory," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 7, pp. 994–1007, July 2012.

[12] T. Instruments, "MSP430F1611 mixed signal controller datasheet," 2006.

[13] L. Zhu, J. Zhou, Z. Guo, and Z. Sun, "An overview of materials issues in resistive random access memory," *Journal of Materiomics*, vol. 1, no. 4, pp. 285–295, 2015.

[14] J. S. Meena, S. M. Sze, U. Chand, and T.-Y. Tseng, "Overview of emerging nonvolatile memory technologies," *Nanoscale research letters*, vol. 9, no. 1, p. 526, 2014.

[15] R. F. Freitas and W. W. Wilcke, "Storage-class memory: The next storage system technology," *IBM Journal of Research and Development*, vol. 52, no. 4.5, pp. 439–447, 2008.

[16] P. Cappelletti, "Non volatile memory evolution and revolution," in *Electron Devices Meeting (IEDM), 2015 IEEE International*. IEEE, 2015, pp. 10–1.

[17] C. Xu, X. Dong, N. P. Jouppi, and Y. Xie, "Design implications of memristor-based rram cross-point structures," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011*. IEEE, 2011, pp. 1–6.

[18] "MSP430x5xx/MSP430x6xx family users guide," *URL:http://www.ti.com/lit/ug/slau208j/slau208p.pdf*, 2012.