Reconfigurable Digital Logic Gate based on Neuromorphic Approach

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***Abstract*— This paper presents low power and highly tuneable LIF (modified) neuron model and its usage to implement reconfigurable digital logic gate. Simulations are done using Tower Jazz Semiconductor's 180nm technology and UMC 28 nm technology in Cadence virtuoso environment. Results show the advantage of neuromorphic approach in terms of re-configurability, power and area when compared to traditional logic gate designs. Reconfigurable gate performs AND/OR/NAND/NOR/XOR/XNOR. It works for both spiking input as well as DC input (current signal). Power consumption of reconfigurable gate designed using modified LIF is at least 45% less than the power consumption of CMOS gates.**

Keywords— Neuromorphic, LIF, CMOS, reconfigurable.

I. INTRODUCTION

Modern chips are majorly populated by digital logic gates to perform multiple functions i.e. digital signal processing, algorithm execution, arithmetic operations, memory etc. The architecture of basic logic gate has remained unchanged over the period of time.

Different design approaches are reported [1-5] but a versatile gate with multiple logic operation with high fan-in and immune to process variation is not yet accomplished. Neuromorphic approach closely matches with the requirements of low power consumption, large fan-in, parallel data processing and versatile/reconfigurable gate. The proposed work addresses the design of such reconfigurable gate in standard CMOS technology which resembles with biological neuron in terms of performing multiple operations without changing its architecture.

II. NEUROMORPHIC DESIGN

Neuromorphic designs make use of very-large-scale integration (VLSI) technology containing electronic analog circuits to mimic neuro-biological architectures present in the nervous system [7]. Neuron models that have been built in silicon are basic building block for neuromorphic design as shown in Fig. 1. The applicability of the proposed circuit is demonstrated on a smaller application consisting of few neurons and synapses (shown in Fig. 1).

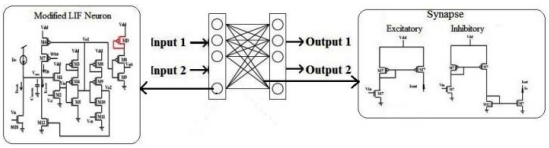

Fig. 1. Spiking neural network.

A. Low power and highly tuneable Modified LIF

Among the reported transistor level neuron models [9-11], LIF [6] has gained wide acceptance because of its ability to generate spikes at accurate time instances, tuning spike characteristics (such as fall time, spike width etc.) and architectural simplicity.

Proposed modified LIF is capable of tuning the rise time of the spikes generated and has less power consumption as compared to the LIF reported in literature [6]. Fig. 2 shows the transistor level connection of modified LIF model. Fig. 4 and Fig. 5 shows the spike output and variation of spike firing rate with applied input current to the neuron model proposed in Fig. 2.

Variation of rise time with external voltage V_{rise} is shown in Fig. 6. Power comparison results in Fig. 7 shows that proposed LIF has 45% low power consumption as compared to reported LIF [6].

The desired neuron operations are achieved by taking all NMOS having W/L ratio of 7.2μm/0.18μm and PMOS 36μm/0.18μm for Tower Jazz Semiconductor 180nm technology. Subplots in Fig. 4 to Fig. 7 show the feasibility of proposed neuron model in 28nm technology. Chip layout (180nm Tower Jazz Semiconductor) having LIF [8], proposed LIF and reconfigurable logic gate is shown in Fig.3.

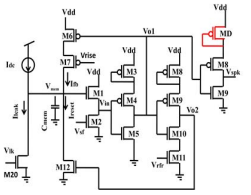

Fig. 2. Modified LIF having control on rise time of spikes.

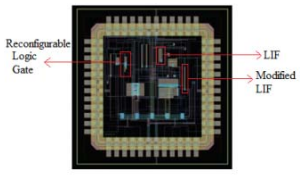

Fig. 3. Chip Layout containing proposed LIF, LIF[8] and reconfigurable logic gate using 180nm CMOS technology.

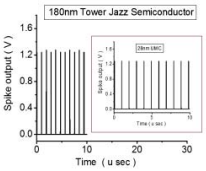

Fig. 4. Spike output of Neuron.

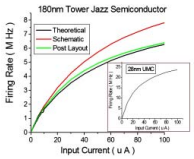

Fig. 5. Variation of frequency of spike with DC input current.

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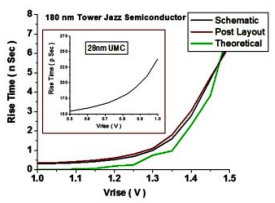

Fig. 6.Variation in rise time with rise time control signal Vrise

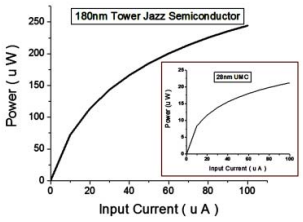

Fig.7. Power dissipation of LIF[8] and modified LIF.

B. Silicon synapse

Synapse plays an important role in connecting two neurons. Synapse produces a positive (*excitatory*) or a negative (*inhibitory*) current with different dynamics [12]. Silicon synapses are circuits that mimic working of biological synapses.

Fig. 8 and Fig. 9 shows circuits that convert incoming voltage spike signal into current spike signal. Fig. 8 produces positive/excitatory current whereas Fig. 9 produces negative/inhibitory current.

III. Reconfigurable Logic Gate Using Modified LIF and Synapse

This paper presents a reconfigurable logic gate (shown in Fig. 10) that can perform AND /OR /NAND /NOR /XOR /XNOR operations without changing its transistor level architecture. Same architecture also works when number of inputs is increased. Different functionality and fan-in is achieved by changing control voltages of neurons used in reconfigurable gate. Output of the reconfigurable gate is shown in Fig. 11.

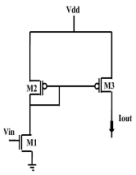

Fig. 8. Synapes circuit producing excitatory current.

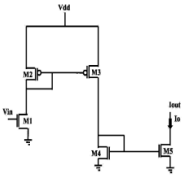

Fig. 9. Synapes circuit producing inhibitory current.

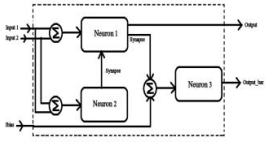

Fig. 10. Reconfigurable logic gate.

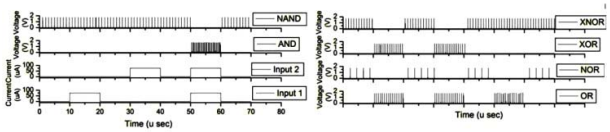

Fig. 11.Output of reconfigurable logic gate.

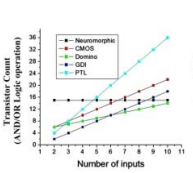

Fig. 12. Transistor Count with respect to number of inputs of gates.

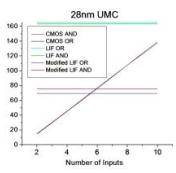

Fig. 13. Power consumption of Logic gates at 28nm.

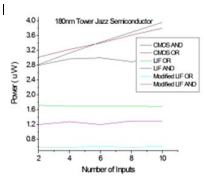

Fig. 14. Power consumption of Logic gates at 180nm.

IV. Comparison

A comparison is done for multiple inputs between neuromorphic gates and traditional logic gates to identify the power and area efficiency. Fig. 12 shows a comparison of number of transistor required for logic operation by different design approaches. For increasing the number of inputs/changing the logic in CMOS, we have to change/redesign complete circuit, but in case of neuromorphic reconfigurable gate number of inputs/Logic operation performed is controlled by voltages used to tune the neurons. Same design is tuned for 2 inputs/10inputs and performing different logic operations.

Fig.13 and Fig.14 also show that reconfigurable gate designed using proposed modified LIF is more power efficient than the gate designed using LIF.

V. Conclusion

Proposed reconfigurable gate has distinct advantage of lower area and power consumption. Apart from area and power, re-configurable and scalability down to 28nm technology without architectural change provides a major advantage. Although there is variation in spike width, fall time and rise time with temperature, process variation but they are tuned by changing V_{sf}, and V_{rise} therefore neuromorphic gates does not require any special circuit or design technique to compensate effect of temperature and process variation. Such kind of modularity in implementation, multi-functionality and in built tunability to external environmental changes will be highly useful for bio-inspired artificial intelligence, robotics etc hardware.

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