Soft Error Resilient and Energy Efficient Dual Modular TSPC Flip-Flop

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***Abstract*— In this paper we propose a novel energy efficient radiation hardened dual modular true single-phase clock flip-flop (DM-TSPC FF). We show that the existing radiation hardened TSPC flip-flop designs, *viz.* TSPC-DICE and TSPC-Quatro, have SEU tolerant latching circuits but can get upset when radiation strikes occur in the sampling circuits. Our proposed DM-TSPC FF elegantly circumvents this problem without increasing area. We have implemented all the designs in UMC 28nm technology node. We report that our proposed DM-TSPC FF has 76.16% less power-delay product (PDP) as compared to TSPC-DICE and 80.76% less PDP as compared to TSPC-Quatro. DM-TSPC FF consumes extremely low energy. It consumes 0.71 fJ compared to TSPC-DICE which consumes 6.62 fJ and TSPC-Quatro which consumes 8.43 fJ. Apart from this, we have compared the DM-TSPC flip-flop designs with other TSPC flip-flops by implementing ISCAS'89 benchmark circuits using these flip-flops. Even for large sequential designs, we find that DM-TSPC based designs consume only about 50% of the power compared to TSPC-DICE based designs and only about 20% power compared to TSPC-Quatro based designs.**

***Index Terms*: Soft error, true single phase clock (TSPC), single event transient (SET), dynamic flip-flop, single event upset (SEU), radiation tolerance.**

I. INTRODUCTION

Continuous scaling of technology has lead to the miniaturization of transistor size making the circuits more prone to errors due to radiations. This is due to the small parasitic capacitance value associated with the transistor that leads to the low critical charge associated with it to flip the bit. Transistor scaling has paved the way for high-performance designs where clock frequencies have reached gigahertz range. In such high-speed designs, alternative designs for flip-flops (FFs) have been used, including true single-phase clock flip-flop (TSPC). Dynamic TSPC FFs are those that do not have latching circuit, and the output node holds the charge using parasitic capacitance. In this paper, we have proposed and analyzed radiation-hardened TSPC flip-flop with latching circuit to be used in high-speed systems designed for space applications.

Unlike memories, which have a modular structure and are confined to a particular area, flip-flops are widespread and scattered across the chip. Hence, techniques such as error detection and correction (EDAC) [1] cannot be easily applied. Existing sequential designs use either spatial redundancy or temporal redundancy to deal with soft-errors. In the earlier works, spatial redundancy solution that has been popularly used is the triple modular redundancy (TMR) [2]. Other spatial redundancy techniques include dual modular redundancy (DMR) [3], guarded dual rail (GDRL) circuits [4], guarded dual modular redundancy (GDMR) [5], etc. The circuit is duplicated or triplicated, and the final output is derived using a voter. Temporal redundancy has a similar approach, except that in temporal redundancy the *voter* samples the same signal two or three times and decides the correct output[6]. Here, it is essential that the sampling instances are chosen such that time difference between two samples should be greater than a SET pulse width. It is clear that spatial redundancy increases the area and power requirement of the design, whereas temporal redundancy reduces the performance of the designs. For latches, flip-flops, and memory elements, Dual Interlocked storage CEll (DICE) [7] and Quatro [8] latches have gained attention as they are SEU immune latches, and at the same time are cost-effective in terms of area and power as compared to TMR or DMR latches.

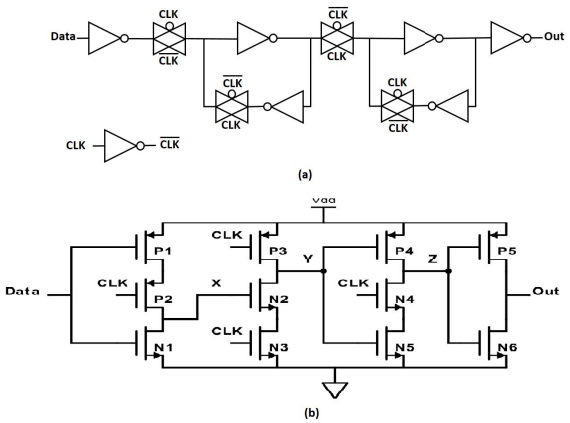

Fig. 1. Schematic Diagram (a) Master-Slave Flip-Flop (b) TSPC Flip-Flop

Flip-flops are fundamental storage elements used in the digital system and consume a significant portion of chip area. The power consumption of the flip-flops used in a digital system along with that of clock tree network constitutes a large share of total system power. Flip-flop designs thus play a major role in deciding the power consumption and performance of the system, and also affect the total chip area. A transmission gate based master-slave topology flip-flop (see Fig. 1(a)) is a widely used flip-flop circuit topology currently, but it needs both true and complementary clock signal. To overcome this drawback of static master-slave transmission gate based flip-flop, TSPC based dynamic flip-

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flop (see Fig. 1(b)) has been proposed, as it does not require a complementary clock signal [9]. The drawback of the conventional TSPC flip-flop, however, is that it fails at low clock frequencies because of leakage associated with the transistor which will flip the stored logic value if the clock period is too long. In this paper, we have proposed a new radiation hardened TSPC flip-flop that has better SEU robustness and lower power-delay product compared to the earlier radiation hardened TSPC flip-flop designs.

Following are the contributions of our work:

- We propose a new dual modular TSPC (DM-TSPC) flip-flop with guard gate voter at the output and carry out an exhaustive analysis for SEUs. Our DM-TSPC FF is immune to single-event upset.
- We show that radiation hardened TSPC-DICE and TSPC-Quatro flip-flops have single-event upset when the radiation strike occurs in the sampling circuits, but this does not happen in the proposed DM-TSPC flip-flop.
- DM-TSPC FF has lower area, average power, energy, and power-delay product as compared to radiation hardened TSPC-DICE and TSPC-Quatro, and can be used for low power applications.
- We have implemented ISCAS89 benchmark circuits to analyze system-level performance of the proposed DM-TSPC FF compared to TSPC-DICE and TSPC-Quatro.

The rest of this paper is organized as follows. In Section II we review the previously proposed TSPC based radiation hardened designs and analyze them for soft error tolerance. Section III proposed radiation hardened DM-TSPC FF design is described and analyzed for soft error robustness. In Section IV performance evaluation and results are analyzed regarding the area, delay, power and soft error robustness of designs. In Section V we show performance evaluation of DM-TSPC FF against TSPC-DICE and TSPC-Quatro at system level in terms of power and area by implementing ISCAS89 benchmark circuits using these flip-flops. Finally, the paper is concluded in Section VI.

II. Existing Soft Error Robust Flip-Flop Designs

In this section, we discuss TSPC-DICE and TSPC-Quatro designs. To compare our proposed DM-TSPC flip-flop design with these, we have also implemented these designs. We have used UMC 28nm technology to simulate all the designs, TSPC-DICE, TSPC-Quatro and proposed DM-TSPC. We have used 1.05V power supply and 1 GHz clock for simulations. All the designs have been made using minimum transistor dimensions in all the three flip-flop designs.

A single event transient (SET) is seen when a high energy particle strikes on the drain node of off transistor, it transfers its energy on its traveling trajectory and generates electron-hole pair (EHP) in the depletion region of the substrate. As the generated EHP are under the influence of reverse bias junction electric field will separate out, and this will result in the unwanted current flow from drain node to body node. We have used the double exponential current source to mimic SETs in the circuit.

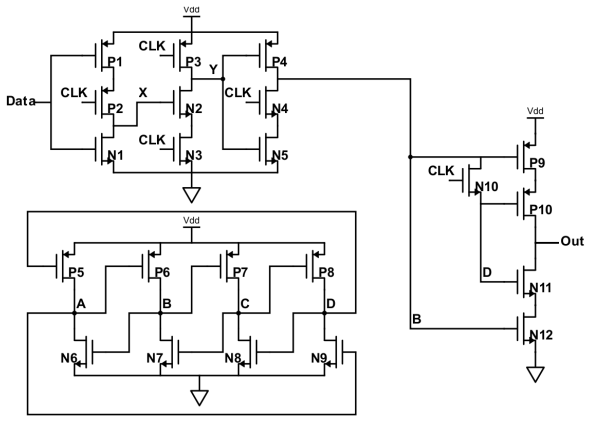

Fig. 2. Schematic Diagram of TSPC-DICE [10]

A. TSPC-DICE

The circuit diagram of true single phase clock DICE (TSPC-DICE) flip-flop [10] is shown in Fig. 2. The TSPC-DICE FF design has three stages. The first stage is TSPC input stage, the Second stage is SEU hardened DICE latch [7] and the third stage, i.e., the output stage is consist of C-element. Transistor N10 works simultaneously with the input stage to enable writing into the DICE latch at the positive edge of the clock signal (CLK). The normal operation of TSPC-DICE is shown in Fig. 5(a) where the data is latched correctly. In Fig. 5(b), we analyze TSPC-DICE for SETs/SEUs. We have used the double exponential current source to mimic SET (see Fig. 5(b)) behavior in design [11]. As shown in Fig. 5(b) the TSPC-DICE flip-flop design is not truly radiation immune.

As we know that DICE is SEU tolerant but if double node upset (DNU) or single event multiple upsets (SEMU) happens, then DICE structure gets upset [12]. In TSPC-DICE design if there is SET event when CLK= 1 such that it will create transient at node B (node D) which will get propagated to node D (node B) through low impedance path of N10 because of that, two nodes of DICE get disturbed which eventually lead to SEU [13].

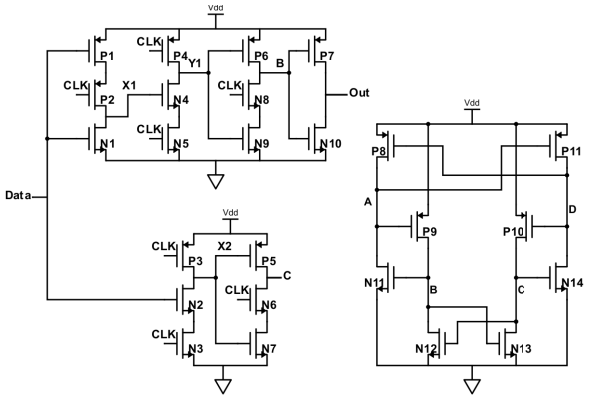

Fig. 3. Schematic Diagram of TSPC-Quatro [14]

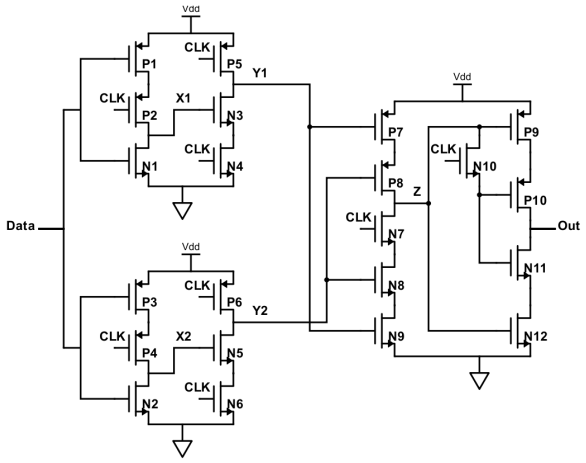

Fig. 4. Schematic Diagram of proposed DM-TSPC FF Design

B. TSPC-Quatro

TSPC-Quatro is yet another radiation tolerant flip-flop proposed in the earlier works [14]. The circuit diagram of TSPC-Quatro FF is shown in Fig. 3. The design consists of two stages, first stage consist of two parallel TSPC positive edge triggered FF and positive level Latch, and the second stage includes SEU hardened Quatro latch [8]. Fig. 6(a) shows the simulation results of TSPC-Quatro under normal condition of latching the data. Fig. 6(b) shows the simulation results when SETs are applied at different nodes in TSPC-Quatro FF. As shown in Fig. 6(b) that given design is not true radiation immune because as analyzed in [8], Quatro is sensitive to SEU, but the value of critical charge at the sensitive node is higher than unhardened design. To analyze this, let us consider the case when the internal nodes are set as, $A = 1$, $B = 0$, $C = 1$, and $D = 0$. If now a SET strike happens at node B, then irrespective of clock signal status, this SET will change the node B value from logic 0 to logic 1. Due to this, N13 and N11 will turn on simultaneously (see Fig. 3) and eventually pull down node C and node A to logic 0, which, in turn, will turn on P11 and pull up the node D to logic 1. As all nodes are now flipped from their previous state, SEU happens.

III. Proposed Soft Error Robust Flip-Flop Design

In this section, we discuss working of the RH DM-TSPC and show its radiation immunity. The circuit diagram of DM-TSPC FF is shown in Fig. 4 and simulation waveforms are shown in Fig. 7. RH DM-TSPC consists of three stages; the first stage consists of dual modular redundancy (DMR) TSPC stage, the second stage comprises of clock sensitive C-element and third stage (output stage) includes the C-element.

a) Working: The working of the DM-TSPC design is explained with the help of Fig. 4 and Fig. 7(a). When CLK=0, node X1, and node X2 is pre-charged to the complement of the logic value of Data while node Y1 and node Y2 is pre-charged to logic value 1. Consequently, P7, P8, and N7 are OFF, leaving node Z and node Out in hold state. When CLK becomes logic value 1, i.e., if Data is 1 and CLK=1, node X1 and node X2 both are a logic value 0, and node Y1 and node Y2 remains at logic value 1 (see Fig. 4), which discharges node Z. A low-resistance path through N10 then discharges both inputs of output stage C-element. Since both inputs of an output stage C-element is at logic value 0, output node Out is charged to 1, which is the same as the input data. On the other hand, if the Data is 0, and CLK=1 (assuming Data input is maintained at logic value 0 and only CLK makes transition from logic value 0 to logic value 1), node X1 and node X2 is logic value 1 and node Y1 and node Y2 are discharged to logic value 0. This charges node Z through P7 and P8 if node Z was previously holding 0. Eventually, node Out is also discharged through N11 and N12.

b) Soft error analysis: We have conducted an exhaustive SET and SEU analysis [13] on proposed dynamic flip-flop designed in 28nm UMC technology. As done in previous cases, we have used a double exponential current source to mimic SET (see Fig. 7(b)) behavior in design. As shown in Fig. 7(b), it is clear that our proposed dynamic flip-flop design is radiation hardened for all cases. As we can see from Fig. 4 that when CLK=0 there is no SET case which will simultaneously disturb both inputs of final stage C-element which will lead to upset at node Out because of high impedance offered by the N10 transistor as it is off. When CLK=1 if there is SET on node Z, then this will be seen as a temporary glitch at node Out as both inputs of clock sensitive C-element, i.e., output stage see that SET (see Fig. 7(b)).

IV. Performance Evaluation and Analysis

In this section, we present the performance analysis of four dynamic flip-flop designs: Unhardened TSPC FF [9] (Fig. 1(b)) RH TSPC-DICE FF [10] (Fig. 2), RH TSPC-Quatro FF [14] (Fig. 3) and RH DM-TSPC FF (Fig. 4). All designs are made using minimum width and length of the transistor in 28nm technology. Simulations were carried out at TT-Corner with clock frequency 1 GHz and operating voltage of 1.05V in Cadence Virtuoso. The performance evaluation is done on five parameters: design complexity which consist of the number of transistors and layout area, propagation delay (C-Q delay), average power, power-delay product, and SEU robustness. Table I clearly shows that our proposed design outperforms the existing radiation hardened TSPC FFs in performance and is truly a radiation hard FF as discussed below.

a) Design Complexity: DM-TSPC consists of 22 transistor which is same as TSPC-DICE but lesser than TSPC-Quatro which has 25 transistor count. But as we have more transistors stacked in DM-TSPC unlike TSPC-DICE, we can significantly save area in layouts due to shared diffusion (As shown in Figure 9, 10, and 11). Hence DM-TSPC will turn

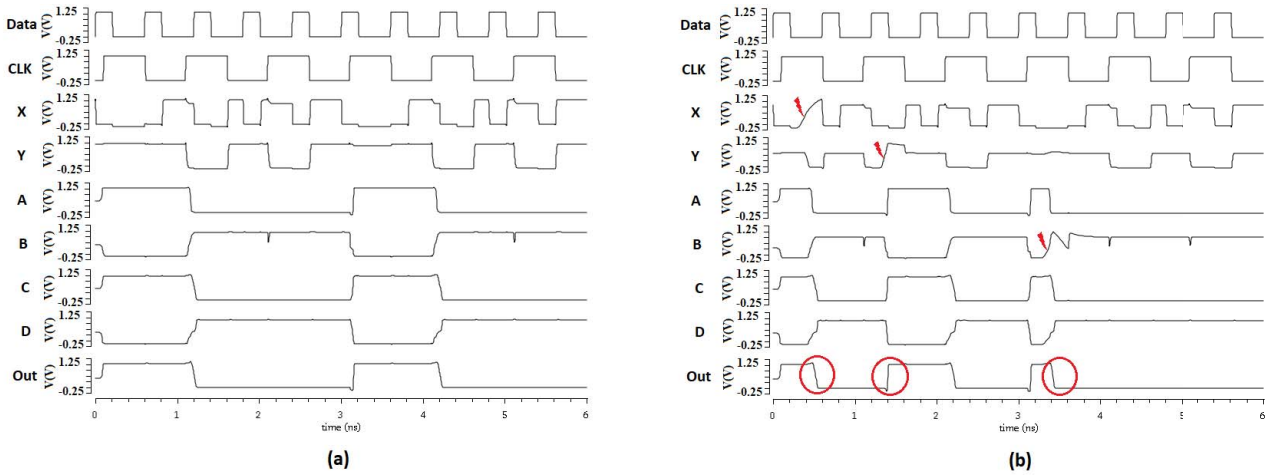

Fig. 5. Simulation waveform of the TSPC-DICE flip-flop [10] (a) Without SET (b) With SET

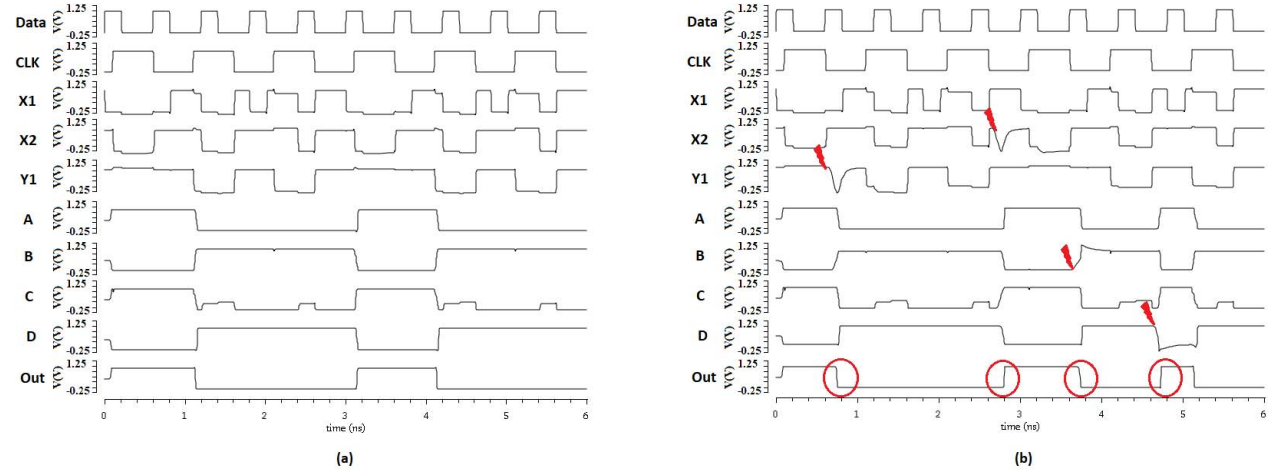

Fig. 6. Simulation waveform of the TSPC-Quatro flip-flop [14] (a) Without SET (b) With SET

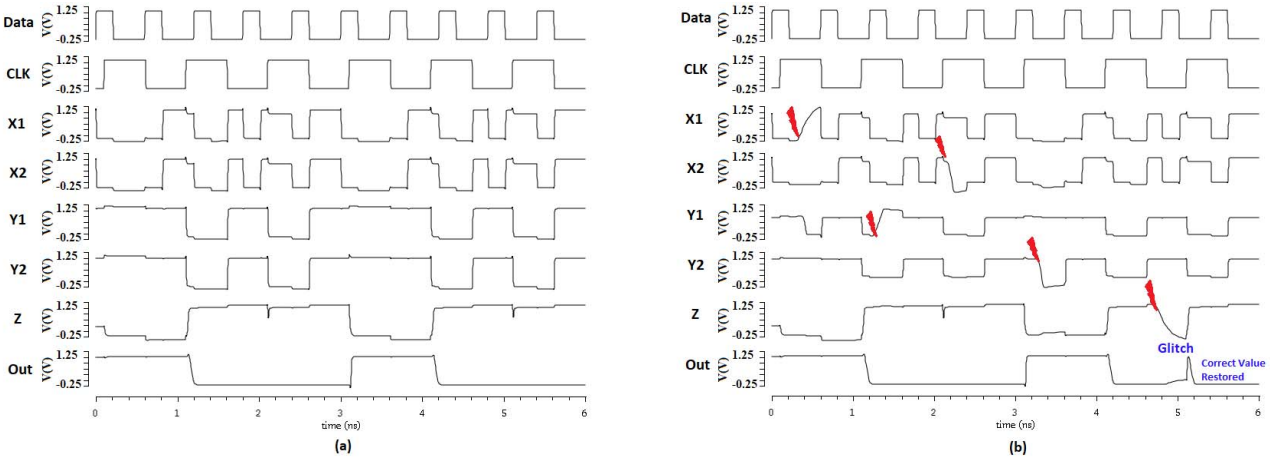

Fig. 7. Simulation waveform of the proposed DM-TSPC flip-flop (a) Without SET (b) With SET

out to be area efficient as compared to TSPC-DICE and TSPC-Quatro.

b) Delay: The propagation delay of the flip-flops (C-Q delay) is calculated by computing average of both transitions. As shown in Table I DM-TSPC outperforms TSPC-DICE by having 34.42% lower C-Q delay but shows degraded performance when compared with TSPC-Quatro by having 50.75% higher C-Q delay. In case of TSPC-DICE and TSPC-Quatro *Out* node is directly connected to first stage TSPC FF output, i.e., node B which sees gate capacitance (CG) of

TABLE I
PERFORMANCE COMPARISON

	Number of Transistors	Layout Area (μm^2)	C-Q Delay (ps)	Power (μW)	PDP (aJ)	Energy (fJ)
Unhardened TSPC FF	11	3.81	16.50	1.04	17.09	0.43
RH TSPC-DICE	22	7.34	77.00	5.05	389.16	6.62
RH TSPC-Quato	25	7.67	33.50	14.39	482.07	8.43
RH DM-TSPC	**22**	**5.71**	**50.50**	**1.84**	**92.77**	**0.71**

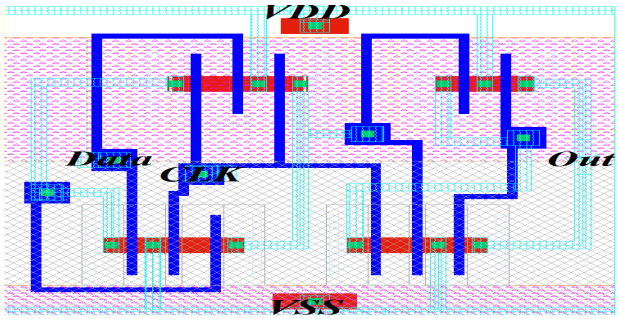

Fig. 8. Layout of Typical TSPC Flip-Flop

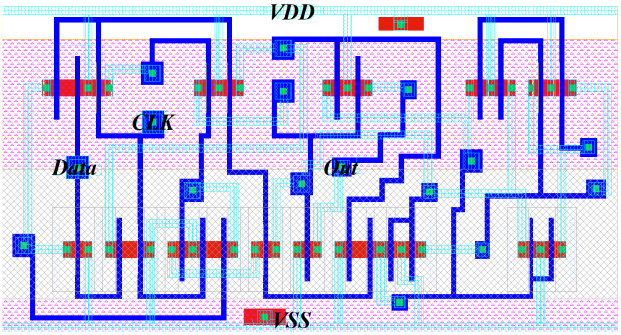

Fig. 10. Layout of Typical TSPC-Quatro Flip-Flop

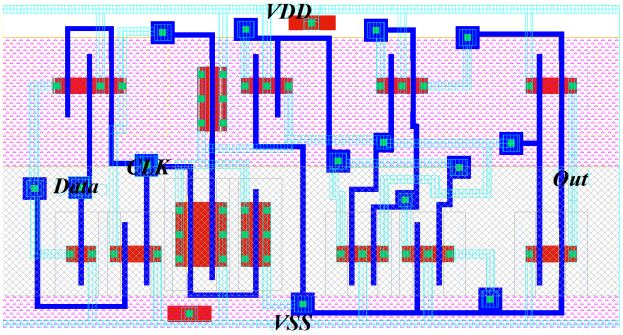

Fig. 9. Layout of Typical TSPC-DICE Flip-Flop

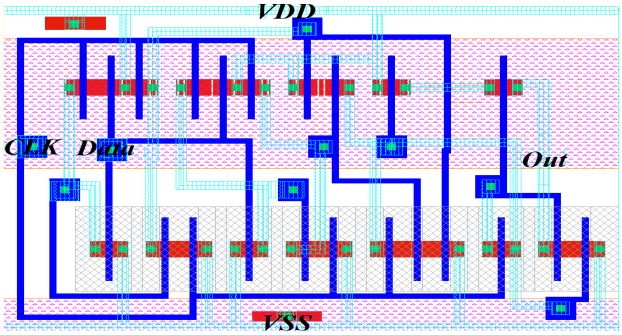

Fig. 11. Layout of Typical DM-TSPC Flip-Flop

4 transistors (see Fig. 2 and Fig. 3) but Out node of TSPC-DICE is driven by 2-level stacked transistor which is not in case of TSPC-Quatro. Therefore, delay of TSPC-DICE is more in comparison to TSPC-Quatro but in DM-TSPC Out node is driven by node Z which sees the only 2 CG, but it is driven by 3-level stacked transistor hence it shows the delay in between TSPC-DICE and TSPC-Quatro.

c) Power Consumption: We have reported average power of all four design (as shown in Table I). The power measurements were performed for simulation run time of 6 ns where clock period is 1 ns. DM-TSPC outperforms both reference designs by having power benefit of 63.56% from TSPC-DICE and 87.21% from TSPC-Quatro. As both TSPC-DICE and TSPC-Quatro consist of a static logic latch structure, i.e., DICE latch and Quatro latch hence writing data in these latched structure will consume more power because of contention current as compared to DM-TSPC which does not have these latch structure. Moreover, DM-TSPC has more stacked transistor as compared to reference designs due to which its leakage power is also less.

d) Power Delay Product (PDP): We have reported PDP as a figure of merit while comparing designs. DM-TSPC shows 76.16 % lower PDP when compared with TSPC-DICE and 80.76 % lower PDP when compared with TSPC-Quatro.

e) SEU Robustness: SEU robustness of designs is analyzed by simulating the impact of SET on the designs as shown in Figs 5(b), 6(b) and 7(b). As it is clear, TSPC-DICE and TSPC-Quatro are not completely radiation-hard solution whereas DM-TSPC is completely upset-hardened. While we might have glitches in the output node, there are no SEUs.

V. ISCAS'89 BENCHMARK RUNS

In this section, we discuss the system level impact of our proposed DM-TSPC flip-flop as compared to existing TSPC based flip-flop designs. We have taken 4 different benchmark designs from ISCAS'89 benchmark suite [15] and replaced all the flip-flops with the TSPC based designs. We have used (a) Normal TSPC design, (b) TSPC-DICE flip-flop, (c) TSPC-Quatro flip-flop, and (d) our proposed dual modular TSPC (DM-TSPC) flip-flop. The following

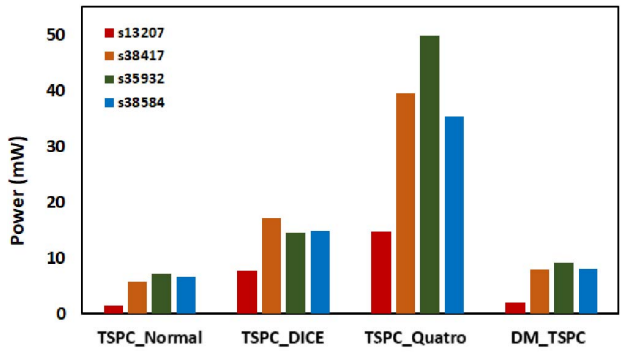

Fig. 12. Power comparison using different ISCAS'89 benchmark designs

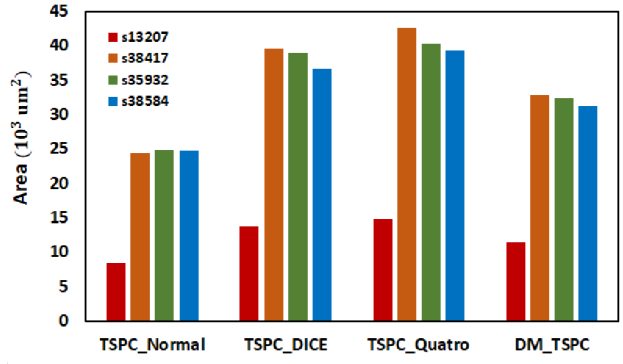

Fig. 13. Area comparison using different ISCAS'89 benchmark designs

benchmark designs have been considered here: (i) BM1: s13207 (with 638 DFF), (ii) BM2: s38584 (with 1426 DFF), (iii) BM3: s38417 (with 1636 DFF), (iv) BM4: s35932 (with 1728 DFF). We have deliberately selected sequential circuits benchmark designs with large number of D flip-flops, so as to ensure that the results are not tainted by the logic gates and the effect of flip-flops is captured correctly.

The following procedure is adopted for finding area and power. The Verilog code of each benchmark design is passed through the design compiler (DC) and synthesized using UMC 65nm. We have chosen UMC 65nm due to availability of standard cell library. We have added the library (.lib) views of normal TSPC flip-flop, TSPC-DICE flip-flop, TSPC-Quatro flip-flop, and the proposed dual modular TSPC (DM-TSPC) flip-flop to the standard cell library of UMC 65nm. We now replace all the flip-flops with each of the TSPC flip-flops and re-synthesize to obtain power and area. The design is constrained to operate at 1 GHz. We have used high speed here as TSPC designs are expected to be used in fast processors. The power and area results for all the benchmark designs are shown in Fig. 12 and Fig. 13. As is clearly visible from the graphs, the proposed DM-TSPC design has far low power with comparable area as compared to TSPC-DICE and TSPC-Quatro. Even for large sequential designs, we find that DM-TSPC based designs consume nearly 50% of the power with TSPC-DICE and nearly 20% power of TSPC-Quatro designs.

VI. CONCLUSIONS

Xontinuous scaling of technology node has reduced the reliability of dynamic flip-flop circuits due to reduced critical charge required to upset a circuit node. In this paper, we have presented novel radiation hardened dual-modular (DM) TSPC FF which has better SEU-tolerance compared to existing designs and has extremely low power-delay product (PDP). In fact, the proposed design has up to 76.16% and 80.76% lower PDP when compared with existing TSPC based RH design, i.e., TSPC-DICE and TSPC-Quatro. We have also demonstrated the benefits of DM-TSPC as compared to other TSPC based flip-flops on ISCAS'89 benchmark circuits. True single phase logic has found widespread use in digital design in recent times as it leads to power-efficient clock trees network as only single phase clock is needed and therefore no clock skew issues arise.

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