A Double Pumped Single-line-cache SRAM Architecture for Ultra-low Energy IoT and Machine Learning Applications

Arijit Banerjee and Benton H. Calhoun
Department of Electrical and Computer Engineering, University of Virginia, Charlottesville VA, USA
Email: {ab9ca, bcalhoun}@virginia.edu

***Abstract*— IoT and machine learning inference SoCs in harvested-energy applications issue repeated memory reads for extended periods. Due to limited energy-budget, these SoCs restrict the use of embedded memories to read-optimized ultra-low energy (ULE) SRAMs. This work proposes an SRAM embedded single-line-cache (SLC) architecture that reduces the read activity factor of near-threshold read-dominated SRAMs. Our scheme employs a double pumped single cycle write-back scheme to avoid the half-select issue in voltage scaled 8T SRAMs. This work shows that employing SLC for sequential reads achieves a worst-case read energy savings of 5.7X in SF_0.5V_27C and saves more than 80% in a column mux scenario for random sequential reads compared to the normal read operations for ULE IoT and machine learning applications.**

Keywords*— *IoT, machine learning, neural network, SRAM, near-threshold, ultra-low energy, SRAM architecture, single-line-cache, 8T SRAM.

I. Introduction

This work proposes a single-line embedded cache (SLC) in near-threshold SRAMs to reduce the read activity factor of the SRAM drastically in repeated spatial and temporal read requests within the same row address space. Energy harvested near-threshold IoT and machine learning applications have limited energy-budget due to the smaller form factor of the energy transducer [1] and lower efficiency of the energy-harvesting DC-DC converter [1]. These IoT SoCs (Figure 1) run programs most of the time by reading the instruction memory continuously for specific event detection, such as ECG-based biomedical applications [1][2][3], etc., and occasionally transmit the data to the receiving end. Moreover, in machine learning applications such as neural network (NN) acceleration [4], the compact NN model [5] has to be read and traversed throughout all the nodes for each inference executions. Evaluating an inference requires a repeated reading of the weights of each neuron before performing multiply-accumulate (MAC) operations and passing through the activation function. Due to heavy usage read-dominated embedded memories consuming up to 60% [3] of SoC power. Thus, these IoT applications require ultra-low energy near-threshold SRAMs. The conventional 6T bitcell suffers from robustness issues due to poor write-ability, readability, and read-stability in near-threshold supplies. Although the conventional 8T bitcell improve over the write and read metrics of 6T bitcell, it still suffers from a

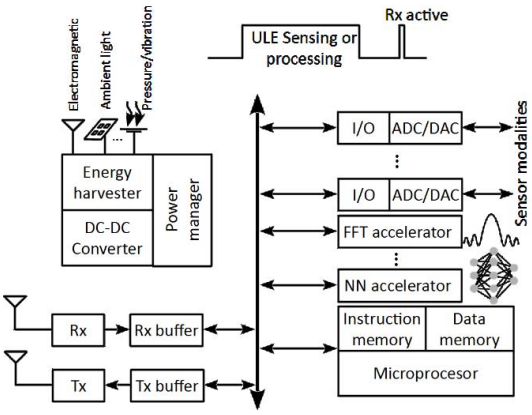

Figure 1: Energy-harvested IoT SoCs with an FFT, NN, etc. accelerators mostly process by reading programs, data, and NN weights from instruction or data memory and seldom transmit data to meet energy budget.

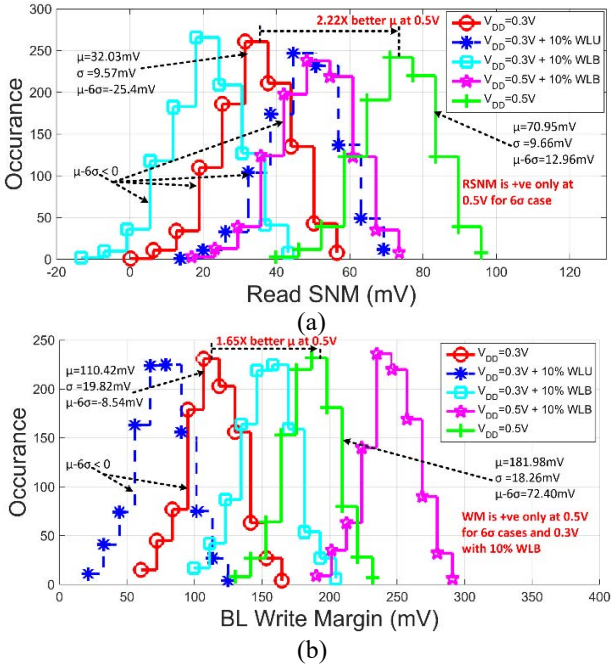

Figure 2: Projected degradation of (a) RSNM and (b) WM of 8T bitcells in scaled sub-threshold supplies.

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row half-select issue [6] in a bitline-interleaving scenario during a write, which uses a peripheral assist, such as boosted wordline. Figure 2 shows an 8T bitcell has 2.22X lower μ write margin (WM) and 1.65X lower μ read static noise margin (RSNM) operating at 0.3V compared to operating at 0.5V in a commercial 130nm technology. The figure also shows that improving write in bitline interleaving scenario using a 10% boosted wordline at 0.3V reduces the μ-6σ RSNM to negative, which indicates failure due to read-stability. Moreover, read peripheral assists, such as V_{DD} boosting for improving the read-stability in 8T sub-threshold bitcell may increase the overall energy of 8T SRAMs, due to a penalty in assist energy. Although alternative sub-threshold bitcells [7][11][12][13][14] claim to operate at lower V_{MIN} for minimizing energy consumption, they have a poor yield in sub-threshold supplies, and incur much higher area penalty and energy due to additional signal capacitances and increase in activity factor of multiple control signals. Moreover, a low-V_{MIN} SRAM does not necessarily yield lower energy consumption, as scaling V_{DD} below the minimum energy point (MEP) supply [6] may further increase the total energy per operation. Furthermore, the state-of-the-art SRAM energy reduction techniques, such as bitline amplitude limiting [8], segmented virtual grounding [9], etc. may not apply in the near or sub-threshold SRAMs, which usually use full swing read operations. In this work, we propose an SLC read (SLCR) architecture that reduces the activity factor for lowering the read energy of the sub-threshold SRAMs in read-dominated IoT applications. This work is based on conventional DRAM architecture using row-buffers for caching the content of a current open row for read energy and column access time improvement. We employ a write-back scheme [7][10] in the SLCR architecture, which allows avoiding the half-select problem at near-threshold supplies. The write-back scheme is usually a multi-cycle operation, which first reads all the words from the SRAM row, and partially modifies the data read using the word to be written, and then it writes back the updated words to the same row address. We use the write-back scheme to be implemented as a single cycle write-back (SCW) operation along with an intermediate latches acting as a single cache line, which supports the low energy SLCR operations. Thus, the SLCR architecture is promising for read energy reduction in read dominated near-threshold SRAMs. The rest of the paper organizes into five additional sections. Section II discusses the state-of-the-art alternative sub-threshold bitcells and their issues. Section III addresses the scope of improvements in the state-of-the-art IoT SRAMs. We present the SLCR architecture in section IV. Section V shows the results and comparison of the SLCR architecture with state-of-the-art and we conclude in section VI.

II. State-of-the-art Alternative Sub-threshold Bit-cells and their Issues

Alternative sub-threshold bitcells claim to have lower V_{MIN}; however, they may fail to operate with relatively larger SRAM capacity and higher yield constraints. State-of-the-art works such as Kulkarni et al. [11] show that the Schmidt-Trigger-based bitcell can operate at 160mV in the deep sub-threshold region. However, the Monte Carlo (MC) data in [11] suggests that the μ-3σ read static noise margin (RSNM) of the Schmidt-Trigger bitcell lies between 50mV to 0mV and the μ+3σ V_{MIN} of the bitcell lies between 350-400mV. Thus, across process variation using 400mV or below supply voltage, the 3σ worst-case V_{MIN} suggests memory failures with higher yield constraints. For another sub-threshold bitcell work [12], using L=120nm at V_{DD}=300mV, the μ-3σ write static noise margin (WSNM) becomes close to 100mV, and μ-3σ HSNM is 35mV, and using L=80nm the μ-3σ RSNM becomes negative; thus it is vulnerable at sub-threshold supplies. Similarly, the Reddy et al. work [13] documents the RSNM distributions of the proposed bitcell vs. the conventional 6T bitcell, where the plots indicate that at 400mV V_{DD} the worst-case μ-3σ RSNM is around 20mV. Thus, across process variation, there can be read failures occurring in Reddy's bitcell beyond 3σ yield. Therefore, we infer from the state-of-the-art bitcell works [11][12][13][14] that lowering the V_{DD} below 400mV may cause write and read failures in most of the published SRAM bitcells limited by their worst-case WSNM, RSNM, HSNM, and data retention V_{MIN}. Thus, V_{DD} scaling using alternative bitcells are limited by their functional operability for ultra-low energy IoT SRAMs, and architectural techniques may help to reduce energy consumption in this regard. The next section discusses the opportunities to improve IoT SRAM energy.

III. Opportunities for Improvement in ULE IoT SRAMs

Energy-harvested IoT SoCs usually uses ULE 8T sub-threshold SRAMs for instruction cache [18] memory, machine learning (ML) data cache memory, Tx and Rx buffers, etc. The functionality of the instruction or ML data cache memory is to store IoT microprocessor instructions or ML weights for the program execution. As the instruction/data memory remains active most of the time, the dynamic and leakage (equation (1), where, $E_{Tot_{op}}$ = total energy per operation; $E_{Dyn_{op}}$ = dynamic energy per operation; $E_{Lkg_{op}}$ = leakage energy per operation; α = activity factor; C= effective energy dissipation capacitance.) energy of the instruction SRAM may consume 60% [3] of the SoC power. Out of the 60% power,

$$E_{Tot_{op}} = E_{Dyn_{op}} + E_{Lkg_{op}} = \alpha * \frac{1}{2} C * V_{DD}^2 + V_{DD} * I_{Lkg_{op}} \quad (1)$$

about 64% [19] is reportedly consumed due to leakage, and the rest 36% is due to dynamic energy. Leakage reduction techniques, such as high-threshold voltage transistors in the SRAM core array, can reduce 50% [20] or more leakage current and hence reduce the leakage power. However, the dynamic energy of near-threshold SRAMs depends on the supply voltage, effective power dissipation capacitance, and the activity factor, which is challenging to reduce. Furthermore, voltage scaling in deep sub-threshold supplies is ineffective to get quadratic energy savings, as it requires SRAM to operate with heavy peripheral assist percentages, which increases the dynamic energy. Moreover, lowering sub-threshold supplies below the MEP [6] point using high percentages of peripheral assists, such as wordline boosting or negative bitline, can cause the row and column half-select issues, respectively. As assists can degrade the read-stability

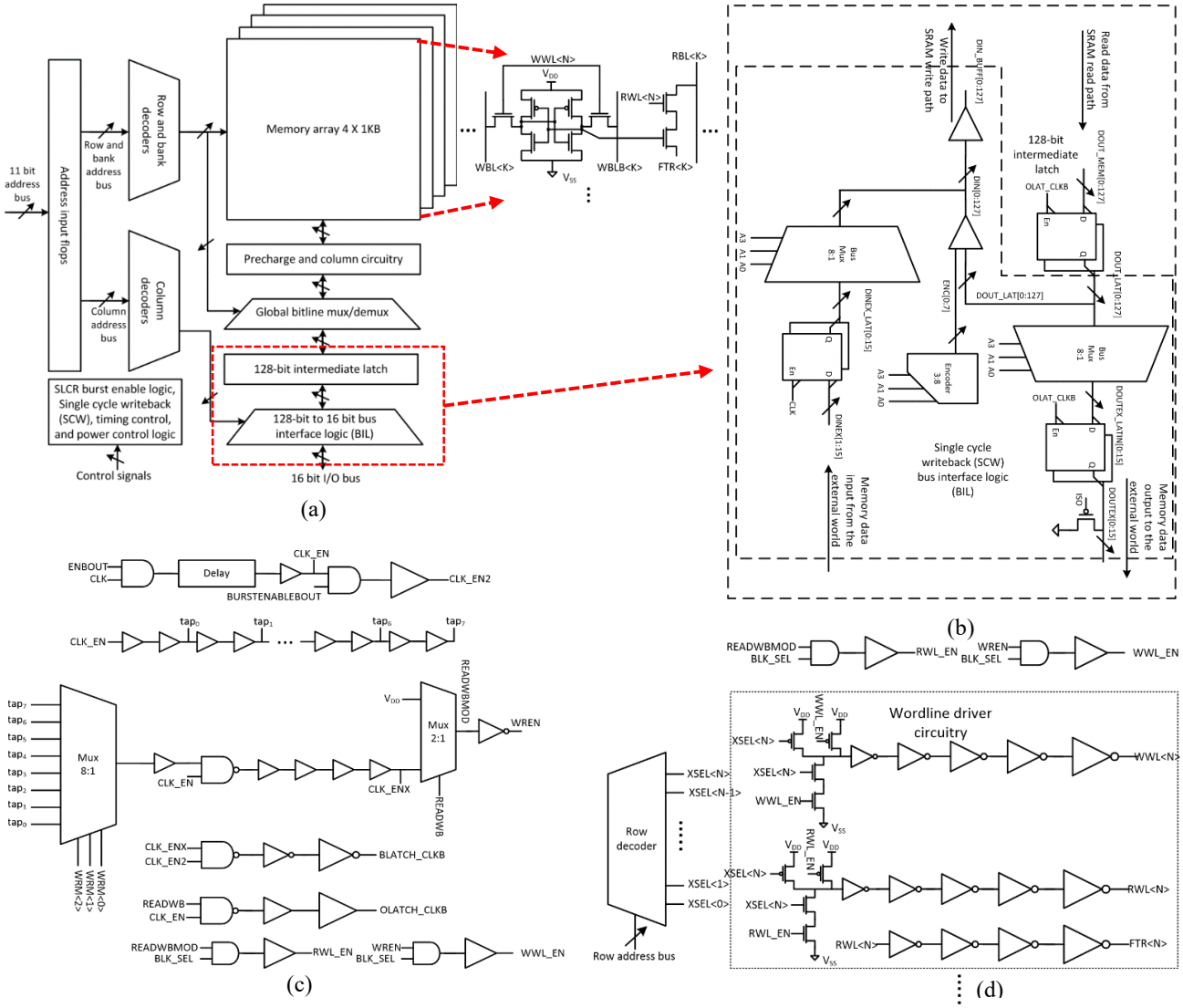

Figure 3: a) The single-line-cache for read (SLCR) architecture. b) The bus interface logic (BIL) and intermediate latch of the SLCR architecture. c) Internal clock generation circuitry for double pumping. d) Double pumped write and read wordline generation circuitry.

of the 8T SRAM, the activity factor (α) in equation (1) is the only promising design knob to control and reduce the overall energy consumption of the SRAMs after applying leakage reduction techniques. However, the read stability of the 8T bitcell has to be improved. As the typical read stability assist wordline under driver (WLU) degrades the writeability, the read-modify-write or write-back [7][9] scheme remains the only architectural technique suitable for near-threshold SRAM operation.

IV. IoT SRAM USING SLCR ARCHITECTURE

We implement an SRAM architecture that supports the single cycle write-back (SCW) scheme [7]. The SCW scheme leverages the separate read-path of 8T bitcell using the two transistor read buffer, which prevents read-stability issues. During the SCW operation, the SRAM first reads the corresponding word, and it stores the word in an intermediate latch buffer. Meanwhile, the data to be written bypass along with the other words stored in the intermediate latch to the write bitlines through a set of multiplexers, such that the order of the words stored in the memory row remains the same. Thus, the active write bitline columns write the new data, and the old data write back into the half-selected bitcells. This way the SCW scheme ensures that the data stored in the half-selected columns remain undisturbed. However, this scheme pays an additional timing penalty for the SCW operation and some hardware overhead.

To achieve the low activity 8T SRAM we update an existing 8T IoT SRAM using the single cycle SCW control logic, single-line-cache for read (SLCR) peripheral logic, 16-bit output flip-flop, 128 to 16-bit bus-interface-logic (BIL), and input flip-flops. Figure 3 (a) shows the architecture of the updated SRAM for our IoT SoC. The function of the 128-bit intermediate latch (Figure 3 (b)) in the SRAM is to latch all 8 words (16-bits

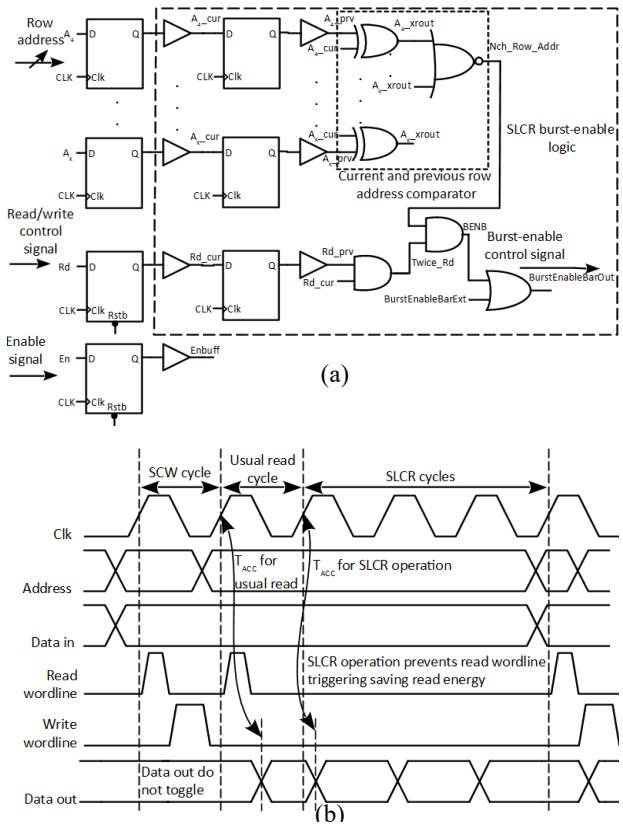

Figure 4: (a) Circuit diagram of the burst-enable logic in SLCR architecture. (b) Waveforms of the SCW and SLCR operations.

each) in a row (column mux factor = 8) in a normal read operation. If the user reads from the same row in two or more consecutive read operations, the SLCR logic disables the read wordline (RWL), and the SRAM reads from the intermediate latches instead. Thus, SLCR logic lowers the activity factor of the 8T SRAM. Figure 3 (b) portrays the BIL and the intermediate latches required for the SCW operation, which implements the write-back operation in the 8T SRAM. On the other hand, the burst-enable logic scans for any previous usual read operation in the same row address space and, if it follows by another read request, it issues the SLCR operation unless the row address has changed. We show the SLCR burst-enable-logic in Figure 4 (a) and the corresponding waveform in Figure 4 (b). With this scheme (CM=8), for each normal read operation in SRAM, a user can have seven (CM-1) distinct SLCR operations without repetitive reads in the same row address that reduces the 8T SRAM activity factor in equation (1) and lowers the overall read energy per operation. Note that an external register as a local buffer, as a cache line, of the same width of the intermediate latch to store all the words in the single row of the sub-threshold SRAM in a usual column mux (CM) 8 scenario would not incur the same benefits of SLCR architecture. It would require 8 usual reads first to populate the external 128-bit register to act as a local buffer and additional address comparator for previous and current row addresses to detect read requests in the same row address space,

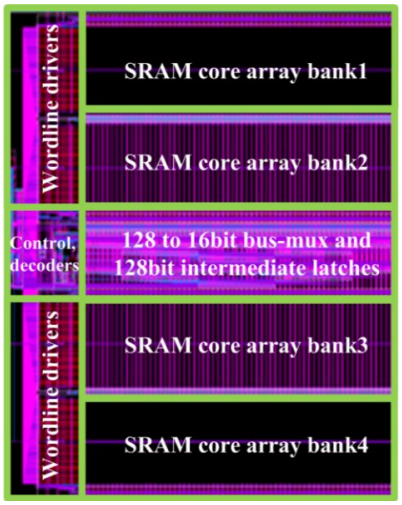

Figure 5: Layout of 4KB near-threshold SRAM (0.584 mm^2).

which would consume much higher effective read energy. Thus, for read energy saving it requires an internal latch that captures the read data in a single usual read operation and using the SLCR burst enable logic it prevents the unnecessary switching of RWL, row and bank decoders in the SLCR operations. The internal circuits for the clocks and double pumped read and write wordline generation are shown in Figure 3 c) and Figure 3 d). Here the CLK_EN signal is passed through a low power buffer chain with eight different tap points. An 8:1 mux selects one of the tap delays using write-after-read margin controls to further mix with the CLK_EN signal using a NAND gate, which is controlled by the READWB signal using a multiplexer control to get the READWBMOD signal. The READWBMOD toggles to high and low in a write-after-read SCW cycle to mix with read and write enable signals (Figure 3 (d)) to generate the write and read double pumped wordlines in the same SCW cycle. On the other hand, NAND operation of CLK_ENX and CLK_EN2 signals generate the intermediate latch clock BLATCH_CLKB. Similarly, the NAND operation of READWB and CLK_EN generates the output latch clock OLATCH_CLKB. Note that the Dout is controlled by the OLATCH_CLKB and in an SCW operation it does not toggle as shown in Figure 4 (b).

We implement the single cycle SCW operation by pulsing the RWL and write wordline (WWL) in the same cycle (Figure 4 (b)) that uses pulse generator circuits. We also incorporated three-bit SCW margin control pins for sub-threshold margin variations to control RWL and WWL pulse widths, externally. The SLCR architecture also employs state of the art memory features, such as clock gating, different power modes using power gating, banking, global and local bitlines, and write and read margining controls. Furthermore, with this scheme, we investigate the energy savings or penalty of implementing single cycle SCW operations. We report the worst-case simulated maximum operating frequency of this work at the SS_0.5V_27C corner is 1.03MHz. As most of the harvested energy sub-threshold IoT SRAM specification requires the SRAM to work in kilohertz frequencies, such as 200 kHz [1][3] at 0.5V with 27C, we had more than sufficient margin to play with timing. We implement the SRAM macro in a commercial 130nm

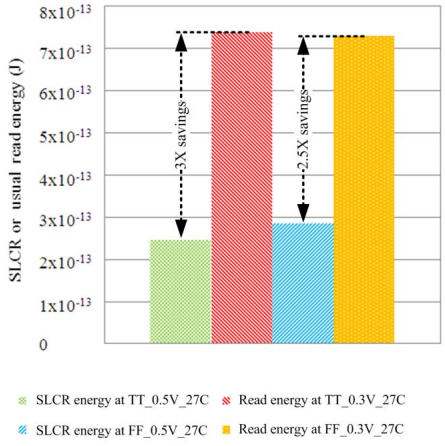

Figure 6: Comparison of active read energy at 0.3V 27C with SLCR energy at 0. 5V 27C in 4KB subthreshold memory.

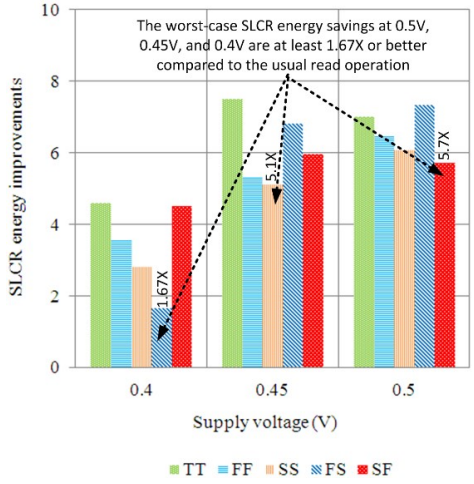

Figure 7: Active energy improvement ratio using SLCR scheme vs. supply voltage bar plot at 27C in 4KB subthreshold SRAM.

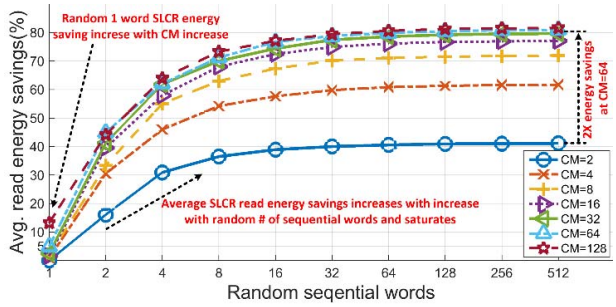

Figure 8: Energy savings using SLCR mode across various random sequential words and column mux factor.

technology and simulate the modeled pre-layout netlist with HSIM using 100% SPICE accuracy. The block diagram of the 4KB sub-threshold SRAM is shown in Figure 3 (a). Figure 5 portrays the annotated layout of the 4KB sub-threshold SRAM macro. The performance of this architecture is limited by the

TABLE 1: COMPARISON OF ENERGY/POWER SAVINGS SCHEMES

	This work	IJEC'16 [21]	ICICDT'12 [16]	ISLPED'06 [9]	ASSCC'11 [8]	VLSI'11 [15]	ISOCC'11 [14]
Technology	130nm	65nm	28nm	130nm	40nm	40nm	65nm
VDD	0.5V	1.2V	0.85V	1.2V	0.5V	0.5V	1V
Capacity	32kb	64kb	4Mb	44kb	256kb	512kb	-
Speed	1.03MHz at SS_27C	900MHz	100MHz	-	-	~6.25MHz	500MHz
Area (sq. mm)	0.584	0.16	0.784	~0.329	-	0.73	-
Energy/ Power savings	Rd 82.5% at 0.5V_SF, 80.39% at 0.45_SS, 40.11% at 0.4_FS for 27C	Wr 64.2%	60%	Rd 44% Wr 84%	26%	32%	21.30%
Area overhead	7%	-	7%	8%	2%	-	-

double pumped SCW operation that generates both the read and write wordline in the same cycle. However, in scaled high-speed FinFET or FDSOI technology (20nm, 16nm, 14nm, 7nm, etc.) this architecture would hardly limit the overall performance compared to the benefits it provides for read energy minimization.

V. RESULTS

Figure 6 depicts the data of active normal read energy and SLCR energy in two different supply voltages, which shows that at the TT_0.5V_27C corner, the SLCR active energy is 3X lower compared to the usual read energy at the TT_0.3V_27C corner. Furthermore, at the FF_0.5V_27C corner, the SLCR energy is 2.5X lower than the normal read energy at FF_0.3V_27C corner. Thus, using SLCR scheme operating sub-threshold SRAMs in near sub-threshold V_{DD}s such as 0.5V is profitable from the standpoint of active energy savings. Moreover, the SLCR scheme avoids V_{DD} scaling, which may cause write and read issues in sub-threshold SRAMs. Figure 7 portrays the bar plot of the ratio of the active usual read energy to the SLCR energy. The figure shows that the SLCR energy is 5.7X lower in the slow NMOS fast PMOS (SF) 0.5V_27C corner, 5.1X lower in the SS_0.45V_27C corner, and 1.67X lower in the fast NMOS slow PMOS (FS) 0.4V_27C corner, compared to the energy in a usual read operation. We further observe that the SRAM's worst-case SLCR energy improvement, compared to usual read energy, is 6X at the SS_0.5V_27C corner, and the best improvement is 7.4X at the FS_0.5V_27C corner. On the other hand, the SLCR energy savings in our work compared to the usual 8T SRAM design's read energy are 7.03X, 4.03X, 3.39X, 7.79X, and 3.2X at the typical NMOS typical PMOS (TT), FF, SS, FS, and SF processes respectively at 0.5V_27C. Note that the SLCR active energy improvements vary with process variation due to variation in sub-threshold leakage and dynamic energy components across processes for a fixed temperature. Nevertheless, the SCW energy improvements in this work compared to the cumulative write and read energy in the usual 8T SRAM design at 0.5V_27C are 2.48X, 2.08X, and 1.59X at FS, FF, and TT processes respectively. However, at the SS and SF processes using the same V_{DD} and temperature, the updated SRAM's SCW energy increases by 23% and 32% compared to the cumulative write and read energy of the usual 8T design. The

increase in SCW energy might be due to longer read and write times in slow NMOS processes, which cause more leakage energy dissipation in the total active energy during the SCW operation. Using a lower leakage device in the 8T bitcell could minimize this issue. The layout area overhead of our work is 7% using the SLCR architecture in this work compared to usual 8T SRAM layout, which can be minimized by optimizing the floorplan and sub-component layouts. For our scheme, the worst-case standby leakage current penalty is 2.35% at the FF_0.5V_27C PVT, and the standby leakage current becomes 15% less compared to the normal 8T design for the best case scenario. Figure 8 shows the energy savings using SLCR mode across various random sequential words and column mux factors among 1K words. With the increase in the number of random sequential reads and column mux factors the energy savings increase and then saturate at a maximum level, which corresponds to more than 80% read energy savings. Noticeably, with increased sequential accesses the SLCR savings would increase within the same row address space. Thus, employing compiler techniques the IoT instructions and trained NN weights can be compiled and kept in a sequential manner in the 8T SRAM exploiting the energy benefits of the SLCR architecture. We compare the SLCR scheme with state-of-the-art energy or power reduction methods in Table 1.

VI. Conclusions

The single-line-cache for read (SLCR) architecture using a single cycle write-back (SCW) scheme allows near-threshold 8T SRAM operations. Our scheme avoids read-stability issues due to voltage scaling, a half-select problem in the bitline-interleaving scenario, and additional area increase with alternative bitcells. The SLCR requires minimal changes in the existing periphery and I/Os and is independent of the choice of SRAM bitcell used, which lowers the SRAM read energy for spatiotemporally accessed addresses in the locality of the same SRAM row address space. This work has a 7.03X energy improvement at 0.5V supply for the single cycle write-back (SCW) operation compared to the cumulative read and write operation in an existing design of a normal 8T SRAM. We achieve a maximum of 7.4X energy improvements for the worst-case in MHz frequencies at 0.5V supply voltage for our 4KB near-threshold SRAM. Finally, we conclude that the SLCR energy savings across various random sequential words and column mux scenarios show promising results for read dominated IoT and inference type machine learning applications.

Acknowledgment

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