2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID)

Design of a Charge Sensitive Amplifier for Silicon Particle Detector in BCD 180 nm Process

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***Abstract*—This paper presents the design of a charge sensitive amplifier (CSA) for an analog processing circuit of 47×6 silicon pixel detector array. The design has been implemented in BCD 180 nm technology. A diode with an area of 250 × 50 μm^2 is used to realize a unit sensor pixel. A 100 $\%$ fill factor is achieved by confining the analog circuit in the diode. Low power and area efficient single ended folded cascode amplifier is employed as a basic building block of the CSA. Further, an on-chip corner control circuit is proposed to make the design insensitive to process variations and to reduce power dissipation in the CSA.**

***Index Terms*—Active pixel sensors, image sensors, low-frequency noise, low-noise amplifiers, radiation hardening.**

I. Introduction

The high voltage and high resistivity CMOS capacitively coupled pixel detectors are gaining popularity for the large area pixel trackers of the large hadron collider (LHC) [1–5]. In these detectors, achieving 100 $\%$ fill factor while maintaining signal integrity is a challenging task. A triple well process can be used for this purpose. Here, deep n-well acts as a collecting electrode, a shallow n-well contains the pMOS transistors of the pixel electronics and the nMOS transistors are hosted in the deep p-well [6]. STMicroelectronics' BCD8 technology is a triple well process. A parasitic diode between the p-substrate and the deep n-well realizes the pixel sensor. An excursion of particle from the substrate will generate a negative voltage spike at the cathode of the pixel. This spike signal is AC coupled with the charge sensitive amplifier (CSA). Design of the CSA is critical because single ended architecture itself is prone to process variations and signal degradation. This paper presents the design of CSA for a silicon detector to achieve 100 $\%$ fill factor and to increase the size of the charge collecting electrode. This work focusses to achieve noise performance and process reliability in a detector. The design is targeted to be compatible for hybridization with front end I4 (FE-I4) chip of ATLAS experiment. A current injection circuit is designed to simulate the operation of sensor. An on-chip corner control circuit is also included in the pixel array separately to obtain the process independent functionality.

II. Analog signal processing circuits

1) Simulation environment for the particle detector: The sensor diode is connected in reverse bias by connecting the p-substrate to a large negative potential, –50 V (refer Fig. 1(a)). The deep n-well is biased using a high resistance (ON resistance of transistor M_B). The resistance is connected to a positive supply (V_{DD}) of 1.8 V. It is a fact that when a charged particle crosses a 10 μm thick depletion region, it generates about 780 e^- [6]. The current injection circuit presented in Fig. 1(a) emulates the behaviour of sensor and injects an equivalent current at the cathode of the diode [3].

2) The charge sensitive amplifier (CSA): The role of the CSA is to amplify the detected transient signal from the sensor. A single stage amplifier with negative capacitive feedback is designed to function as CSA. The CSA consists of a gain stage, a DC blocking capacitor (C_C) and a DC biasing circuit as depicted in Fig. 1(a). The complete schematic of folded cascode amplifier used in the CSA is shown in Fig. 1(b). The pMOS transistors are placed in shallow n-well and therefore, they help to reduce crosstalk. Moreover, the pMOS devices exhibit better noise performance because of their relatively slow mobility while comparing with the nMOS transistors. Hence, the CSA is designed with a pMOS input stage. A resistive feedback and continuous reset formed by the transistor M_F (in Fig 1(a)) provide the DC bias to the input transistor [7]. Further, a buffer shaper circuit consisting of a common-drain amplifier (not shown here for simplicity) is connected at the output of CSA to drive the capacitive load of 1 pF.

Noise is a trade-off between gain, area and power consumption of the CSA. It is worth analyzing the noise of CSA because single ended architecture tends to contribute noise if not designed carefully. In addition to the noise contribution by transistors M_0, M_1 and M_3, common-mode noise arises from the current mirrors used to generate the bias current of CSA. Analysis reveals that the presence of finite resistance at node A of Fig. 1(b) introduces noise, coming from the current mirror formed of M_0 and M_4. This noise can be reduced by connecting a large capacitor between the gate of the transistor M_0 and the reference node [8]. Fig. 1(c) shows the input referred noise of the amplifier, plotted for different values of capacitance at the gate of M_0. It is possible to achieve around 25 $\mu\mathrm{V_{rms}}$ reduction in the noise with a 3 pF of capacitor. However, area overhead introduced by this capacitor makes this technique impractical in this scenario. Therefore, we resort to increase the gate capacitance by increasing the width of tail current M_0 and generating bias voltage for the succeeding circuit from the current mirror M_4. This increases the gate-source capacitance (C_{GS}) to reduce noise by decoupling it to a ground potential. Additionally, noise reduction is achieved by increasing the lengths of M_0, M_3, M_4 and M_5, in order to reduce the channel

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00126

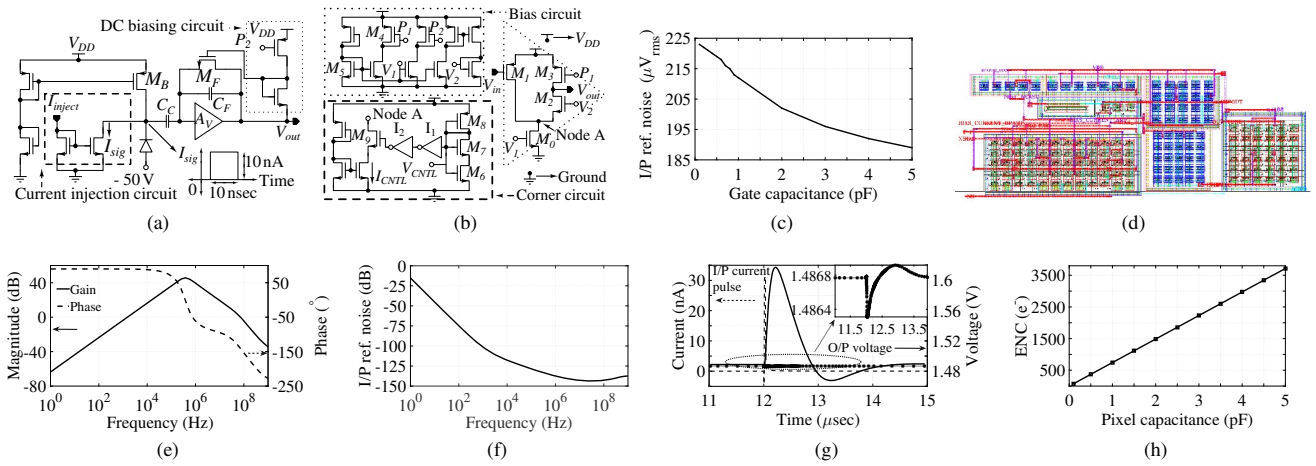

Fig. 1. (a) Analog signal processing circuitry, (b) the schematic of folded cascode amplifier used in the CSA with corner tuning circuit, (c) input (I/P) referred noise of the CSA for different values of the gate capacitance of M_0, (d) layout of the CSA, (e) magnitude and phase response of the CSA, (f) input referred noise of the CSA, (g) transient response of the CSA, where inset shows the voltage spike at the input of CSA, (h) ENC with respect to pixel capacitance.

length modulation and the transconductance.

3) Corner control circuit: The single ended folded cascode amplifier in the CSA has a technological and architectural drawback when subjected to power and area constraints. It is difficult to achieve cross-corner functionality without compromising on power budget. The simulations at low gain corner reveal that the current flowing through the transistor M_0 drops severely and M_0 enters into the linear region. A separate corner control circuit is designed to obtain high gain of the amplifier at process corners (dashed block in Fig. 1(b)). The circuit is active only for a given corner and is idle otherwise. The working of this circuit relies on tuning of the switching threshold of back-to-back inverters I_1 and I_2, at different corners. This controls an additional current source connected in parallel with the tail current of the CSA. The controlling branch (formed by M_6, M_7 and M_8) generates a DC voltage (V_{CNTL}) greater than the switching threshold of an inverter I_1 at low gain corner. This action turns on M_9 to connect the current source (I_{CNTL}) at node A of CSA. V_{CNTL} is less than the switching threshold of the inverter in other corners and hence no current flows through M_9. The corner control circuit consumes 4.6 μA when idle and 23.8 μA when active. Note that, without this circuit, 20 μA current source would have been required to achieve the cross-corner functionality.

III. Layout and Simulation Results

The CSA occupies 65 $\times$ 25 μm^2 of the diode area. The layout of CSA is shown in Fig 1(d). Fig. 1(e) shows the AC response of the CSA. The effect of zero frequency (because of AC coupling) in the circuit is visible from Fig. 1(e). Fig. 1(f) shows noise performance of the amplifier. The CSA has thermal noise of 201 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and the input referred noise of 168 $\mu\mathrm{V_{rms}}$ in the signal band of 225 kHz to 1.225 MHz. The transient response of the CSA is as shown in Fig. 1(g). A current pulse with an amplitude of 30 nA and width of 30 ns (5617 e^-) is injected at the cathode of the sensor diode. The inset shows the negative voltage spike generated at the deep n-well of the sensor. The output (O/P) of CSA achieves peak amplitude of 1.62 V and decreases thereafter because of the feedback action. Fig. 1(h) shows the equivalent noise charge (ENC) with respect to pixel capacitance. The integrated noise at the output of the buffer shaper circuit is simulated in the frequency band of 1 kHz–100 MHz to calculate the ENC.

IV. Conclusion

A low noise and area efficient CSA is designed in BCD 180 nm technology. The CSA with an on-chip corner control circuit shows robust performance against process variations. The designed corner control circuit occupies only 38 $\times$ 21 μm^2 area and reduces current consumption in the CSA from 30 μA to 15.6 μA per pixel. The CSA can be used in low noise applications such as particle detection, biomedical and imaging.

Acknowledgment

This work is partly funded by AIDA-2020 Project EU-INFRA Proposal no. 654168.

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