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On-chip MISR compaction technique to reduce diagnostic effort and test time

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***Abstract*—MISR compaction technique has multiple advantages like single cycle signature comparison, effective use of scan I/Os compared to XOR-based compaction. Main disadvantages with this technique are poor diagnostic capabilities due to loss of data correlation during compaction and complete signature corruption due to X-sources. In this paper, we present a new MISR architecture and methodology to improve the diagnostic resolution of MISR signatures by comparing the intermediate MISR signatures after regular intervals of time. We also propose an enhancement to this architecture with reset logic to improve the diagnosis further, improve the immunity against X-sources and also detect the faults early, thus reducing the tester time and test cost. These logic changes were implemented on ISCAS benchmarking designs and results have been tabulated.**

I. Introduction

In the current day multi-million flop designs with high logic content, manufactured at lower technology nodes with complex techniques like double patterning, the manufacturing defects are also becoming prominent. This has led to increase in test requirements in terms of types of tests, number of test patterns etc to achieve very low Defective Parts Per Million (DPPM) and it becomes more challenging with the test time, test cost and test volume restrictions. Due to the large number of tests being performed, the amount of time spent on the tester is increasing and this is resulting in increase in test cost. It is being predicted that the cost of an Integrated Circuit(IC) is being dominated by the cost required to test the IC rather than its manufacturing cost. Along with testing, the diagnosis of the faults is also important in order to identify and correct any issues early in the process to prevent fallouts and improve the yield during the volume production.

These high quality test requirements are also resulting in increase in test volume due to more number of test patterns. In order to restrict its impact on the test time and test volume, decompression and compaction structures have become inevitable in the present day ICs[1]. The large scan chains are now broken into shorter scan chains because shorter the chains, lesser the scan cycles to load/unload the flops, reducing the test time. Decompressor techniques like Illinois scan[2] or Linear Feedback Shift Registers (LFSRs)[3] expand the initial stimulus driven by scan input ports from the tester and apply them to the short chains. After scanning in the stimulus, the response of the circuit is captured into the scan flops after single or multiple capture cycles. This is followed by scan out cycles to serially shift out the captured response data present in the short scan chains into a compactor (the next stimulus is scanned into the scan flops at the same time to save test time). The compaction techniques like XOR-tree compaction[4][5][6][7], Multiple Input Signature Register (MISR)[8][9] etc generate a signature which is brought out via the scan output ports into the tester. The obtained signature is then compared with the expected value stored in the patterns on the tester and a mismatch indicates the presence of a single or multiple faults in the IC. The failing chips are sorted and using their test data dump, a complete diagnostic is carried out in order to locate and determine the exact cause of failure. The process of diagnostics to be followed and the effort is dependent on the compaction method used.

The regularly used XOR-tree and MISR compaction techniques have their own advantages and disadvantages. Table I shows the comparison between the 2 techniques. As the name suggests, the XOR-tree compaction contains multiple levels of XOR gates. The compacted signature comparison happens every cycle and the location of the fault capturing flop can be easily identified by tracing back from the mismatching bits of the signature through the XOR tree. The MISR technique contains XOR gates and shift registers with configurable feedback paths. The response data gets compacted both in space and time domain and hence, the signature comparison happens only once per pattern after all the captured data is scanned out. Since the scan outputs are not required to dump out the signatures every cycle, they can be configured as scan inputs to increase the stimulus throughput and similarly, when the signature is ready to be compared, all the scan I/Os can be configured as scan outputs to observe the final signature in one cycle (OPMISR+)[10]. But from the diagnostics perspective, it is very difficult to find the cycle with the wrong data.

The other important aspect is the effect of X-sources on the compacted signatures. These X-sources are unknown values originating from analog logic, unconstrained asynchronous set/reset circuits, memories etc and getting captured on the scan flops. Since the data is unknown, the compacted signature cannot be determined correctly, leading to ineffective patterns. Currently, the problem of X-sources has been addressed to a large extent using channel masking techniques[11] wherein the

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ATPG tool recognizes the potential X-sources, their positions in the scan chains and gates these chains during their scan out cycles using special channel masking registers and enable pins. On the down side, it may lead to masking of output care bits which again degrades the efficiency of the patterns. In case of MISR compaction, the masking technique has to be more aggressive compared to XOR-tree compaction since even a single X can corrupt the whole signature.

Hence, even though the MISR compaction achieves better compaction ratio and better utilization of scan I/Os, the XOR-tree compaction is the more popular and more widely used technique during manufacturing test mainly because of its ease in diagnostics and tolerance towards X-sources. MISRs are extensively used for Built In Self Test (BIST) circuits where the signature is generated and compared after running many patterns. In this paper, we focus on improving the MISR compaction technique so that it becomes suitable for manufacturing test as well.

TABLE I
XOR-TREE VS MISR COMPACTION

	XOR-tree	MISR
Circuit type	Purely Combinational	Combinational + Sequential
Compaction type	Space	Space + Time
Signature Comparison	Every cycle	Only once after all scan out cycles
Diagnosibility	High	Low
Immunity from X-sources	High	Low
Utilisation of Scan I/Os	Scan Ins and Scan outs active every cycle	Scan outs idle during scan cycle. Can configured as scan ins to increase throughput

A. Signature comparison

The present day manufacturing test process involves generation of a compacted signature inside the chip, unloading the signature into the tester through the scan out pins and finally comparing the obtained signature with its expected value on the tester. This process requires scan out pins which are an overhead and the signature transfer is slow since the data transfer is between 2 different interfaces (chip to the tester). A better approach has been proposed in [12] to load the expected signature into the chip through new test pins, compare the signatures on-chip to determine pass/fail and send the information to the tester. The advantages of this approach is reduced test overhead due to non-requirement of scan out pins but on the other hand, there is only a pass/fail information and diagnostics using signatures cannot be performed due to the absence of obtained signatures.

B. Diagnostics from compacted signature

The initial step in the failure analysis is to identify the location of the flop/s capturing the fault. After identifying the locations, the fanin cones of the data input of the fault capturing flops are analyzed and the possible locations, type of faults are determined. But the identification of the location of the fault capturing flop/s becomes challenging when the response data is compacted, especially for MISR techniques since the amount of data compaction is high leading to more data loss. We can find quite a few research publications and literature on MISR based diagnostics, mainly for designs with BIST. Some of the techniques involve offline diagnosis using the signature based on certain algorithms[13][14][9][15] and few others discuss about hardware enhancements to shape the signatures to provide better aid to diagnostics[16][17][18]. But offline diagnostics is slower and in hardware approach, more circuitry is required to achieve better diagnostics. Hence, the usual approach for MISR diagnostics that is followed across the industry is :

1) Identify and note the pattern having the MISR signature mismatch (failing pattern) from the tester data dump
2) Reapply the failing pattern and scan out the uncompacted data through the scan outs (bypassing the MISR logic)

With this approach, the exact location of the failing flop can be identified but it consumes tester time. The impact is more if different ICs fail with different patterns since each one of them have to be diagnosed with the same method, leading to more time on the tester. However, the currently available commercial ATPG tools claim good diagnostics directly from the MISR compacted signatures but they are compute intensive and their fault location accuracy is inconsistent, especially when the number of fault locations increase.

In this paper, we propose an architecture enhancement to the MISR technique which not only improves its diagnostic capabilities by aiding the diagnostics to find the fault locations directly from the signature, but also improves X-source tolerance in addition to the existing masking techniques and achieves early fault detection which saves tester time and test cost. The architecture and methodology is discussed in Section II, the experimental results in Section III, the advantages are listed in Section IV and finally, the details are summarized along with few points on future work.

II. ARCHITECTURE AND METHODOLOGY

The on-chip signature comparison techniques are gaining prominence The proposed architecture and methodology involves the techniques listed below and these are performed on-chip.

1) Comparing the MISR signatures after fixed intervals of time
2) Resetting all the MISR registers to 0s after the same intervals

In order to explain the methodology better, we consider a regular test architecture with a decompressor at the scan inputs and MISR type of test data compaction on the output side, shown in Fig 1, with the following parameters:

- S = Number of compressor scan chains
- L = Length of the longest compressor scan chain (= Number of scan cycles to scan in the stimulus into the flops and scan out the responses into the MISR)
- M = Length of the MISR signature (= Number of scan ins and scan outs)

- T = Number of cycles after which the MISR signature comparison and MISR register reset is to be performed

We define the diagnostic resolution of MISR compaction as the number of scan out cycles after which the compacted response(signature) is compared and available for diagnostics in case of a fail. Higher the number of cycles, more data compaction which leads to lower diagnostic resolution. For a regular MISR, we obtain the signature for diagnostics only after all the response data is compacted. Hence, the diagnostic resolution is fixed to the number of scan cycles.

$$D = L \tag{1}$$

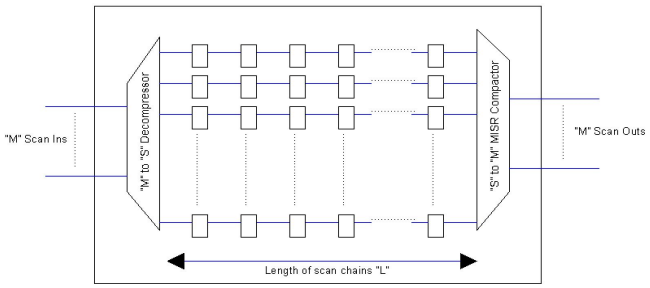

Fig. 1. Typical Test architecture with compression

A. Determining the value of T

The parameters S, L and M are the usual design parameters and the value of T is governed by:

$$1 \leq T \leq L \tag{2}$$

In order to determine the optimal value of T , we need to factor in certain constraints like minimum area overhead (both in terms of logic and number of additional test pins required) and maximum diagnostic resolution. We sampled the values of T and analysed the effect on area overhead and diagnostic resolution.

- When $1 < T < M$, the diagnostic resolution improves since lesser cycles of response data are compacted between each comparison. But in order to perform the comparison, the M-bit expected signature needs to be scanned into the chip before T cycles which translates to increase in number of test pins. For example, if $T = M/2$, then we would require 2 additional test input pins to scan in the M-bit expected signature (one to scan in the MSB $M/2$ bits and the other to scan in the LSB $M/2$ bits).
- When $T > M$, the diagnostic resolution will decrease since more number of scan out cycles are compacted
- When $T = M$, we observe that the area overhead is lesser since we can scan in the expected signature using only a single additional test pin and the diagnostic resolution is also better than the previous case

Hence, we fixed the value of $T = M$ so that after every M scan out cycles, the MISR value is compared with the expected value and the MISR registers are reset to 0s, in addition to the complete MISR reset which happens after L cycles in a regular MISR. The number of such intervals per pattern, N, can be obtained by,

$$N = floor(L / T) \tag{3}$$

The floor() function gives the greatest integer less than or equal to a given real number. It is used to cover even the cases where L is not completely divisible by T. In such scenarios, we perform the regular MISR signature observe after L cycles, so that the data captured in the final Y cycles are not lost.

$$Y = L - (N * T) \tag{4}$$

B. MISR signature comparison

In this approach, we perform on-chip comparison of the obtained MISR signature with its expected value after every M cycles to improve the diagnostic resolution. The architecture details are shown in Fig 2. The ATPG tool generates the required stimulus, determines the expected signature after every M cycles and encodes it in the pattern, so that the expected value is serially shifted into a M-bit shift register inside the IC through a new test input port named as MISR_Enable. Along with this, we have a mod-M counter which issues a pulse after every M cycles and a M-bit comparator which compares and issues a Pass/Fail information to the tester via the test output port, Pass_Fail. After every M scan cycles, the M-bit shift register now contains the M-bit expect and the counter issues a pulse which enables the comparison of the MISR compactor output with its expected value in the shift register and indicates whether a fault has been captured or not. After all the data is scanned out, we perform the regular MISR signature download via the scan outs and enable the chip-level master reset signal so that all the MISR registers, the M-bit shift registers and the mod-M counter are reset and they are ready for the next round of scan unload cycles.

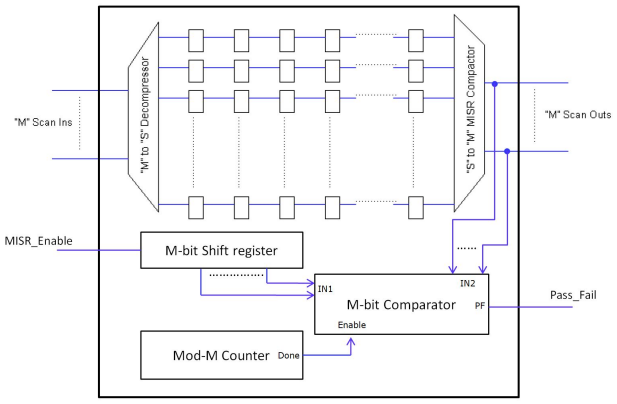

Fig. 2. On-chip MISR signature comparison architecture

With this approach, we can determine the location of the fault capturing flop with a better resolution. If we assume

that the fault was captured by a flop in the H^{th} cycle, then the diagnostic resolution is given by (5) and the resolution improvement is D - D_1. However, the amount of improvement is dependent on the location of the fault capturing flop. Farther the flop is to the MISR, better is the improvement in resolution and it deteriorates as we move closer to the MISR.

$$D_1 = (L - (M * floor(H/M))) \tag{5}$$

C. MISR Reset after T cycles

The architecture and methodology mentioned in the previous section does have few advantages over the regular MISR architecture but it does not address some of the basic disadvantages like loss of data correlation, complete corruption of MISR signature due to X-sources etc. Hence, we enhanced the MISR architecture to reset all the MISR registers after every M scan cycles as shown in Fig 3.

The Reset signal is driven by the inverted version of the Done output of the mod-M Counter. When counter value is less than M, the Done bit is 0 and the AND gates transform into buffers (regular MISR operation). After M cycles, the Done bit of the counter becomes 1 and the output of the AND gates are 0, creating the scenario as if the MISR registers are reset. At $(M+1)^{th}$ cycle, the Done bit again becomes 1 and the process repeats. With this approach, the diagnostic resolution is now fixed to M (6) which is much better than D and D_1. This architecture has lot of advantages and they are mentioned in Section IV.

$$D_2 = M \tag{6}$$

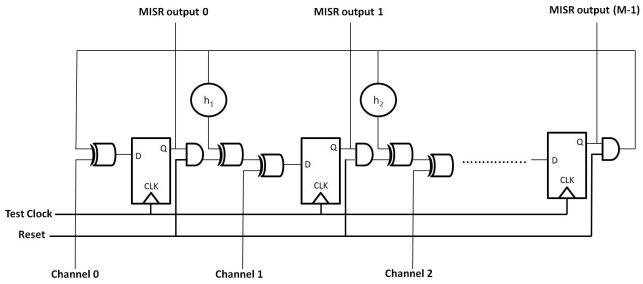

Fig. 3. Enhanced MISR architecture with reset after M cycles

D. Diagnostic data unload

The M-bit comparator not only provides the pass/fail information but the output also contains diagnostic data. In the presence of a fault, when the MISR value is compared with its expected value after M cycles, the scan out cycle containing the fault capturing flop can be determined based on the position of the mismatching bits of the comparator output. Different mechanisms can be used to dump this on-chip data for diagnostics depending on the type of test program applied to the IC.

During the initial bring-up, it is required to accumulate as much diagnostic data as possible. A simple shift register and a test output port can be used to accomplish this, as shown in Fig 4. The length of the shift register will be $M+1$ in order to prevent reading of incorrect data from the last flop at the test output port during M^{th} cycle. Before the scan unload cycle begins, the shift registers are reset and hence, for the initial $M+1$ cycles, the output will be 0s. After every M cycles, the comparator output will be parallely loaded into the shift register and they get serially shifted out every cycle via the test output port. With this data dump, we can obtain all the diagnostic data required for analysis. A bypass structure can also be introduced to skip the diagnostic unload architecture for high volume production test at the wafer level since we require only the pass/fail information.

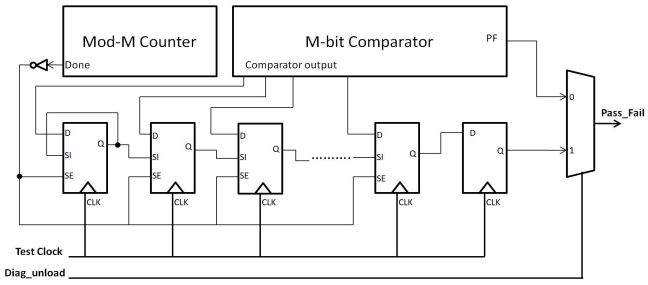

Fig. 4. Comparator data unload architecture

III. Experimental results

Experiments were conducted on a design with ISCAS bench-marking modules to validate the claims. We introduced Illinois type of decompressor and OPMISR compactor in the design during scan synthesis. The statistics of the design post scan synthesis are given below:

- Number of flops in the design = 17280
- Number of Scan inputs = Number of scan outputs = 16. Hence, $M = T = 16$
- Compression factor = 4. Hence, $S = 16*4 = 64$
- Number of flops in each of the short chains, $L = 17280/64 = 270$
- MISR settings h_2, h_3 and $h_5 = 1$ (h_0 is always 1)

The new architecture for intermittent MISR signature comparison and MISR reset were also added to the design. Various random faults were injected in the circuit and simulations were run to compare the diagnostic capabilities of the enhanced architecture with the regular MISR. The actual fault cycle is constant for faults 1, 2 and 3 because there is only one flop in the fanout cone of the logic where the fault is present. The fault 4 gets captured in 2 different flops in 2 different patterns and hence we have multiple entries.

Firstly, we observed that for all cases, the new architecture is able to find all the faults with same set of patterns similar to traditional MISR thus proving that there are no fallouts. The diagnostic resolutions D, D_1 and D_2 have been tabulated in Table II. We observe that D_1 is better than D but the amount of improvement reduces when the fault cycles occur early.

With the MISR reset enhancement, we observe significant improvement and it is consistent for all the faults.

TABLE II
DIAGNOSTIC RESOLUTION COMPARISON

	Fault 1	Fault 2	Fault 3	Fault4	
Fault cycle	196	52	74	17	127
D	270	270	270	270	270
D_1	78	222	206	254	158
D_2	16	16	16	16	16

Table III shows the savings in the number of cycles for each failing pattern per die during the production test. If we extrapolate these results for the complete wafer, the savings are significant. This reduces the total time spent on the tester since we get a fail indication much earlier and the test can be shifted to the next die. From Fig 5, we can also conclude that the proposed architecture is always able to determine the presence of faults within M cycles as compared to the regular MISR approach which always requires L cycles.

TABLE III
SAVINGS IN NUMBER OF TEST CYCLES

	Fault1	Fault2	Fault3	Fault4	
Actual fault cycle	196	52	74	17	127
Regular MISR	270	270	270	270	270
With MISR reset	208	64	80	32	128
#No.of cycles saved per failing pattern	62	206	190	238	142

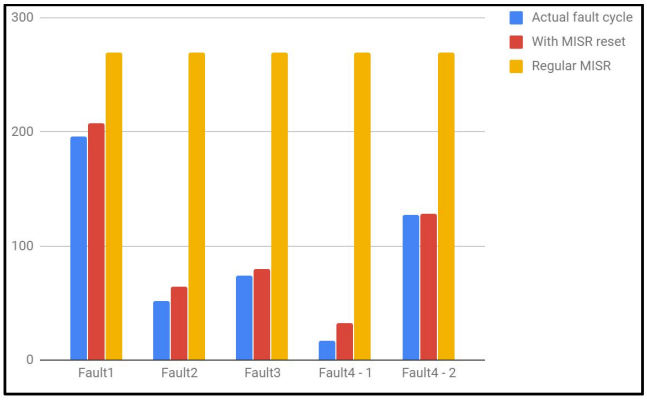

Fig. 5. Comparison of #cycles for fault detection

The number of mismatching bits during comparison of expected and obtained MISR signatures for the faults is shown in Table IV. We observe that the faulty value affects most of the bits in the regular MISR signature whereas in the MISR reset approach, a maximum of 4 bits, equal to the number of feedback paths in the MISR equation, get affected.

A. Area overhead analysis

The proposed architecture requires very few basic combinational gates and flip-flops along with 2 extra test ports,

TABLE IV
#BIT MISMATCHES AFTER SIGNATURE COMPARISON

	Fault1	Fault2	Fault3	Fault4	
Regular MISR	10	6	7	8	7
With MISR reset	1	1	1	4	1

MISR_Enable on the input side and Pass_Fail on the output side. The gate count in each block of the enhanced architecture are given below:

- M-bit shift register storing the expects = M flops
- M-bit comparator = M XOR gates + M-bit AND gate
- M-bit MISR = Extra M AND gates for reset
- Mod-M counter = ceil($\log_2(M)$) number of flops + few combinational gates based on the required mod value
- If diagnostic unload is required, $(M+1)$-bit shift register to store the comparator output = $(M+1)$ flops

In the design used for the experiment, we have M=16 and the diagnostic unload architecture was not introduced. The total hardware added was 20 flops, 19 XOR gates, 26 AND gates, 2 NOR gates and 4 inverters. We can observe that the area overhead is minimal.

IV. ADVANTAGES OF THE PROPOSED ARCHITECTURE

The advantages of the enhanced MISR reset architecture are listed below:

1) The diagnostic resolution is fixed to M and not dependent on the location of the fault capturing flop. The improvement D - D_2, is significant
2) Early pass/fail indication, especially during production test, reduces the test time and test cost
3) The reset ensures that the wrong value does not stay in the MISR signature for more than M cycles. This reduces the number of bit mismatches in the comparator output, improving the diagnostic capabilities. It also helps in finding all the fault locations if they are distributed between multiple intervals for the same pattern as well.
4) The MISR signature corruption due to any unmasked X-sources are also restricted to M cycles and ensures that we do not lose the whole signature for the pattern
5) The idea is simple, involves minor changes to the architecture and area overhead is minimal
6) This architecture and methodology can aid the current commercial tools to achieve better diagnostic results with reduced computation effort

V. CONCLUSIONS AND FUTURE WORK

We have proposed a new hardware architecture to improve the diagnostic capabilities of MISR compaction techniques and reduce test time and test cost. The idea involves comparison of MISR signatures after a fixed number of cycles. An enhancement to this idea has also been proposed to reset the MISR registers after the same number of cycles so that any fault can be detected early and the corruption of the signature

due to any fault or unmasked X-sources is restricted to only few cycles. Experimental results have fulfilled the claims and the overall area overhead is also minimal.

The proposed architecture still requires M scan outs and a MISR signature observe cycle after all scan unload cycles to prevent losing the data in the final Y cycles. As a part of future work, few enhancements can be made to the idea which can eliminate these requirements and reduces test overhead by a significant amount. The idea also needs to be evaluated for designs with multiple faults, especially if they are getting captured within the same interval.

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