Current DAC based -40dB PSRR Configurable Output LDO in BCD Technology

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***Abstract*— This paper presents a current DAC based configurable wide output voltage range Low Drop-Out (LDO) regulator. This LDO uses a multi-supply operational amplifier architecture that uses low supply voltage (1.8V) for input stage in differential amplifier and high supply voltage (5V) for output stage. A nested miller compensation combined with buffer compensation scheme is presented that provides a fast transient response and full range AC stability from 0 to 100mA load current for an output capacitive load of 50pF using compensation capacitor of 5pF. LDO output is configurable using internal current based digital to analog converter (DAC) and output voltage ranges from 2.3V to 5.5V with a step of 107mV. Total loop gain of LDO is 127dB at DC and PSRR is -40dB at 1MHz frequency for no current load condition. Presented LDO is designed in 110nm STMicroelectronics BCD9s technology; consuming 30µA of total ground current (without current DAC).**

Keywords—BCD, LDO, DAC, Voltage Regulator, PSRR, Line Regulation, Load Regulation.

I. INTRODUCTION

Power Management system has become very important module for any System on Chip (SoC) design specifically with introduction of Artificial Intelligence (AI) and Internet of Things (IoT) applications. The principle of dynamic voltage and frequency scaling (DVFS) is widely used in controlling the power consumptions of SoC [1]. A Power Management Unit (PMU) contains several sub-systems including linear regulators, switching regulators and control logic. The control logic changes the attributes of each subsystem; and controls the output voltage levels according to requirement and thus controls the power consumption of SoC. The programmability in the output voltage range of regulator helps in the voltage scaling during different operation mode of SoC, which overall helps in controlling the power consumption.

In literature, there are various cap-less regulator designs available, that uses large capacitive load in range of (nF-μF) for stability purpose [2-5]. These large capacitances are often present off-chip, and their on-chip realization consumes large silicon area. These designs are also inherently stable due to addition of left half plane zero introduced due to equivalent series resistance with high capacitive load. For most of the automotive and embedded SoC targeted for AI and IoT applications, the capacitive loads are often on-chip in the range of few pF and the current loads in tens of mA. The stability of regulator for capacitive loads (tens of pF), often poses challenge for designer to guarantee its stability for varying current load conditions. This work is designed for driving the on-chip capacitive and current load and employs on-chip compensation capacitors for achieving the stability.

There are various programmable output range architectures available in literature. In [6] and [7], floating gate transistors are used in the voltage regulator architecture. The output voltage is the function of the charge stored in the floating gate. The programming of floating gate is done by changing the charge stored in floating gate. This approach requires On-chip high voltage generator charge pumps to modulate the charge stored in floating gates. This makes the overall design complex and consumes area as well.

The modulation of reference voltage also can result in the programmable output voltage. In [8], reference voltage is scaled for regulator using the metal-insulator-metal (MIM) capacitive voltage divider digital to analog converter (DAC). This approach is good enough to obtain wide programmable voltage range, but implementing capacitive DAC consumes significant area, and output voltage range also suffers from non-linearity associated with capacitors. This paper mainly focuses on design and implementation of a programmable LDO module targeted for embedded and automotive applications. LDO is generally perceived as the simplest and inexpensive way to regulate and control the output voltage that is delivered from a higher supply voltage. In this work, we proposed an architecture of operational amplifier (op-amp) that works on dual supply voltages. In addition, a current DAC based configuration possibility is presented to regulate a range of output voltages, without significant large area overhead. Furthermore, a detailed small signal analysis is also presented to analyze different figure of merit (FOM) and pole-zero analysis of LDO.

This paper is organized in subsequent section as follows: Section II discusses about the conventional programmable regulator and architecture of proposed regulator, along with its detailed small signal and pole-zero analysis. Section III discusses about the post layout simulated results and various figure of merits along with the comparisons with state-of-the-art architectures. In Section IV, we present the conclusions.

II. CIRCUIT DESCRIPTION

The conventional voltage regulator architecture uses an op-amp (A0) in a feedback loop with the pass transistor (P0) and resistance ladder as shown in figure 1.

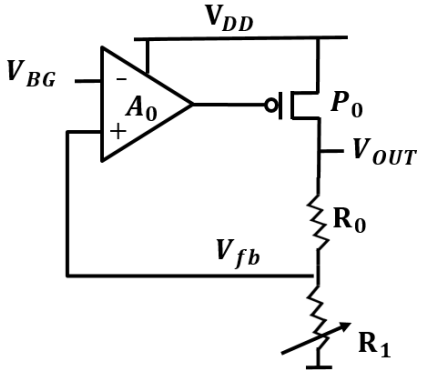

Fig. 1. Conventional Voltage Regulator

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The op-amp controls the gate of pass transistor to keep the 'V_{fb}' node fixed to fixed reference 'V_{BG}' across PVT and load current variations.

$$V_{OUT} = V_{BG}(1 + \frac{R_0}{R_1}) \quad (1)$$

In order to cater the requirement of different magnitude of regulated voltage during different modes of operation, often 'R_1' is made variable to control the amount of current flowing through the ladder. However, this approach itself suffers from few shortcomings listed below.

a. The variable resistance (R_1) is controlled through switches, and if multiple series resistance are to be controlled through their respective switches, than switch resistance itself comes into consideration due to rise in threshold voltage of switches. This results in significant error in the desired magnitude of regulator and non-linear step size between two consecutive voltage steps. Furthermore, this approach also results in area overhead due to large sizes of resistances.
b. If the ground connection of voltage reference 'V_{BG}' and resistance ladder are not same (which is often the case), then magnitude of regulated output voltage gets impacted severely due to ground bounce (due to large current injection in ground) of ladder.

To solve above-mentioned issues in conventional regulator, a current mode architecture is presented in this work to generate the variable magnitude regulated voltage. The complete architecture of regulator is shown in figure 2. The first op-amp 'A0' operates on lower supply 'V_{DD}' and regulates the node 'fb_1' to 'V_{BG}'. This loop is used to generate the reference current 'I_{R0}'.

$$I_{R0} = \frac{V_{BG}}{R_0 + R_{TRIM}} \quad (2)$$

Here, 'V_{BG}'is the fixed reference voltage generated from on-chip bandgap reference, 'R_0' is the fixed poly resistance and 'R_{TRIM}' is the small magnitude poly resistance used to make the 'I_{R0}' fixed during process variations.

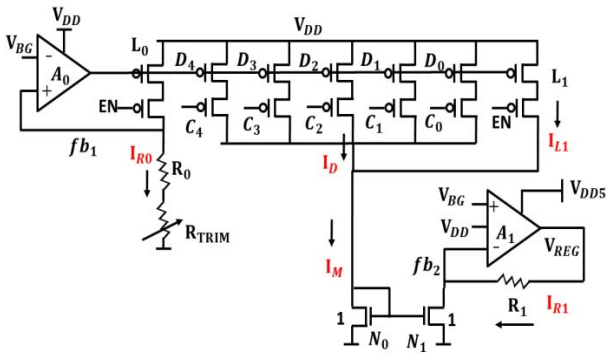

Fig. 2. Complete architecture of proposed regulator

Furthermore, 'I_{R0}' is mirrored to produce 'I_M' with the help of PMOS (L1) and D0-D4 transistors. The mirror transistor L0 and L1 are equal sized transistors.

$$I_{L1} = I_{R0} \quad (3)$$

The D0-D4 transistors forms the binary weighted current DAC (digital-to-analog converter), and this current DAC is controlled by five digital bits 'C [4:0]'. If all five bits are disabled, then maximum 'I_D' will flow through DAC. The Total current 'I_M' can be written as:

$$I_M = I_{R0} + I_D \quad (4)$$

$$I_M = N_{REG}.I_{R0} \quad (5)$$

Here, 'N_{REG}' is the scaling factor introduced in the reference current 'I_{R0}' due to additional current from the current DAC. The current 'I_M' is further mirrored by a unity factor with help of N0 and N1 and passed through R1 to generate 'V_{REG}', which is the final output of regulator. Another op-amp 'A1' is used to regulate the node 'fb_2' to 'V_{BG}'.

$$I_{R1} = I_M = \frac{V_{REG} - V_{BG}}{R_1} \quad (6)$$

$$V_{REG} = V_{BG} + R_1.I_M \quad (7)$$

$$V_{REG} = V_{BG} + R_1.N_{REG}.\frac{V_{BG}}{R_0 + R_{TRIM}} \quad (8)$$

$$V_{REG} = V_{BG}(1 + \frac{R_1.N_{REG}}{R_0 + R_{TRIM}}) \quad (9)$$

The magnitude of regulator 'V_{REG}' is dependent on current DAC configuration ('N_{REG}'). In current DAC the switches 'C[4:0]' are present in parallel connection, hence there inherent on-resistance does not introduce non-linearity in magnitude of output as much significantly as introduced in conventional regulator due to presence of switches in series. Moreover, complete regulator architecture and reference generator block can also have different ground connections. The rise in ground voltage for regulator still keeps the 'V_{GS}' equal for mirror transistors N0 and N1 and will not affect the magnitude of regulated output voltage 'V_{REG}'.

In addition to regulation, op-amp 'A1' is also capable of providing the maximum desired load current. The output voltage of regulator ('V_{REG}') can be even higher than lower supply 'V_{DD}', hence its final stage operates on higher supply 'V_{DD5}'. The complete schematic of op-amp 'A1' is shown below in Figure 3. The lower supply 'V_{DD}' is used in op-amp 'A1' to operate the differential pair folded cascode stage at lower supply voltage using only low-voltage (LV) transistors, that can provide higher value of transconductance as compared to high voltage (HV) transistors. The multiple bias voltages 'V_{B1}', 'V_{B2}' and 'V_{B3}' are also generated using lower supply 'V_{DD}' to bias the cascode transistors present in op-amp.

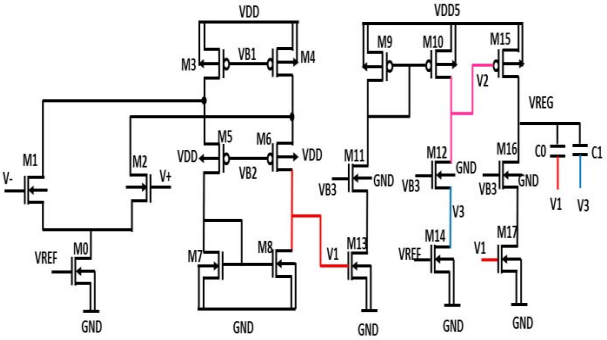

Fig. 3. Circuit schematic of op-amp 'A1'

The first stage of the op-amp 'A1' is folded cascode stage. M1-M2, M3-M4, M5-M6 and M7-M8 are equal sized transistors. The output of first stage 'V_1' acts as an input for the third stage transistor 'M17' and output of second stage 'V_2' acts as an input for third stage transistor 'M15'. The final stage

of op-amp 'A1' is a class A-B stage, which is able to acts as both current source and current sink, depending upon load requirement.

A. Small Signal Gain of op-amp A1.

The small signal equivalent circuit of first stage is as shown in figure 4.

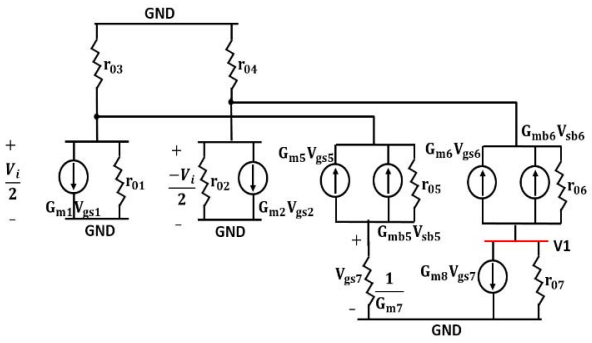

Fig. 4. Small signal equivalent circuit of first stage.

$$V_1 = G_{m1}.R_{out1}\,V_i \quad (10)$$

$$R_{out1} = \{r_{07}|||[(G_{m6}+G_{mb6})r_{06}(r_{04}||r_{02})]\} \quad (11)$$

Here G_m denotes the equivalent transconductance of that transistor G_{mb} denotes the transconductance due to body bias effect and r_0 represents the output resistance of the transistor. The output of first stage is denoted as 'V_1', output resistance of first stage is denoted by 'R_{out1}', DC gain is denoted by 'A_{v1}' and the input signal is denoted by 'V_i'. The cascode combination of M6 and M4 exhibits much higher output resistance than M7. We can approximate 'V_1' and 'A_{v1}' as:

$$V_1 \approx G_{m1}.r_{07}\,V_i \quad (12)$$

$$A_{v1} \approx G_{m1}r_{07} \quad (13)$$

The small signal equivalent circuit of the second stage of op-amp is shown below in figure 5.

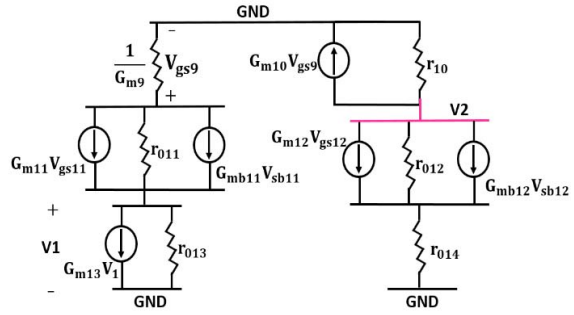

Fig. 5. Small signal equivalent circuit of second stage.

In the second stage 'M9-M10', 'M11-M12' are equal sized transistors. M13 is driven by the output of first stage 'V_1'and M14 is used as a constant current source. The second stage comprises of diode connected 'M9' and cascode NMOS 'M11' and 'M13'. The diode connected 'M9' acts as a mirror transistor and helps in mirroring the signal current to output stage consisting of M10 and cascoded NMOS 'M12' and 'M14'.

$$V_{gs9} = -G_{m13}\{[(G_{m11}+G_{mb11}).r_{011}.r_{013}]||\frac{1}{G_{m9}}\}V_1 \quad (14)$$

The cascode combination of M11 and M13 exhibits very high output resistance as compared to diode connected M9. Hence, the equivalent value of 'V_{gs9}' can be approximated as:

$$V_{gs9} \approx -\frac{G_{m13}}{G_{m9}}V_1 \quad (15)$$

The output of second stage 'V_2' will be as shown below:

$$V_2 = -G_{m10}V_{gs9}R_{out2} \quad (16)$$

$$R_{out2} = \{r_{o10}|||[(G_{m12}+G_{mb12}).r_{o12}.r_{o14}]\} \quad (17)$$

The 'V_2' can be approximated as shown in eq.(18), since cascode combination of M12 and M14 exhibits much higher output impedance as compared to output resistance offered M10.

$$V_2 \approx -G_{m10}.V_{gs9}.r_{o10} \quad (18)$$

On equating the eq. (15) in above eq. (18), we can get the 'V_2' and the equivalent dc gain of second stage.

$$V_2 \approx G_{m10}.r_{o10}.\frac{G_{m13}}{G_{m9}}V_1 \quad (19)$$

$$A_{v2} \approx G_{m10}.r_{o10}.\frac{G_{m13}}{G_{m9}} \quad (20)$$

The small signal equivalent circuit of final stage is shown below in figure. 6.

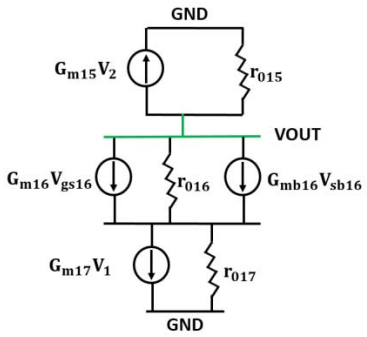

Fig. 6. Small signal equivalent circuit of third stage.

The final stage PMOS ('M15') is driven by the output of second stage (V_2). Furthermore, final stage NMOS ('M17') is driven by the output of first stage (V_1).

$$V_{OUT} = -(G_{m17}V_1 + G_{m15}V_2).R_{OUT} \quad (21)$$

$$R_{OUT} = \{r_{o15}||\,[(G_{m16}+G_{mb16}).r_{o16}.r_{o17}]\} \quad (22)$$

B. Stability Analysis of op-amp A1.

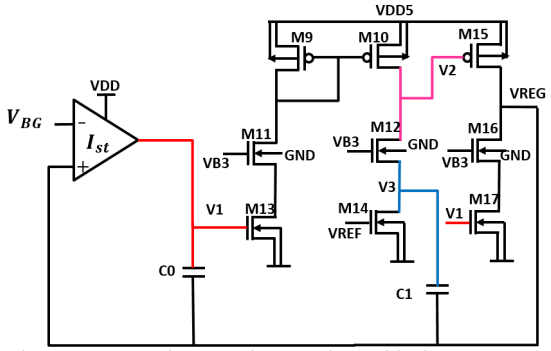

Fig. 7. Compensation capacitors used to stable the op-amp A1

The nested miller compensation combined with buffer compensation (Fig.7) strategy is employed in op-amp 'A1' to guarantee its closed loop stability across PVT, load current and load capacitance variations. The miller capacitance 'C_0' is

introduced between output 'V_{REG}' and first stage output 'V_1' and it acts as a dominant pole for the regulator.

$$\omega_{p1} = 1/A_{v2}\,A_{v3}.C_0.R_{out1} \quad (23)$$

$$R_{out1} = \{r_{07}||[(G_{m6}+G_{mb6})r_{06}(r_{04}||r_{02})]\} \quad (24)$$

'A_{v2}' and 'A_{v3}' are the voltage gain of second and third stage respectively. 'R_{out1}' is the output resistance seen from the output of first stage amplifier. The current buffer compensation strategy [9] is utilized with capacitor 'C_1' and it is connected to source node of transistor M12. The capacitor 'C_0' can be considered as a short circuit for high frequency, therefore 'V_{REG}' and 'V_1'are actually connected, thus second and third stage acts as independent two stage operational amplifier ("partial amplifier") in unity gain feedback provided by 'C_0'. The second pole 'ω_{p2}' is the unity gain frequency of this partial amplifier and it is equal to G_m of first stage divided by compensation capacitance.

$$\omega_{p2} = G_{m13}/C_1 \quad (25)$$

The transistor M12 acts as a resistance of approximate value '$1/(G_{m12}+G_{mb12})$' in series with capacitor 'C_1' and provides the left half plane zero. The location of left half plane zero can be controlled by adjusting the correct aspect ratio of transistor M12.

$$\omega_z = \frac{1}{C_1(G_{m15}{}^{-1}-R_z)} \quad (26)$$

$$R_z \approx \frac{1}{(G_{m12}+G_{mb12})} \quad (27)$$

The output pole 'ω_{p3}' is associated with output node 'V_{REG}' and it is equal to the non-dominant pole frequency of the "partial amplifier" which corresponds to the pole associated to the output node. We can assume that G_{m12} is very large and entire compensation current ($V_{REG}.s.C_1$) flows through M12. This current flows through parasitic impedance ($1/\ s.C_2$) present at node ('V_2')

$$V_2 = V_{REG}.s.C_1/s.C_2 \quad (28)$$

The current produced at output node is G_{m15} times the 'V_2'.

$$I_{M15} = G_{m15}.V_{REG}.C_1/C_2 \quad (29)$$

Moreover, the output impedance seen through 'V_{REG}' node can be expressed as:

$$R_{OUT} = V_{REG}/I_{M15} = 1/[G_{m15}.(C_1/C_2)] \quad (30)$$

The output pole frequency is written as:

$$\omega_{p3} = 1/(R_{OUT}.C_{LOAD}) \quad (31)$$

$$\omega_{p3} = G_{m15}.C_1/C_{LOAD}.C_2 \quad (32)$$

C. Power Suppy Rejection

The Power Supply Rejection is directly proportional to the feed forward path gain between input supply and output of regulator. It is also inversely proportional to loop gain [2].

$$PSR_{LDO} \propto 1/(1+A_{LG}) \quad (33)$$

$$A_{LG} \approx A_{v1}A_{v2}A_{v3} \quad (34)$$

'A_{LG}' represents the loop gain and 'A_v' represents the voltage gain of individual stages. The proposed regulator uses three gain stages that provides very high dc gain as well as high rejection of supply noise till the bandwidth of the regulator.

III. SIMULATION RESULTS

The presented current DAC based low-dropout (LDO) voltage regulator is designed in triple well 110nm STMicroelectronics BCD9s Technology. All the simulations are performed on the post layout extracted spice netlist using mentor-graphics ELDO simulator. The performance parameters of regulator are characterized across all process corners, temperature range from -40℃ to 175℃, lower supply 'V_{DD}' variations of 1.5-1.98V and higher supply 'V_{DD5}' variations of 3.5-6V. The trimmed bandgap reference voltage is on-chip available for the voltage regulator having magnitude of 1.2V. The proposed design is suitable for driving the on-chip capacitance load of up-to 50pF, current load of up-to 100mA, and consumes static current of 20µA from V_{DD5} supply and 10µA from V_{DD} supply. The design uses two on-chip capacitors 'C_0' of 4pF and 'C_1' of 1pF for the purpose of stability.

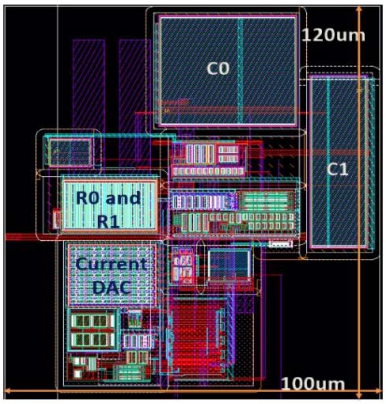

Fig. 8. Layout View of proposed current DAC based Voltage Regulator

The uniqueness of the proposed design lies in its ability to provide constant voltage step across entire range of configuration bits. The output voltage of regulator is programmable between 2.38V and 5.5V. The minimum possible voltage step of 107mV is present in between two successive possible output voltages. It is also evident from Figure.9, that the voltage step will remain fixed for entire programming range of regulator.

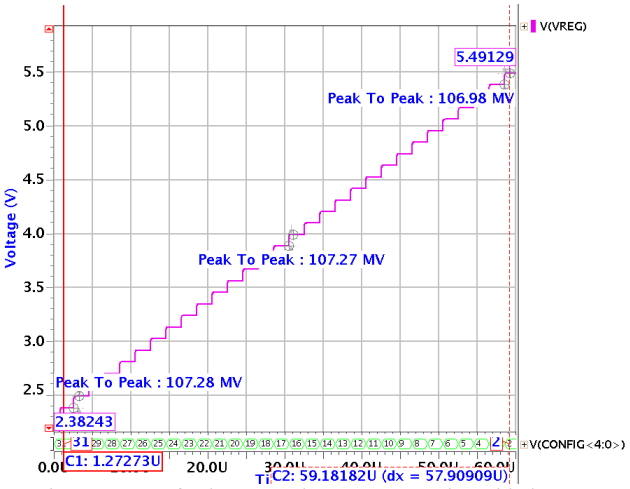

Fig. 9. Output of voltage Regulator 'Vreg', varying with the 'Nreg<4:0>' bits

Another important performance characteristic of voltage regulator is its ability to maintain desired voltage level irrespective of current load sink from the regulator. The worst-case dc-load regulation of proposed regulator is 0.13mV-pp (Figure.10). The transient load behavior of regulator (Figure. 11) shows that output of voltage regulator is fast enough to support the sudden current requirements of 20mA in 100ns. The ripples produced in output due to sudden requirements is 632mV, for regulator output of 3V driving a capacitance load of 50pF.

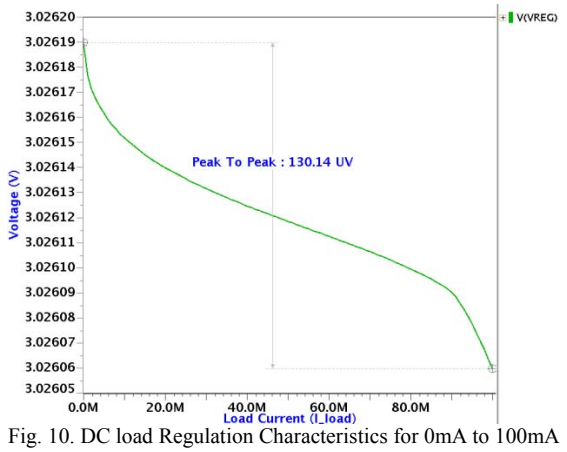

Fig. 10. DC load Regulation Characteristics for 0mA to 100mA current load at output of 3V.

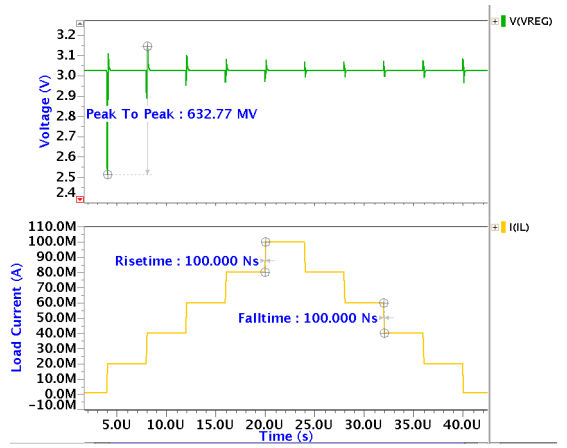

Fig. 11. Variation in output voltage for 20mA steps of load current

The output resistance seen by the output stage will be maximum for no current load, which causes the non-dominant pole due to load capacitor of 50pF to come closer to unity gain frequency and deteriorate the phase margin. The worst case no load phase margin is 59.7° across all PVT conditions for 50pF load capacitor (Figure. 12). The three-stage amplifier used in the design of regulator ensures high DC loop-gain of 127.1dB.

As the load current starts increasing from the regulator, the output resistance starts reducing and pushes the non-dominant pole due to load capacitor away from the unity gain frequency. This phenomena overall improves the stability of the regulator by increasing the phase margin.

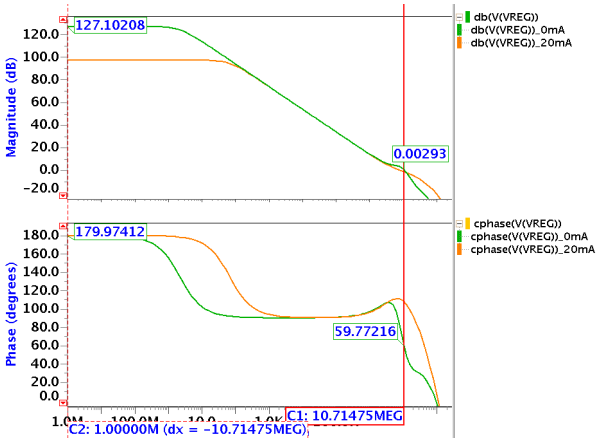

Fig. 12. AC stability analysis at no load current condition and 20mA load current condition

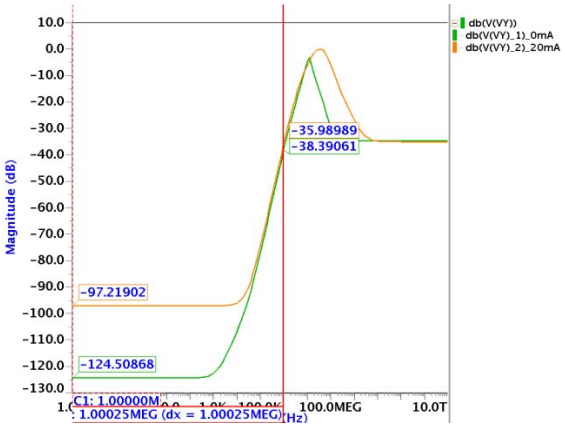

Fig. 13. PSRR plot for regulator at no load current condition and 20mA load current condition

The power-supply rejection ratio is another figure of merit associated with the regulator's performance. The designed regulator is able to reject the supply noise even at 1MHz, by -40dB (Figure.13). The line regulation for 3V output, with supply varying between 3.5V-6V is 1.80µV. (Figure.14).

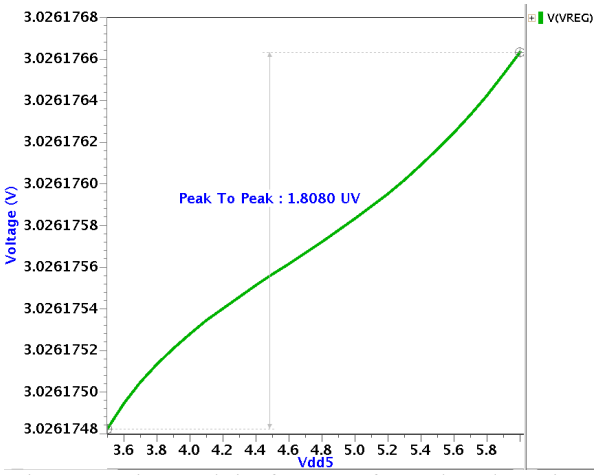

Fig. 14. DC Line Regulation for output of 3V and supply varying from 3.5V to 6V.

Table. 1. Comparison of proposed voltage regulator with recent state-of-the-art-designs

	[10]	[11]	[12]	[13]	[14]	**This work**
Year	2014	2015	2012	2012	2014	**2018**
Technology	180nm	65nm	130nm	65nm	65nm	**110nm**
Final-Stage	Class A	Class A	Class A	Class B	Class A	**Class A-B**
Vsupply	1.8	1.15-1.4	2.07-5.5	2.0-5.5	1.2	**1.5-1.98V & 3.5-6V**
Vout	1.6	0.95-1.2	1.3	1.3	1	**2.38-5.5V**
Imax(mA), C_{Load}	50, 128pF	50, 140pF	50, 20pF	200, 4.4nF	50, 10nF	**100, 50pF**
DC Load Regulation(mV/mA)	NA	1.1	0.055	NA	0.034	**0.0013**
Line Regulation (mV/V)	NA	37	8.1	NA	8.89	**0.00072**
Active Area (mm^2)	0.14	0.026	0.018	0.21	NA	**0.012**
PSRR (@1MHz)	-37dB	-12dB	-15dB	-50dB	NA	**-40dB**
FOM($C_L \Delta V_{OUT} I_Q / {I_{MAX}}^2$) ps [15]	0.21	5.74	0.017	23	94	**0.45**

IV. CONCLUSION

A wide output range (2.38-5.5V), linear programmable voltage regulator having minimum granularity of 107mV between two successive voltages is presented in this work. The voltage regulator uses configurable current DAC to produce variable output voltage. The regulator consumes active area of $0.012mm^2$, quiescent current of 30µA from two supplies, and suitable to drive capacitance and current load of 50pF and 100mA respectively. The comparison of different figure of merits with state-of-the-art regulator architecture is shown in Table1. The simulation results validate the advantages of proposed design.

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