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Novel Low and High Threshold TFET Based NTI and PTI Cells Benchmarked With Standard 45 nm CMOS Technology for Ternary Logic Applications

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***Abstract*—For the first time, innovative low (LVT) and high (HVT) threshold tunnel FET devices have been reported for ternary logic applications. Based on an iterative algorithm, the DG TFET structures have been optimized such that the TFET characteristics are better than the MOSFETs having same width at the standard 45 nm technology node. These devices are designed in such a way that the low and high threshold voltages are $V_{TL} = V_{DD}/3$ and $V_{TH} = 2V_{DD}/3$ respectively, with the ranges {0 to $V_{DD}/3$}, {$V_{DD}/3$ to $2V_{DD}/3$} & {$2V_{DD}/3$ to V_{DD}} representing the 3 logic states 0, 1 & 2 respectively. Device optimization has been carried out by studying the impact of changes in various device parameters on performance. Optimized TFET devices have been benchmarked with standard CMOS for the same circuit designed using same technology. TFET device characteristics were simulated using synopsys® TCAD tools and circuit performance benchmarking was carried out with the standard 45 nm CMOS library using cadence® EDA tool. Proposed LVT & HVT TFETs have ON currents (I_{ON}) roughly twice and OFF currents (I_{OFF}) at least an order of magnitude lower than the corresponding MOSFETs. The performance of the optimized TFET based NTI & PTI ternary logic cells have been benchmarked with analogous CMOS circuits at same technology node. The overall Power Delay Products (PDP) of the TFET based logic cells have been demonstrated to be around 99.9% lower than the corresponding CMOS based logic cells. The proposed LVT & HVT TFET based NTI and PTI cells will serve as the starting point for any ternary logic applications.**

***Index Terms*—NTFET & PTFET Devices, Low and high threshold voltages (LVT & HVT), Threshold voltage (V_t), 45 nm CMOS technology, I_{ON}:I_{OFF} ratio, band-to-band tunneling BtB.**

I. Introduction

At the nm-scale dimensions, subthreshold leakage becomes extremely detrimental for the device operation [1], [2]. Hence, researchers all over the world have become interested in TFET technology which replaces conventional diffusion current transport in case of MOSFET with band-to-band (BtB) tunneling [3], [4]. This results in a considerable improvement in subthreshold swing and power consumption characteristics far beyond the standard CMOS technology [5], [6]. Gate controlled BtB generation is the working principle of TFET and its basic structure is the gated PIN diode whose ON current arises from BtB generation [7]. Thus, TFETs are promising alternative devices to the MOSFETs for low power applications.

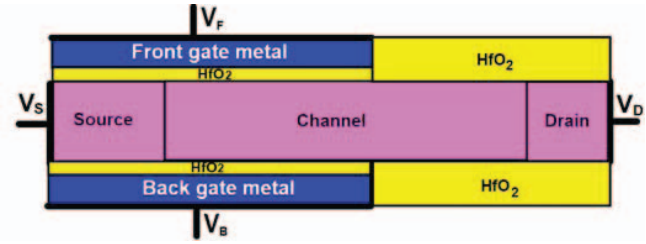

Fig. 1. Schematic of the proposed LVT and HVT symmetric DG TFET.

Ternary logic has gained considerable popularity in recent years as they yield new functionalities in VLSI applications, which cannot be achieved (or difficult to achieve) through conventional CMOS based binary logic [8], [9]. Ternary logic offers several important advantages such as reduced interconnects, smaller chip area and higher operating speeds over binary logic in the design of digital systems as reported earlier [8], [9]. The primary requirement of ternary logic is that the devices used to implement them must have 2 distinct threshold voltages (V_T) [10]. In this work, Low V_{TL} TFET (LVT) & High V_{TH} TFET (HVT) devices have been introduced which switches among 3 logic states, viz, 0, 1 & 2. Thus, LVT & HVT TFETs are promising alternatives to the MOSFETs for low power ternary logic applications.

In the present work, innovative LVT & HVT NTFET and PTFET structures have been proposed. V_T usually varies with respect to geometry, the channel length, doping concentration, gate material and the drain bias [11], [12]. In the proposed TFETs, the type of gate material and doping concentration have large influence on V_T. Considering the influence of various gate material work functions, the device structures have been optimized to fix the lower V_{TL} & higher V_{TH} at $V_{DD}/3$ and $2V_{DD}/3$ respectively. Section II discusses the optimized LVT & HVT NTFET structure along with their characteristics. Similarly, section III discusses the characteristics of the proposed LVT & HVT PTFET devices. Section IV benchmarks the performance of the proposed LVT & HVT TFETs with respect to the corresponding CMOS devices. Finally, section V benchmarks the performance and characteristics of the proposed TFET based standard ternary logic NTI & PTI cells

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with their CMOS counterparts, inherently demonstrating that the proposed TFETs are much better suited for low power ternary logic implementation than the MOSFETs at the same technology node.

II. Parameters Used in TCAD Simulations

All the device simulations reported in this work were carried out using the standard doping dependent mobility model, high field saturation model, SRH and Auger recombination models in addition to non-local Band-to-Band generation models. ITRS specifies 1 V to be the limit of biasing at the 45 nm technology node. We have followed the same regulation for all the simulations.

III. Proposed LVT and HVT NTFETs

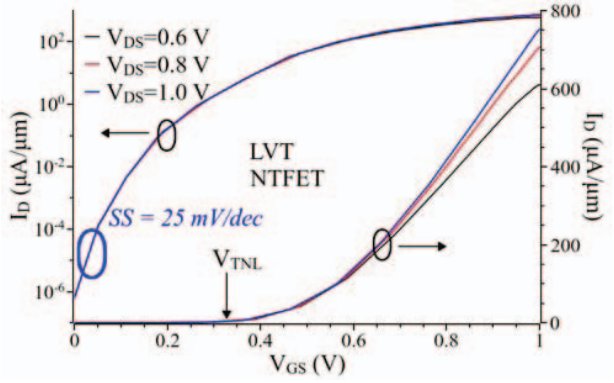
Fig. 1 shows a schematic of the proposed LVT & HVT NTFET & PTFET structures. V_T of the optimized TFET structures can be adjusted by a proper selection of the gate material and the doping concentration at various regions of the device. The electrical characteristics of the proposed devices, all with an effective channel length of 45 nm and a thickness of 9 nm were simulated using industry-standard synopsys® TCAD tool [13]. The gate metal thickness is 3.5 nm and the oxide thickness is 1.5 nm. Clearly, drain current (I_D) increases with decreasing gate dielectric thickness due to better capacitive coupling, however, extremely low dielectric thicknesses may lead to direct gate tunneling, hence a 1.5 nm high-κ dielectric (HfO_2) has been used at the oxide material. Keeping reliability in mind, the dielectric thickness has not been reduced further, since 1.2 nm was reported as the minimum gate oxide thickness in Intel's process [14]. Furthermore, 3.5 nm thick gate material provides the best DC characteristics. The LVT & HVT NTFETs & PTFETs have been optimized such that the I_{ON} is roughly twice the corresponding MOSFETs, while the I_{OFF} remains at least an order of magnitude lower than the MOSFETs at the same 45 nm technology node as discussed in section V.

A. Device Structure

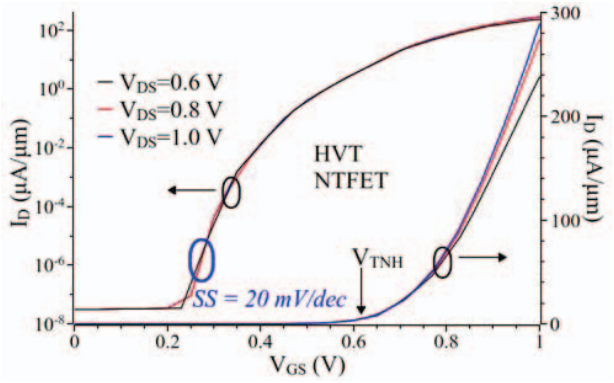
Device parameters used for optimization are listed in Table I. Materials with appropriate work functions used as the gate contacts enhance I_{ON} and V_T can be adjusted accordingly. It has been observed that among all the possible gate materials Al & $TiSi_2$ provide excellent DC characteristics for LVT & HVT NTFET devices respectively.

TABLE I
Parameters of the Optimized LVT & HVT NTFET

	LVT NTFET		*HVT NTFET*	
Region	*Material*	*Doping* (/cm^3)	*Material*	*Doping* (/cm^3)
Source	$Si_{0.1}Ge_{0.9}$	10^{20} P$^+$	$Si_{0.15}Ge_{0.85}$	10^{20} P$^+$
Channel	undoped Si	–	undoped Si	-
Drain	Si	10^{20} N$^+$	Si	10^{18} N
Gate	Al	–	$TiSi_2$	–



(a)



(b)

Fig. 2. I_D-V_{GS} characteristics of (a) LVT (b) HVT NTFETs for different values of V_{DS}. V_{TNL} & V_{TNH} denote the Low & High threshold voltages of the LVT & HVT NTFETs respectively. The minimum inverse subthreshold slopes (SS) observed were 25 & 20 mV/dec for LVT & HVT NTFETs respectively.

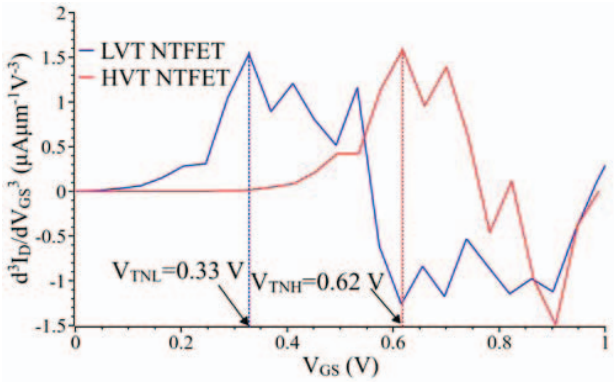


Fig. 3. Lower V_{TNL} and higher V_{TNH} threshold voltages extracted from the LVT & HVT NTFET characteristics of Fig. 2.

B. Characteristics of Symmetric DG LVT and HVT NTFETs

The I_D-V_{GS} characteristics of LVT & HVT NTFETs obtained using non local BtB generation model with increasing V_{DS} are shown in Fig 2. Fig. 3 shows the lower (V_{TNL}) and higher (V_{TNH}) threshold voltages of the proposed NTFETs

extracted using the 3^{rd} derivative method [11]. $\partial^3 I_D/\partial V_{GS}^3$ for $V_{DS} = 1$ V has its first peak at $V_{GS} = 0.33$ V & $V_{GS} = 0.62$ V in Fig. 3, representing the V_{TNL} & V_{TNH} of the optimized LVT & HVT NTFETs respectively [11].

IV. Proposed LVT and HVT PTFETs

A. Device Structure

Device parameters used for LVT & HVT PTFET devices are listed in Table II. As in case of NTFETs in section II, Proper material with appropriate work function used as the gate contacts enhance I_{ON} and V_T can be adjusted accordingly. It has been observed that among all the possible gate materials TiN & $TiSi_2$ provide excellent DC characteristics for LVT & HVT PTFET devices respectively.

TABLE II
Parameters of the Optimized LVT & HVT PTFET

	LVT PTFET		*HVT PTFET*	
Region	*Material*	*Doping* (/cm^3)	*Material*	*Doping* (/cm^3)
Source	$Si_{0.26}Ge_{0.74}$	9×10^{19} N	$Si_{0.25}Ge_{0.75}$	10^{20} N^+
Channel	$Si_{0.26}Ge_{0.74}$	5×10^{16} P	$Si_{0.25}Ge_{0.75}$	5×10^{17} P
Drain	$Si_{0.26}Ge_{0.74}$	5×10^{18} P	$Si_{0.25}Ge_{0.75}$	10^{17} P
Gate	TiN	–	$TiSi_2$	–

B. Characteristics of Symmetric DG LVT and HVT PTFETs

The I_S-V_{SG} characteristics of LVT & HVT PTFETs with increasing V_{SD} are shown in Fig 4. Fig. 5 shows the lower (V_{TPL}) and higher (V_{TPH}) threshold voltages of the proposed PTFETs using the third derivative method [11]. $\partial^3 I_S/\partial V_{SG}^3$ for $V_{SD} = 1$ V has its first peak at $V_{SG} = 0.36$ V & $V_{SG} = 0.62$ V in Fig. 5, representing the V_{TPL} & V_{TPH} of LVT & HVT PTFETs respectively.

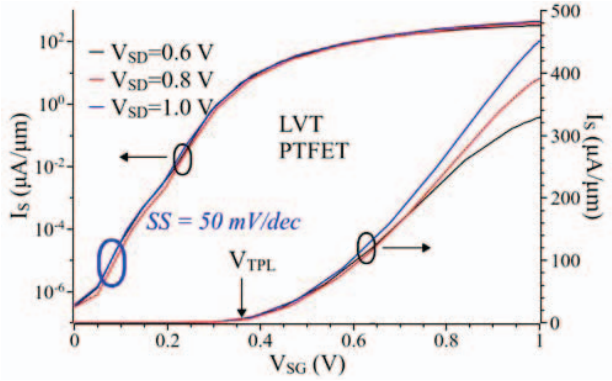
V. Comparison of Proposed LVT & HVT TFETs with LVT & HVT MOSFETs

A. Comparison of LVT and HVT NTFET with NMOSFET

I_D-V_{GS} characteristics of LVT & HVT NTFETs and corresponding NMOSFETs are compared in Fig. 6 for different values of V_{DS}. It has been observed that the I_{ON} of the proposed LVT NTFET is approximately double that of the LVT NMOSFET while the I_{OFF} remains at least an order of magnitude lower than the LVT NMOSFET. Similarly, optimized HVT NTFET has I_{ON} higher than HVT NMOSFET while I_{OFF} remains at least an order of magnitude lower than HVT NMOSFET at the same technology node.

B. Comparison of LVT and HVT PTFET with PMOSFET

I_S-V_{SG} characteristics of LVT & HVT PTFETs and corresponding PMOSFETs are compared in Fig. 7 for different values of V_{SD}. It has been observed that the I_{ON} of the proposed LVT PTFET is approximately double that of the LVT PMOSFET while I_{OFF} remains at least an order of magnitude lower than the LVT PMOSFET. Likewise, optimized HVT PTFET has I_{ON} higher than HVT PMOSFET while I_{OFF} remains at least an order magnitude lower than HVT PMOSFET at same technology node.



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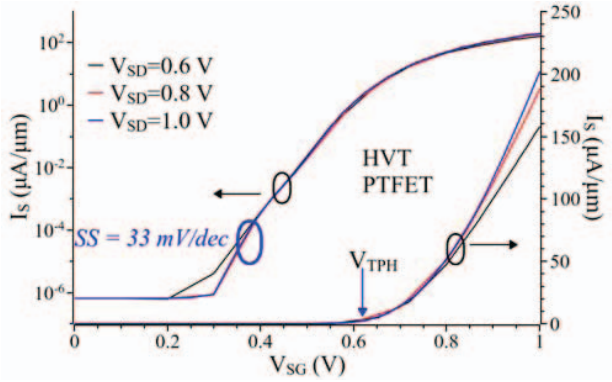


(b)

Fig. 4. I_S-V_{SG} characteristics of (a) LVT and (b) HVT PTFETs for different values of V_{SD}. V_{TPL} & V_{TPH} denote the Low & High threshold voltages of the LVT & HVT PTFETs respectively. The minimum inverse subthreshold slopes (SS) observed were 50 & 33 mV/dec for LVT & HVT PTFETs respectively.

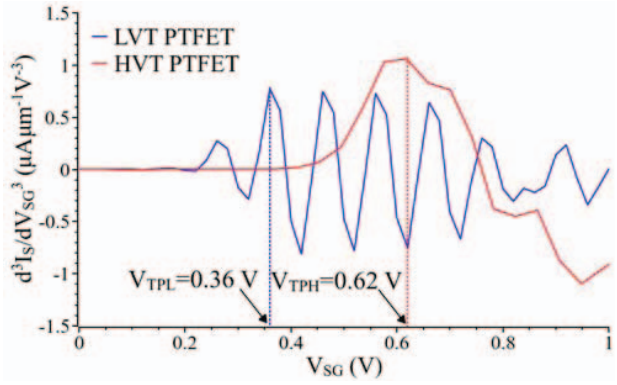
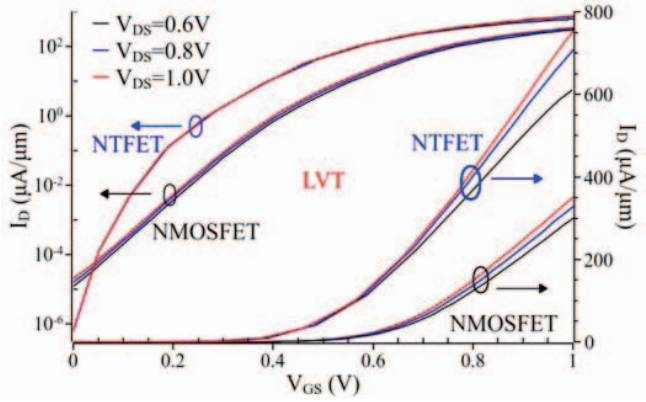


Fig. 5. Lower V_{TPL} and higher V_{TPH} threshold voltages extracted from the LVT & HVT PTFET characteristics of Fig. 4.



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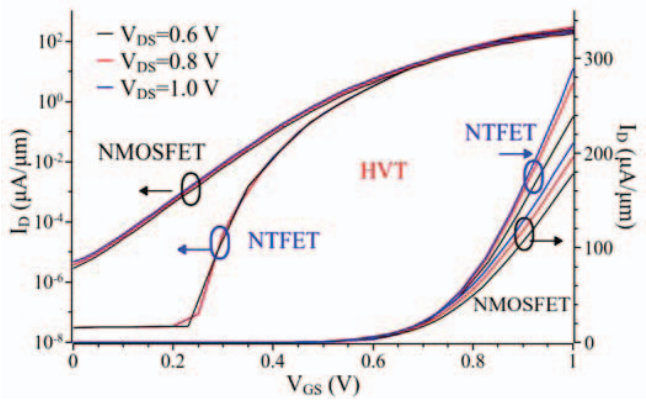
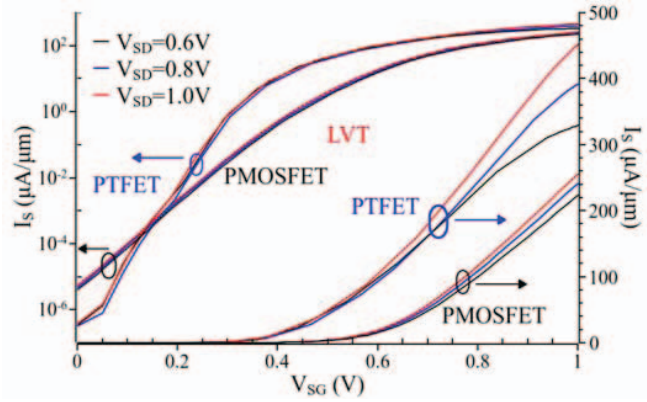


(b)

Fig. 6. I_D-V_{GS} characteristics of (a) LVT (b) HVT NTFET & NMOSFET for different values of V_{DS}.



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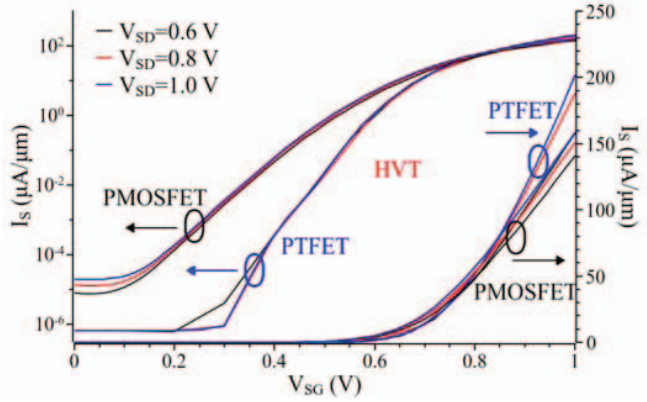


(b)

Fig. 7. I_S-V_{SG} characteristics of (a) LVT (b) HVT PTFET & PMOSFET for different values of V_{SD}.

VI. Benchmarking the Performance of NTI and PTI Ternary Logic Cells

Negative Ternary Inverter (NTI) and *Positive Ternary Inverter* (PTI) are the basic logic cells in ternary logic applications [8]. The following subsections benchmark the characteristics of TFET based NTI & PTI cells with CMOS based cells at 45 nm technology node. The schematics of the NTI & PTI logic cells are shown in Fig. 8 for reference.

A. Benchmarking proposed TFET based NTI performance with standard CMOS NTI

The circuit performance of a TFET based NTI logic cell has been compared with CMOS based NTI circuit at 45 nm technology node. The circuit simulations done using cadence® EDA tool are shown in Figs. 9 & 10. It has been observed that an average static power in TFET based NTI is 0.174 pW which is significantly lower than the CMOS based NTI which consumes 73.7 pW as shown in Fig. 9 and listed in Table III. The PDP of TFET based NTI is 1.57×10^{-23} J which is 0.19% of the PDP of standard 45 nm CMOS based NTI cells (810.7×10^{-23} J). Overall decrement in PDP owing to the proposed TFET based NTI logic cell is 99.81%, as summarized in Table III.

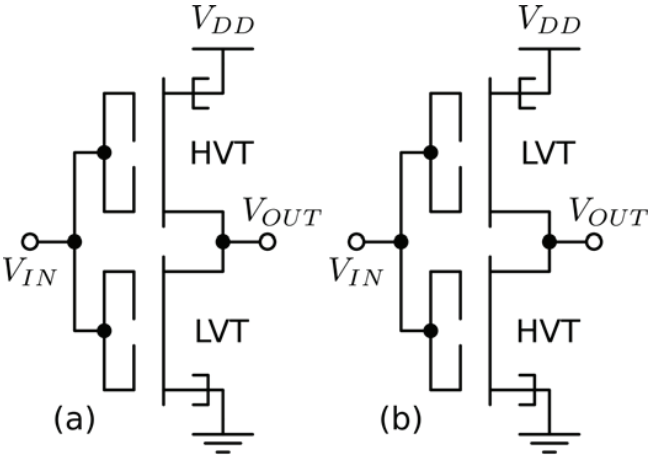
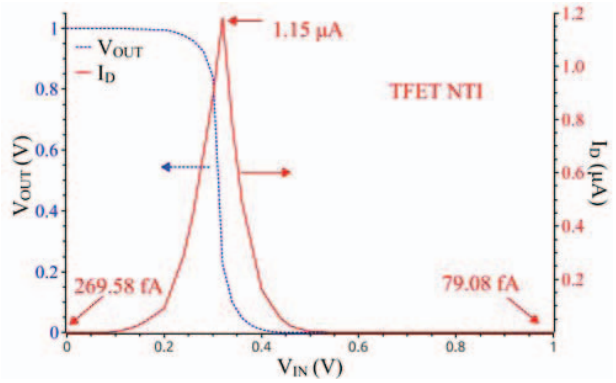
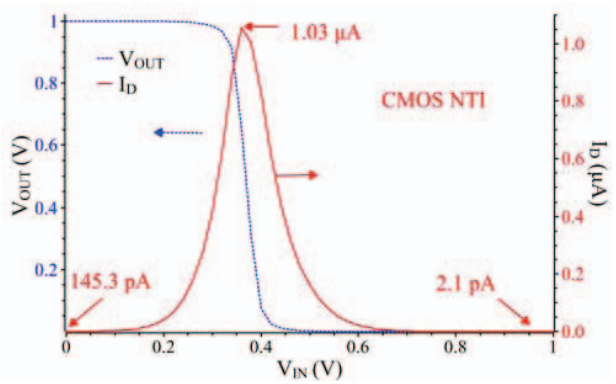


Fig. 8. Schematics of the LVT & HVT TFET based (a) NTI & (b) PTI cells.



(a)



(b)

Fig. 9. Static Power Consumption (a) TFET (b) CMOS NTI .

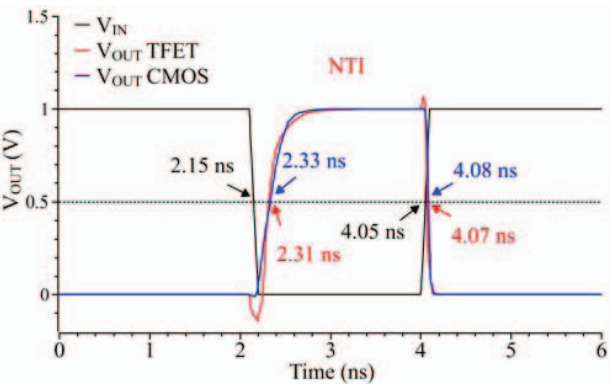
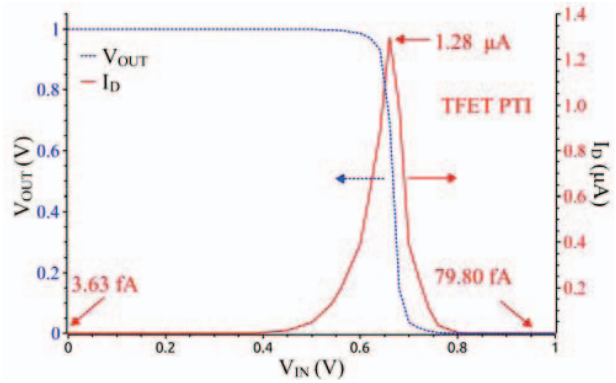
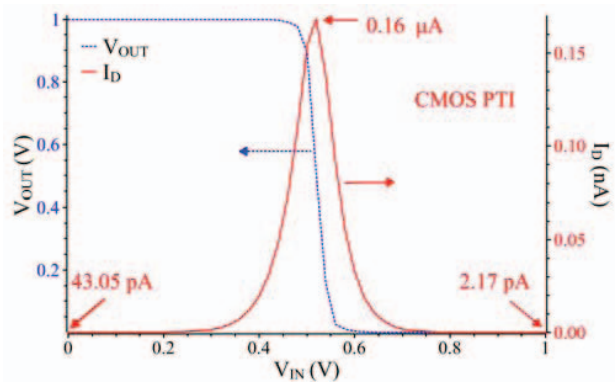


Fig. 10. Comparison of Delay Characteristics TFET vs. CMOS NTI cell.



(a)



(b)

Fig. 11. Static Power Consumption (a) TFET (b) CMOS PTI .

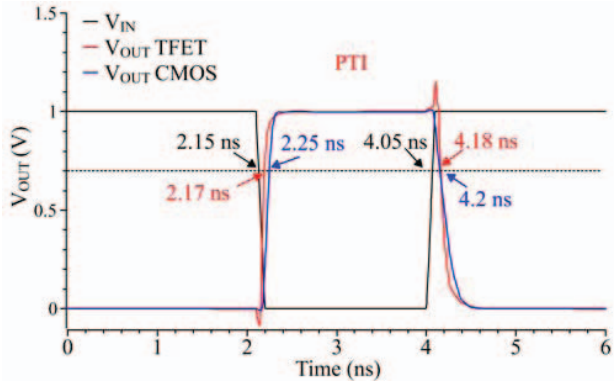


Fig. 12. Comparison of Delay Characteristics TFET vs. CMOS PTI cell.

B. Benchmarking proposed TFET based PTI performance with standard CMOS PTI

The circuit performance of a TFET based PTI logic cell has been compared with CMOS based same circuit at 45 nm technology. The simulation results are shown in Figs. 12 & 11. The average static power consumed in TFET based PTI is 0.041 pW, which is significantly lower than the CMOS based PTI which consumes 22.60 pW, shown in Fig. 11 and listed in Table IV. The PDP of TFET based PTI is 0.31×10^{-23} J,

TABLE III
COMPARISON OF DELAY AND STATIC POWER CONSUMPTION OF TFET AND CMOS BASED NTI

Circuit parameter	*TFET*	*CMOS*
Power supply V_{DD} (V)	1	1
Delay (ns)	0.09	0.11
Average static power (pW)	0.174	73.7
PDP ($\times 10^{-23}$ J)	1.57	810.7
Decrease in PDP	99.81%	

TABLE IV
COMPARISON OF DELAY AND STATIC POWER CONSUMPTION OF TFET AND CMOS BASED PTI

Circuit parameter	*TFET*	*CMOS*
Power supply V_{DD} (V)	1	1
Delay (ns)	0.075	0.13
Average static power (pW)	0.041	22.6
PDP ($\times 10^{-23}$ J)	0.31	293.8
Decrease in PDP	99.89%	

which is only 0.11% of the PDP of standard 45 nm CMOS based PTI cells (293.8×10^{-23} J). Overall decrement in PDP owing to the proposed TFET based PTI logic cell is 99.88%, as summarized in Table IV.

VII. CONCLUSIONS

The proposed LVT & HVT TFETs for low power ternary logic circuits designed in this paper have I_{OFF} at least an order magnitude lower than the MOSFET while I_{ON} is roughly twice the MOSFET at same technology node. The higher I_{ON} make ternary logic circuits operate much faster while lower I_{OFF} leads to significant reduction in static power consumption. The influence of various device parameters have been optimized to improve the electrostatics, leading to better device characteristics and circuit performance. Proper material with appropriate work functions have been optimized in such a way that the LVT & HVT voltage are $V_{DD}/3$ and $2V_{DD}/3$ respectively. The NTI & PTI logic cells have been designed using LVT & HVT TFET devices and compared with analogous CMOS based logic cells. The overall power delay product of TFET based logic cells are much lesser than corresponding CMOS based logic cells. The NTI and PTI cells designed with the proposed LVT & HVT TFETs are excellent starting points for any ternary logic applications

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