A Mismatch Resilient 16-bit 20 MS/s Pipelined ADC

Satyajit Mohapatra[1], Hari Shanker Gupta[2], Nihar R. Mohapatra[1], Sanjeev Mehta[2], Arup Roy Chowdhury[2], Nisha Pandya[3]
1, Department of Electrical Engineering, Indian Institute of Technology, Gandhinagar-382355, India.
2, Space Application Centre, Jodhpur Tekra, Ahemdabad-380015, India.
3, LD College of Engineering, Ahmedabad-380015, India

***Abstract*—In various imaging applications with relaxed Integrated Non-Linearity (INL) requirements, the Commutated Feedback Capacitor Switching (CFCS) technique enables scaling down the sampling capacitors to the thermal limits. The 3.5-bit MDAC architecture combined with CFCS has been envisaged to provide high linearity with power requirement needed for high resolution space imaging applications. In this work, we have discussed various design challenges involved in the design and implementation of the 3.5-bit MDAC with MCS-CFCS architecture. We have proposed various techniques that helps to overcome the linearity constraints at the sub-module, module and chip level. We have designed a 5mm×5mm prototype ADC which consumes 240mW of power (when designed using 1P6M UMC 0.18µm CMOS process). Our design achieves an ENOB of 15.4 bits and FoM of 289 fJ/conversion step. Various design challenges faced during the implementation of the ADC and techniques to overcome them are discussed in details.**

Keywords—Commutated feedback capacitor switching (CFCS), Capacitor Mismatch, Space Imaging Applications, Oxide Gradient.

I. INTRODUCTION

Pipelined ADCs are widely preferred for high speed high resolution space imaging applications [1] and for implementation of cellular base station receivers [2]. Resolving multiple bits (~3-4) in the first stage relaxes the matching requirements of higher stages [2,3] as the non-idealities of higher stages are suppressed by the intermediate gain. It provides area and power advantages in terms of stage scaling [4]. It also makes the stage suitable for multi-bit techniques like Merged Capacitor Switching (MCS) that reduces the number of unit sampling capacitors to half and Commutated Feedback Capacitor Switching (CFCS) which enables sampling capacitor to be scaled to the KT/C limits [3]. Each pipelined stage (refer Fig.1) typically consists of a Sample and Hold (SHA), Sub-DAC (SDAC), Sub-ADC (SDAC) and intermediate residue amplifier (IRA). Each stage operates on orthogonal clock phases $\phi1$ and $\phi2$. During the sampling phase $\phi1$, the analog input V_{IN} is transferred onto the sampling capacitors followed by a coarse digitization by the SADC. During the hold phase, the SDAC is used to approximate the analog value and generate an un-quantized residue. This residue is restored to full scale by the residue amplifier before being transferred to the next stage in the pipeline. The process is replicated by all stages till an N-bit approximate for the analog input is finally generated. Further, the component matching is highly critical for the linearity of converters fabricated in the pipelined architecture. The linearity errors can in general occur at any stage of the conversion process. These are primarily attributed to the non-idealities associated with the SADC (Comparator offset), SDAC (Capacitor Mismatch), IRA (Gain Error) and SHA (Clock Jitter and the Aperture Effects).

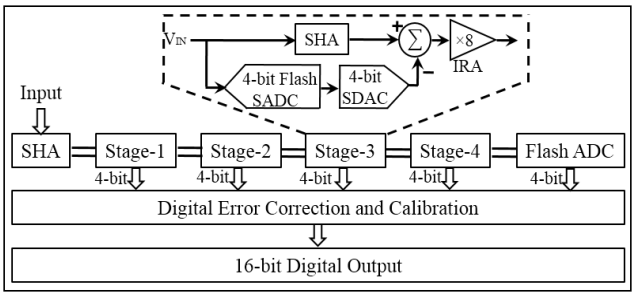


Fig. 1. Architecture of the 16 bit pipelined ADC implemented in this work

Traditionally, the SHA, SDAC and IRA functionalities are implemented by means of a single switch capacitor circuit known as the Multiplying DAC (MDAC) [2,3]. Though such implementation saves power, it limits the resolution to the accuracy of fabricated capacitors. Typically Metal-Insulator-Metal (MiM) and Metal-Oxide-Metal (MoM) capacitors are preferred options for high accuracy data conversion applications. MiM Capacitors are implemented with thin dielectric placed between "capacitor top metal" and the metal layer just below it. However, such capacitors are limited to ~0.1% accuracy and also increases the cost of fabrication because of additional mask requirement [2]. These factors limit the achievable linearity of these converters to ~ 12 bits [2-4].

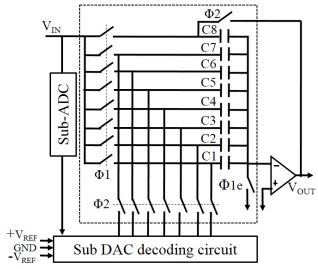
The sampling capacitors of MDAC-1 is typically large in order to suppress various random noise sources (i.e. thermal and random mismatch) below the quantization noise floor. High power amplifier required to drive these capacitors at MHz range result in higher order systematic components across the die. Considering the fact that the capacitance densities of MIM/MOM are much lower [5], MDAC implementation with MIM/MOM capacitors makes the size of the array large [5]. Moreover, accounting for parasitic mismatch due to intensive wiring of unit cells makes the dimension even larger [12]. Consequently the larger arrays induce systematic effects degrading the linearity. The 3D integration of sensitive data converters adjacent to digital chips [4] further makes the array susceptible to hotspot effects. Hence, care needs to be taken at various levels of the design while targeting linearity higher than 16-bit resolution on silicon. In this work, we follow a systematic design methodology and suggested various techniques to overcome the linearity constraints. The design achieves an ENOB of 15.4 and FoM of 289 fJ/conversion step.

The rest of the paper is organized as follows. The mismatch resilient array is discussed in Section II. The design of CFCS decoder is discussed in Section III. The high-speed comparator and high gain OTA design are discussed in Section IV and V. The achieved performance (from post-layout simulations) are presented in Section VI followed by the concluding remarks.

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00071

II. CAPACITOR ARRAY DESIGN

The merged capacitor implementation [3] of the 3.5-bit MDAC requires the total sampling capacitor to be split into 8 highly matched unit capacitors. During the sampling phase ϕ_1, the analog input is stored on these sampling capacitors. Based on the output code of SADC, the sampling capacitors C_1-C_7 are connected to reference voltages $+V_{REF}$, $-V_{REF}$ or GND while the capacitor C_8 is dedicatedly flipped into feedback (Fig. 2).



MCS	C1	C2	C3	C4	C5	C6	C7	C8
0001	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	F/B
0010	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	GND	F/B
0011	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	GND	GND	F/B
0100	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	GND	GND	GND	F/B
0101	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	GND	GND	GND	GND	F/B
0110	$-V_{REF}$	$-V_{REF}$	GND	GND	GND	GND	GND	F/B
0111	$-V_{REF}$	GND	GND	GND	GND	GND	GND	F/B
1000	GND	GND	GND	GND	GND	GND	GND	F/B
1001	$+V_{REF}$	GND	GND	GND	GND	GND	GND	F/B
1010	$+V_{REF}$	$+V_{REF}$	GND	GND	GND	GND	GND	F/B
1011	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	GND	GND	GND	GND	F/B
1100	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	GND	GND	GND	F/B
1101	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	GND	GND	F/B
1110	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	GND	F/B
1111	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	F/B

Fig. 2. The MCS implementation of 3.5bit MDAC and switching sequence.

The random mismatch could be suppressed by making the capacitors large. But, the large capacitors consume more power and are susceptible to systematic effects. In this work, each of the 8 capacitors are divided into 8 sub-units and smartly distributed over an 8×8 array to compensate for the systematic errors arising due to process and temperature variations. The gradient errors ξ across array is generally modelled as (1) [6-9].

$$\xi(x, y) = k_{00} + k_{10}.x + k_{01}.y + k_{20}.x^2 + k_{02}.y^2 + k_{11}.xy + \ldots \quad (1)$$

Here, $k_{i,j}$ represent the coefficients associated with profile $x^i y^j$. The additional effects such as local hotspots, edge effect variations and metal coverage need to be considered while designing the array. It is very challenging for any arraying technique to meet all these requirements simultaneously. Traditional placement techniques [6-9] for MDAC implementation show certain shortcomings that needs to be addressed. They are optimized for one or a few of above discussed effects but not all of them together. More importantly, most of them do not compensate for localized gradients and hotspots that arise during integration of sensitive data converters adjacent to digital dies. The array that we have implemented in this work is a modified form of [4]. The implemented array is illustrated in Fig. 3 (left). The CFCS calibration decoder switches are integrated on either side of the MDAC capacitor array as shown in stage layout Fig. 3 (right).

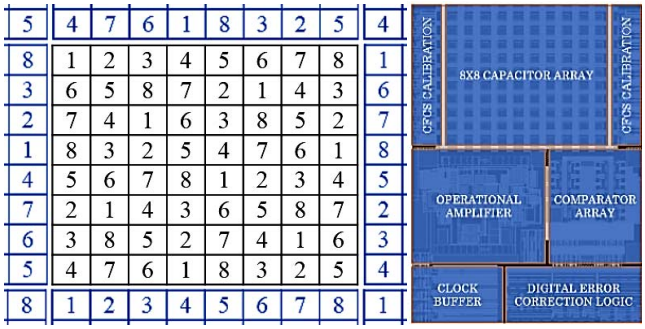


Fig. 3. The implemented array (left) and the integrated stage layout (right).

The rows and columns of the array contains units of all the capacitors. Each quadrant and sub-quadrant have equal number of units of all capacitors. More importantly, any capacitor is surrounded by all other capacitors other than itself which helps to cancel the local gradients and hotspots. For larger capacitors the array can be extended by placing 4 arrays adjacently. In such a case the capacitors at the opposite edges becomes neighbours. Keeping this in mind, the array is designed in K-Map fashion. The capacitors with errors are represented as $C_i = C(1+ \varepsilon_i)$ where, C is the ideal value of capacitor and ε_i is the fractional mismatch associated with the i^{th} capacitor. The linearity errors in MCS-CFCS are directly proportional to the mismatch coefficients, $\Delta\varepsilon$ [3]. Hence, the worst mismatch ε_{max} (defined as maximum of ε_i) is used for verifying effectiveness of the array. The performance of array is compared with the existing techniques [6-9] and the data is summarized in Table. I.

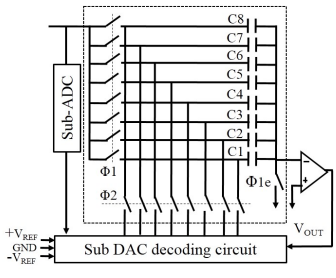
TABLE I. THE PERFORMANCE OF ARRAY TO VARIOUS ERROR PROFILES

Gradient:	X+Y	X^2+Y^2	XY	Joint	Local	Edge
×0.1 %	Linear	Quad.	Rotated	Profile	hotspot	tolerant
This Work	0	0	0.10	0.02	0.06	✓
Work [6]	0	0	0.43	0.10	0.19	✓
Work [7]	0	0.6	0	0.15	0.19	✗
Work [8]	0	0	0.43	0.10	0.19	✓
Work [9]	0	0	0.10	0.02	0.19	✓

Since the array is designed considering both systematic as well as random effects and hotspot, the unit capacitor sizes can be scaled further. This will lead to smaller array dimensions along with power advantages. The array is immune to local hotspots and edge effects that are likely to occur during 3D integration of chips [10]. Any residual mismatch between the unit capacitors is further addressed by digital error correction and calibration implementation described in further sections.

III. CFCS DECODER DESIGN

The implementation of CFCS on top of the MCS architecture necessitate a decoder for generating the complex feedback capacitor commutation patterns as shown in Fig. 4a. Unlike 1.5-bit decoder, the design of decoder [4] for 3.5-bit MDAC is challenging. We transformed the original commutation sequence into a new sequence without affecting principle of operation (refer Fig. 4b). Such transformation has helped to minimize the delay involved in decoder logic circuitry. It also helped in decoder realization with minimum number of gate count and die area. The 3.5-bit decoder logic circuit and its layout are given in Fig. 5(a) and (b) respectively.



CFCS	C1	C2	C3	C4	C5	C6	C7	C8
0001	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	F/B
0010	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	F/B	GND
0011	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	F/B	GND	GND
0100	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	F/B	GND	GND	GND
0101	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	F/B	GND	GND	GND	GND
0110	$-V_{REF}$	$-V_{REF}$	F/B	GND	GND	GND	GND	GND
0111	$-V_{REF}$	F/B	GND	GND	GND	GND	GND	GND
1000	F/B	GND	GND	GND	GND	GND	GND	GND
1001	$+V_{REF}$	F/B	GND	GND	GND	GND	GND	GND
1010	$+V_{REF}$	$+V_{REF}$	F/B	GND	GND	GND	GND	GND
1011	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	F/B	GND	GND	GND	GND
1100	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	F/B	GND	GND	GND
1101	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	F/B	GND	GND
1110	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	F/B	GND
1111	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	F/B

Fig. 4. The 3.5bit decoder architecture (left) and modified switching (right).

Based on the modified sequence, reference selection signals V_{CN}, V_{CP} and V_{CZ} are derived from output of the 15 differential SADC comparators (T_1- T_{14}). The feedback generation signals (A_1- A_{15}) are generated subsequently by passing the output of adjacent comparators T_N and $T_{(N-1)B}$ through an AND logic. The A_i, A_j then represent complementary differential feedback generation signals. These are used to generate the flip enable signal V_{FPS} that throws a capacitor into feedback based on the decoding logic. Note that the V_{FPS} signal overrides a capacitor being earlier connected to ground during merged switching, as the generation of V_{CZ} now additionally requires V_{FPS} to be low. Finally the V_{FPS} is gated via G_3 to ensure that the feedback action happens only at onset of ϕ_2. Here, one critical observation is that since differential capacitors are flipped simultaneously, negative side logic can simply be realized by interchanging i/p pins V_{REF+} and V_{REF-} of the decoder module.

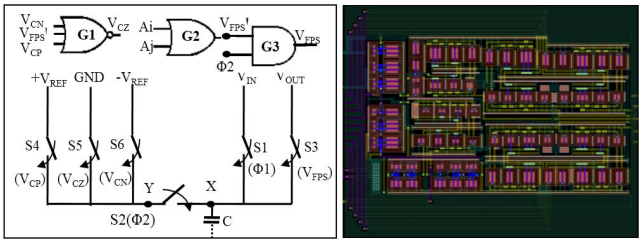


Fig. 5. (a) The 3.5bit CFCS decoder logic implementation (b) and its layout.

The decision made by the decoder needs to be fast enough so that switched references are settled till 16-bit accuracy prior to residue generation. The proposed logic circuit consumes an additional delay of 2 logic gates (G2, G3) on top of the 3.5-bit MCS decoder that lies well within non overlap period. Since all the elements are accessible from any side of array it is convenient to implement calibration options. The array is shielded with grounded Metal-3 plate while horizontal and vertical routings are run on M2 and M4 for noise isolation. The calibration blocks are suitably placed at opposite edges of the array. Dual NP guard rings are used to isolate the array from calibration switches and radiation hardening purposes. The decoder and array consume area of $60\times60\mu m^2$ and $0.7\times0.8mm^2$ respectively when realized in 1P6M UMC180 CMOS process.

IV. High Speed Comparator Design

The design of comparator topology for high speed applications involve tradeoff between achievable accuracy, speed and power. For the case of 3.5-bit MDAC, 15 differential comparators are needed to implement the 4-bit SADC. Based on the residue output of the previous stage, a fast decision needs to be made within a short non-overlap period. The topology of comparator incorporated in our design is shown in Fig. 6. It consists of a comparison stage followed by inversion and latch. Here, the transistors M_1-M_4 serve as discharge control transistors, that are connected to flip flop structure formed by the cross coupled inverter pairs (M_6, M_9, and M_7, M_{10}). The transistors M_5 and M_8 serve as the pre-charge transistors. The inverter pairs formed by M_{11} -M_{14} serve as output drivers. Both the latches are strobed at the drain terminal rather than the source. This is advantageous in terms of regeneration speed and offset. The transient response of the comparator excited at ±100 μV close to the reference voltage is

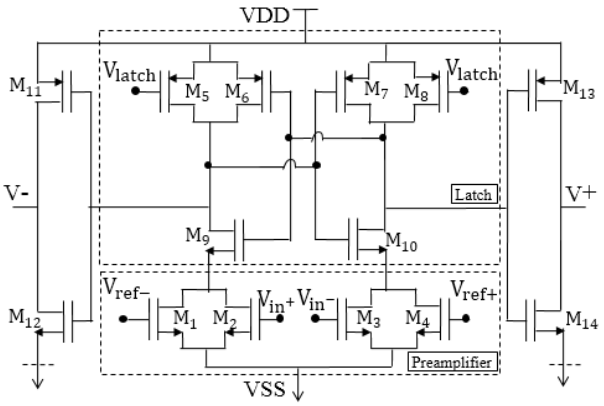


Fig. 6. Architecture of high speed differential latch comparator implemented

shown in Fig. 7a and 7b. As opposed to the 1.5-bit architecture, the amount of offset that can be tolerated and compensated via redundancy in the error correction module is significantly reduced (~ 4X) for the 3.5-bit case. Therefore the offset simulations at process corners is critical for the on chip performance. The post layout simulation of comparator yields an offset of 0.2μV at its input. The array of 15 comparators consume total area of 0.3mm×0.3mm in each stage when realized in 1P6M UMC180 CMOS process. These are guarded with dual NP guard rings to avoid latch-up and provide radiation hardening. It also eliminates any possible crosstalk with the adjacently placed high gain amplifier module (OTA).

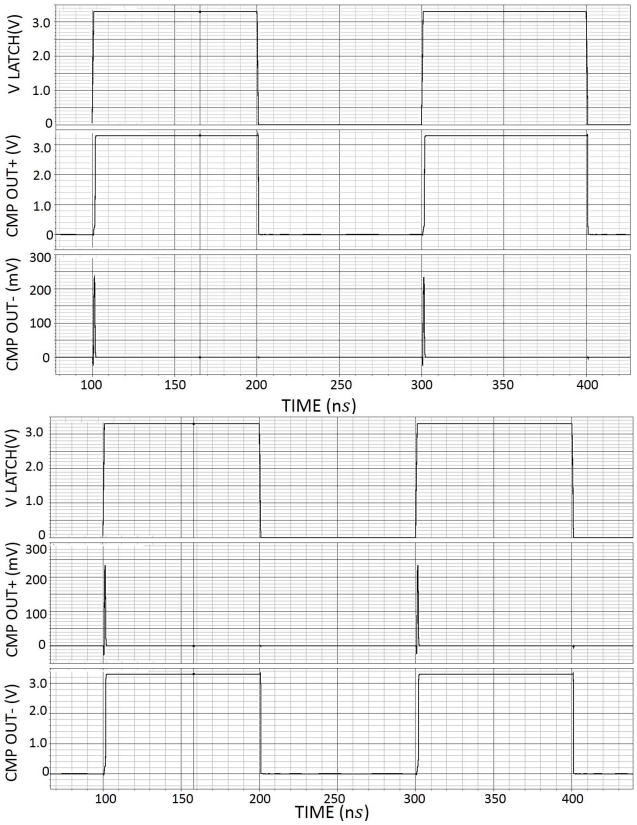


Fig. 7. The graph showing the response of designed comparator to a differential input, (a) 100μV above reference and (b) 100μV below reference.

V. High Gain Amplifier Design

It is challenging to meet the stringent design requirements of the OTA for a 3.5-bit MDAC. The open loop gain of IRA influences the precision in closed loop. The closed loop gain error (1/Aβ) arising due to finite output impedance must be limited to 1/4 LSB. This demands an open loop gain of ~120 dB with considerable margin for fabrication. Similarly, to meet settling time within 50ns (F_S=10 MHz), the unity gain bandwidth of the OTA needs to be higher than 240MHz. The differential gain boosted folded cascode topology (refer Fig. 8) is incorporated in this chip to meet the critical gain and bandwidth requirements along with a rail to rail swing of ±2V.

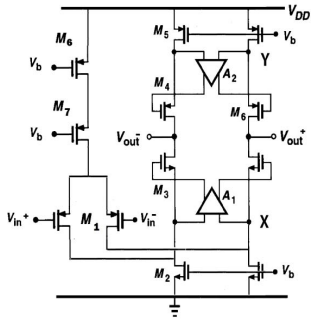


Fig. 8. Topology of main stage OTA implemented with gain boosting stages.

The addition of boosting stages introduces a pair of pole zero doublet [11] that typically results in a long settling tail. In our design, the selection of tail current and optimal sizing of transistors helped in avoiding doublet degradation of transient response. The optimal choice of tail current ratio [11] between main and the boost amplifiers helped in pushing the pole zero doublet pair far beyond the unity gain bandwidth (UGB) frequency of the amplifier to achieve desired linearity and phase margin. The layout of the designed OTA is shown in Fig. 9. A 2-dimensional common centroid approach is adapted for implementing highly matched input transistors of the OTA. Any degradation in OTA gain within certain limits can further be addressed by the implemented digital gain error correction and calibration support. The frequency response, transient settling response and input referred spectral noise density of the designed high gain OTA is shown in Fig. 10, Fig. 11 and Fig. 12 respectively. The designed amplifier achieves a high gain of 140 dB and UGB of 255 MHz. Certain necessary post layout optimizations are carried out to achieve better matching. The post layout results of the amplifier is presented in Table.II.

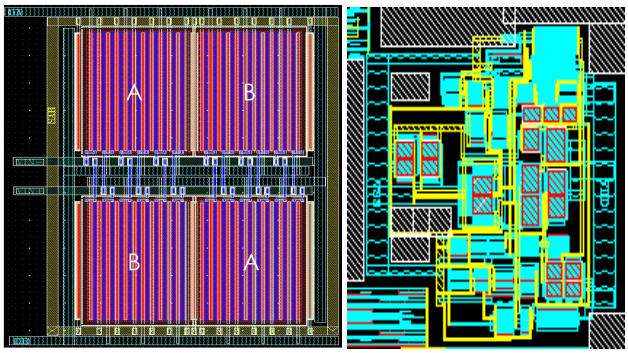


Fig. 9. (a) common centroid layout of i/p transistor (b) complete OTA layout

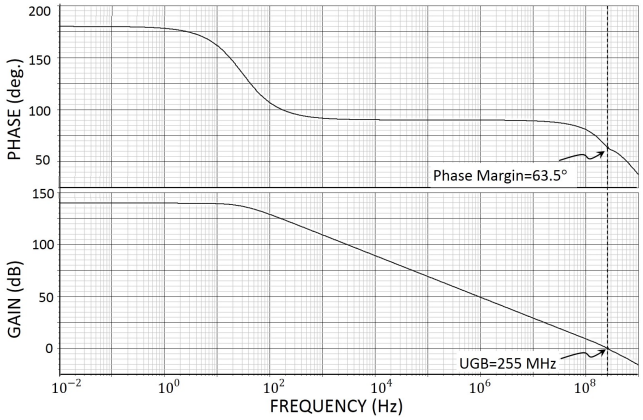


Fig. 10. Frequency response of gain boosted OTA implemented in MDAC-1

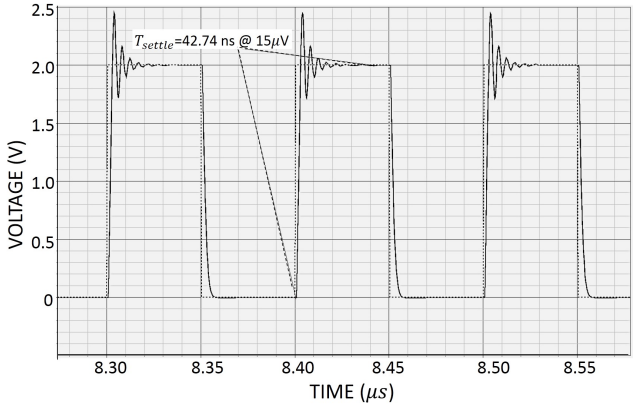


Fig. 11. Settling response of designed amplifier to worst case input (V_{IN}=2V)

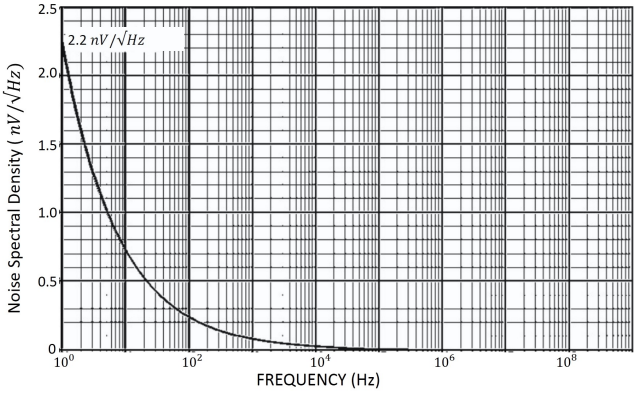


Fig. 12. Input reffered spectral noise density for designed high gain amplifier

TABLE II. Postlayout Performance of Gain Boosted Amplifier

No.	Parameter	Requirement	Achieved
1.	DC Gain	120 dB	139.7 dB
2.	UGB	240 MHz	255 MHz
3.	Phase Margin	60°	63.5°
4.	Settling @ 15µV	50 ns	41.8 ns
5.	Output Swing	2V p-p	2.1 V p-p
6.	Power	40 mW	31 mW
7.	Load Capacitor	10 pf	12 pf
8.	Spectral Noise	15 µV	2.2 nV

VI. Simulation Results & Discussion

The residual nonlinearity (INL) resulting from the 4-bit SDAC (integrated array and modified switching scheme) is shown in Fig. 13. It is observed that accumulation of systematic error is avoided as the INL is pulled back to zero at regular intervals. This resulted in 3rd harmonic suppression [8] at output of the converter thus improving dynamic linearity.

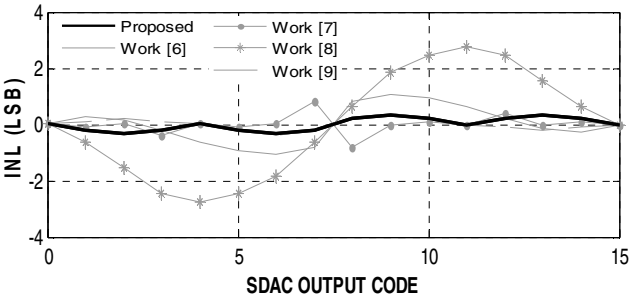


Fig. 13. The comparision of Sub-DAC nonlinearity with various techniques.

The speed of SADC is highly dependent on the settling response of differential comparator array and the implemented thermometer to binary decoder. The post layout response of the SADC to 1624.8 mV differential input is shown in Fig. 14. As seen, fast settling and minimal delay to clock edge is achieved.

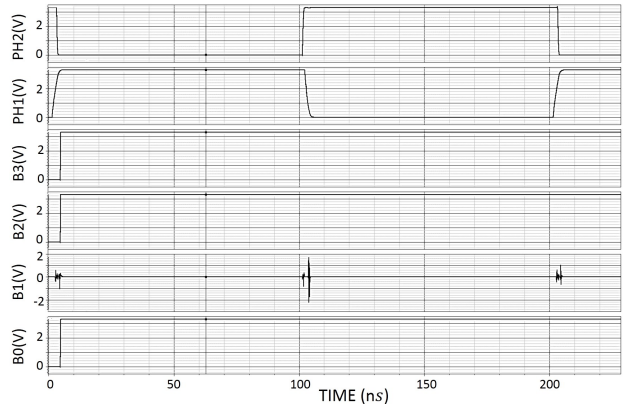


Fig. 14. Sub-ADC settling response to test differential input (Vin=1624.8 mV)

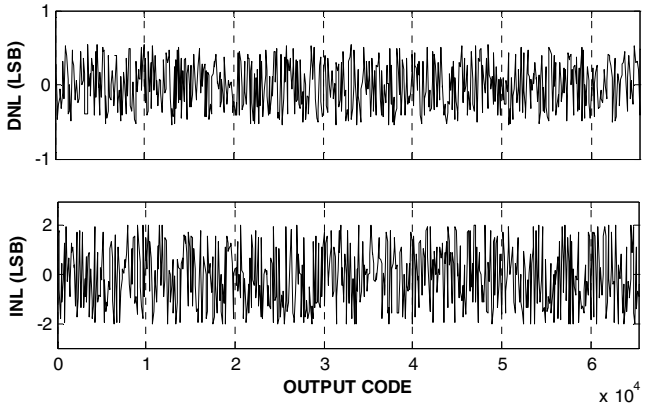


Fig. 15. DNL (top) and INL (bottom) plot obtained from integrated ramp test

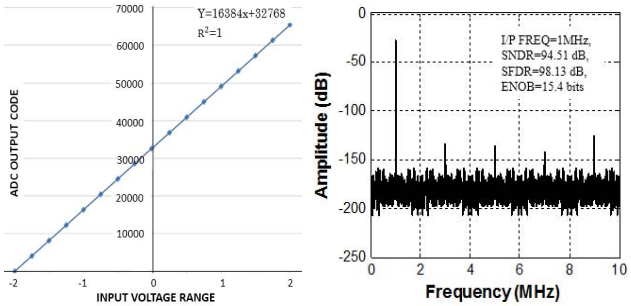


Fig. 16. (a) Code inearity fit test (b) FFT spectrum at Fs=20MHz, Fin=1MHz.

The linearity parameters, INL and DNL obtained from integrated ramp test is shown in Fig. 15. The ADC achieves a DNL of ±0.5 LSB and INL of ± 2 LSB. The linearity of the ADC is tested at full sampling rate of 20MHz and input signal range of 1MHz. The output spectrum is shown in Fig. 16b. As shown, SNDR of 94.5 dB and SFDR of 98.13dB are achieved. The achieved linearity specifications are further verified through regression testing and linearity fit as shown in Fig.16a.

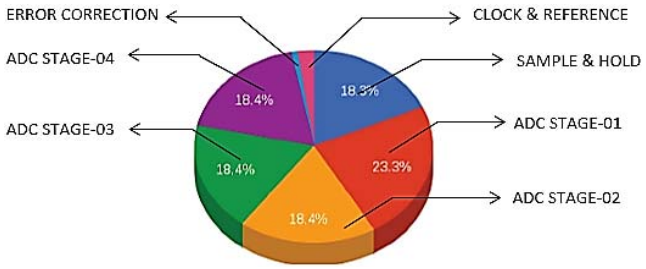


Fig. 17. An overview of the power consumption in various stages of the ADC

The power budget of the designed ADC is shown in Fig. 17. Due to higher settling requirements (15µV) and linearity, a significant portion of power is spent in dedicated sample and hold amplifier (SHA). We have verified through simulations that the SHA less topologies can be implemented at 20 MS/s throughput. However, it is not implemented in the current design since we need a design which will work even under harsher environments (like in space). The capacitors could have been aggressive scaled by 8X to leverage the complete power advantage of a 3.5-bit stage but, we have kept the scaling factor low from a conservative design aspect. An overview of achieved performance is summarize in Table- III.

TABLE III. Summary of Post Layout Performance of the ADC

No.	Parameter	Specification
1.	Resolution	16 bit
2.	Speed	20 MHz
3.	Input range	± 2V p-p
4.	LSB step Size	61 µV
5.	Power	250 mW
6.	DNL	± 0.5 LSB
7.	INL	± 2 LSB
8.	Spectral Noise	2.2 nV/Hz$^{0.5}$
9.	Figure of Merit	0.3 pJ/step
10.	Power Supply	3.3V/1.8V
11.	Die Area	5mm×5mm
12.	Latency	5.5 clock cycle

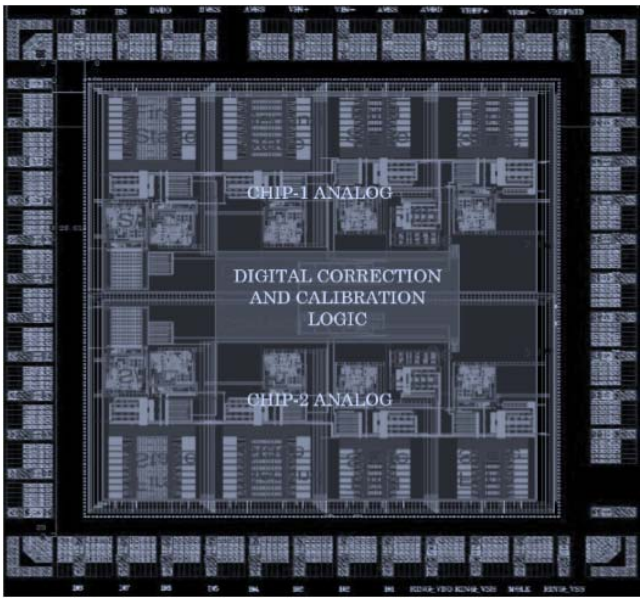


Fig. 18. Complete layout of ADC realized in 1P6MUMC 0.18µm cmos process

Fig.18 shows the layout of complete chip (realized in 1P6M UMC 0.18µm CMOS process). It consists of two interleaved ADC cores to achieve a sampling rate of 20MS/s. Each ADC core occupies an area of 500×240µm2. The chip consumes a power of 240mW at a throughput rate of 20MS/s. It uses separate supply voltages for analog and digital modules (i.e. 3.3V for analog and 1.8V for digital). It is intended to quantize the output from hybrid IR photo-detectors on focal plane array (FPA), bump-bonded to the silicon readout integrated circuit chip. The digital section of the chip, particularly the calibration module and IRA are heavily guarded by dual rings for radiation hardening purposes. The capacitor arrays are shielded by intermediate metal layers (Metal-3) held at analog ground.

TABLE IV. A COMPARATIVE OVERVIEW OF PERFORMANCE ACHIEVED

Parameter	Res. (bits)	Speed (Ms/S)	Power (mW)	ENOB (bits)	F.O.M (fJ/step)	Tech. (nm)
Proposed	16	20	250	15.4	289	180
Work [12]	12	20	56.3	11.8	780	350
Work [13]	10	125	20	9.26	270	65
Work [14]	13	125	134	11	610	65
Work [15]	12	10^4	2900	8.84	631	28

The performance of the designed ADC is summarized in Table-IV and compared with the existing works [12-15]. Our design achieves an effective linearity (ENOB) of 15.4. it also achieves high energy efficient figure of merit (FoM) of 289fJ/conversion. The capacitors of later stages are not scaled aggressively to provide sufficient margins for fabrication. Thus, there exist a scope to achieve better FoM while keeping the linearity intact. Though integrated post-layout simulation results are presented here, by virtue of high dispersion achieved by the array (Section-II) it is envisaged that the process gradients during fabrication can effectively be handled.

VII. CONCLUSION

To summarize, we discussed the design and integration challenges to implement a 16-bit pipelined ADC with 3.5-bit/stage architecture. A mismatch resilient arraying technique for implementation of the 3.5-bit MDAC with MCS-CFCS architecture was discussed. The structure attained maximal dispersion to compensate for both systematic as well as random errors. This consequently allows further scaling down of sampling capacitors leading to smaller array dimension and lower power. CFCS calibration on top of merged switching was implemented to implement an accurate SDAC. A modified switching sequence was strategically used to implement a fast CFCS decoder. Amplifiers with gain of 140 dB and unit bandwidth of 255 MHz were implemented to achieve highly linear residue amplification. The designed ADC has an area of 5mm×5mm and consumes only 250mW power when realized in 1P6M UMC 0.18µm CMOS process. With certain post layout corrections, the test chip achieved an effective linearity of 15.4-bits and FoM of 0.3 pJ/conversion step. The proposed technique has potential application in high performance data converters for mobile communications and space applications where the linearity as well as energy efficiency are at priority.

REFERENCES

[1] T. Yasue, et al. "A 33Mpixel CMOS imager with multi-functional 3-stage pipeline ADC for 480fps high-speed mode and 120fps low-noise mode." Solid-State Circuits Conference-(ISSCC), pp:90-92 IEEE, 2018.

[2] I.Ahmed, et.al "An 11-bit 45 MS/s pipelined ADC with rapid calibration of DAC errors in a multibit pipeline stage." IEEE JSSC, vol.43.7, 2008.

[3] S.M. Yoo, Jong-Bum Park, S. H. Lee, and Un-Ku Moon "A 2.5-V 10-b 120-MSample/s CMOS pipelined ADC based on merged-capacitor switching." IEEE TCAS-II , Express Briefs, vol. 51.5, pp:269-275, 2004

[4] S. Mohapatra, H. S. Gupta, and N. R. Mohapatra. "Mismatch Resilient 3.5-Bit MDAC with MCS-CFCS." IEEE Computer Society Annual Symposium on VLSI (ISVLSI) Hong Kong. pp. 175-180 , July 8, 2018.

[5] P. Y. Chiu P. Yen, and M. Ker. "Metal-layer capacitors in the 65 nm CMOS process and the application for low-leakage power-rail ESD clamp circuit." Microelectronics Reliability Vol 54.1, pp: 64-70, 2014.

[6] D. C. Reynolds, "MOS current source layout technique to minimize deviation." U.S. Patent No. 5,568, 145. 1996. Asignee: Analog Devices.

[7] D. Mercer, "Current Steering D/A Converters", Analog Devices,2014 https://wiki.analog.com/university/courses/tutorials/cmos-dac-chapter.

[8] G. S. Ostrem, "Current source array for high speed, high resolution current steering DACs." U.S. Patent 6,720,898. Washington DC, 2004.

[9] J. Deveugele, et al. "A gradient-error and edge-effect tolerant switching scheme for a high-accuracy DAC." IEEE, TCAS-I 51.1, 191-195, 2004.

[10] A. Zjajo, "Temperature Effects in Deep Submicron CMOS" Stochastic Process Variation in Deep-Submicron CMOS.pp. 83-115.Springer, 2014

[11] K. Bult and G. Geelen. "The CMOS gain-boosting technique," Analog Integrated Circuits and Signal Processing, vol.1.2 . pp. 119-135. 1991.

[12] J. Yuan, et al. "A 12-bit 20 MS/s 56.3 mW pipelined ADC with interpolation-based nonlinear calibration." IEEE TCAS-1: 59.3, 2012.

[13] P. N. Singh, et al. "20mw, 125 msps, 10 bit pipelined adc in 65nm standard digital cmos process." IEEE CICC, conf., pp: 189-192, 2007.

[14] C. Erdmann, D. Lowney, A. Lynam, A. Keady, J. McGrath, E. Cullen, D. Breathnach, et al. "A heterogeneous 3D-IC consisting of two 28 nm FPGA die and 32 reconfigurable high-performance data converters." IEEE Journal of Solid State Circuits, vol. 50.1, pp: 258 -269, 2015.

[15] S. Devarajan, L. Singer, D. Kelly, T. Pan, J. Silva, J. Brunsilius, R. L. Daniel F. Murden et al. "A 12-b 10-GS/s Interleaved Pipeline ADC in 28-nm CMOS Technology." IEEE JSSC vol.52.12, pp.3204-3218, 2017.