MOS Varactor RO architectures in Near Threshold Regime using Forward Body Biasing techniques

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***Abstract*— Due to small output swings and series stack transistors, Differential Ring Oscillators (DRO) and current starved ROs are not well suited for Near Threshold Voltage (NTV) regime. MOS varactor based Single Ended Ring Oscillators (SERO) is well suited in NTV regime as it gives full swing characteristics, wide tuning range and has very low power consumption. This paper proposes different architectures using MOS Varactor SERO (VBRO) that gives high oscillation frequency, wide tuning range, low area and power consumption without degrading the phase noise as compared to existing VCO topologies in NTV regime. The improvement in the tuning range of the VCO is because of the change in body capacitance of the DTMOS configuration used in the VBRO. The change in the center frequency with PVT variations is compared with that of an NTV DRO. Post layout simulations have been performed on parasitic extracted netlist using HSPICE in industrial 65nm CMOS Process Design Kit (PDK). Our VBRO architecture has tuning range of 0.425 - 2.13 GHz with phase noise of -95dBc/Hz at 0.6V supply. The power consumption is only 127µW and the Figure Of Merit (FOM) is 164.96dBc/Hz.**

***Index Terms*—Near threshold voltages, MOS Varactor, forward body biasing, Process-Voltage-Temperature variation, ring oscillator.**

I. INTRODUCTION

Ring Oscillators (ROs) are mainly used in systems on chip (SOCs) for clock signal generation, PLL based frequency synthesis, in clock recovery circuits and in A/D conversion. LC VCO provides high-noise rejection but requires very large chip area limiting its applicability. RO VCOs are being actively considered because of their relatively wide tuning range, small area, lower power consumption, much less coupling to and from other circuits [1], and multiple phase output generation. Low voltage or near threshold circuits are used for internet of things (IoT) and ultra low power applications such as biomedical systems, energy harvesting systems, etc. DROs are used mainly to suppress the noise using tail current transistor and, therefore, these have the advantage of phase noise cancellation and even phase outputs. However, in NTV regime, DROs [3]-[4], [5] and current starved ROs face limitations due to series-stack transistors. Pseudo DROs [2], [6] are used in NTV regime but they lose the advantage of common mode noise rejection. DROs in NTV regime restrict VCO output frequency range and frequency dependence on PVT variations. Since PVT variations have a direct impact on oscillation frequency, a wide tuning range should be provided by VCO at NTV regime. MOS varactor based VCOs (VBRO) are now being explored for NTV regime as they overcome the problem of series-stack transistors, rail to rail swing, low area and power consumption. Another advantage of the circuit is that for a given power consumption, varactors cause least degradation in phase noise [7] as compared to the current starved topology. However, in a conventional VBRO the varactor transistor remains mostly in deep depletion region, limiting the tuning range in NTV regime. This paper presents a new forward body biasing (FBB) based architectures [2] of VBRO that improve the performance parameters in NTV regime. This paper is organized as follows: Section II presents performance parameters and MOS varactor capacitance analysis of a VBRO. Section III presents proposed VBRO architectures and a performance comparison is made with other low voltage structures. Section IV presents the variation of the centre frequency with the PVT variation. A comparison is done of the proposed VBROs with the existing architectures. Finally conclusions are drawn on Section V.

II. CONVENTIONAL MOS VARACTOR BASED SERO

In this section, we discuss the conventional VBRO (Fig. 1) performance parameters. The dependence of varactor capacitance on these parameters is studied for different control voltages. We use the analysis to understand and improve the design parameters of the new FBB based VBRO.

A) Performance Parameters:

1) Oscillation Frequency: For an N-stage CMOS ring oscillator, the frequency is given as

$$f = \frac{1}{2Nt_d} \tag{1}$$

where t_d is average of rise time and fall time of each stage given as

$$t_d = \frac{C_{total} * V_{DD}}{I_{eff}} \tag{2}$$

where I_{eff} is the effective switching current [8] of the inverter in a VBRO. In a VBRO the total capacitance at the oscillating node is the sum of inverter's gate (input) and parasitic (output)

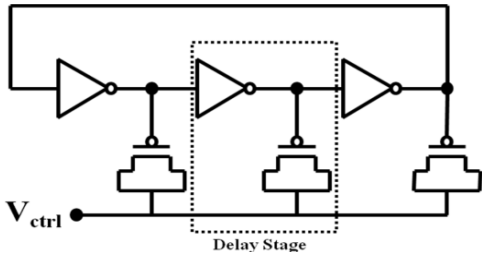

Fig. 1. Conventional Varactor based ring oscillator (VBRO).

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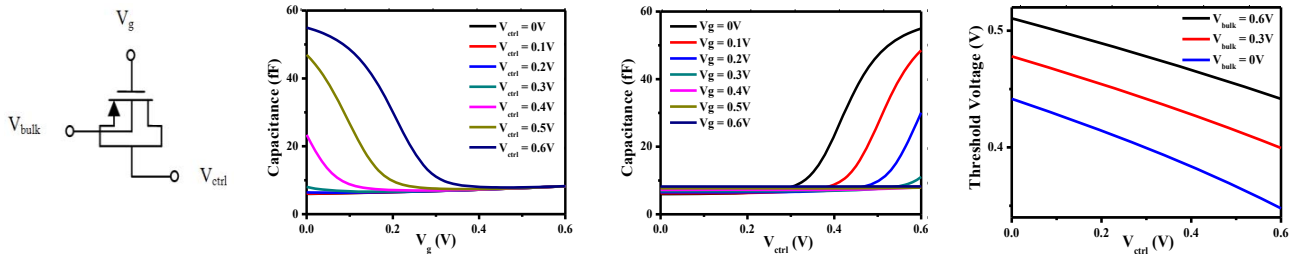


(a) (b) (c) (d)

Fig. 2. (a) PMOS varactor (D-S as Vctrl), (b) C-V characteristics of varactor at different control voltages, (c) C-V characteristics of varactor at different gate voltages, (d) Threshold voltages at different bulk voltages

capacitance (C_{inv}) and varactor capacitance (C_{var}) and is given by,

$$C_{total} = C_{inv} + C_{var} \quad (3)$$

where

$$C_{inv} = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{gfn} + C_{gfp} \quad (4)$$

$C_{gdn,p}$: Gate-drain capacitance of NMOS (PMOS)
$C_{dbn,p}$: Drain-bulk diffusion capacitance of NMOS (PMOS)
$C_{gfn,p}$: Gate capacitance of next stage NMOS (PMOS)

2) Tuning Range: In VBRO the tuning range depends on the ratio of the maximum to minimum capacitance (C_{max}/C_{min}) of the varactor. However, the value of C_{inv} should be as small as possible to achieve high tuning range. The value of varactor capacitance changes with control voltage V_{ctrl} when it operates in moderate inversion and depletion regimes. The varactor capacitance is almost constant when it operates in strong and deep depletion regions. So the ratio (C_{max}/C_{min}) can be increased by changing the threshold voltage of the transistor.

3) Phase Noise: Phase noise of single ended ring oscillator reduces by lowering the threshold voltage [9] and keeping same rise and fall time (symmetric transitions). Also by keeping size of PMOS and NMOS device same gives low-flicker-noise-induced phase noise [7]. The figure of merit for a VCO is given as

$$FOM = L\{\Delta\omega\} + 10\log\left(\frac{P_D}{1mW}\right) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) \quad (5)$$

where

ω_0 = oscillation frequency

P_D = power dissipation

$L\{\Delta\omega\}$ = phase noise at 1MHz offset frequency

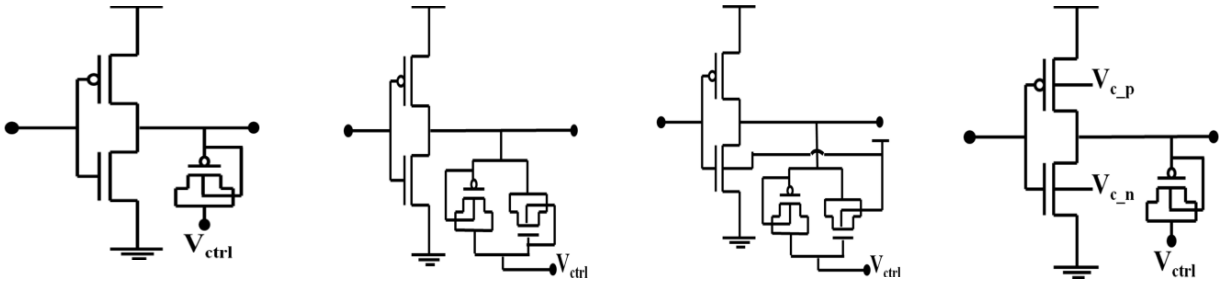
B) MOS varactor capacitance analysis:

The varactor in a VBRO (Fig. 1) is implemented using a PMOS transistor. In this paper we implement all the circuits using STMicroelectronics 65nm CMOS PDK. The varactor is realized using a transistor with three terminals: gate, drain-source connected (D-S) and bulk terminal [10] as shown in Fig. 2(a). In a conventional VBRO V_{bulk} = VDD. For a given control voltage, the varactor capacitance C_{var} varies with the gate voltage (oscillating node), and therefore assumes an average value for a given control voltage. Fig. 2(b) shows the capacitance variation of the varactor at different gate voltages. The transistor moves into deep depletion region with an increase in gate voltage, resulting in an almost constant value of C_{var}. This is the main drawback of the conventional VBRO. Fig 2(c) show the varactor capacitance variation with the control voltage at different gate voltages. The figure shows that for small values of control voltages the varactor capacitance is almost constant ($C_{max}/C_{min} \approx 1$) with gate voltage variation. Fig. 2(d) shows the threshold voltage at different V_{bulk}.

III. PROPOSED MOS VARACTOR BASED SERO ARCHITECTURES

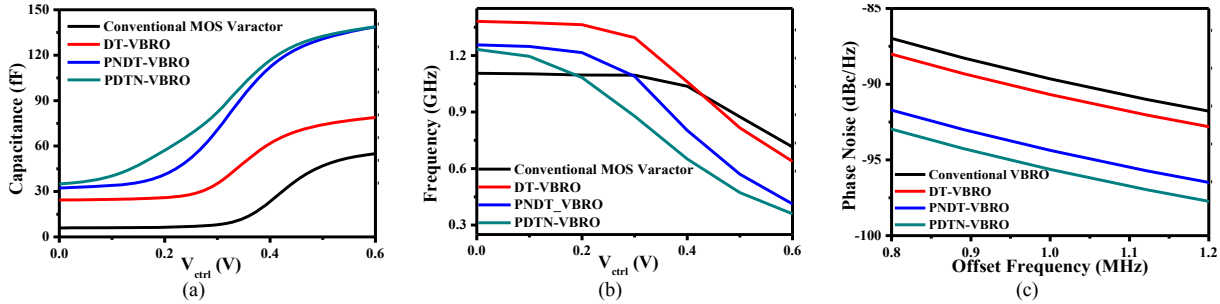
The conventional VBRO in NTV regime faces the problem of the PMOS varactor going into depletion region for small values of V_{ctrl}. Due to this, the varactor capacitance remains constant and the hence the VBRO oscillation frequency, as shown in Fig. 4(a) and Fig. 4(b) respectively. We propose new architectures of VBRO suitable for NTV regime, as shown in Fig. 3. The motivation for these designs is to reduce the threshold voltage of the varactor so that it is not driven into deep depletion for small values of V_{ctrl}. The second motivation is to vary the varactor capacitance as linearly as possible. This will give the linear tuning range (linear VCO gain) of a ring oscillator. The proposed architectures overcome the problem of constant varactor capacitance and improve the performance of a VBRO.

1. DT-PMOS Varactor SERO (DT-VBRO): Instead of using Inversion MOS (IMOS) as varactor [10], in this configuration, we use Dynamic-Threshold-MOS (gate and bulk shorted). The delay stage of a DT-VBRO is shown in Fig. 3(a). In this design the bulk voltage will vary with the gate voltage due to which the transistor will operate mostly with a forward body bias. This will reduce the threshold voltage for V_g not equal to VDD. Therefore the varactor MOS moves into depletion for higher values and/or lower value of V_{ctrl} as shown in Fig. 4(a). The figure show that the capacitance curve shifts towards left when compared to conventional MOS varactor. The oscillation frequency of a 3-stage DT-PMOS varactor SERO is shown in Fig. 4(b). The figure show an increase in tuning range and linear VCO gain as compared to conventional MOS varactor. Fig. 4(c) shows the phase noise of different VBRO architectures at 1MHz offset frequency. This configuration gives a better phase noise when compared with the conventional VBRO. This is because of the increase of average varactor capacitance in the total capacitance of an oscillating node. The varactor capacitance now also includes the body



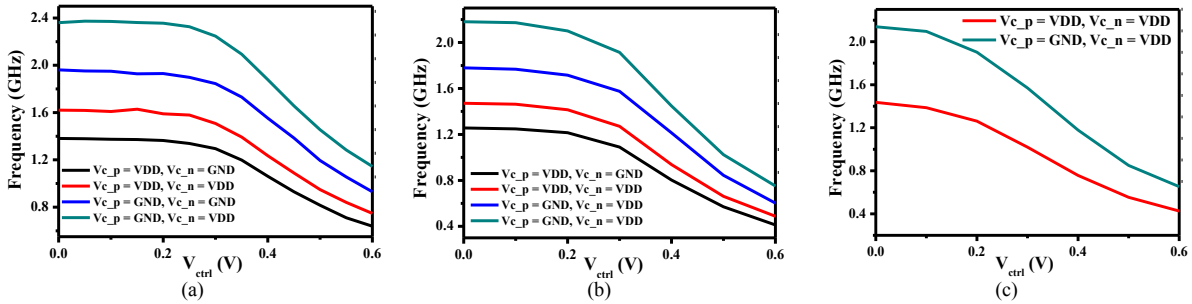
(a) (b) (c) (d)

Fig. 3. Delay stage of different architectures (a) DT-VBRO, (b) PNDT-VBRO (possible in twin tub technology), (c) PDTN-VBRO, (d) Inverter transistor bulk voltages for coarse tuning



(a) (b) (c)

Fig. 4. (a) C-V_{ctrl} characteristics of different architectures, (b) Tuning range of different architectures, (c) Phase noise curve of different architectures at 1MHz offset frequency



(a) (b) (c)

Fig. 5. Frequency curve for inverter bulk as coarse tuning (a) DT-VBRO, (b) PNDT-VBRO (possible in twin tub technology), (c) PDTN-VBRO

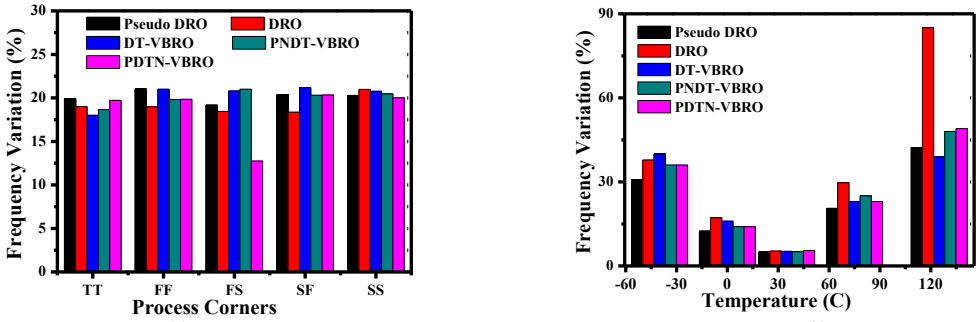
capacitance of mosfet in addition to the gate capacitance. The analysis show that DT-VBRO have around10% increase in oscillation frequency with more than twice the increase in the tuning range as compared with the conventional VBRO in NTV regime.

2. DT-PMOS and reverse DT-NMOS varactors in parallel (PNDT-VBRO): The PMOS and NMOS transistors have reverse capacitance behavior with the gate voltage. Because the gate and the body of NMOS varactor device are at voltage V_{ctrl}, the value of its capacitance spans a large range for 0.6V larger than V_{ctrl}. This architecture will work only on twin tub technology. Therefore we did not implement this architecture at layout level. For all other architectures the results are from their parasitic extracted netlist. The delay stage is shown in Fig. 3(b). The oscillation frequency of a 3-stage PNDT-VBRO will decrease more at higher control voltages as shown in Fig. 4(b). This allows an increase in tuning range and VCO gain in comparison to the conventional VBRO. The phase noise also improves due to increase in varactor capacitance as shown in Fig. 4(c).

TABLE I
Transistor Sizes used in VBRO

Transistors		Width (um)	Length (um)	Fingers
Inverter	PMOS	10	0.06	20
	NMOS	10	0.06	20
Varactor	PMOS	3	3	1
	NMOS	3	3	1

3. DT-PMOS and reverse NMOS varactors in parallel (PDTN-VBRO): In this architecture both the DT-PMOS and inversion NMOS (in reverse) are used as VBRO delay stage (Fig. 3(c)). The NMOS transistors are forward body biased and therefore have large change in the value of capacitance with the change in value of V_{ctrl} even for small values of V_{ctrl}. Please note that the PMOS varactor device would have a very small change in capacitance for small values of V_{ctrl} because its average FBB has a smaller value (Fig. 4(a)).



(a) (b)

Fig. 6 Center frequency variation of proposed VBROs and DROs at VDD = 0.6V (a) at different process corners, (b) at different temperature (TT corner)

TABLE II
COMPARISON OF ROs AT NTV REGIME

Performance Parameter	[2]	[3]	[4]	[5]	[6]	Conventional VBRO	This Work	
							DT-VBRO	PDTN-VBRO
Technology (nm)	90	130	65	65	180	65	65	
V_{DD} (V)	0.5	0.5	1	0.7	0.5	0.6	0.6	
Topology	PD-Ring	FD-Ring	FD-Ring	FD-Ring	PD-Ring	SERO	SERO	
Tuning Range (GHz)	0.16-2.5	0.4-0.433	0.352-0.454	0.882-1.36	0.082-0.37	0.714-1.1	0.638-2.36	0.425-2.13
Phase Noise @ 1MHz offset	-87	-91.5	-111	-90	-82	-88	-90	-95
Number of Stages	3	3	5	4	3	3	3	3
Power (mW)	1.157	0.44	0.158	0.36	0.06	0.127	0.127	0.127
FOM @ 1MHz (dBc/Hz)	-152.3	-	-171.05	-153	-145.5	-156.04	-162.46	-164.96

This architecture has an almost linear VCO gain for full control voltages as shown in Fig. 4(b). This is because it has a large change in varactor capacitance over entire range of V_{ctrl}. Due to the same reason this architecture gives the best phase noise among all VBRO architectures compared (Fig. 4(c)). Since the body bias for all NMOS transistor in the circuit is equal, there is no need to isolate the NMOS devices within the circuit. However an effective layout level guard bending (as proposed in [11]) is required to isolate NMOS devices of the circuit from other circuits.

4. Inverter transistors bulk terminals for coarse tuning: Forward body bias (FBB) is commonly used in existing ROs to decrease the threshold voltage and to increase the oscillation frequency and tuning range of an RO. Using the bulk of inverter transistors as coarse tuning and DTMOS varactor for fine tuning tremendously improves the RO performance. Vc_p and Vc_n (only for DT-VBRO) are the control voltages applied to the bulk of PMOS and NMOS transistors respectively of an inverter shown in Fig. 3(d). Fig. 5 show the tuning range for all three proposed architectures by varying the inverter bulk voltages to the maximum (VDD) and minimum (GND) values. The figure show that the oscillation frequency increases almost twice using these configurations.

The analysis for VBRO architectures is done keeping the transistor sizes equal for conventional and proposed VBROs. TABLE I shows the sizes used for the inverter transistors and the varactor transistors. The sizing of the inverters and the varactors is done such that the impact of the varactor is maximum (for a target oscillation frequency) total capacitance at the oscillating node. TABLE II shows a simulated performance comparison of the proposed VBRO architectures with other state of the art low voltage structures. Among all VBRO architectures PDTN gives the best performance. This architecture gives an increase of 33% oscillation frequency, a four times increase in tuning range, 8% improvement in phase noise with equal power consumption as compared to conventional VBRO as shown in TABLE II. Our proposed architectures gives a very high tuning range as compared to previous architectures without compromising the phase noise and power dissipation at VDD = 0.6V. The paper [4] gives good phase noise but delivers small tuning range (102 MHz) at high supply voltages (1V). The paper [2] has more tuning range but lacks in phase noise improvement, complex circuitry (variability issues) and high power consumption.

IV. VARIABILITY ANALYSIS OF VBRO ARCHITECTURES

PVT variations are the main concern in NTV regime. DROs and Pseudo DROs also face variations in NTV regime due to series stack transistors and low overdrive voltages. VBROs on the other hand have maximum control of varactor capacitance at the oscillating node making them less susceptible to substrate noise voltages. Also the small variations in supply voltage are less noticeable at the oscillating node due to large capacitance. A comparison of the proposed VBRO architectures is done with the conventional DRO and Pseudo DRO architectures. The Monte Carlo Simulations is configured to the supply variation on the oscillation frequency for 1000 runs. The mean and standard deviation of the distribution are analyzed. Fig. 6(a) shows frequency variation for typical (TT), fast (FF), slow (SS), fast-NMOS/slow-PMOS (FS) and slow- NMOS/fast-PMOS (SF) process corners at VDD = 0.6V. The power voltages for simulations are VDD±10%. Fig. 6(b) shows the frequency variation at -40℃, 0℃, 25℃, 75℃, 125℃ (ideal frequency at 27℃) temperatures at TT process corner at a VDD of 0.6V.

The result shows almost same variation in center frequency of single ended VBROs architectures as compared to DRO architectures at VDD = 0.6V.

V. CONCLUSION

The VBRO architectures with DT-MOS varactors and applying FBB technique are presented in NTV regime (VDD = 0.6V). The PDTN architecture gives wide tuning range of around 1.6 GHz (0.459-2.13GHz), phase noise of -95dBc/Hz with power consumption of only 127µW. The DT-MOS configuration varies the body capacitance for full control voltages. This gives almost linear VCO gain and full tuning range. PDTN architecture gives an increase of 33% oscillation frequency, a four times increase in tuning range, 8% improvement in phase noise with equal power consumption as compared to conventional VBRO. The architecture is less prone to supply and substrate noise voltage due to the varactor capacitance at the oscillating node.

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