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A 75-μW 2.4 GHz Wake-up Receiver in 65-nm CMOS for Neonatal Healthcare Application

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***Abstract*—A 2.4 GHz low power, Internet-of-Things (IoT) based system for neonatal health-care application is presented. The system includes an ultra-low power receiver compatible with a wearable device with interface-connectivity to the sensors and a controller. A novel design of a "wake-up" receiver architecture is presented, where an LC oscillator and a ring oscillator combination provides a desired ultra-low power solution. The proposed receiver front-end consists of a gm-boosting current-reuse based low noise amplifier (LNA) and a transmission-gate based passive switching mixer. The prototype is designed in a 65-nm CMOS technology. The simulation results show a gain of 14.9 dB while consuming 75μW from a 0.75 V supply. The LNA gain is 16 dB with a noise figure of 5.7 dB and IIP3 of 18.16 dBm.**

I. INTRODUCTION

Neonatal babies are born premature, and their body weight or fat is not sufficient to keep the body temperature within a normal range. They are at risk of an abnormally low body temperature (hypothermia). Thus, such babies are kept in a specialized neonatal intensive care unit (NICU), with constant health monitoring and regular medical supervision. After being discharged from the NICU, the remote location of the neonates and the inaccessibility of medical facilities pose additional challenges in providing emergency medical assistance. An IoT-based low-power wearable solution, which constantly monitors the neonates' health parameters and provides predictive measures to deal with abnormalities, is very desirable. Fig. 1 provides the details of such a proposed neonatal health care system.

A Radio Frequency (RF) receiver front-end for Ultra Low Power (ULP) operation, can use a conventional low power design technique to extend the battery lifetime [1]–[3] or a wake-up based receiver architecture (WuRX), a method gaining wide popularity [4]–[6]. The "wake-up" part of the receiver continuously monitors the channel to detect the presence of the desired signal, and "wakes up" the transceiver upon detection. The proposed RF receiver front-end consists of a low-noise amplifier (LNA), a mixer driven by a voltage controlled LC oscillator (LCO) [7] and a ring oscillator. The input RF signal is amplified by the low-noise amplifier. Then, the RF signal is converted to an intermediate frequency (IF) using a mixer. The IF is further used for baseband processing in the wakeup portion of the radio. The primary aim of a ULP receiver

[1] These three authors contributed equally to the paper

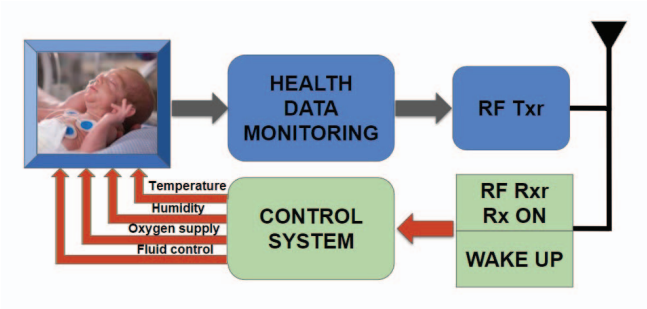

Fig. 1: Block diagram of a neonatal healthcare system (NHS).

design is to obtain maximum gain with minimum power and minimum noise figure. A widely accepted Figure of merit (FoM) of an ultra-low power receiver is given by [8]:

$$FOM = \frac{Gain}{(NF-1)P_{DC}} \quad (1)$$

where the gain is determined by the transconductances and output impedances of individual stages, which also set the power consumption. The noise figure (NF) is also included to incorporate the impact of the signal to noise (S/N) ratio on the bit error rate (BER) at ultra low power levels. The above performance parameters can be tuned to improve the FOM, but cannot achieve a substantial improvement due to circuit-design tradeoffs. Further reduction in power consumption is possible with system-level techniques such as the WuRX.

In this paper, the proposed WuRX architecture is discussed in Section II. The details of the design approach and the implementation are presented in Section III. The results are presented in Section IV and Section V concludes the work.

II. PROPOSED RECEIVER ARCHITECTURE

The block diagram of the complete transceiver of the neonatal healthcare system (NCS) is shown in Fig. 2. The receiver architecture (Fig. 3) is based on the premise that a low power (and low quality) ring oscillator (RO) can be used as the local oscillator to monitor the spectrum when the receiver is "asleep". After a desired signal is detected, and the receiver "wakes up", this oscillator can then be replaced by a high power (and high quality) LC VCO. The operating

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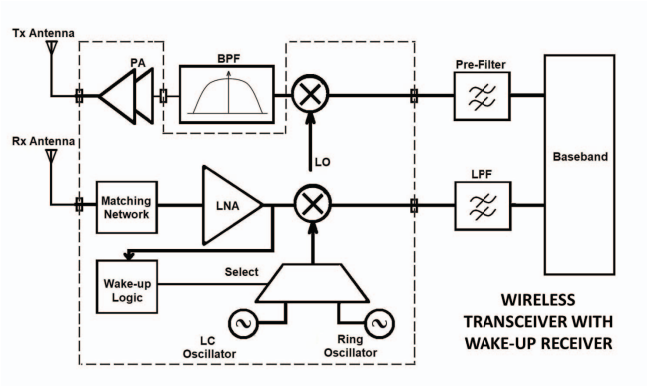


Fig. 2: Block diagram of the wireless transceiver

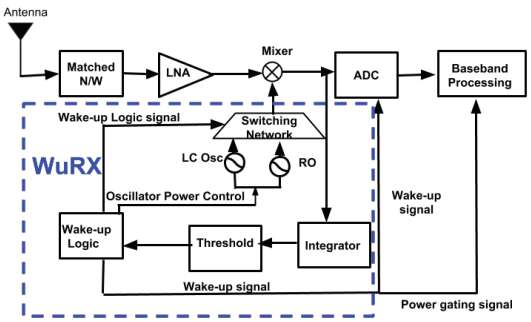


Fig. 3: Block diagram of the receiver

power levels of the two oscillators are different enough to significantly reduce the power consumption in the receiver. The receiver has two parts: the main signal path and the wake-up receiver (WuRX) path, as shown in Fig. 3. The main path consists of the receiving antenna and matching network, a low-noise amplifier (LNA), a mixer, a frequency generation circuit (LC Oscillator), a demodulator and the baseband processing block. The WuRX path consists of a low power ring oscillator, the wake-up logic to control the power gating and to generate the wake-up signal and a switch to choose between the two power modes.

The receiver architecture consists of a high gain low noise amplifier, with a twin T-network based passive mixer. The transistors used in the low power LNA are operated in the sub-threshold region [9], [10] with current-reuse. It has been shown that current reuse and the optimization of noise parameters for constrained current [8], [11]–[16], can provide a significant improvement in LNA performance. The mixer is a passive switching network based on the MOS-switch and it consumes zero DC current [17]. The mixer is driven by an LC-oscillator or a ring oscillator (RO). The wake-up receiver path consists of an energy detection circuit [17] along with a comparator (for thresholding), to indicate the received signal strength. During energy detection, the RO drives the mixer and once the desired signal is detected, the LC-oscillator drives the mixer. Such "agile frequency synthesis", has been described in the context of PLL component optimization [18], but requires a different approach for low-power operation.

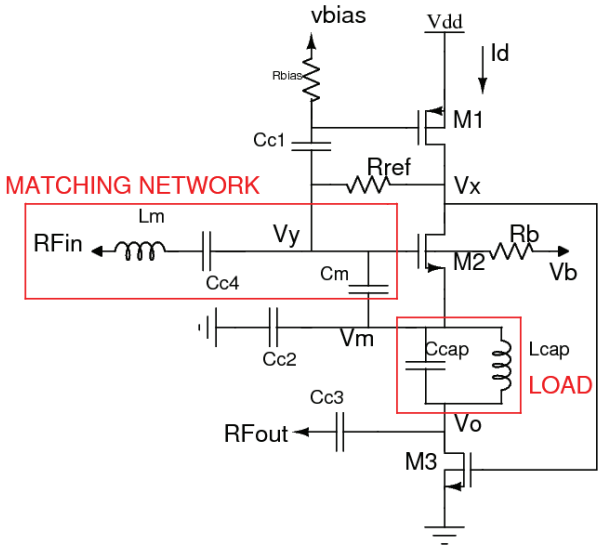


Fig. 4: Schematic of the Low Noise Amplifier (LNA).

III. Design Implementation

A. High-gain low-noise amplifier

Fig. 4 shows the schematic of the proposed low noise amplifier (LNA) consisting of two cascaded amplifier stages with current reuse for low power operation.

The first stage is a complementary Gm-boosting stage formed by M1, M2 and R_{ref}. The transistor M1 is directly biased at the gate with Vbias through R_{bias}. R_{ref} provides the drain-gate feedback for M2. The body of M2 is separately biased (using Rb) to adjust the threshold voltage for low voltage operation. The decoupling capacitor C_{c1} isolates the DC biasing to M2. Hence, it can be sized independently for the required *gm*.

The second stage is a common source amplifier (around M3) with a tank circuit as its load. The LC tank formed by C_{cap} and L_{cap} is used to resonate the second stage and, to reduce the signal leakage between the two gain stages. The capacitor C_{c2} separates the first amplification stage from the second. M3 is stacked below M2 for current reuse. C_m and L_m are used to match the input impedance of the circuit to 50Ω. All transistors are biased to operate in the sub-threshold region for low power consumption and to obtain the maximum $g_m f_t / I_D$.

The combined gain (A_{tot}) for the low noise amplifier is given by,

$$A_{tot} = K(1-(g_{m1}+g_{m2})R_{ref})(g_{m3}Z_{out2}) \quad (2)$$

$$K = \frac{ro_{m1}||ro_{m2}||\frac{1}{j\omega C_{gs3}}}{(ro_{m1}||ro_{m2}||\frac{1}{j\omega C_{gs3}})+R_{ref}} \quad (3)$$

$$Z_{out2} = ro_{m3}||Z_{LC} \quad (4)$$

where g_{m1}, g_{m2} and g_{m3} are the transconductance values of M1, M2 and M3, respectively. C_{gs3} is the gate source capacitance of M3 . Z_{out2} is the second stage output impedance and Z_{LC} is the impedance presented by the on-chip LC tank.

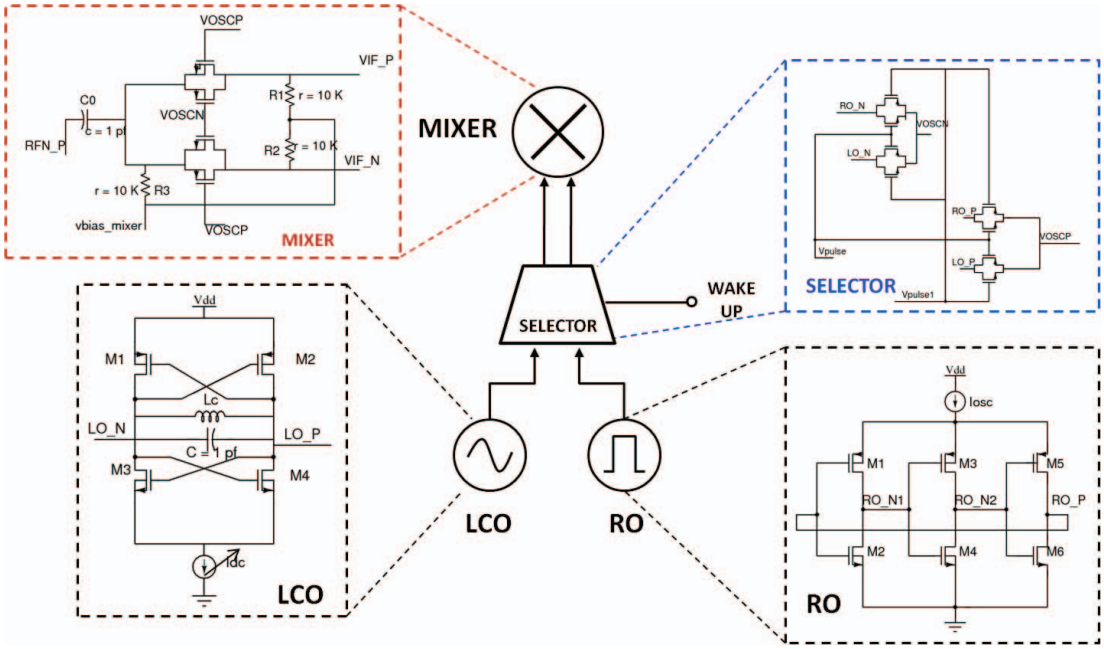


Fig. 5: Block diagram of the mixer, the selector and the two oscillators along with the corresponding schematics.

The total LNA noise figure using the Friis equation, is given by,

$$NF_{tot} \approx (1 + \frac{4R_{ant}}{R_{ref}} + \gamma) + \frac{NF_{2nd} - 1}{A_1} \tag{5}$$

where R_{ant} is the antenna impedance (50Ω), NF_{2nd} is the noise figure of the second stage and A_1 is the gain of the input stage. The input impedance of the LNA is given by,

$$Z_{in} = \frac{ro_{m1}||ro_{m2}||\frac{1}{sC_{gs3}}}{(ro_{m1}||ro_{m2}(g_{m1} + g_{m2})) + 1} \tag{6}$$

If C_{gs3} is made small by choosing a smaller size for transistor M3, then the input impedance of the second stage increases making Z_{in} dependent only on the input stage parameters. Consequently, as A_1 increases, the NF_{tot} also becomes dependent only on the input stage parameters. For the same reason, an NMOS is chosen for M3 to provide a higher g_m.

B. Oscillator Design – LCO & RO

Fig. 5 shows the schematics of the LC oscillator with a cross-coupled complementary architecture and a three-stage current controlled ring oscillator. The LC oscillator provides a high quality output with reduced phase noise. The inductance (L_c) and capacitance (C) are selected for an operating frequency of 2.375 GHz. To compensate for the PVT variations, a digitally-tuned capacitor is placed in parallel with the LC tank. The RO is used only during the WuRX operation to drive the mixer. The frequency of the RO is controlled by changing the current (I_{osc}).

C. Mixer Design

Although current switching provides better linearity, it is not preferred due to the power consumption of the intermediate stages for voltage-to-current and current-to-voltage conversion [8]. Fig. 5 shows the schematic of the proposed voltage switching differential passive mixer. The mixing operation is performed using a transmission gate for better linearity. The high frequency (RF) port and the low frequency (IF) ports are biased to the common mode voltage of V_{cm} through resistors R1, R2 and R3. In the T-gate configuration, the PMOS conducts when $V_{RF} > V_{cm}$ and the NMOS conducts when $V_{RF} < V_{cm}$, thus preventing clipping of the signal at the output. The LO leakage to RF and IF paths is also reduced in the T-gate because the NMOS and PMOS LO leakage gets canceled out with each other, provided that they are sized with the same aspect ratio ($\frac{W_n}{L_n} = \frac{W_p}{L_p}$).

D. Wake Up Receiver Logic

The design criterion for the RF receiver is to reduce the power consumption without degrading the data quality. In a typical RF protocol, the initial part of the transmitted data consists of packets with the preamble which are well known to the receiver prior to transmission. Extracting this information with low signal quality is possible. Fig. 6 shows the power utilization by the receiver front-end along with the control signal. If the data is transmitted and received in bursts with a low duty-cycle, significant power savings can be achieved.

Fig. 7 shows the energy detection-based wake-up circuit. On startup, the transmission gate will pass the RO output. Once the desired signal is detected by the energy detection circuit, the LCO power gating switch will be turned on. After the LCO stabilizes, the transmission gate will switch on the LCO path and the RO power gating switch is turned off. The LCO is disabled only after post-amble detection by the baseband processor indicating the end of transmission (EoT). After receiving EoT, the receiver is switched to the low power mode till the WAKE UP signal is received again.

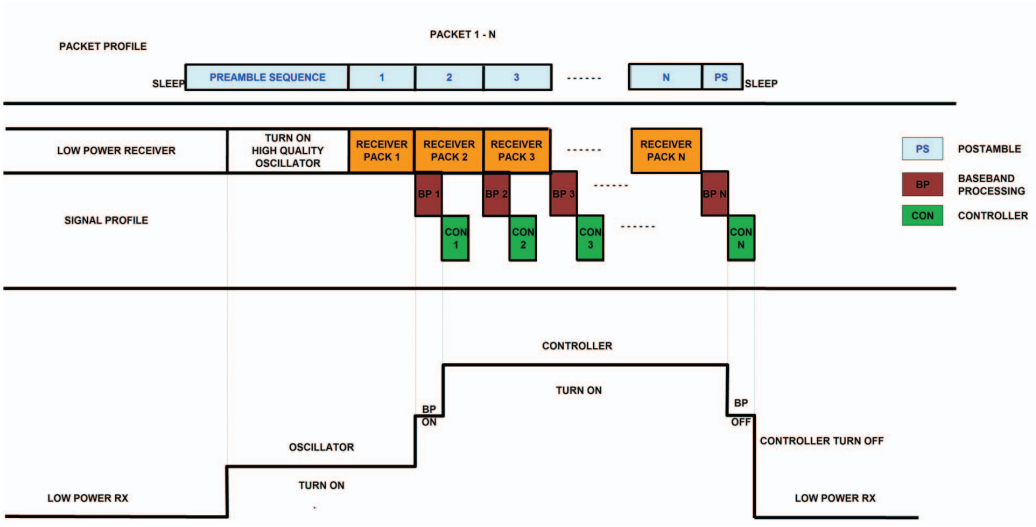


Fig. 6: Energy profile of the wake-up receiver.

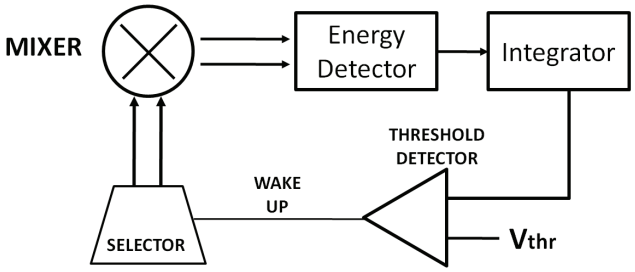


Fig. 7: Block diagram of the wake-up circuit

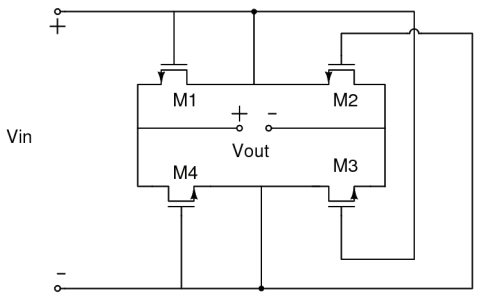


Fig. 8: Schematic of the product-modulator based energy detector

1) Energy Detector: The energy detector (Fig. 8), is a product modulator circuit with the same input fed to both the input ports to obtain a voltage proportional to the energy of the desired signal. This is fed to the integrator for a specific time window. Once the integrated output crosses a threshold, it generates a valid signal for "wake up".

2) LO Selector: In the proposed architecture (Fig. 3), the receiver will be working with a ring oscillator during the initial phase of operation. Once a proper preamble signal is detected, the demodulated signal quality is enhanced using a high quality LC oscillator. However, switching from one oscillator to the other should not affect the continuous supply of the LO signal to the mixer. The LO selector is implemented

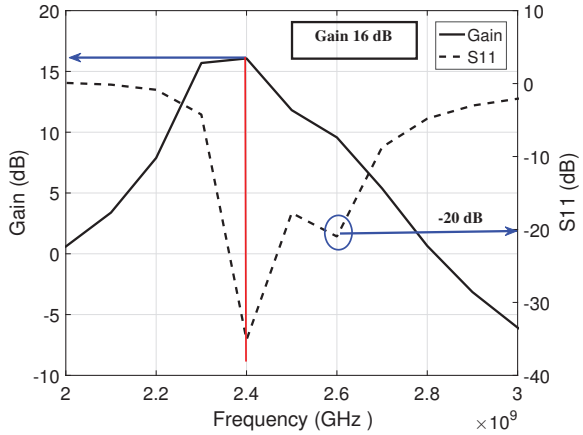


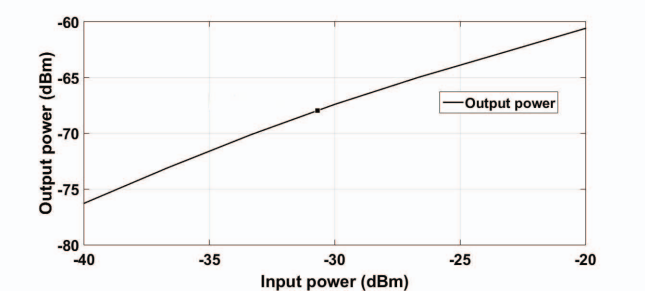
Fig. 9: Gain and S11 plot for the proposed LNA

using transmission gates as shown in Fig. 5. The WAKE UP signal selects the LO between the LCO and RO and performs power gating of the RO and LCO circuits. The implemented digital logic will first turn on the RO. The NMOS-PMOS structure ensures a large output without reducing the voltage swing. The W/L ratio of the NMOS and PMOS transistors is balanced for optimum performance.

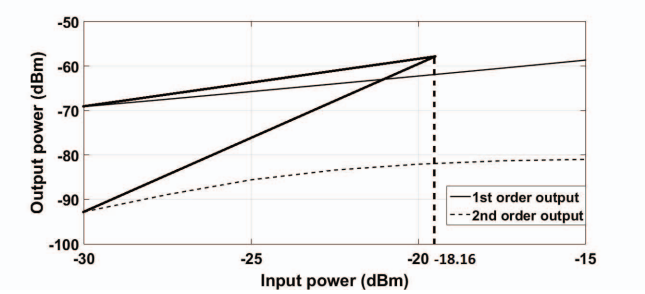
With this design approach, a 1000x reduction (approximately) in the VCO power consumption is obtained: from $2.7mW$ to $3.06\ \mu W$. For the proposed neonatal IoT applications, where the receiver spends most of its time in idle mode (low duty-cycle of operation), this solution results in very low power consumption.

IV. Results and Discussion

The proposed 2.4 GHz wireless receiver with a WuRX was designed and simulated in 65-nm CMOS technology. The simulations were performed to test the performance of the receiver in two operating modes: (a) active mode and (b) sleep mode. The LNA and mixer are 'ON' all the time while the



(a)



(b)

Fig. 10: Low noise amplifier linearity performance parameters: (a) 1-dB compression point, P_{-1dB} = -30.75 dBm and (b) IIP3 of -18.16 dBm.

RO is 'ON' in the sleep mode and the LCO is 'ON' in the active mode.

Table I lists the component-wise break-up of the power dissipation of the receiver. The LNA is designed to consume 75μW of power, while the mixer consumes 0.5μW of power, operating at 0.75 V. The LCO in "wake-up" mode consumes 2.751 mW which is a significant portion of the power budget of the receiver in active mode.The total power in the sleep mode is 36X less than that of the active mode. Significant power savings can be achieved if the data transmission and reception happens in bursts with a low duty cycle.

TABLE I: Power performance of RF front-end components.

Parameters	Sleep mode	Active Mode
LNA	75 μW	75 μW
Mixer	0.5 μW	0.5 μW
LCO	$\approx 0\mu$W	2.75 mW
RO	3.0 μW	$\approx 0\mu$W
Total	**78.5 μW**	**2825 μW**

The low noise amplifier, made up of two cascaded amplifiers, has a gain of 16 dB and a noise figure of 5.7 dB at the operating frequency of 2.4 GHz, as shown in Fig. 9. It consumes 90 μA from the 0.75V supply. Fig. 10 shows the linearity performance parameters of the LNA. The LNA has an IIP3 of -18.16 dBm and the 1-dB compression point, P_{-1dB} is -30.75 dBm.

The phase noise for the LCO is -120 dBc/Hz at an offset frequency of 1 MHz and the stabilization time is 500ps, which is significantly less than the "minimum total time to send data" specified for low energy standards (3ms in Bluetooth Low Energy). The phase noise for the RO is -86.64 dBc/Hz at an offset frequency of 1 MHz, which is much worse than that of the LCO, but sufficient for the energy detection in the WuRX.

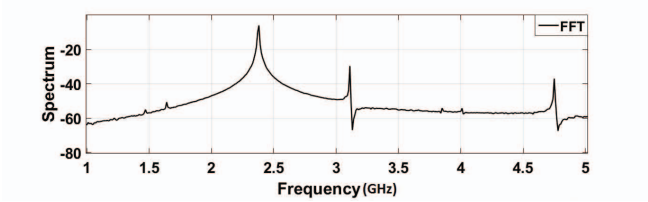


Fig. 11: The frequency-domain response of the LC Oscillator at 2.4 GHz.

Fig. 11 shows the frequency spectra of the LC Oscillator at 2.4 GHz. The conversion gain of the mixer was found to be 0.876. Fig. 12 (a) shows the mixer output when the LO switches between RO and LCO. Fig. 12 (b) and (c) shows the output spectrum of the mixer with the local oscillator inputs with RO and LCO, respectively.

Table II presents the summary of the design and the performance comparison with various low power wireless receivers reported in the literature. The FoM used to compare the parameters is,

$$FoM = \frac{Gain}{(NF-1)f_c P_{DC} Technology} s^2/J \qquad (7)$$

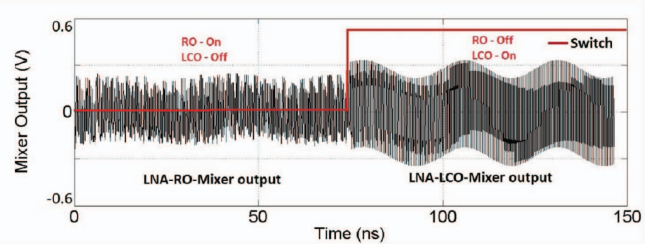
TABLE II: Performance Comparison.

Parameters	This Work	[8]	[19]	[20]	[21]
VDD $[V]$	0.75	0.6	0.8	0.9	0.4
Technology [nm]	65	65	130	65	130
f_c $[MHz]$	2400	2400	2400	915	2400
$P_{DC}[\mu W]$	75	64	600	282	60
Gain $[dB]$	14.9	22.9	56.1	30	13.1
NF $[dB]$	5.7[1]	8	15.1	9	5.3
IIP3 $[dBm]$	-18.16[1]	-21	-15.8	-28	-12.2
FoM $[s^2/J]$	17.61	21.29	1.38	14.53	10.58

[1] Includes only LNA

V. Conclusion

A novel design of a wake-up based receiver architecture at 2.4 GHz is presented, where a local oscillator and a ring oscillator combination provides a desired ultra-low power solution. An on-chip receiver front-end is simulated using a 65-nm (low leakage) technology. The components of the receiver were designed for optimum performance while consuming minimum current. A gain of 14.9 dB while consuming 75 μW from a 0.75 V supply is achieved in a pre-layout simulation. Since the design is at 2.4 GHz, where the device models are mature and most parasitics are accurately modeled, we do not expect the results to change significantly after layout. A gm-boosting current-reuse based low noise amplifier (LNA) design with a gain of 16 dB and noise figure of 5.7 dB is used to design a low bit-rate receiver with very low power dissipation. This ultra-low power IoT system is well suited for neonatal health-care monitoring applications in remote locations, where battery life-time is critical.



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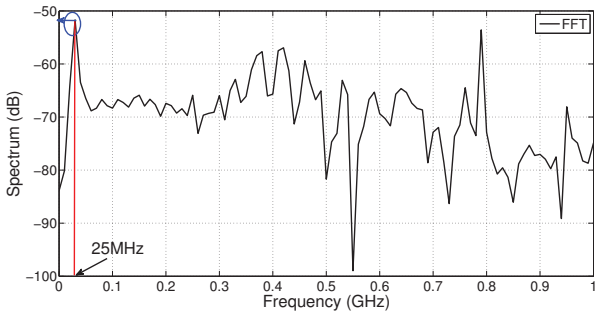

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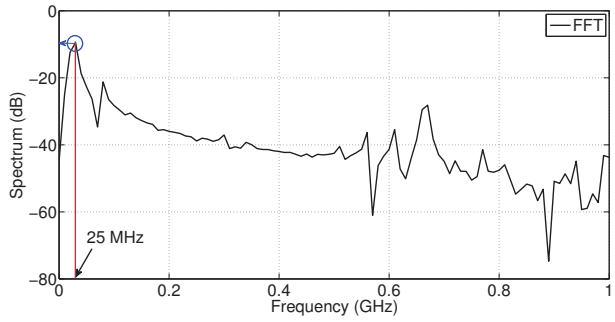

(c)

Fig. 12: Energy Detection and Signal Extraction: (a)Simulation result showing output of the LNA and mixer when driven by the RO and LCO (Fig. 5). The energy contained in the signal is larger in the LCO-On state. The WAKE UP signal (shown in red) indicates the LO select signal for the RO and LCO. (b) Output spectrum of the mixer with RO input (c) Output spectrum of the mixer with LCO input.

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