A 19.3-24.8 GHz Dual-Slope VCO in 65-nm CMOS for Automotive Radar Applications

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***Abstract*—This paper presents a dual-slope K-band voltage controlled oscillator (VCO) for automotive radar applications. The frequency range of the VCO is from 19.3 GHz to 24.8 GHz. The dual-slope operation is implemented using a negative inductor. The K-band VCO generates a signal with a phase noise less than -90.4 dBc/Hz at 1 MHz offset frequency at 24.1 GHz. The VCO achieves a figure-of-merit (FOM_T) of -175.71 dBc/Hz. The design is implemented in a 65-nm CMOS process. It consumes 10.62 mW of power from a 1.2 V supply, and occupies an area of $0.23 \times 0.11mm^2$.**

I. Introduction

Short range automotive radars, implemented for parking assist and collision avoidance systems, are operated in the K-band. A voltage controlled oscillator (VCO), which determines the frequency of operation, is a key block for such radars. Apart from the usual requirements of low power, low phase noise and wide tuning range, an automotive radar VCO also requires a small K_{VCO}. A small K_{VCO} variation allows for a linear frequency chirp and stable phase locked loop (PLL) characteristics. The phase noise of an LC VCO is affected by the tank Q-factor [1]. The quality factor of the tank degrades as the frequency increases due to the skin effect. The C_{max}/C_{min} ratio of the varactor affects the tuning range [2].

Various VCO implementations, focusing on low phase noise and high Figure of merit (FoM), have been reported. Techniques for device, circuit and layout optimization, such as band-gap engineering [3], current source filtering [4], and Q-enhancement with defected ground structures [4], [6] have been used to improve the phase noise of VCOs. A quadrature VCO for K-band radars is presented in [7]. Switched inductors are used in [2] to vary the inductance of the tank. This provides a wide tuning range with increased area and power overhead. A transformer based design is described in [9] with switches placed at different locations on the secondary coil to increase the number of sub-bands. The total parasitic capacitance in such an implementation degrades the overall performance.

This paper presents a method to minimize the phase noise of the VCO, and provide a wider frequency tuning range with a lower area. The proposed VCO has a frequency range from 19.3 GHz to 24.8 GHz with a dual-slope. The simulated phase noise is -90.4 dBc/Hz at 1MHz offset. The power consumption is 10.62mW.

The rest of the paper is organized as follows. Section II describes the VCO design along with the analysis and design of tunable negative inductance. Section III describes the phase noise analysis. Section IV presents simulated results, based on layout based parasitic extraction and Section V concludes the paper.

II. VCO Design

The schematic of the proposed VCO with switchable cross-coupled transistors with variable L and C, is shown in Fig.1. The cross-coupled NMOS transistor pair (M1, M2) is biased with the help of I_{bias} for which, the sizing of the current mirror is determined by the need to preserve circuit symmetry. A

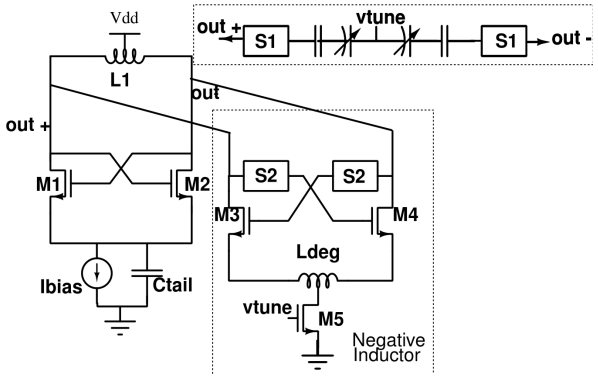

Fig. 1. Schematic of the proposed VCO.

capacitance C_{tail} is used to generate an impulse like current waveform provided the transistors are working in the active region [12]. The switches S1 and S2 are used to turn on the negative inductor, the varactor or both at a time, which provides the dual slope characteristics discussed in Section II-B.

A. Negative Inductance Realization

Fig. 2 shows the circuit implementation of negative inductance using cross-coupled transistors degenerated by an inductor [8]. This topology provides a complex impedance and it can be transformed into a parallel R-L combination given by

$$R_{p,NI} = -\frac{2}{g_m} - \frac{g_m \omega^2 L_{deg}^2}{2} \quad (1)$$

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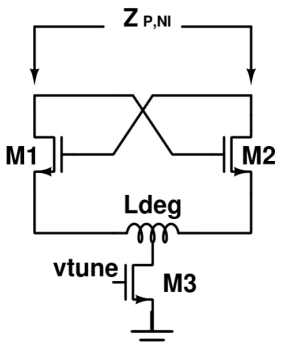

Fig. 2. Schematic of the negative inductor.

$$L_{p,NI} = -L_{deg} - \frac{4}{g_m^2 \omega^2 L_{deg}} \tag{2}$$

where g_m is the transconductance of the cross coupled pair and L_{deg} is the degeneration inductance. This provides a negative resistance and negative inductance which can be tuned using the transistor (M3) which biases the cross-coupled pair. Thus, from (1) and (2), the change in g_m changes the impedance and g_m is linearly dependent on V_{tune} (Fig. 2). This tunable impedance appears in parallel with the L and C of the tank as shown in Fig. 3, which changes the oscillation frequency and

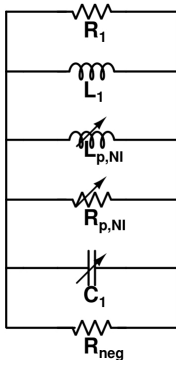

Fig. 3. Equivalent circuit of the tank with R_{neg} generated by the cross-coupled transistors.

the Q factor of the circuit. The oscillation frequency without the negative inductor cell is given by

$$\omega = \frac{1}{\sqrt{L_1 C_1}} \tag{3}$$

where L_1 and C_1 are the inductance and capacitance (parasitic and varactor) respectively. This equation changes when the effect of negative inductance is included and is given by [8]

$$\omega = \sqrt{A - B \cdot g_m^{-2} + \sqrt{B^2 \cdot g_m^{-4} + C \cdot g_m^{-2} + D}} \tag{4}$$

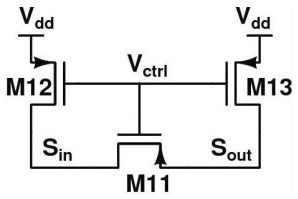

Fig. 4. Switch schematic.

TABLE I
SWITCHING STATES.

State	$S1$	$S2$	Description	Slope
State 1	ON	ON	Both ON	negative
State 2	OFF	ON	negative Inductor ON	negative
State 3	ON	OFF	Varactor ON	positive
State 4	OFF	OFF	Both OFF	positive

where the coefficients A-D are given by

$$\begin{aligned} A &= \frac{1}{2} L_1^{-1} C_1^{-1} - \frac{1}{2} L_{deg}^{-1} C_1^{-1} \\ B &= 2 L_{deg}^{-2} \\ C &= 2 L_{deg}^{-3} C_1^{-1} + 2 L_1^{-1} L_{deg}^{-2} C_1^{-1} \\ D &= \frac{1}{4} \left(L_{deg}^{-1} C_1^{-1} - L_1^{-1} C_1^{-1} \right)^2 \end{aligned} \tag{5}$$

The oscillation frequency is thus dependent on the g_m of the negative inductor cell, L_1, variable C_1 and L_{deg}. The derivative with respect to g_m will have a negative slope which implies that the oscillation frequency decreases monotonically with g_m which is linearly dependent on V_{tune}. Thus from [8]

$$\frac{\partial \omega}{\partial g_m} < \frac{-C}{2B\sqrt{A}} \cdot g_m^{-1} < 0 \tag{6}$$

The switches S1 and S2 (Fig. 1) are designed to minimize loading in the tank. Fig. 4 shows the schematic of the switch used in the proposed VCO [11]. The transistors M12 and M13 are used so that there will be a common mode voltage at S_{in} and S_{out} when M11 is turned on. Since the gates of M11, M12 and M13 are connected this will ensure that when M11 turns on, both M12 and M13 will turn on and the drain and source voltages of M11 will be at V_{dd}, which will result in zero drop across M11. This arrangement will also ensure that the drain body voltage (V_{DB}) of M11 is not forward-biased, so that no current flows through the substrate.

B. Dual Slope and Radar Synthesizers

As shown in Fig. 1, the VCO has two switches (S1, S2) which connect the negative inductor and varactor blocks to the tank.When S1 is turned on and S2 is turned off, the circuit will behave like a conventional VCO with a varactor and its oscillation frequency is given by (3) with $\frac{\partial \omega}{\partial g_m} > 0$. Whereas, when S1 is turned off and S2 is turned on, the VCO will have a negative slope as evident from (6). The various switching states and their corresponding slopes are listed in Table I.

A conventional "frequency-modulated continuous wave" (FMCW) radar synthesizer uses an unsettled phase-locked loop, in which the control voltage is ramped up and down to produce the chirp. Having the flexibility to switch the mode of the VCO during a chirp provides the ability to change the slope of the tuning curve. The adaptive tuning of various components in a phase locked loop has been previously attempted [16], [17] but the dual-slope provides an additional degree of freedom in setting the loop-parameters. If the mode of operation is "switched-frequency continuous wave" (SFCW), where the loop has to settle before resolving a target, a dual-slope architecture can simplify the loop design. Due to its dual-slope tuning curve, we expect this VCO topology to play an important role in radar frequency synthesis.

III. Phase noise analysis

According to [1], the output phase noise of an LC VCO is given by,

$$L(\omega) = F\frac{4kTR}{V_0^2}\left(\frac{\omega_0}{2Q\omega}\right)^2 \tag{7}$$

$$F = \left(2 + \frac{8\gamma R I_{bias}}{\pi V_0} + \frac{8}{9}\gamma g_m R\right) \tag{8}$$

where γ represents the MOSFET noise coefficient and g_m, I_{bias} are the transconductance and current of the tail transistor, respectively. Q is the quality factor of the LC tank, and V_0 is the output amplitude. F is the thermally induced phase noise arising from the resonator, differential oscillator pair and tail current source [1].
In a parallel combination of R, L and C as shown in Fig. 3, the voltage to current transfer function is given by

$$H(s) = \frac{\frac{s}{C}}{s^2 + \frac{s}{CR} + \frac{1}{LC}} \tag{9}$$

The quality factor Q and oscillation frequency ω are then given by

$$Q = R\sqrt{\frac{C}{L}} \tag{10}$$
$$\omega = \frac{1}{\sqrt{LC}}$$

The Q can be increased, if R and C are increased or L is decreased. The equivalent resistance of the tank R_{equi} is given by

$$R_{equi} = (R_{neg} \| R_{p,NI} \| R_1) \tag{11}$$

where R_{neg}, $R_{p,NI}$ and R_1 are the resistances due to the core cross-coupled pair, negative inductance cell and inductor loss respectively. Therefore,

$$\begin{aligned} R_{equi} &= \frac{1}{\frac{1}{R_{neg}} + \frac{1}{R_{p,NI}} + \frac{1}{R_1}} \\ &= \frac{1}{\frac{Q_{L_1}}{\omega L_1} - \frac{g_{m_{core}}}{2} - \frac{1}{\frac{2}{g_m} + \frac{g_m \omega^2 L_{deg}^2}{2}}} \\ &= \frac{\frac{4\omega L_1}{Q_{L_1} g_m^2}}{\frac{4}{g_m^2} + \omega^2 L_{deg}^2 - \frac{4\omega L_1}{g_m Q_{L_1}}} \end{aligned} \tag{12}$$

Since, $\frac{2}{g_m} >> \frac{g_m \omega^2 L_{deg}^2}{2}$ we can ignore that term and assume that $g_m \approx g_{m_{core}}$. To increase the resistance, g_m and L_{deg} values must be reduced. The equivalent capacitance (C_{equi}) and inductance (L_{equi}) can be written as

$$C_{equi} = C_{parasitics} + C_{varactor} \tag{13}$$

$$\begin{aligned} L_{equi} &= L_1 \| L_{p,NI} \\ &= \frac{L_1 L_{p,NI}}{L_{deg} + \frac{4}{g_m^2 \omega^2 L_{deg}} - L_1} \end{aligned} \tag{14}$$

Hence, if the denominator is maximized, the inductor value will decrease which will lead to an increase in the Q factor. In a similar way if we decrease the value of g_m and L_{deg}, the Q factor will be enhanced. The Q-factor (Q_{equvi}) of the tank can be written as

$$Q_{equi} = R_{equi}\sqrt{\frac{C_{equi}}{L_{equi}}} \tag{15}$$

where $R_{equi}, C_{equi}, L_{equi}$ are obtained from (12)-(14). The switches used will reduce the oscillation frequency and will also affect the phase noise. This is primarily due to the series resistance of the switch reducing the tank Q and the drain-junction capacitance adding to the parasitic capacitance in the tank.

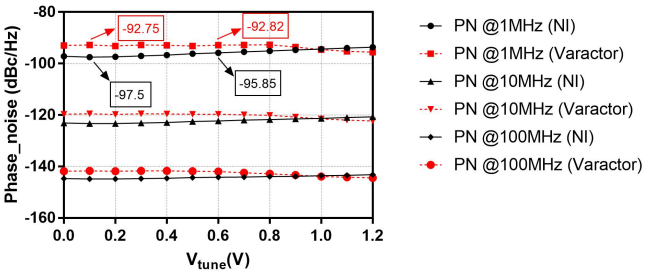

Fig. 5. Phase noise comparison with and without negative inductor. The V_{tune} range (0.0-1.2 V) corresponds to a frequency range of 25.89-24.3 GHz.

The Q-enhancement results in a 3-dB improvement in the phase noise due to the use of the negative inductor. In Fig. 5, the phase noise of the negative inductance (NI) based VCO is compared with that of the varactor tuned VCO. The same LC core was used to ensure that the phase noise impact of

the unloaded VCO was identical in both cases. The VCO was tuned from 24.3 GHz to 25.89 GHz. We observe that there is a significant (about 3 dB) improvement in the phase noise performance of the VCO.

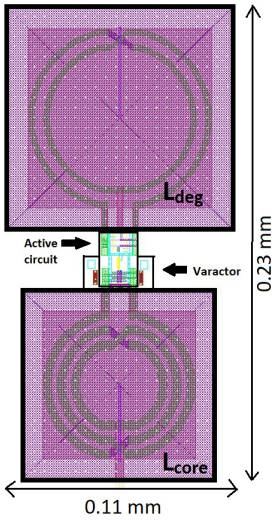

Fig. 6. Layout snapshot of the VCO.

IV. Post Layout Simulation Results

The design was implemented in a 65-nm CMOS process. The layout snapshot of the VCO is shown in Fig.6. The layout was parasitic extracted with the Calibre RC-extraction tool which is silicon-calibrated to 20 GHz. We do not expect additional parasitics between 20-24.8 GHz to significantly impact the performance as most parasitics can be extrapolated for a further 4 GHz. We have observed a 10% reduction in the operating frequency range after parasitic extraction, which is expected at such high frequencies. The total area is $0.23 \times 0.11mm^2$.

The post layout tuning range of the VCO is from 19.3-24.8 GHz (Fig. 7). When the negative inductor turns on, the

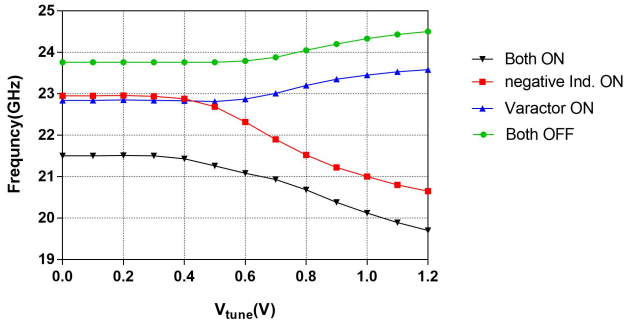

Fig. 7. Tuning Range of the VCO.

tuning characteristics have a negative slope. When it is off, the tuning characteristics have a positive slope which is also observed when both the negative inductor and the varactor are disconnected from the tank. A summary of the switching states is presented in Table I. S1 and S2 are the switches shown in Fig.1.

We note that between V_{tune} = 0.6 V to 1.2 V, depending on the switching state, a positive or negative slope is obtained for the tuning-curve. As stated earlier, this leads to the dual-slope characteristics of the VCO. These characteristics, with opposite slopes, can be shifted with respect to each other by adding a switchable capacitance to the tank. This results in the FMCW triangular wave, used in automotive radar systems.

The associated phase noise at 1 MHz offset and 10 MHz offset for the V_{tune} sweep is shown in Fig. 8 and Fig. 9 respectively.[1] We observe that the phase noise of the unloaded tank (state 4) is comparable to the phase noise of the tank, when loaded with the negative inductor (state 2). This proves that due to the Q-enhancement, the negative inductor does not impact the phase noise of the VCO. Fig. 10 shows the phase noise plot with respect to offsets from carrier frequencies of 19.3 (state 1) and 24.8 GHz (state 4). The total power

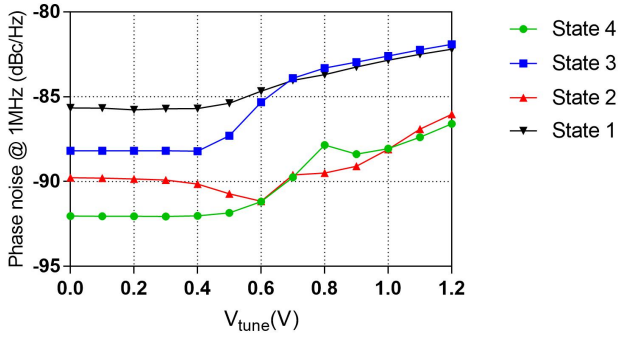

Fig. 8. Phase noise variation with V_{tune} @ 1MHz offset.

consumption variation with control voltage V_{tune} is shown in Fig. 11. The power consumption is consistent across all the states as it is primarily set by the bias current in the VCO. The FOM_T (Figure Of Merit with Tuning range) is given by

$$FoM = PN_{\Delta f} - 20\log\frac{f_{osc}.\ TR}{\Delta f.\ 10} + 10\log P_{DC} \qquad (16)$$

where, $PN_{\Delta f}$ is the phase noise at an offset frequency of Δf from the oscillating frequency f_{osc}, TR is tuning range (per cent) and P_{DC} is the power consumed at a given frequency. The measured FOM_T is -175.71 dBc/Hz at 24.1 GHz with a power consumption of 10.62 mW. Fig.12 shows the corner simulation results for the most extreme variation in device and passive component parameters. Figs. 13 and 14 show the variation of phase noise at 1MHz and 10MHz offsets for the device and passive corners. State (a) in Figs. 12-14 refers to

[1]The small glitches ($< 1dBc/Hz$) in the phase noise for State 2 and State 4 in Fig. 8 are presumably due to V_{tune} being in the range of V_{th} for M5, which injects noise in the tank, when turned on.

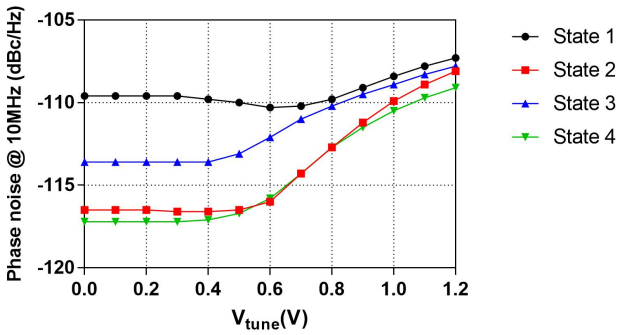

Fig. 9. Phase noise variation with V_{tune} @ 10MHz offset.

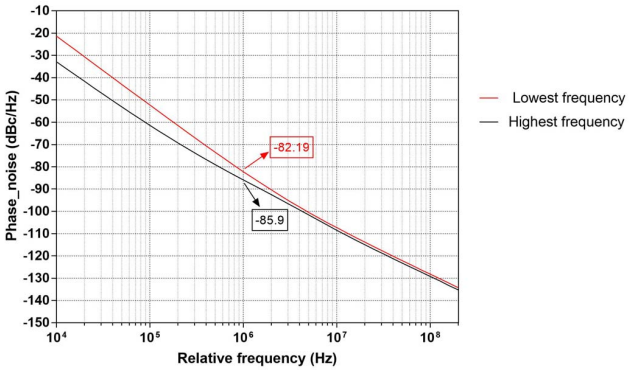

Fig. 10. Phase noise plot with respect to offset frequency (first relative harmonic).

the simulation environment consisting of slow devices and maximum passive parameter values, while state (b) represents fast devices and minimum-value passives. We observe that with a proper selection of states, it is possible to preserve the wide-tuning range and the low phase-noise of the VCO, across all the process corners.

A comparison with the existing state-of-the-art is shown in Table II. We observe that while [2] and [14] achieve

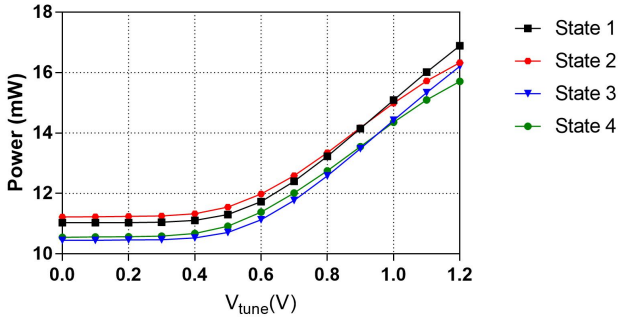

Fig. 11. Power Consumption of the VCO.

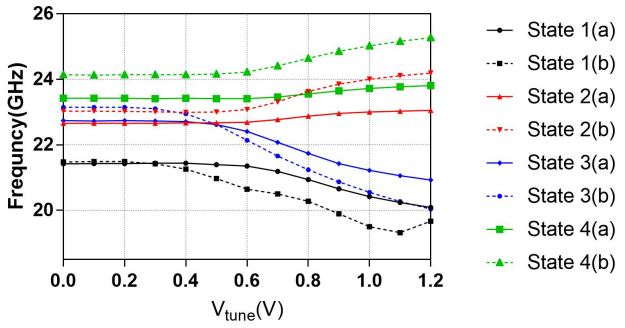

Fig. 12. Tuning range across process corners.

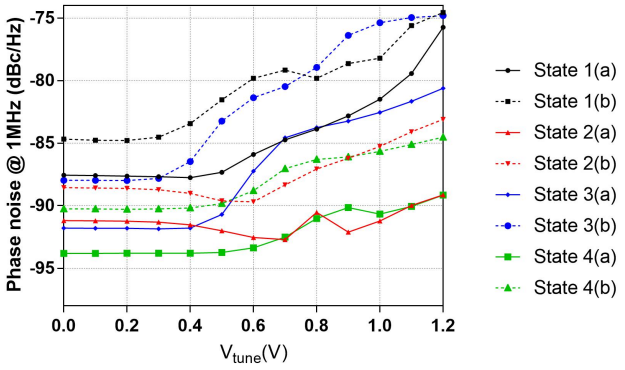

Fig. 13. Corner simulation of Phase Noise @ 1MHz offset.

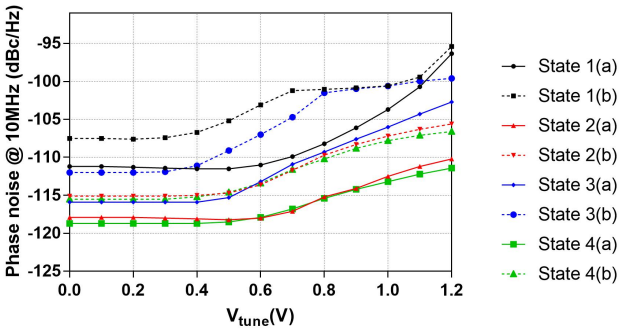

Fig. 14. Corner simulation of Phase Noise @ 10MHz offset.

better figures of merit due to a wider tuning range, they have comparable phase noise to the proposed architecture. The use of switched inductors in [2] results in a larger area than our design which uses only two inductors. The phase noise of [14] is slightly worse than that of our design, although they use substrate shielding, and we do not. This is possibly due to the Q-enhancement in our design. We expect that this design technique, when combined with other techniques, such as those described in [2] and [14] will result in even better

TABLE II
COMPARISON WITH THE EXISTING STATE OF THE ART.

Reference	Technology CMOS	f_{osc} (GHz)	Tuning Range%	Phase Noise (dBc/Hz) @ 1MHz	P_{DC}(mW)	FoM_T (dBc/Hz)	Area (mm^2)
[2]	65nm CMOS	27.5	43.3	-95	4.8(VCO Core)	-189.7	0.9×0.9
[4]	0.18μm CMOS	21.07	4.8	-108.1	7.5	-179.4	0.6×0.6
[10]	0.18μm CMOS	24	12.6	-101.3	25	-176.9	0.5×0.46
[13]	0.18μm CMOS	24.27	2.2	-100.7	7.8	-166.33	0.6×0.7
[14]	65nm CMOS	25.3	34.8	-89.5	4.1	-182.26	0.05×1
[15]	65nm CMOS	24.3	3.4	-104.6	4.8	-176.12	0.16×1
This work	**65nm CMOS**	**24.1**	**26.9**	**-90.4**	**10.62**	**-175.71**	$\mathbf{0.23 \times 0.11}$

FOM values in future designs.

V. CONCLUSION

A dual-slope K-band VCO using a negative inductance and a varactor is proposed. The negative inductance provides a negative K_{VCO} which can be used to help in the efficient generation of frequency chirps for automotive radars. The use of negative inductance also improves the phase noise performance of the VCO by about 3 dB, when compared with a conventional varactor based VCO. The design is implemented in a 65-nm CMOS process.

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