Optimization of Multiple Physical Phenomena through a Universal Metric in Junctionless Transistors

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***Abstract*—The work reports on the identification and applicability of a universal metric to suppress gate induced off-state tunneling while preserving impact ionization triggered sub-60 mV/decade current transition and hysteresis in 25 nm Junctionless (JL) MOSFET. At shorter gate length limit, two contrasting physical mechanisms, namely, impact ionization and Band-to-Band Tunneling (BTBT), affect device functionality. Both these phenomenon are analyzed through the evaluation of the product of current density (*J*) and electric field (*E*), which defines power generated per unit volume in the device. Hysteresis, in forward and reverse sweeps of applied gate bias, can be accompanied by an undesirable increase in off-current due to BTBT, thus limiting the device performance. The work showcases the relevance of *J.E* optimization in 25 nm JL device to achieve a subthreshold swing (*S*) < 5 mV/decade along with a wider hysteresis window ~140 mV at a drain bias (V_{ds}) of 1 V with suppressed off-state tunneling.**

***Keywords*—Junctionless, MOSFET, Impact ionization, Band-to-Band Tunneling, Hysteresis, Off-current, Steep switching.**

I. INTRODUCTION

In the nanoscale regime, multiple physical effects can occur in a Metal-Oxide-Semiconductor (MOS) transistor. As these effects are related to a physical phenomenon in the device and impact the performance, a careful identification and optimization of the same is required to achieve application specific optimal performance. This is more relevant in case of 'unipolar' Junctionless (JL) [1] devices which despite being free of traditional *pn* junction can achieve full CMOS functionality [1]. JL devices have shown to exhibit strong Floating Body Effects (FBEs) [2-4] and Band-to-Band Tunneling (BTBT) [5-9] despite being doped with only one type of dopants throughout the silicon film.

The off-current in a MOSFET increases due short channel effects (SCEs) associated with gate length downscaling [10]. However, an additional component contributing to the increase in off-current is BTBT [5-9] which increases the static power consumption and further degrades the on-to-off current ratio. While BTBT is considered to be detrimental due to an increase in off-current, FBEs can be useful for initiating impact ionization in the subthreshold region which can be utilized to achieve a sharp increase in drain current [2-4] at the threshold. Lee *et al*., [2] have experimentally demonstrated that JL devices can trigger impact ionization due to FBEs and achieve sharp rise in drain current with a Subthreshold swing (*S*) of ~1 mV/decade at relatively lower drain bias in comparison to inversion mode transistors [2]. The reason for the enhanced degree of impact ionization is the higher current density (*J*) and wider area over which impact ionization takes place which results in an enhanced Impact Generation Rate (*IGR*) [2].

An important feature associated with impact ionization facilitated steep switching in drain current is the occurrence of hysteresis in forward and reverse sweeps of applied gate voltages [11-14]. Previously, hysteresis effect have been observed by various research groups in inversion mode transistor [11], Punch through Impact ionization MOS (PIMOS) [12] and JL [13-14] devices. The impact ionization induced hysteresis in transfer characteristics results in results in two threshold voltage associated corresponding to forward and reverse sweeps of gate voltage and thus, is not suitable for logic applications. Hysteresis can be utilized for realizing a single transistor dynamic memory [12-14]. An important aspect describing hysteresis is the width of hysteresis window, which is also referred to as the memory window (ΔW) and represents the range over which write and read operations can be performed [11-14]. While FBEs can be useful to trigger impact ionization and achieve steep current transition with *S* value lower than 60 mV/decade, the degradation due to an increase in the off-current because of BTBT is detrimental for the device. As gate length (L_g) is scaled down, BTBT can become dominant and deteriorate the performance of JL devices [5-9] at lower gate biases, thus counteracting any advantage due to dominant FBEs. In addition, the requirement of a higher drain bias (V_{ds}) to enhance impact ionization, and thus, ΔW for memory operation can further increase gate induced BTBT and off-current in JL devices. Also, tunneling at lower gate biases can even cause degradation in Write 0 (W0) state for dynamic memory applications. Hence, it is crucial to identify approaches to suppress BTBT while maintaining FBEs to benefit from sub-60 mV/decade steep switching and hysteresis without increasing the applied drain bias.

In this work, we investigate the influence of gate length downscaling on the functionality of silicon JL transistors by analyzing two contrasting physical phenomenon, namely, FBEs and BTBT, occurring in the device through a universal parameter defined as the product of current density (*J*) and electric field (*E*) i.e. *J.E*. The product (*J.E*) signifies the total

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power generated per unit volume due to any physical process occurring in the device [12]. If two or more physical processes occur in the device then the total *J.E* will be due to the contribution of each physical phenomenon. While FBEs are favorable for achieving a steep rise in drain current at lower gate lengths, the off-state tunneling can potentially limit the usable range of the device for dynamic memory applications. The trade-off between impact ionization induced hysteresis and tunneling limited off-state current is discussed in detail. The composite metric (*J.E*) is understood, evaluated and then utilized to optimize silicon JL transistor for steep switching applications with low values for off-state tunneling current. The work presents new possibilities to design JL transistor for energy efficient memory applications.

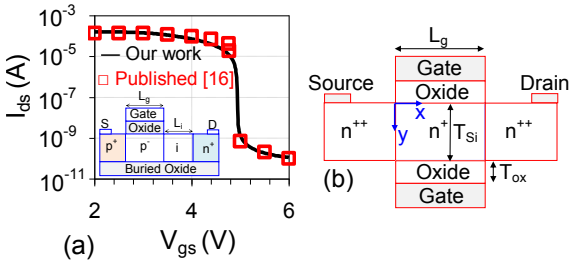

Fig.1 (a) Comparison of the simulated drain current (I_{ds}) - gate voltage (V_{gs}) characteristics with published experimental data [16] for steep switching Si Depletion Impact ionization MOS (DIMOS) transistor with gate length (L_g) of 0.8 μm. DIMOS device works on the principle of impact ionization and its schematic diagram is shown in inset of fig. 1(a). (b) Schematic diagram of Double Gate (DG) Junctionless (JL) transistor analyzed in the work. Source/Drain regions are counter doped to minimize the series resistance.

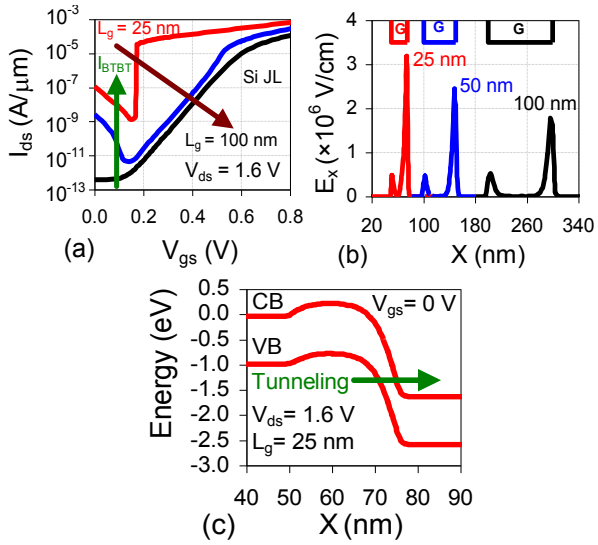

Fig. 2 (a) Drain current (I_{ds}) - voltage (V_{gs}) characteristics showing steep switching due to impact ionization and drain current increase at lower gate biases due to BTBT in Double Gate (DG) JL transistor. (b) Variation in lateral electric field (E_x) extracted at V_{gs} = 0 V along the *x*-axis at $y = T_{si}/2$ with varying gate length (L_g) from 100 nm to 25 nm. Lateral electric field under the gate for three different devices (100 nm, 50 nm and 25 nm) is shown in the same graph with gate (G) being indicated for each. (c) Variation in Conduction Band (CB) and Valence Band (VB) energy along the channel direction at V_{ds} = 1.6 V and V_{gs} = 0 V showing the tunneling direction of electrons in a DG JL MOSFET at L_g = 25 nm.

II. Simulation

In order to understand the occurrence of multiple physical phenomena (BTBT and FBEs) and their impact on the device performance, Double Gate (DG) JL transistors were analyzed with ATLAS simulation tool [15]. The ability of our simulations to capture essential aspects of FBEs and the associated steep increase in current due to impact ionization in Depleted Impact ionization MOS (DIMOS) devices was compared with experimental results of DIMOS device [16] and the same is shown in fig. 1*a*. JL devices (fig. 1*b*) were analyzed with gate length (L_g) varying from 100 nm to 25 nm with a channel doping (N_d) of 10^{19} cm^{-3}. The source/drain regions were heavily doped with 10^{20} cm^{-3} dopant atoms. A silicon film thickness (T_{Si}) of ~9 nm and gate oxide thickness (T_{ox}) of 1 nm was used in the work. In order to obtain a reasonable assessment of impact ionization in JL devices, the parameters (AN and BN) for electron and hole ionization coefficients (α_n, α_p) [15] were decreased by a factor of 2 to be consistent with the theory of Lee *et al*., [17] and Anderson *et al*., [18] for the requirement of minimum voltage to initiate impact ionization. Other relevant modules included in the analysis were field and concentration dependent Lombardi mobility model [19], non-local BTBT model, bipolar effects and bandgap narrowing [15]. The applicability of non-local BTBT model has been demonstrated in previous published works [20-21]. Also, the simulation methodology to incorporate impact ionization is consistent with approach of Mayer *et al*., [22].

III. Results And Discussion

Fig. 2*a* shows drain current (I_{ds}) - gate voltage (V_{gs}) characteristics of JL transistor for three different gate lengths (L_g) at a drain bias (V_{ds}) of 1.6 V. At L_g = 100 nm, a conventional subthreshold swing (*S*) of 60 mV/dec is observed, while at L_g = 50 nm, a marginally lower than 60 mV/dec swing is seen. At L_g = 25 nm, *S* lower than 5 mV/decade is evident. The improvement (reduction) in *S* is due to the increase in lateral electric field (E_x) i.e. from 1.8×10^6 V/cm (@ L_g = 100 nm) to 3.2×10^6 V/cm (@ L_g = 25 nm) as shown in fig. 2*b*. The relatively higher value of E_x at the gate edge towards the drain side at L_g = 25 nm provides sufficient energy to electrons to facilitate impact ionization. The electrons generated due to impact ionization contribute to I_{ds} whereas impact generated holes accumulate at lower potential region underneath the gate and forward bias source-channel junction. The successive accumulation of holes triggers FBEs, and thus, results in a sharp rise in I_{ds} with $S < 5$ mV/decade. Also seen in the graph is the degradation in I_{ds}-V_{gs} characteristics at V_{gs} lower than threshold voltage (V_{th}) where a higher value of E_x (@ L_g = 25 nm) at the gate edge towards the drain triggers tunneling of electrons from the channel to drain due to proximity between valence and conduction bands (fig. 2*c*) [5-6]. This causes an increase in the drain current for $V_{gs} <$ 0.15 V as shown in fig. 2*a*. The observed behavior of drain current at lower gate voltages in this work agrees qualitatively with the experimental work of Adell *et al*., [23], and reported simulation study by Hur *et al*., [6] indicating tunneling contribution at lower V_{gs} values. Results clearly indicate the benefit of dominant impact ionization in JL devices through lower *S* values, while the degradation in off-current due to BTBT limits the applicability of steep switching JL devices.

In order to confirm the increase in carrier concentration at lower V_{gs} due to BTBT with varying L_g, electron and hole concentrations were analyzed. Fig. 3*a-b* shows a comparison of hole (n_h) and electron (n_e) concentrations in DG JL devices

for L_g = 100 nm, 50 nm and 25 nm at V_{ds} = 1.6 V. The results are extracted at V_{gs} = 0 V along y-axis at midgate position (x = L_g/2, y). The increase in electric field i.e. from 1.8×10^6 V/cm to 3.2×10^6 V/cm increases the tunneling of electrons which results in ~2 orders of increase in minimum hole concentration in JL device (L_g = 25 nm) at V_{gs} = 0 V. The successive accumulation of holes underneath the gate (at lower V_{gs}) contributes to a positive potential, and hence, lowers the barrier between source and channel region which can be seen from the significant increase in peak n_e (fig. 3*b*) i.e. from ~10^8 cm^{-3} (L_g = 100 nm) to ~10^{15} cm^{-3} at L_g = 25 nm.

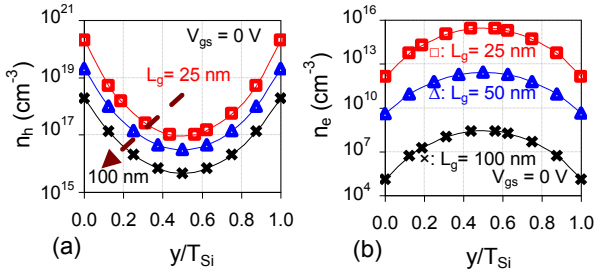

Fig. 3 Variation in (a) hole (n_h) and (b) electron (n_e) concentration along the y-direction for different gate lengths (100 nm, 50 nm and 25 nm) at V_{ds} = 1.6 V, V_{gs} = 0 V. Carrier concentration was extracted mid-gate position along the cutline at $x = L_g/2, y$.

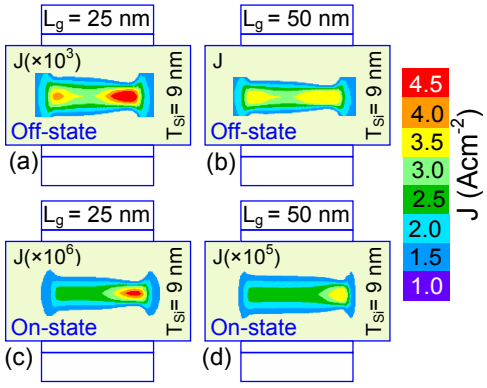

Fig. 4 2D Contour plot showing current density (J) in off-state at V_{gs} = 0 V in a JL transistor with gate length of (a) 25 nm and (b) 50 nm. 2D Contour plot of J in the on-state extracted at (V_{gs} - V_{th}) = V_{go} = 10 mV in a JL transistor with L_g of (c) 25 nm and (d) 50 nm. Results were extracted at V_{ds} = 1.6 V and T_{Si} = 9 nm.

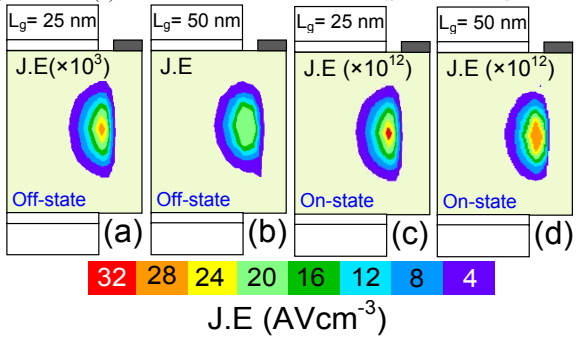

Fig. 5 Contour plot showing $J.E$ in the off-state (V_{gs} = 0 V) for L_g of (a) 25 nm and (b) 50 nm, and in the on-state (V_{go} = 10 mV) for L_g of (c) 25 nm and (d) 50 nm. As impact ionization and BTBT are significant towards the drain, contours (half structure) are shown in the semiconductor region corresponding to gate edge towards drain. Parameters are same as mentioned in fig. 4.

The impact of higher electron concentration due to BTBT and impact ionization can be seen from 2D contour plots (fig. 4*a*-*b*) of current density (J) extracted at two different gate biases i.e. at V_{gs} = 0 V (BTBT is dominant @ fig. 4*a*-*b*) and at V_{go} = V_{gs} - V_{th} = 10 mV (FBE is significant @ fig. 4*c*-*d*). The relatively higher J (~4.5×10^3 Acm^{-2}) at L_g = 25 nm in comparison to that (~3.5 Acm^{-2}) observed in device with L_g = 50 nm (fig. 4*b*) indicates a higher off-current (I_{off}) and translates into a higher value of $J.E$ due to BTBT in the off-state, and the same is undesirable. As the current density in 25 nm JL device is substantially high, a factor of 10^3 is mentioned in contour plot for comparison on the same legend (color bars) shown alongside the figures. The increase in I_{off} from ~10^{-13} A/μm to ~10^{-7} A/μm for L_g varying from 100 nm to 25 nm, respectively, corresponding to the different values of J, was shown in fig. 2*a*.

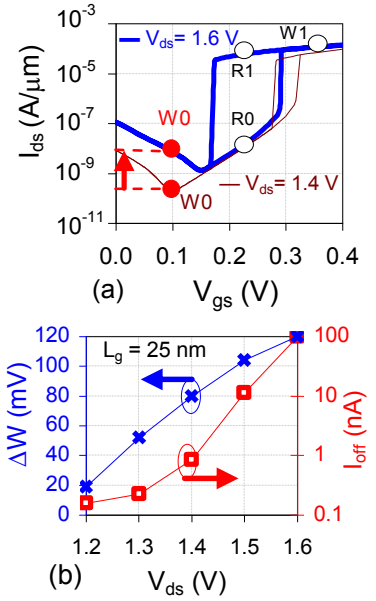

Fig. 6 (a) I_{ds}-V_{gs} characteristics with hysteresis in the forward and reverse sweeps of gate voltage at V_{ds} = 1.4 V and V_{ds} = 1.6 V. (b) Variation in hysteresis window (primary y-axis) and off-current (I_{off}) with V_{ds}.

On comparing fig. 4*c*-*d*, it is evident that ~10 times higher J is obtained at L_g = 25 nm at an overdrive (V_{go} = V_{gs} - V_{th}) of 10 mV (on-state) is indicative of a steep rise in current. This increase in current density in the on-state (just after V_{th}) is desirable as it reflects steep current transition. In steep switching devices, on-state is defined immediately after the threshold to benefit from the sharp current transition. At gate voltages much higher than threshold i.e. ~(500 mV + V_{th}), the performance of steep switching (S < 60 mV/dec) JL transistor and conventional (S = 60 mV/dec) JL device in terms of on-current is nearly same, and any advantage due to steep current transition is limited as holes recombine with the expanding electron channel and FBEs reduce. Results endorse the contribution of current density (J) through the product $J.E$ [13] apart from electric field (E_x). Higher $J.E$ values in the on-state (immediately after threshold) imply generation of sufficient number of electrons and holes due to impact ionization. An optimal device design for steep switching applications should exhibit a lower $J.E$ in the off-state to suppress BTBT while maintaining a high $J.E$ in the on-state (immediately after threshold) to yield a sharp increase in I_{ds} with S < 60

mV/decade. Thus, *J.E* is identified as a universal performance metric due to two different phenomenon (BTBT and FBEs) occurring in JL devices, and its optimization is necessary for enhanced performance.

Fig. 5*a-b* compares 2D contour plots of *J.E* for 25 nm and 50 nm JL devices at V_{gs} = 0 V (off-state) and fig. 5*c-d* shows *J.E* at V_{go} = 10 mV (on-state, immediately after threshold). Higher value (~10^3 times @ L_g = 25 nm) of *J.E* at V_{gs} = 0 V (off-state) is undesirable while the ~1.5 times higher value in the on-state (V_{go}= 10 mV) as shown in fig. 5*c-d* is beneficial to preserve the sharp rise in drain current. Next, we focus on 25 nm JL transistor to explore options to limit BTBT in the off-state while enhancing impact ionization in the on-state. In order to reduce *J.E* in off-state while maintaining higher values of the same in on-state, (i) reduction of drain bias (V_{ds}), (ii) adopting an underlap architecture, and (iii) simultaneous optimization of silicon film thickness (T_{si}) and drain bias (V_{ds}), can be adopted.

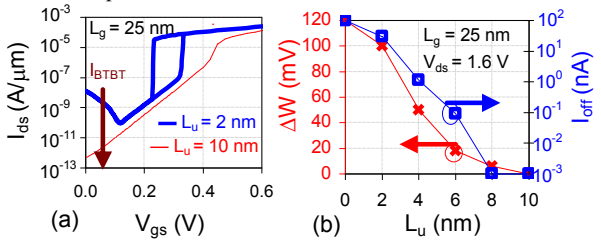

Fig. 7 (a) I_{ds}-V_{gs} characteristics for 25 nm JL device with underlap length (L_u) of 2 nm and 10 nm for forward and reverse sweeps of gate voltage. (b) Variation in hysteresis window (primary *y*-axis) and I_{off} (secondary *y*-axis) with varying L_u varying from 0 nm to 10 nm. V_{ds} was fixed at 1.6 V.

Fig. 6*a* shows I_{ds}-V_{gs} characteristics of JL device showing hysteresis at V_{ds} = 1.4 V and 1.6 V for forward and reverse sweeps of gate bias. The variation in hysteresis window and off-current (I_{off}) with varying V_{ds} is shown in fig. 6*b*. The occurrence of hysteresis is clearly visible at L_g = 25 nm while the same is suppressed at lower drain biases i.e. V_{ds} = 1.2 V (fig. 6*b*). Transfer characteristics shown in fig. 6*a* is interesting as it shows the potential of utilizing JL transistors for dynamic memory applications at lower gate lengths. The concern of operating at higher V_{ds} (1.6 V) is reflected in a higher I_{ds} corresponding to Write 0 operation which is nearly similar to that obtained for Read 0 operation, thus signifying the nearly similar values hole concentration which should not be the case. A lower V_{ds} (1.4 V) does reduce the current level of Write 0 in comparison to that for V_{ds} = 1.6 V. However, as the difference between threshold voltages corresponding to forward and reverse sweeps represents the hysteresis window (Δ*W*), a reduction in V_{ds} reduces the same owing to the lower degree of FBEs (fig. 6*b*) [13]. Also, *S* (although lower than 60 mV/decade) increase from 1 mV/decade to 15 mV/decade with V_{ds} increasing from 1.2 V to 1.6 V, respectively. The number of decades of current transition at threshold also decreases at lower V_{ds}. Threshold voltage (V_{th}) of JL device was extracted by transconductance-to-current ratio (g_m/I_{ds}) change method [24]. Hysteresis window defines Read 0 (R0) and Read 1 (R1) operation after writing the memory cell with Write 0 (W0) and Write 1 (W1), respectively (fig. 6*a*). W0 and W1 operations of dynamic memory are governed by the presence (storage) and absence, respectively, of holes that are generated due to impact ionization. Fig. 6*a* shows that it is possible to perform Write operation at V_{gs} ~0.1 V (for V_{ds} = 1.4 V) although with a reduced memory window (Δ*W* ~ 80 mV). While ×1.5 higher Δ*W* (~120 mV) achieved for V_{ds} = 1.6 V is beneficial to perform memory operation over wider range of V_{gs} along with the increased difference between states R0 and R1, I_{off} increases from 0.1 nA (@ V_{ds} = 1.2 V) to ~ 10^2 nA (@ V_{ds} = 1.6 V) (fig. 6*b*), and therefore negates any improvement in Δ*W*. In addition, as W0 state in dynamic memory corresponds to absence of holes, BTBT at lower V_{gs} results in a higher hole concentration which leads to the degradation in W0 state (fig. 6*a*). While reducing V_{ds} has its advantages, the reduction in memory window and reduced number of decades of current transition at threshold limits the potential of V_{ds} reduction for optimal performance. Also, BTBT current in the off-state is still existent although lower than that for V_{ds} = 1.6 V. Hence, lowering V_{ds} is not expected to balance the conflicting requirements of *J.E* in off and on states.

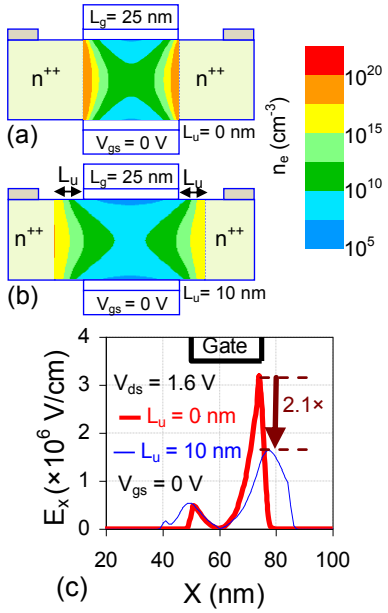

Fig. 8 2D contour plot showing electron concentration underneath the gate at zero bias (V_{gs} = V_{ds} = 0 V) for (a) L_u = 0 nm and (b) L_u = 10 nm. (c) Variation in lateral electric field (E_x) along the *x*-axis extracted at $y = T_{si}/2$, *x* in JL transistor designed with L_u = 0 nm and L_u = 10nm at V_{ds} = 1.6 V.

Authors in [6] have showed that off-state tunneling can be suppressed by designing JL devices with source/drain underlap (L_u). Fig. 7*a* shows I_{ds}-V_{gs} characteristics of JL transistor with L_u = 2 nm and 10 nm. While the underlap is beneficial to suppress off-state tunneling, it also results in a degradation in *S* values i.e. *S* increases from ~2 mV/decade (L_u = 0 nm) to ~10 mV/decade (L_u = 5 nm), and to ~40 mV/decade for an underlap of 10 nm. Fig. 7*b* shows the variation in hysteresis window (primary *y*-axis) and I_{off} (secondary *y*-axis) with varying underlap length from 0 nm to 10 nm. At L_u = 2 nm, Δ*W* ~ 100 mV is achieved with significantly higher value of I_{off} ~ 10 nA. While the increase in underlap length to ~10 nm is beneficial to suppress off-state tunneling, it also results in substantial degradation in impact ionization, and the associated memory window i.e. from ~100 mV (L_u = 2 nm) to ~0 mV (L_u = 10 nm) at V_{ds} = 1.6 V. Even at

a moderate underlap of 5 nm, the hysteresis window (~40 mV) is relatively suppressed.

In order to understand the trade-off between hysteresis window and tunneling governed off-current, 2D contour plots of electron concentration obtained at V_{gs} = V_{ds} = 0 V are shown in fig. 8*a*-*b*. JL transistor with an underlap causes the lateral electric field at the gate edge near to the drain to reduce (fig. 8*c*), and also increases the effective channel length (L_{eff}) in the subthreshold region [6]. The reduction in lateral electric field (fig. 8*c*) is beneficial for the off-state as it increases the tunneling width and lowers the generation of holes due to reduction in tunneling of electrons at lower V_{gs}. The reduced hole concentration in JL transistor with L_u = 10 nm in comparison to the device with L_u = 2 nm (for same L_g) results in higher barrier between source and channel. The impact of relatively higher barrier can be confirmed through the lower electron concentration underneath the gate in JL device with L_u = 10 nm (fig. 7*a*) in comparison to the device without underlap (fig. 7*a*). While the reduction in electric field is beneficial to suppress the tunneling, the longer L_{eff} reduces the current density (J). Therefore, the reduction in J deteriorates $J.E$ and hysteresis window. Results indicate that utilizing underlap architecture leads to the reduction of impact ionization and off-state tunneling, and therefore, is unlikely to be optimal for balancing the trade-off in $J.E$ values for off and on states.

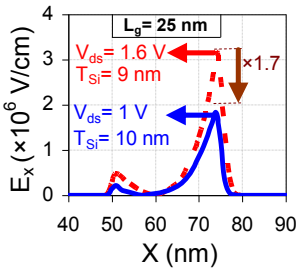

Fig. 9 Variation in lateral electric field (E_x) along x-axis extracted at (y = T_{si}/2, x) in JL transistor designed with (i) T_{si} = 9 nm @ V_{ds} = 1.6 V and (ii) T_{si} = 10nm @ V_{ds} = 1 V. The gate bias was fixed at 0 V.

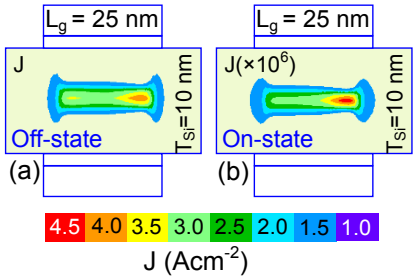

Fig. 10 2D contour plot showing current density (J) at (a) V_{gs} = 0 V and (b) V_{go} = 10 mV in JL transistor designed with T_{si} = 10 nm at L_g = 25 nm. V_{ds} is fixed at 1 V.

The next option is to explore the feasibility of utilizing optimal values of silicon film thickness (T_{si}) and drain bias (V_{ds}) to suppress BTBT in the off-state while maintaining higher $J.E$ in the on-state. In order to curtail BTBT at lower V_{gs} while enhancing impact ionization (in on-state), JL devices should be designed with maximum possible T_{si} so as to facilitate full depletion (in off-state for a given set of film thickness, doping, gate oxide and workfunction), and also, operate at lower V_{ds}. While reducing V_{ds} lowers the electric field in the off-state, an increase in T_{si} (while maintaining full depletion) will enhance J in the on-state due to an increase in the number of carriers which facilitate impact ionization. Full depletion in off-state with maximum possible T_{si} ensures low I_{off} while a reduction in V_{ds} further reduces BTBT. Thus, the advantage is two-fold i.e. (i) lower V_{ds} reduces E_x and $J.E$ will be minimized in the off-state, and (ii) $J.E$ will be enhanced in the on-state due to the greater number of carriers due to the use of maximum possible T_{si} (permitting full depletion in off-state)

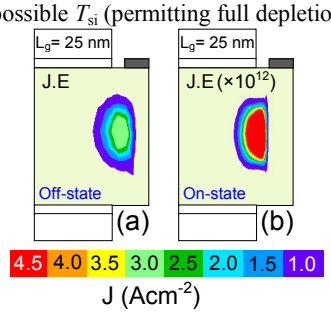

Fig. 11 2D contour plot showing $J.E$ at (a) V_{gs} = 0 V and (b) V_{go} = 10 mV in JL transistor designed with T_{si} = 10 nm at L_g = 25 nm. V_{ds} is fixed at 1 V.

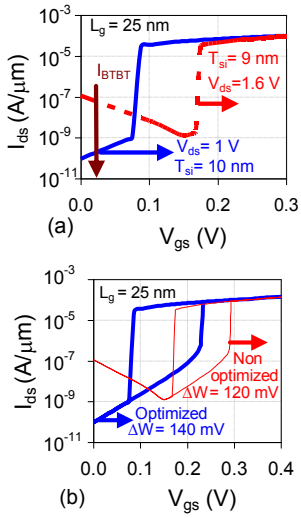

Fig. 11 (a) Comparison of I_{ds}-V_{gs} characteristics for JL transistor with T_{si} = 9 nm, V_{ds} = 1.6 V and T_{si} = 10 nm, V_{ds} = 1 V. (b) I_{ds}-V_{gs} characteristic of JL device for forward and reverse sweeps of gate voltage corresponding to fig. 11*a*. All results are shown for L_g = 25 nm.

In order to confirm the advantage gained by adopting a universal metric $J.E$ for optimizing the device in different regions of operation, JL devices were designed with a film of 10 nm and operated at V_{ds} = 1 V (lower as compared to the previous case of V_{ds} = 1.6 V). Clearly, ×1.7 reduction in E_x (fig. 9) at gate edge towards the drain suppresses BTBT, and thus, reduces J to ~4 Acm^{-2} (in comparison to non-optimized result with J = ~4.5×10^{3}Acm^{-2} as shown in fig. 4*a*) in the off-state. The benefit of a marginal increase in T_{si} despite operating at lower V_{ds} of 1 V (with respect to 1.6 V in fig. 4*c*) is reflected in a nearly similar value of J (~4.5×10^6 Acm^{-2}) at V_{go} = 10 mV (on-state). The composite metric ($J.E$) shown in fig. 11*a*-*b* for off and on states, respectively, demonstrates the advantage in comparison to non-optimized devices (figs. 5*a*-*c*). Due to heavy doping, JL devices require precise control of film thickness for optimal performance. The results also indicate the sensitivity of JL devices on film thickness due to higher doping

[13]. Nevertheless, optimal values of film thickness and drain bias are helpful to achieve best possible performance of a steep switching JL transistor with low values of BTBT and off-current while maintaining higher hysteresis window. Fig. 11 shows the comparison of I_{ds}-V_{gs} characteristics of an optimized and non-optimized 25 nm JL MOSFET in which the enhanced degree of impact ionization can be seen through the lowering of V_{th} from 175 mV (@ T_{Si} = 9 nm, V_{ds} = 1.6 V) to 85 mV (@T_{Si} = 10 nm, V_{ds} = 1 V) with a sufficient number of decades of current transition. The benefit in terms of an improvement in the number decades of steep current transition yields an enhanced hysteresis window with low off-current to perform memory operation (Write 0) over a wider range of gate biases.

IV. Conclusion

The work demonstrates unique approach of balancing conflicting requirements through an insightful analysis for achieving lower off-current and a higher on-current without compromising the sub-60 mV/decade current transition. The universal optimization metric i.e. *J.E* is particularly interesting when multiple physical phenomenon such as impact ionization and band-to-band tunneling occur in a device, and the optimization of each is critical to enhance the performance. The trade-off between wider hysteresis window and off-state tunneling in a non-optimal device reveals that memory operation cannot be sustained. Adopting *J.E* as a composite and pragmatic parameter to aid in design optimization of JL devices with thicker film (which can be depleted at zero bias) and operating at a lower drain bias reduces the tunneling current (lower *J.E*) appreciably while enhancing the impact ionization induced steep switching (higher *J.E*). The work provides new insights into the functionality, design and optimization of steep switching JL MOSFETs for memory applications at lower gate lengths.

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References

[1] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O. Neill, A. Blake, M. White, A. Kelleher, B. Mccarthy, and R. Murphy, "Nanowire transistors without junctions," *Nature. Nanotechnology,* vol. 5, no. 3, pp. 225–29, Feb. 2010.

[2] C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J. P. Colinge, "Low subthreshold slope in junctionless multigate transistors," *Appl. Phys. Lett.*, vol. 96, no. 10, 102106, Mar. 2010.

[3] R. Yu, A.N. Nazarov, V.S. Lysenko, S. Das, I. Ferain, P. Razavi, M. Shayesteh, A. Kranti, R. Duffy and J.-P. Colinge, "Impact ionization induced dynamic floating body effect in junctionless transistors," *Solid. State. Electron.*, vol. 90, pp. 28–33, Mar. 2013.

[4] S.M. Lee and J.T. Park, "The impact of substrate bias on the steep subthreshold slope in junctionless MuGFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3856-61, Nov. 2013.

[5] S. Gundapaneni, M. Bajaj, R.K. Pandey, Kota V. R. M. Murali, S. Ganguly and A. Kottantharayil, "Effect of Band-to-Band Tunneling on Junctionless Transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1023-29, Apr. 2012.

[6] J. Hur, B.-H. Lee, M.-Ho Kang, D.-C. Ahn, T. Bang, S-B. Jeon, and Y.-K. Choi, "Comprehensive analysis of gate-induced drain leakage in vertically stacked nanowire FETs: Inversion-mode versus junctionless mode," *IEEE Electron Device Lett*., vol. 37, no. 5, pp. 541-544, May 2016.

[7] T.A. Oproglidis, T.A. Karatsori, S. Barraud, G. Ghibaudo, C.A. Dimitriadis, "Leakage current conduction in metal gate junctionless nanowire transistors," *Solid. State. Electron*., vol. 131, pp. 20–23, May 2017.

[8] C. Sun, R. Liang, L. Liu, J. Wang, and J. Xu, "Leakage current of germanium-on-insulator-based junctionless nanowire transistors," *Appl. Phys. Lett.*, vol. 107, no. 26, pp. 132105, Sep. 2015.

[9] S. Sahay and M.J. Kumar, "Insight into lateral band-to-band-tunneling in nanowire junctionless FETs," *IEEE Trans. on Electron Devices*, vol. 63, no. 10, pp. 4138-42, Oct. 2016.

[10] I. Ferain, C.A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors," *Nature*, vol. 479, no. 7373, pp. 310-16, Nov. 2011.

[11] A.Boudou and B.S. Doyle, "Hysteresis *I-V* effects in short channel silicon MOSFET's," *IEEE Electron Device Lett.,* vol. 8**,** pp. 300-2, 1987.

[12] K.E. Moselund, D. Bouvet, V. Pott, C. Meinen, M. Kayal, and A. M.Ionescu, "Punch-through imapct ionization MOSFET (PIMOS): From devcie principle to applications," *Solid-State Electron.*, vol. 52, 1336-44, 2008.

[13] M.S. Parihar, D. Ghosh, and A. Kranti, "Single transistor latch phenomena in junctionless transistors", *J. Appl. Phys.*, vol. 113, pp. 184503, 2013.

[14] M.S. Parihar, D. Ghosh, G. A. Armstrong, R. Yu, P. Razavi, and A. Kranti, "Bipolar effects in unipolar junctionless transistors," *Appl. Phys. Lett.*, vol. 101, pp. 093507, 2012.

[15] ATLAS Users Manual, Silvaco.

[16] C. Onal, R. Woo, S. H-Y Koh, P. B. Griffin and J.D. Plummer, A novel depletion-IMOS (DIMOS) device with improved reliability and reduced operating voltage," *IEEE Electron Device Lett*., vol. 30, no. 1, pp. 64-67, Jan. 2009.

[17] C. L. Anderson and C. R. Crowell, "Threshold energies for electron-hole pair production by impact ionization in semiconductors," Physical Review B, vol. 5, no. 6, pp. 2267–72, Mar. 1972.

[18] C.A. Lee, R. A. Logan, R. L. Batdorf, J. J. Kleimack and W. Wiegmann, "Ionization Rates of Holes and Electrons in Silicon," *Physical Review B*, vol. 134, no. 3A, pp. A761–A773, May 1964.

[19] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Trans. Computer Aided Design of Integrated Circuits*, vol. 7, no. 11, pp. 1164-1171, 1988.

[20] A. Biswas, S. S. Dan, C. Le Royer, W. Grabinski, A. M. Ionescu, "TCAD simulation of SOI TFETs and calibration of non-local band-to-band tunneling model", *Microelectronic Engineering*, vol. 98, no. 10, pp. 334-337, Jul. 2012.

[21] K. Fukuda,T. Mori, W. Mizubayashi, Y. Morita, A. Tanabe, M. Masahara, T. Yasuda, S. Migita, and H. Ota, "A compact model for tunnel field-effect transistors incorporating nonlocal band-to-band tunneling," *Journal of Appl. Phys*., vol. 114, no. 14, 144512, Oct. 2013.

[22] F. Mayer, C. Le Royer, G. Le Carval, L. Clavelier and S. Deleonibus, "Static and dynamic TCAD analysis of IMOS performance: from the single device to the circuit," *IEEE Trans. Electron Devices,* vol. 53 pp. 1852-57, 2006.

[23] P. C. Adell, H. J. Barnaby, R. D. Schrimpf and B. Vermeire, "Band-to-Band Tunneling (BBT) induced leakage current enhancement in irradiated fully depleted SOI devices," *IEEE Trans. on Nuclear Science*, vol. 54, no. 6, pp. 2174-80, Dec. 2007.

[24] T. Rudenko, V. Kilchytska, Mohd. Khairuddin Md Arshad, J.-P. Raskin, A. Nazarov and D. Flandre, "On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part II—effect of drain voltage," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4180–4188, Dec. 2011.