Machine Learning based Power Efficient Approximate 4:2 Compressors for Imprecise Multipliers

Lavanya Maddisetti
C-ACRL, Department of ECE
Vardhaman College of Engineering
Shamshabad, Telangana, India
lavanya.maddisetty@gmail.com

JVR Ravindra
C-ACRL, Department of ECE
Vardhaman College of Engineering
Shamshabad, Telangana, India
jayanthi@ieee.org

***Abstract*—Machine Learning (ML) has been one of the applications of approximate circuits. These circuits, part of approximate computing, can be implemented using either probabilistic pruning or inexact logic minimization. Since low power consumption and smaller silicon area are the critical parameters in portable devices, approximate circuits have been the current topic for discussion. This paper presents a 4:2 compressors with inexact logic minimization by flipping some of the output bits considering efficiency/accuracy into account. The proposed 4:2 compressor has been utilized in an 8×8 Dadda multiplier and average power, area and propagation delay of the architectures have been computed. All the simulations have been performed using spectre simulator of Cadence Design Systems in 45nm technology node. To find the difference between the exact and approximate proposed circuits, error analysis has been performed using MATLAB. The application idea of this paper is to employ Python TensorFlow in Google Co Laboratory© to Upload, download the approximate 4:2 compressor which has been implemented in Cadence Virtuoso.**

I. Introduction

Compressors have become essential components for partial product reduction stage of multiplier architectures. Formerly, different adders like carry save adders were used for partial product reduction but with the requirement of low power and smaller area, adders were replaced with different order compressors such as 3:2, 4:2, 5:2 [1].

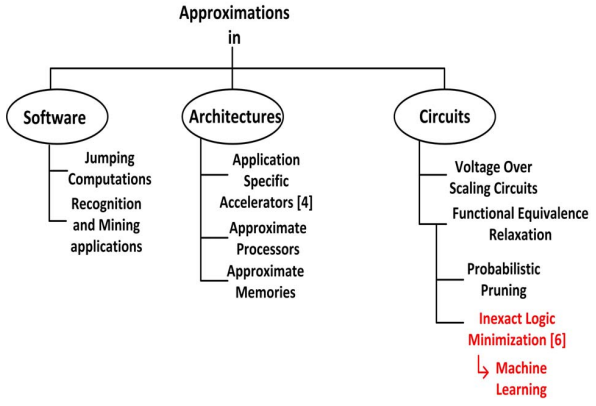

Fig. 1. Taxonomy of Approximate Computing

With the growth in usage of portable devices, smaller area and lower power have been evolved into extremely important parameters. Thus approximate computing need to be employed in digital architectures such that the desired power is obtained. Approximate computing has been given kind attention where accuracy is not critical in applications like signal and video processing hardware, application specific accelerators, machine learning etc. Fig. 1 displays different applications of approximate computing and narrowed it to VLSI work which has been employed in this work.

II. Related Work

Veeramachaneni *et.al* have proposed 4:2 compressors with XOR-XNOR circuits and transmission gate multiplexers with complemented and uncomplemented outputs [1]. In [2], different XOR-XNOR circuits have been displayed with different number of transistors, one eliminating the disadvantage of the other. The proposed XOR-XNOR circuit is employed in 4:2 and 5:2 compressors. A transmission gate multiplexer using CMOS logic with a buffer to enhance the current carrying capacity was used in [3] to employ it in 4:2 compressor. Since the usage of portable devices are increasing and to reduce the supply voltage and in turn power consumption, the concept of approximate computing has been evolved in VLSI architectures. Approximate computing is being utilized in numerous applications and is exhibited in [4]. Approximate compressors were proposed in [5], employing spintronic devices consisting of magnetic domain wall motion stripe and magnetic tunnel junction, thus it was utilized in Discrete Cosine Transform. Avinash *et.al* have proposed two approximate functional equivalence relaxation techniques namely probabilistic pruning and inexact logic minimization for approximating digital circuits and the later approach is shown in [6]. Approximate compressors with half of the outputs when compared with inputs was shown in [7] where the output weights of proposed compressor has same as input weights. Two 4:2 compressor designs were proposed in [8] where in the design1 has 12 incorrect outputs out of 32 outputs and in design2 four incorrect outputs out of 16 outputs of 4:2

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00057

compressors were shown. These compressors were utilized in Dadda multipliers and error analysis was done with image processing applications.

Different error metrics like error distance (ED), mean error distance (MED) and normalized error distances (NED) were proposed in [9-10] which can be utilized in error analysis of compressors and multipliers. A tool was proposed in [11] where the user can mention the error rate that the circuit can tolerate such that the imprecise multiplier with minimized performance metrics like area, delay and power provides specified accuracy. The application of ML on existing CAD algorithms to build new hardware is presented in [12]. A methodology developed into tool named ABACUS was proposed in [13] for generating automatic synthesized approximate circuits from verilog code. In [14], a methodology was presented for automatic generation of approximate circuits. This was achieved by including a module in the ASIC design flow such that there was substantial reduction in power, area and delay.

III. Proposed 4:2 Compressor Model

This research work employs probabilistic logic minimization on exact 4:2 compressor, where bit flipping in the minterms of Boolean functions of SUM, Carry and C_{out} is done to minimize the number of literals, thereby reducing power consumption, area and delay of the circuit. To identify the favorable bit flips, different combinations are attempted at the expense of error which is proportional to the number of bit flips introduced. After implementing this process on any exact circuit, the size of the circuitry should decrease with less error rate.

Since MSB's plays important role than LSB's in producing the result, lower order bits of 4:2 compressor are flipped from 1's to 0's which produces an error rate (ratio of no. of inexact outputs to correct outputs) of 25% without loss in the count of number of inputs and outputs. The bits can be flipped either from '1 to 0' or '0 to 1', but in this paper '1 to 0' is chosen to reduce the size of the circuitry. C_{out}, Carry, SUM bits are flipped by 8, 4, 8 in number respectively. The Sum, Carry and C_{out} k-maps are shown from Fig. 2 to Fig. 4.

The actual minterms of SUM in exact 4:2 compressor is given by eq.(1)

$$\text{Sum} = \sum \text{m} \left(\begin{array}{c} 1,2,4,7,8,11,13,14,16,19,21, \\ 22,25,26,28,31 \end{array} \right) \quad (1)$$

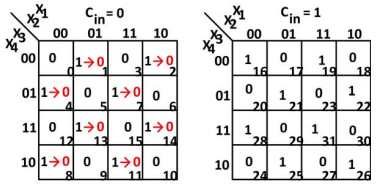

Fig. 2. SUM: a) Lower Order bits flips to '0' b) Exact Higher Order bits

After flipping lower order bits, the Boolean function of SUM is reduced to

$$\text{Sum} = \sum \text{m}\,(16,19,21,22,25,26,28,31) \quad (2)$$

For this approximated SUM, the Boolean expression is represented as eq.(6)

$$\begin{aligned} \text{Sum} = {} & \text{C}_{\text{in}}\text{X}_1'\text{X}_2'\text{X}_3'\text{X}_4' + \text{C}_{\text{in}}\text{X}_1\text{X}_2\text{X}_3'\text{X}_4' + \\ & \text{C}_{\text{in}}\text{X}_1\text{X}_2'\text{X}_3\text{X}_4' + \text{C}_{\text{in}}\text{X}_1'\text{X}_2\text{X}_3\text{X}_4' + \\ & \text{C}_{\text{in}}\text{X}_1'\text{X}_2'\text{X}_3\text{X}_4 + \text{C}_{\text{in}}\text{X}_1\text{X}_2\text{X}_3\text{X}_4 + \\ & \text{C}_{\text{in}}\text{X}_1\text{X}_2'\text{X}_3'\text{X}_4 + \text{C}_{\text{in}}\text{X}_1'\text{X}_2\text{X}_3'\text{X}_4 \end{aligned} \quad (3)$$

$$\text{Sum} = \text{C}_{\text{in}}\left[(\text{X}_1 \oplus \text{X}_2)'(\text{X}_3 \oplus \text{X}_4)' + (\text{X}_1 \oplus \text{X}_2)(\text{X}_3 \oplus \text{X}_4)\right] \quad (4)$$

For Carry,

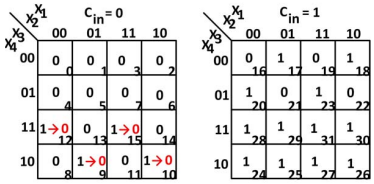

Fig. 3. Carry: a) Lower Order bits flips to '0' b) Exact Higher Order bits

The actual minterms of Carry in exact 4:2 compressor is given by eq.(7)

$$\text{Carry} = \sum (9,10,12,15,17,18,20,23,24,25,26,27,28,29,30,31) \quad (5)$$

After making lower order bits zeros, the carry minterms are reduced to

$$\text{Carry} = \sum (17,18,20,23,24,25,26,27,28,29,30,31) \quad (6)$$

$$\begin{aligned} \text{Carry} = {} & \text{C}_{\text{in}}\text{X}_4 + \text{C}_{\text{in}}\text{X}_1'\text{X}_2'\text{X}_3 + \text{C}_{\text{in}}\text{X}_1\text{X}_2\text{X}_3 + \\ & \text{C}_{\text{in}}\text{X}_1\text{X}_2'\text{X}_3' + \text{C}_{\text{in}}\text{X}_1'\text{X}_2\text{X}_3' \end{aligned} \quad (7)$$

$$\begin{aligned} = {} & \text{C}_{\text{in}}\text{X}_4 + \text{C}_{\text{in}}\text{X}_3\left(\text{X}_1'\text{X}_2' + \text{X}_1\text{X}_2\right) + \\ & \text{C}_{\text{in}}(\text{X}_1 \oplus \text{X}_2)'\left(\text{X}_1\text{X}_2' + \text{X}_1'\text{X}_2\right) \end{aligned} \quad (8)$$

For C_{out},

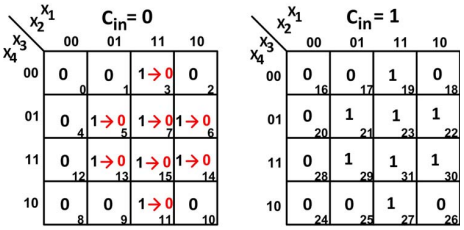

Fig. 4. C_{out}: a) Lower Order bits flips to '0' b) Exact Higher Order bits

$$\text{C}_{\text{out}} = \text{C}_{\text{in}}\left[\text{X}_1\text{X}_2 + \text{X}_1\text{X}_3 + \text{X}_2\text{X}_3\right] \quad (9)$$

$$\text{C}_{\text{out}} = \text{C}_{\text{in}}\left[\text{X}_1(\text{X}_1 \oplus \text{X}_2)' + \text{X}_3(\text{X}_1 \oplus \text{X}_2)\right] \quad (10)$$

From the above approximated equations, the proposed approximated 4:2 compressor is obtained as in Fig. 5.

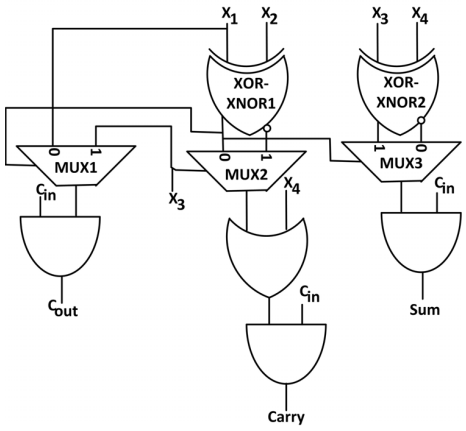

Fig. 5. Proposed Approximate 4:2 Compressor

On comparison of exact [1] and approximated 4:2 compressor, the number of components is increased in the form of AND and OR gates in the proposed structure but the XOR-XNOR and MUX circuits of the exact compressor is using increased number of transistors, which increases the power consumption of this circuit and also the multiplier structure. The power consumption and circuit size of the proposed 4:2 compressor has been reduced due to usage of all pass transistor logic based modules like AND, OR, 2T MUX and 6T XOR-XNOR and the transistor count of the proposed compressor is reduced to 34 from 52 [2] and 50 [1].

In the proposed design the maximum number of bit flips is only 8 and hence the error rate is 25%. When compared the proposed design with [8], the error rate of design1 and design2 in it are 37.5% and 25% respectively. The error rate of the proposed design is same as the design2 of [8] but the number of inputs is only four with the removal of carry C_{in} in [8]. In the proposed design, the number of inputs is same as the exact compressor but with little increase in the transistor count and power consumption than [8].

IV. Proposed 4:2 Compressor in Parallel Multipliers

Out of all the parallel multipliers, Dadda multiplier is the fastest one. Hence, in this work, multiplication operation is performed using this technique. For the three phases of multiplication, basic AND gates were employed to generate the partial products, Carry Save and Carry Propagate Adders were used for second and third stages respectively in the literature. Out of the three, the second stage is the critical one in the design of a multiplier since it slows down the operation and consumes more power. Thus, compressors are being employed in the second stage which reduces the power consumption and speeds up the operation of the entire multiplier circuit. The multiplier structure with exact compressors is shown in Fig. 6.

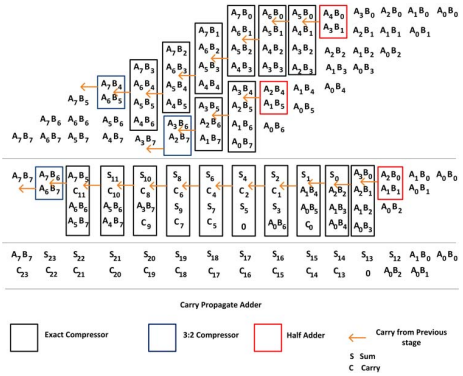

Fig. 6. Multiplier with Exact Compressors

In this section, the proposed approximate compressor is placed to make an exact multiplier as approximate one. An n=8 Dadda multiplier is designed in this work employing AND gates, the proposed approximated 4:2 compressor in the second stage and an exact carry propagate adder in the third stage.

In this paper, five Dadda multipliers have been simulated.

- The first multiplier employs all exact 4:2 compressors of [2].
- The second multiplier also employs all exact 4:2 compressors of [1].
- The third multiplier uses exact multipliers of [2] in the first stage of Dadda multiplier and proposed approximated 4:2 compressor in the second stage. Exact compressors are utilized in the first stage to enable approximations only from the second stage.
- The fourth multiplier uses exact multipliers of [1] in the first stage of Dadda multiplier and proposed approximated 4:2 compressor in the second stage.
- The fifth multiplier uses all approximate proposed 4:2 compressors in the first and second stages of Dadda multiplier.

The first two are exact multipliers with zero error distance but consumes more power with increased delay. The third and fourth are partially approximate multipliers since only one stage of the multiplier is utilizing approximate compressor. The fifth is completely approximate multiplier since it is employing all approximate multipliers and thus error distance increases while power consumption and area decreases. The architectures of third and fourth multipliers are not shown here as the the structure looks same as Fig. 6 but the exact compressors in stage1 is replaced with approximate 4:2 compressor and the fifth multiplier has all proposed compressors. The architecture of the multipliers does not vary since there is no change in number of inputs and outputs.

V. Results and Discussions

This section describes the performance and error metrics like power, delay, area and error distance, MED, NMED [9-10] respectively of 4:2 compressors and different multipliers.

A. Simulation Results of Compressors

All the simulations have been performed using spectre simulator of Cadence Design Systems in 45nm technology node. Exact compressors of [1-2] are executed and design 1 of [8] is implemented in different ways as shown in Table I, also the transistor count of each 4:2 compressor is given in the same.

TABLE I
TRANSISTOR COUNT OF 4:2 COMPRESSORS

Exact and Approximate 4:2 Compressors	Modules Employed	No. of Transistors in Each Module	Total Transistor Count
Exact 4:2 compressor[2] (4:2[2])	3 XOR-XNORs	10	52
	1 XOR	6	
Exact 4:2 compressor[1] (4:2[1])	2 2-input MUX	8	50
	2 XOR-XNORs	12	
	4, 2-input MUX	6	
	1 Inverter	2	
Design1 of [8] using PTL (14:2[8])	5 PTL NORs	6	42
	2 PTL XNORs	6	
Design1 of [8] using CMOS NORs (24:2[8])	5 CMOS NORs	4	32
	2 PTL XNORs	6	
Design1 of [8] using CMOS inverter based NORs (34:2[8])	5 CMOS NORs	4	28
	2 Inverter		
	Based XNORs	4	
Proposed	2 XOR-XNORs	6	34
	3 2-input MUX	2	
	3-ANDs	4	
	1-OR	4	

Design 2 of [8] is not considered in this research work since it has only four inputs. Area, delay and power consumption of all the above mentioned compressors are simulated in 45nm technology using Virtuoso Schematic XL Editor and Virtuoso Layout GXL of Cadence. The comparison of the performance metrics are shown in Table II.

According to the transistor count, the power consumption and area of the circuits are varying. The approximate design 1 of [8] utilizing 28 transistors has consumed least power than the proposed one of this work, since the maximum number of errors in the proposed is only 8 where as in the design 1 of [8], the errors are 12. i.e, as the error rate (no. of error outputs per total number of outputs) is increasing the size of the circuitry is decreasing. To improve the accuracy of the proposed 4:2 compressor, little difference in the size of the circuitry can be accepted. Fig. 7 displays the average power, Delay, Area and transistor count of 4:2 compressors.

TABLE II
AVERAGE POWER, DELAY AND AREA OF 4:2 COMPRESSORS

Exact and Approximate 4:2 Compressors	Average Power Consumption (nW)	Delay (nS)	Area(nm^2)
Exact 4:2 compressor[2]	344.7	20.195	37.118
Exact 4:2 compressor[1]	178.9	20.2	29.893
Design1 of [8] using PTL	162.7	0.1414	25.439
Design1 of [8] using CMOS NORs	126	0.05	20.118
Design1 of [8] using inverter based XNORs	102.4	0.05	18.923
Proposed	110	15.615	20.34

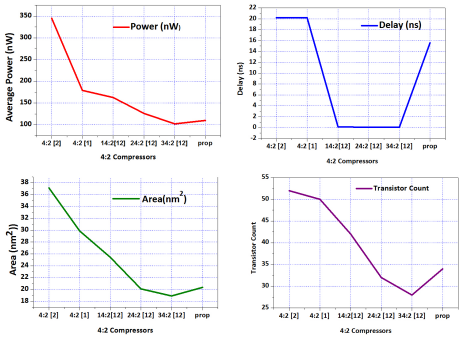

Fig. 7. Performance Metrics of 4:2 Compressors

Error metrics discussed in the introduction section by various researchers [9-10] is implemented on the above 4:2 compressors. The ED, MED and NED of exact and approximate 4:2 compressors are tabulated in Table III.

TABLE III
ERROR METRICS OF 4:2 COMPRESSORS

Compressors	Pass Rate (%)	Error Distance	MED (10^{-3})	NED (10^{-4})
Exact compressor [1-2]	100	0	0	0
Design1 of [8]	62.5	0.375	10.17	3.662
Proposed	75	0.25	7.812	2.441

The ED is zero for the first two as they are exact, for design 1 of [8] and exact compressor, C_{out}, Carry and SUM bits differ by 6, 8, 8 and between the proposed and exact compressors the C_{out}, Carry and SUM differ by 8, 4, 8 bits.

B. Simulation Results of Multipliers

This part of the experimental results explains different multipliers in which the proposed 4:2 compressor has been

placed in the partial product reduction stage of the multiplier. All the five multipliers discussed in section IV are simulated in 45nm technology node using Cadence Virtuoso schematic XL and Layout GXL and found average power consumption, delay and area. The circuit measures of 8×8 Dadda multiplier are shown in Table IV.

TABLE IV
POWER, AREA AND DELAY OF DIFFERENT MULTIPLIERS

Designs	Multiplier Design	Power (uW)	Area (nm^2)	Delay (ns)
Mul D1	Exact Multiplier using [2] Compressors	151.6	6617.823	0.097
Mul D2	Exact Multiplier using [1] Compressors	124.33	6104.297	9.98
Mul D3	Approximate Multiplier using [2] and proposed Compressors	89.35	5960.609	0.098
Mul D4	Approximate Multiplier using [1] and proposed Compressors	83.18	5720.653	10.13
Mul D5	Approximate multiplier using Proposed compressors	38.76	5410.336	9.809

The approximate 4:2 compressor design 1 of [8] has been implemented in different ways employing pass transistor logic and CMOS logic in NOR and XNOR gates, the combinations are shown in Table I. As per the transistor count of 4:2 compressors, exact and approximate, the area and power consumption of the multipliers are varying. The first and third stages in all the above multipliers are same and are exact (not approximated) modules, in the second stage the 4:2 compressors have been replaced according to the type of the multiplier implementation. Fig. 8 displays the performance metrics of multipliers.

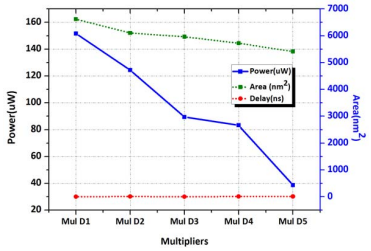

Fig. 8. Performance Metrics of Multipliers

1) Error Analysis: The accuracy measures in comparison with the approximate and exact has been done for which transient simulation is performed for the given binary inputs A[0-7] and B[0-7] with a stop time of 100ns. Error distance of a multiplier is absolute difference between exact product (P) and approximate product (P'), which is calculated for every 5ns of time period from 0ns to 100ns. All these are performed using MATLAB. As an example, ED, MED and NED calculations for the time period 10ns to 15ns is taken and P, P'are shown in Fig. 9

```
  7 6 5 4 3 2 1 0
  0 1 0 0 0 1 1 1  A
  1 0 0 1 0 1 0 1  B
-----------------------
0 0 1 0 1 0 0 1 0 1 0 1 0 0 1 1 ←P
0 1 1 1 1 0 1 1 0 1 1 1 0 1 1 1 ←P'
```

Fig. 9. Exact and Approximate Products

$$\mathrm{ED} = \mathrm{P} - \mathrm{P}'[9] \tag{11}$$

$$\mathrm{ED} = \mathrm{A}\sum_{\mathrm{i}=0}^{15}\mathrm{B_i}2^{\mathrm{i}} - \mathrm{A}\sum_{\mathrm{i}=0}^{15}\mathrm{B_i}2^{\mathrm{i}} \tag{12}$$

$$= \left[\begin{array}{l} 2^{15}(0)+2^{14}(0)+2^{13}(1)+2^{12}(0)+2^{11}(1)+ \\ 2^{10}(0)+2^{9}(0)+2^{8}(1)+2^{7}(0)+2^{6}(1)+ \\ 2^{5}(0)+2^{4}(1)+2^{3}(0)+2^{2}(0)+2^{1}(1)+2^{0}(1) \end{array}\right] - \left[\begin{array}{l} 2^{15}(0)+2^{14}(1)+2^{13}(1)+2^{12}(1)+2^{11}(1)+ \\ 2^{10}(0)+2^{9}(1)+2^{8}(1)+2^{7}(0)+2^{6}(1)+ \\ 2^{5}(1)+2^{4}(1)+2^{3}(0)+2^{2}(1)+2^{1}(1)+2^{0}(1) \end{array}\right] \tag{13}$$

$$= \left[\begin{array}{l} 2^{14}(0)+2^{12}(0)+2^{9}(0)+ \\ 2^{5}(0)+2^{2}(0) \end{array}\right] - \left[\begin{array}{l} 2^{14}(1)+2^{12}(1)+2^{9}(1)+ \\ 2^{5}(1)+2^{2}(1) \end{array}\right] \tag{14}$$

$$= \left[\begin{array}{l} 2^{14}(|0-1|)+2^{12}(|0-1|)+2^{9}(|0-1|)+ \\ 2^{5}(|0-1|)+2^{2}(|0-1|) \end{array}\right] \tag{15}$$

$$= 21028 \tag{16}$$

All the EDs from 0 to 100ns are added to get ED. To find MED [10]

$$\mathrm{MED} = \sum_{\mathrm{A,B}} \mathrm{P_A}(\mathrm{A}).\mathrm{P_B}(\mathrm{B}).\mathrm{ED}(\mathrm{A},\mathrm{B}) \tag{17}$$

$$= \frac{1}{2^{\mathrm{n}}}.\frac{1}{2^{\mathrm{n}}}.\sum_{\mathrm{A,B}} \mathrm{ED}(\mathrm{A},\mathrm{B}) \tag{18}$$

$$= \frac{\sum\limits_{\mathrm{A,B}} \mathrm{ED}(\mathrm{A},\mathrm{B})}{2^{2\mathrm{n}}} = \frac{199139}{2^{16}} = 3.0386 \tag{19}$$

$$\mathrm{NED} = \frac{\mathrm{MED}}{(2^{\mathrm{n}}-1)^2} = 4.6730\times10^{-5} \tag{20}$$

The MED, NED for all the above multipliers are found as shown in Table V.

TABLE V
ERROR ANALYSIS OF MULTIPLIERS

Multiplier Design	MED	NED(10^{-5})
Exact Multiplier using Exact Compressors	0	0
Approximate Multiplier using Exact and proposed compressors	3.0386	4.673
Approximate Multiplier using only Design 1 of [8]	5.0815	7.8146
Approximate multiplier using Proposed compressor	4.196	6.452

VI. APPLICATION: MACHINE LEARNING IN APPROXIMATE CIRCUITS

Machine Learning (ML) has been the current issue in almost all the principal fields nowadays. In continuation with this, ML can be applied to VLSI in two approaches. One is hard coded coding where the program specific rules and the outcomes that are required are mentioned and the instructions for the whole process with reasons for all the possible options that the program has to deal with are specified.i.e, by utilizing ML algorithms VLSI procedures are to be made accurate and easier. On the other hand, a facility to a neural network in the form of architecture is created to understand what it needs to do on its own. For this to happen, inputs are provided and tell it what outputs are required and then let it figure out everything on its own. i.e, developing efficient VLSI hardware architectures using neural networks to support ML based applications. The first approach has been chosen in this paper. ML is not algorithms alone, but can be an optimization, which is a procedure executed iteratively by comparing various solutions till satisfactory solution is found. The main concentration of this paper is to reduce the number of errors present between exact and approximate 4:2 compressors. Hence different combinations of approximate compressors are implemented till less error rate is obtained employing imprecise logic minimization. To interlink VLSI approximate circuits with ML, TensorFlow has been utilized. An algorithm to select an approximate 4:2 compressor with less error rate is shown.

Algorithm 1 ML in Approximate Circuits

16 to 31 inputs of 4:2 compressor are remained unchanged.
Let number of inputs be [31:0]
while $bits \leq 32$ **do**
  if $(0\&1\&2\&3\&4\&5\&6\&7) = 0$ **then**
    Circuit1 from Google CoLab gets selected which is designed with 0 to 7 bits of k-map as 0's and remaining inputs are according to exact inputs and evaluate power consumption & no. of errors.
  else
   if $(0\&1\&2\&3\&4\&5\&6\&7\&8\&9\&10\&11\&12\&13\&14\&15) = 0$ **then**
     Circuit2 from Google CoLab gets selected which is designed with 0 to 15 bits of k-map as 0's and remaining inputs are according to exact inputs and evaluate power consumption & no. of errors.
   end if
  end if
end while
Identifying the circuit with less number of errors
Return circuit.

VII. CONCLUSION

A demonstration of approximate 4:2 compressors employing inexact logic minimization with error analysis has been presented in this paper and the state-of-art 4:2 compressor has been positioned in 8×8 Dadda multiplier. The simulations and error anlaysis of these architectures have been performed using spectre simulator of Cadence Design Systems and MATLAB respectively. The comparison results shows that the average power has been diminished for the proposed circuits and have less error rate when considered with the number of transistors. Finally, as an application, the concept of connecting VLSI approximate circuits with machine learning using Keras with TensorFlow background and Google CoLaboratory has been delineated in this work.

REFERENCES

[1] Veeramachaneni *et.al*., Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors, Proc. Int. Conf. on VLSI Design (VLSID), 2007, pp. 324-329.
[2] Chang *et.al*, Ultra low voltage, low power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits, IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., 2004, 51, (10), pp. 19851997.
[3] Raphael, D *et.al*, A Power-Efficient 4-2 Adder Compressor Topology, 15th IEEE (NEWCAS), Strasbourg, France, 2017, pp. 281-284.
[4] Swagath, V *et.al*, Approximate Computing and the Quest for Computing Efficiency, 52nd (DAC), 2015, San Francisco, CA, USA.
[5] Shaahin, A *et.al*, Majority-Based Spin-CMOS Primitives for Approximate Computing, IEEE Trans. on Nanotech., 17(4), 2018, pp. 795-806.
[6] Avinash, L *et.al*, Parsimonious Circuits for Error-Tolerant Applications through Probabilistic Logic Minimization, Int. Workshop on PATMOS 2011, pp.204-213.
[7] Darjn, E *et.al*, Approximate Multipliers Based on New Approximate Compressors, IEEE Trans. on CAS-I: Reg. Pap, PP(99), 2018, pp. 1-14.
[8] Momeni, A *et.al*, Design and analysis of approximate compressors for multiplication, IEEE Trans. on Comp., 64 (4), 2015, pp. 984994.
[9] Liang, J *et.al*, New Metrics for the Reliability of Approximate and Probabilistic Adders, IEEE Trans. on Comp., 63(9), 2013, p. 1760-1771.
[10] Zervakis, G *et.al*, Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation, IEEE Trans. on VLSI Systems, 24(10), 2016, pp. 3105-3117.
[11] Sina,B *et.al*, Exploration of approximate multipliers design space using carry propagation free compressors, ASP-DAC, 2018, Jeju, southkorea, pp.611-616.
[12] Peter, A *et.al*, "Opportunities for Machine Learning in Electronic Design Automation," in ISCAS, 2018, Italy.
[13] Kumud,N *et.al*, ABACUS: A Technique for Automated Behavioral Synthesis of Approximate Computing Circuits, DATE, 2014, Dresden, Germany.
[14] Schlachter,J *et.al*, Design and Applications of Approximate Circuits by Gate-Level Pruning, IEEE Trans. on VLSI Systems 25 (5), 2017, pp.1694-1702.