VLSID 2019 Tutorial Abstracts

T1A: The Autonomous Automotive Robustness Duo: Challenges and Practice in Functional Safety and Security

Sandip Ray (U. Florida)

Abstract: As we move towards increasingly autonomous vehicles, it is getting increasingly crucial to ensure that they behave safely, securely, and reliably. Automotive robustness refers to the study of synergies and trade-offs between these requirements. In this tutorial, we will present the state of the art in two critical components of automotive robustness, functional safety and security. We will discuss the challenges towards developing a comprehensive solution, and the complexities induced as we move towards an eco-system of increasingly autonomous connected vehicles. We also discuss the potential application of a flexible architecture for systematically implementing these requirements.

T1B: Designing in the Next Generation IoT-AI Ecosystem

Manish Sharma (Samsung)
Mahesh Babu A K (Samsung)

Abstract: In this tutorial, we will explore how IoT systems are transformed when AI-based analytics is built on top. Traditionally, the field of IoT has focused on connectivity and security. However, just transferring data from the sensors as inputs to the servers as back-end analytics engines isn't enough. We will look at the interaction mechanisms at the input end, where multiple sensors not just generate data but part of analytics is also done at the edge. This means the digested data reaching the server can be used for further meta- analyses and decision making at higher levels. This changes the whole architecture of the decision making process, and we will describe how it affects hardware design.

We will also describe the building blocks of a next-generation AI-IoT ecosystem by introducing you to Samsung's Artik family (Artik0, Artik5 and Artik7), which provides a complete set of H/W for many needs: Connected, Flexible, Economical, tiny, balance power and performance, powerful secure and communicative. We will also introduction Samsung's Tizen OS platform, which includes Tizen for Mobile wearables and TV including deep dive into TizenRT as a lightweight IoT Platform. This includes a technical overview and business case development on the latest advancements in lightweight voice solution and IoT Support for TizenRT. Finally, we will showcase the Smart Things IoT platform, Bixby vision and voice API and integration with the Artik Cloud.

T1C: Architecture and circuits for fractional-N clock synthesis in wireline/wireless applications

Prof. Saurabh Saxena (IIT Madras)
Prof. Nagendra Krishnapura (IIT Madras)

Abstract: Precision clock is a primary requirement in computation and communication. Precise allotment of time for computation, sampling of data at a low bit error rate, and generation of precisely defined carrier frequencies necessitate clock generation with a wide range and fine resolution. This tutorial will present the basic requirements of clocks, particularly in those applications which demand fractional-N PLLs. The tradeoffs between different fractional-N PLL architectures and circuit-level implementations will be discussed. Concepts of in-loop phase/frequency modulation

for RF signals and spread spectrum clocking to reduce EMI through fractional-N PLLs will be elaborated. Multiple clock multipliers while producing different clock frequencies on the same chip have been used for energy efficient systems while employing dynamic voltage and frequency scaling (DVFS) to reduce overall energy. This tutorial will compare open loop and closed loop fractional-N clock synthesis to generate energy efficient low jitter clock for systems with DVFS.

T1D: Logic Locking: Current Trends, Attacks and Future Directions

Prof. Ujjwal Guin (Auburn University)

Prof. Pramod Subramanyan (IIT Kanpur)

Abstract: Relentless device scaling has enabled designers to fit more and more functionality on a system-on-chip (SoC) while reducing the overall area and cost of an integrated circuits (ICs). As complexity has grown exponentially, the semiconductor industry has shifted gears to design reuse rather than designing the whole SoC from scratch. Concomitantly, increased fabrication complexity has resulted in a majority of SoC design houses no longer maintaining a fabrication unit (or foundry) of their own. As a result, the semiconductor business has largely shifted to a contract-foundry business model/horizontal business model over the past two decades.

However, these changes have resulted in the extensive (re-)use of untrusted designs and untrusted IC manufacturing facilities, thus rendering ICs vulnerable to intellectual property (IP) piracy, malicious design modification and the overproduction of ICs. To combat these problems, researchers have proposed logic locking, a technique that can inject trust into an untrusted semiconductor manufacturing process by preventing unauthorized use of ICs. In this tutorial, we will present - (i) an overview of logic locking methods, (ii) an overview of attacks and countermeasures, and (iii) systematic and formal techniques for reasoning about the security of proposals for logic locking.

T1E: The Black Art of Analog Design and validation: Where Search and Optimization Meet

Prof. Shobha Vasudevan (University of Illinois at Urbana Champaign, USA)

Abstract: Analog and mixed signal (AMS) chips pervade all aspects of our lives. In the iPhone 6, 20 out of 25 are AMS chips. Their verification, though, is at a stage of evolution similar to digital hardware verification of the 1980s. It is unsystematic, ad-hoc and manually intensive. With the rising demand for AMS chips in mobile and IoT devices, streamlining their design and verification is important and imminent. In this tutorial, we introduce the AMS verification problem, its unique challenges and opportunities. We will go through the state-of-the-art (random Monte Carlo simulations) in AMS verification. Through Duplex, our research software tool suite, we will teach concepts of directed testing, goal oriented and coverage directed stimulus generation, and runtime monitoring in AMS. We will teach the principle of separation of spaces in Duplex, that makes the orders of magnitude improvement in efficiency possible. We will also teach the robot motion planning inspired algorithms and data structures within Duplex. We will also cover critical analog validation tasks like eye diagram analysis and test compression, and algorithms for increasing their quality and efficiency. Finally, we will outline the landscape of AMS design optimization and develop a hyper efficient approach for it using Duplex. We will motivate problems that are as yet unsolved in this space, and some approaches we are exploring.

T1F: [Hands-on Tutorial] Architecture & Methodology for DFT of Low Power SoCs

Jais Abraham (Qualcomm)
Arvind Jain (Qualcomm)

Abstract: Low power SoCs impose unique challenges for DFT and for silicon testing. Tests have to be created so as not to exceed the power budget of the design, while, at the same time not imposing excessive costs for testing under these constraints. DFT techniques are also needed to detect manufacturing defects on the power management structures introduced in the design. It is imperative for the DFT engineers to plan for these challenges starting from design architecture and implementation stage till the generation of manufacturing test patterns and application on silicon.

In this tutorial, we will cover the challenges posed for DFT in low power designs like mobile processors and complex 5G modems. We will present the analysis techniques, architecture and design solutions available to address these challenges. In addition, we will also cover the EDA solutions available, both from test hardware and pattern generation methodology to handle the requirements of low power designs. The DFT practitioner will get an in-depth overview of the requirements of low power designs and some examples of the solutions available to deal with them.

T1G: [Hands-on Tutorial] Accelerating Deep Learning Inference On FPGAs Using OpenVINO

Vikas Hosoor (Intel)

Abstract: The Tutorial Aims to provide a quick learning about using Intel SDKs available for Intel FPGAs, Accelerating Inference is one of the use cases that has been selected for the Tutorial. FPGA is an acronym for field programmable gate array. It is a semiconductor IC where a large majority of the electrical functionality inside the device can be changed; changed by the design engineer, changed during the PCB assembly process, or even changed after the equipment has been shipped to customers out in the 'field'. The tutorial will cover:

1. Introduction to features of Latest Intel FPGAs
2. Introduction to Acceleration Cards with Intel FPGAs
3. Introduction to OpenVINO Toolkit and Demo
4. OpenCL SDK tool flow
5. Customization on Intel® Deep Learning Deployment Toolkit

T2A: Offset in Low-Voltage Sense Amplifiers and its Implication on Memory Testing

Prof. Manoj Sachdev (University of Waterloo, Canada)

Abstract: Static Random Access Memories (SRAMs) often occupy a significant area of contemporary Systems on Chip (SoC) integrated circuits (ICs) and therefore determine their energy consumption, yield, and reliability. The sense amplifier (SA) is a critical SRAM circuit that requires careful design. The offset in the SA does not scale well with technology scaling and has become an impediment for low-voltage SRAMs. Additionally, the offset in SAs can also give rise to intermittent failures (soft-failures) in SRAMs that are difficult to detect through traditional march test algorithms. This tutorial is divided into two parts. The first part focuses on SA design and contrasts techniques for mitigating SA offset voltage. The second part addresses test considerations for SA offset voltage.

T2B: Validation Coverage: Extending the Validation Coverage Continuum from Pre-silicon to Post-silicon

Gaurav Verma (NXP)
Ashish Gupta (NXP)
Nagabhushan Reddy (Intel)

Abstract:
The modern electronic systems we use today are predominantly a combination of Hardware(HW) and Software(SW). Typically, System on a Chip (SoC) IC's are at the heart of these products, running embedded SW across multiple CPU cores, and communicating with the rest of the product and the user through a multitude of I/O protocols. Developing and validating these SoC's is a challenging task due to the sheer complexity of the HW, SW, and their overall interaction. System validation of the SoC is required to ensure that the overall product requirements have been met before general release to manufacturing. Use case testing in both pre-silicon and post-silicon validation is becoming a key activity in SoC Validation and being able to leverage tests and functional coverage from pre-silicon to post-silicon is seen as a key contributor to reducing functional escapes to customers and improving time to market. This tutorial will focus on methods and examples of extending the validation continuum from pre-silicon to post-silicon, based on the work from the IEEE CEDA System Validation and Debug Technology Committee's Coverage Working Group

T2C: Vision Based Autonomous Systems

Prof. Chetan Arora (IIT Delhi)
Prof. Saket Anand (IIIT Delhi)

Abstract: Autonomous systems have a potential to revolutionize our society by fundamentally changing the way humans and machines co-operate. Computer vision is often the central component for perception and understanding capabilities of such autonomous systems. Improvement in availability of large annotated datasets, coupled with exponential increase in the computational power, and advances in machine learning algorithms, notably deep learning, have led to renewed interest in computer vision based autonomous systems. However, with this rapid growth, it has also become difficult to enter the field as a beginner or stay up-to-date after entering. The goal of this tutorial is to expose the audience to state of the art techniques needed to build a vision based autonomous system. We will start with the fundamentals of computer vision with focus on recognition, reconstruction, motion estimation, tracking, scene understanding and end-to-end learning. We will then present their applications in autonomous navigation and special challenges in the Indian environments.

T2D: Hardware Security of Embedded Systems and IoT Environment

Prof. Susmita Sur-Kolay (ISI, Kolkata)
Prof. Debasri Saha (University of Calcutta)

Abstract: In recent times, the paradigm of design automation has advanced to system level. In order to realize large applications on a chip, the stages of chip design cycle are often distributed across the globe. For multiple applications on a single platform with a short time-to-market, the component chips acquired from various sources are integrated to realize the system. As a result, unauthorized access of resources by adversaries, counterfeiting, attacks on functionality or performance by malicious circuitry, leakage/alteration of security-critical information by such unintended circuitry and fraudulent software at design/booting/runtime, may pose threat of loss of billions of dollars for IC and EDA industry.

This tutorial focuses on the major threat models, and their respective countermeasures, such as lock-based mechanisms to prevent unauthorized access, authentication of each component, masking of security-critical information leakage, test time and runtime protection and recovery from the effect of compromised components on chips and in systems. Growing use of continuously connected IoT/Cloud-based shared architecture and realizing medical facilities on chip pose more critical, even life threats due to the presence of heterogeneous architecture and environment and possibility of diverse attacks from various domains like hardware, firmware, software, network, etc. Therefore, modern IoT-based systems and applications demand continual efforts to ensure security on those.

T2E: Energy-Efficient Resilience for Cognitive Systems

Pradip Bose (IBM)
Prof. Subhasish Mitra (Stanford University, USA)

Abstract: Computing systems can be subject to errors in the underlying hardware (i.e., a signal produces incorrect logic value), which can prevent correct system operation. Ensuring resilient operation, i.e., the system operates correctly despite such hardware errors, is a major challenge (e.g., in the face of extreme constraints on energy) across a wide range of application domains: from intelligent edge-devices all the way to large-scale supercomputers. Automotive intelligence at the edge (e.g., that powers self-driving cars and drones) demands very stringent resilience features.

Large-scale cloud servers and supercomputers demand accurate high-performance calculation prowess for big data at affordable energy cost. In cloud-backed cognitive Internet of Things (IoT), energy-efficient resilience constraints apply to the entire range of compute, storage and networking elements. In this tutorial, we will cover two broad topic areas:
(a) General principles of resilient computing systems, with special emphasis on cross-layer resilience: achieve desired resilience targets at low cost (energy, power, execution time, area) by combining resilience techniques across various layers of the system stack (circuit, logic, architecture, software, algorithm).
(b) Low-power, resilient acceleration of specialized functions, with a focus on AI (e.g., machine learning/deep learning) applications.

We will show which aspects of the general principles in topic area (a) naturally apply to topic area (b); and, we will also delve into problems that are unique to the cognitive IoT domain represented by topic area (b). We will comprehensively cover resilience to various sources of hardware errors, including radiation-induced transient errors (soft errors), manufacturing defects, device degradation over time (circuit aging), and variability induced by manufacturing and operating conditions (e.g., supply voltage). From application standpoint, error propagation characteristics and inherent resilience properties will be factored into the overall design consideration for energy-efficient systems. Systematic approaches to cross-layer resilience, that explore the vast space of various resilience techniques and derive cost-effective solutions, will be explored. Latest results from academic research together with state-of-the-art application case studies practiced in industry will be covered.

T2F: IoT for Smarter Healthcare: From Device to Architecture, Applications and Analytics

Prof. Nikil Dutt (University of California at Irvine, USA)
Prof. Iman Azimi (University of Turku, Finland)

Abstract: Internet-of-Things (IoT) is remodeling the healthcare sector in terms of social benefits, market penetration, as well as through its economics. Enabled by ubiquitous computing, IoT enables all the healthcare system entities to be monitored and managed continuously. IoT allows remote monitoring and tracking of patients living alone at home or treated in hospitals. On one hand, data generated from sensors attached to patients is made available to doctors, family and interested parties giving them the ability to check the subject's vital signs and contextual information from anywhere at any time; and on the other hand it can assist healthcare workers for intelligent and informed decision making to enable better health outcomes and overall well-being. However, IoT- based healthcare systems necessitate a higher degree of dependability, accessibility, efficiency, robustness, and privacy, compared to IoT applications in other sectors. In this talk, we present state-of-the-art in healthcare IoT, including background from recent years. The tutorial aims at covering different key aspects of general-purpose IoT technologies as well as the recent achievements in the context of e-health systems including low-latency and real-time application requirements, interoperability, federation, energy efficiency, mobility, hierarchical Fog-assisted computing and data analytics, geo-distribution and context awareness, and the notion of Internet-of-Cognitive-Things (IoCT). In addition, we present our recent contributions in developing IoT-based remote patient monitoring-intervention systems for three healthcare problems: a) Family-Centered Maternity Care, b) Smart Pain Assessment, and c) Early Warning Score System for high-risk patients.