A Transimpedance Amplifier with Improved PSRR at High Frequencies for EMI Robustness

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***Abstract* –A two-stage folded cascode (FC) architecture with good PSRR response at frequencies above 10MHz has been designed in 0.18µm CMOS technology to be used for transimpedance amplifiers (TIA). The high-frequency PSRR improvement boosts the EMI/RF immunity of the TIA for moderate injected power level. With a single supply of 1.8V, the simulation results show that the circuit had DC PSRR of -133.7dB. At 100MHz, the OTA shows a good PSRR of -60dB.**

Keywords – Transimpedance amplifier, EMI/RF immunity, power supply rejection ratio

I. INTRODUCTION

A capacitive-feedback transimpedance amplifier (CTIA) provides the high impedance gain with low silicon area. Selection of a suitable amplifier to be used as a TIA is a critical and a juggling act between the electrical parameters of an opamp and the tradeoffs between them. The dominant source of EMI disturbances [1] is through power supply and hence the PSRR of the operational transconductance amplifier (OTA) plays a major role in making the TIA robust to these interferences. Results in [2] show that high PSRR of 120dB is achieved but in a limited frequency range. The tail compensation technique used to improve PSRR in [3] cannot be used for TIA with PMOS input pair as the PMOS tail will directly couple to supply and also creates complex poles. In [4], two current reference circuits are used to improve CMRR and PSRR which increases the chip area. This paper discusses a simple technique to improve the high-frequency PSRR. The paper is organized as follows. Section II gives the design of the two-stage OTA with PSRR improvements. Section III gives the small signal PSRR model with the mathematical analysis. Comparison of the TIA results using the conventional and improved design is shown in section IV.

II. MODIFIED OTA FOR PSRR IMPROVEMENT

The schematic of the proposed composite folded cascode OTA and small signal model of output stage is given in figure 1. To eliminate supply noise coupling through the bulk terminal, all the PMOS transistors have their bulks connected to local source. Since the parasitic capacitances of the PMOS load transistors play a major role in the high-frequency PSRR response, the composite circuit is designed with 1.8V NMOS transistors and 3.3V PMOS transistors except the input pair. In the proposed design, the gate of transistor M_{11} is biased individually by V_{b4} and not V_{b1} so that its size can be reduced compared to M_{b7}, M_{b6}, M_{01}, M_9 and M_{10} (shaded region in figure 1). Hence, by using isolated bias the small size of M_{11} results in smaller parasitic coupling capacitors.

III. SMALL SIGNAL MODEL OF OUTPUT STAGE

To analyze the effect of the proposed changes on high-frequency PSRR, a partial circuit i.e. the output stage along with its bias circuit and the RC-filter of the proposed design is considered. A ripple on the supply directly transfers to the gates of M_{11} and M_{12} through the diode-connected bias transistors. R_1 is chosen small enough so that the output voltage headroom is not degraded significantly. The values of r_{0M11} and r_{0M12} are very large compared to R_1. The values of parasitic capacitances are small compared to C_1 and C_{out}. The load capacitance used for the OTA is 2pF. Using nodal equations in figure 2, the transfer function V_{out} /V_{dd} (assuming that $sC_{out} >> sC_{gd12}$) is obtained as follows.

$$\left|\frac{V_{out}}{V_{dd}}\right| \approx \frac{sC_1R_1[sC_{gd12} - g_{m12}]r_{0M13}}{[1 + sC_{out}r_{0M13}][1 + sC_1R_1]} \quad (1)$$

Figure 2 gives the PSRR response of the complete proposed OTA. It can be observed from equation (1) that the RC-filter pole introduces a roll-off at high frequencies above its cut-off frequency (region B) with a slight degradation in the PSRR in the mid-band frequencies of 2KHz to 1MHz due to the zero introduced by this filter (region A). Due to this trade-off, the R_1C_1 product cannot be increased to a large value. In our present design, the RC-filter has a cut-off frequency of about 80MHz with the values set to R_1=5kΩ and C_1=400fF. Also, since the C_{gd12} is small, the numerator of equation (1) is dominated by g_{m12}. Compared to the conventional OTA, the proposed OTA, with reduced g_{m12} and C_{gd12}, gives an improvement of 12dB in PSRR at high frequencies as seen in region B. The C_{out} (load capacitance) value in the denominator of equation (1) is dominated by the feedback capacitance (C_f) of the TIA, which is chosen based on the input photocurrent range.

IV. DESIGN OF CTIA USING IMPROVED OTA

Figure 3 shows the block diagram of the setup used to test the capacitive TIA. The loop consists of the integrator followed by a comparator block which is closed by the discharge circuitry of the integrator. The photodiode sensor is modeled as a current source I_{in} with a photodiode capacitance C_{pd} in parallel.

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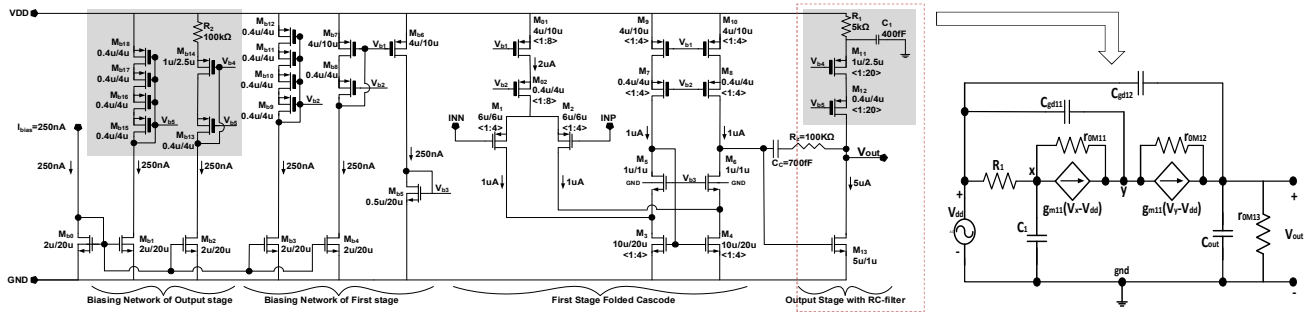

Fig. 1. Schematic of proposed OTA with improved PSRR using 3.3V transistors and small-signal model of output stage

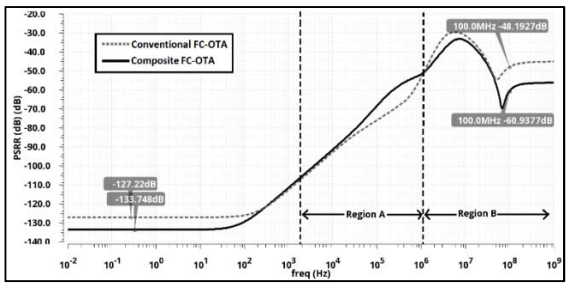

Fig. 2. PSRR improvement using proposed OTA

The TIA was tested for a known input current of 50pA. Interfering EMI signals often couple through PCB wires and supply lines. The EMI signals from the supply can directly get coupled to the input leads of active capacitive feedback devices like TIAs.

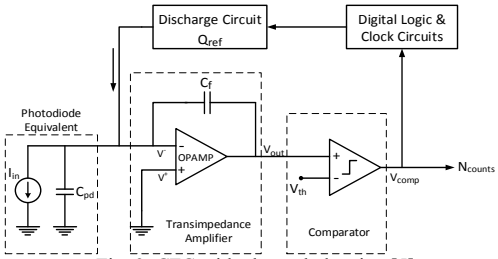

Fig. 3. CFC with charge balancing [5]

This results in AC-induced input offset and along the signal path it can get amplified and appear as a DC offset error at the opamp output [1]. By improving the OTA PSRR, the AC-induced input offset ($V^- - V^+$) of the TIA is reduced by 6.6dB at high frequency of 100MHz as shown in figure 4. The Table I gives the state-of-art comparison of the designed OTA (in unity gain configuration) with existing architectures. The PSRR results in [2] and [4] are comparatively higher than the proposed circuit of this paper till the mid-band frequencies (up to 10MHz) because they use a larger supply voltage of 3.3V. However at higher frequency of 100MHz, the proposed circuit gives a 20dB improvement in the PSRR response compared to [4].

V. CONCLUSIONS

The proposed composite two-stage OTA improves the PSRR by 12dB compared to a conventional FC-OTA at extended frequencies of 100MHz. When used in CTIA, the

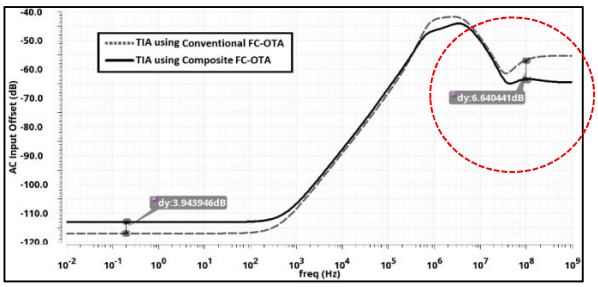

Fig. 4. AC-induced input offset ($V^- - V^+$) of TIA up to 1GHz

TABLE I: COMPARISON OF OTA WITH SIMILAR WORKS

Ref	This Work	[2]	[3]	[4]
Technology	0.18µm	0.5µm	0.5µm	0.35µm
Supply	1.8V	3.3V	±1.5V	3.3V
DC Gain	139dB	52dB	69dB	58dB
GBW	2MHz	10MHz	10.3MHz	489MHz
PSRR (1KHz)	-111.6dB	-120dB	-77dB	-105dB
PSRR (100KHz)	-68.5dB	-105dB	-66dB	-101dB
PSRR (1MHz)	-52dB	-67.5dB	-	-88dB
PSRR (10MHz)	-34dB	-40dB	-	-76dB
PSRR (0.1GHz)	-60.9dB	-	-	-40dB
Supply Current	10.3µA	25µA	90µA	-

OTA gives a reasonable EMI rejection by reducing the input offset by 6.6dB at high frequencies above 100MHz.

VI. REFERENCES

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