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Neuromorphic Circuits on FDSOI Technology for Computer Vision Applications

Dinesh Rajasekharan*, Amit Ranjan Trivedi†, and Yogesh Singh Chauhan*
*Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur, India 208016.
†Department of Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, Illinois, United States.
Email: dineshr@iitk.ac.in, chauhan@iitk.ac.in

***Abstract*—Potential of neuromorphic circuits on FDSOI technology for computer vision applications is demonstrated in this paper. Computer vision systems based on conventional Von Neumann architecture consume large area and energy. The FDSOI inverter-based circuits proposed in this work, require only 11 transistors per pixel for colour detection, and only 59 transistors per pixel for erosion and dilation operations, whereas the CMOS-based Boolean circuit requires more than 300 transistors per pixel, and 2700 transistors per pixel, respectively, for these operations.**

I. Introduction

Neuromorphic computing is useful for large data processing, and visual data is one of the major sources of data for human beings. Image processing using conventional Boolean computing platform, requires many multiplication and accumulation operations to be done serially and, therefore, consumes larger area and power [1]. In this work, we show that neuromorphic circuits, based on FDSOI inverters, can be used for computer vision applications. We have performed circuit simulations for detecting colours in the images, and also shown two basic morphological operations on the images, namely, erosion and dilation. The simulations were carried out using BSIM-IMG MOSFET model, calibrated with the experimental FDSOI transistors [2] [3]. The $I_{DS} - V_{FG}$ characteristics used for the FDSOI NMOS and PMOS devices are shown in Fig. 1a and Fig. 1b, respectively.

II. FDSOI inverters for image processing

The variation of output voltage and current, flowing through FDSOI MOSFET-based inverter (Fig. 1c), with input front gate voltage V_{in1}, for different back gate voltages, V_{in2}, are shown in Fig. 1d and Fig. 1e, respectively. Figs. 1d and 1e show that significant current flows through the inverter, only when V_{in1} is close to the switching threshold of the inverter, and this switching threshold can be changed by V_{in2}. Fig. 1e shows the variation in peak current with change in V_{in2}, and this variation is due to substrate depletion effect [4]. By providing offset voltage, V_{offset}, to the back gate voltages of the transistors in the inverter, we can also control the peak current and the shape of current characteristics, as shown in Fig. 1f.

III. Colour detection circuit

The block diagram representation of the circuit, for detecting a colour from an image of size $n \times n$, is shown in Fig. 2. Inputs to the system are the intensities of the three primary colours for each pixel in the image. Every pixel processing block (PPB) contains three inverters, each one of them processing pixel intensity of one of the three primary colours. The back gate voltages of transistors in PPB are designed such that maximum current flows, when the inputs to the PPB correspond to that of the colour to be detected.

The output current of each PPB is fed to the corresponding WTA cell [5], [6]. Output voltage of WTA cell will be lower, if the input current to the cell is large. Results of colour detection performed on some input images [7] are shown in Fig. 3, which shows that the circuit is more selective for larger V_{offset}. For processing one pixel of the image, this system requires only 11 transistors, whereas, the CMOS-based Boolean system requires more than 300 transistors.

IV. Morphological image processing

Morphological image processing is used for identifying and analysing the geometrical shapes in the images, and erosion and dilation are two fundamental morphological operations [8]. In an erosion (dilation) operation, the value of each pixel in a colour channel is replaced by the minimum (maximum) value among the pixels, enclosed by the structuring element (SE), as shown in Fig. 4a. The implementation of SE is shown in Fig. 4c, in which the back gates of all the transistors are provided with the same voltage. For erosion (dilation) operation, the back gate voltage is provided such that maximum current flows through the SE for the smallest (largest) input voltage.

Circuit for erosion and dilation operations is similar to the colour detection circuit, and is shown in Fig. 5. In the circuit, the output currents of SEs are provided to WTA cells, which give the corresponding output voltages. The input images [9], the results of erosion and dilation operations and one of the applications of these two operations, edge detection, are shown in Fig. 6. Edge is detected by subtracting the area identified by erosion, from the area recognised by dilation. For erosion/dilation operation, the proposed FDSOI-based implementation, requires only 59 transistors per pixel, whereas the CMOS-based Boolean implementation requires more than 2700 transistors. The performance of the system is tabulated in Table I. Here selectivity, defined in percentage, is the fractional range of input voltage for which the output current of inverter is more than 10% of the maximum current through the inverter.

V. Conclusion

Neuromorphic computing circuits, based on FDSOI technology, for colour detection, and for erosion and dilation operations have been implemented in this work. The proposed non-Boolean implementation requires only 11 transistors per pixel for colour detection, and only 59 transistors per pixel for erosion/dilation operation. In comparison, the CMOS-based Boolean implementation requires more than 300 and 2700 transistors per pixel, respectively, for the same operations.

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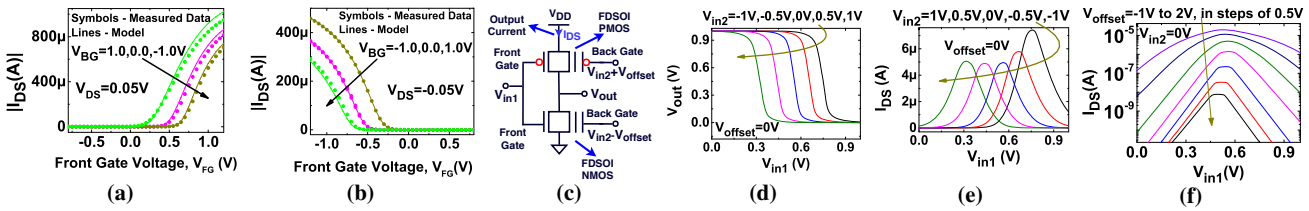
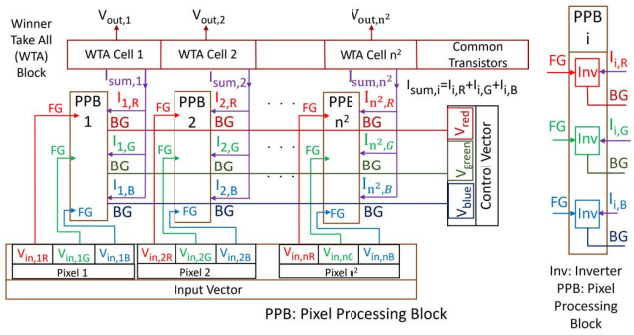


(a) (b) (c) (d) (e) (f)

Fig. 1: $|I_{DS}|-V_{FG}$ characteristics of the 50 nm technology node FDSOI (a) NMOS and (b) PMOS devices ($W = 10\,\mu$m and $L = 52$ nm), calibrated with the BSIM-IMG MOSFET model [2] [3]. Symbols denote the measurement data for the devices [4], [10] and the lines denote the model. (c) FDSOI MOSFET-based inverter used in this work. (d) Output voltage and (e) $I_{DS} - V_{in1}$ characteristics of the inverter ($W = 0.156\,\mu$m and $L = 52$ nm for the MOSFETs) for $V_{offset} = 0$ V. V_{in2} is varied from -1 V to 1 V. (d) $I_{DS} - V_{in1}$ characteristics of the inverter with $V_{in2} = 0$ V. V_{offset} is varied from -1 V to 2 V.



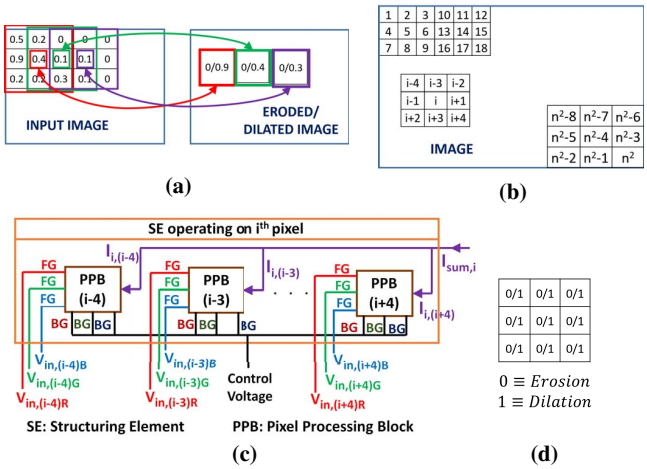
(a) (b)

Fig. 2: Block diagram for (a) colour detection circuit for an image of size $n \times n$ and (b) pixel processing block.

(a) (b) (c) (d) (e) (f) (g)

(h) (i) (j) (k) (l) (m)

Fig. 3: (a)-(c) Input images [7] (d) Colour to be detected. Output images for (e)-(g) $V_{offset} = -0.5$ V, (h)-(j) $V_{offset} = 0$ V and (k)-(m) $V_{offset} = 0.5$ V. In the output images, lighter shades indicate higher colour match.



(a) (b) (c) (d)

Fig. 4: (a) Illustration of erosion/dilation operation on an image. Here values in square indicate pixel intensity. (b) Representation of an image with pixel references, shown inside square. (c) Block diagram for structuring element of size 3×3, operating on pixel i. (d) Conditions on control voltages for the erosion and dilation operations.

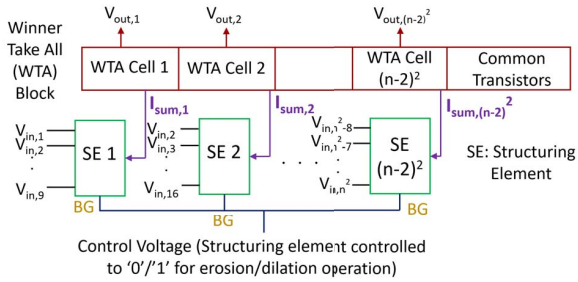
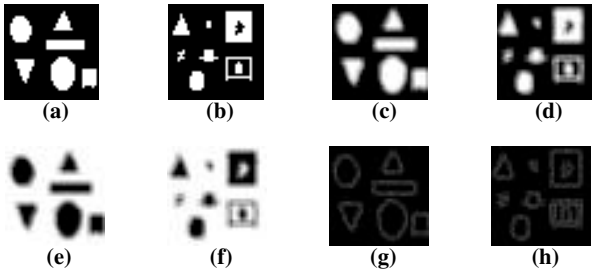


Fig. 5: Block diagram of circuit for erosion/dilation operation on the images of size $n \times n$.



(a) (b) (c) (d)

(e) (f) (g) (h)

Fig. 6: (a), (b) Input images [9]. (c), (d) Outputs of dilation operation (e), (f) Outputs of erosion operation. The operations were performed for $V_{offset} = 0$ V. (g), (h) Outputs, obtained by subtracting the area identified by erosion operation from the area identified by dilation operation (dilation - erosion).This operation identifies the edges of the objects in the images.

TABLE I: Performance of proposed methodology

Circuit operation	$V_{offset} = -0.5$ V	$V_{offset} = 0$ V	$V_{offset} = 0.5$ V	Performance metric
Colour detection	76.6%	39.1%	29.8%	Selectivity (in %) of input to the inverter
Erosion, dilation	4.98%	29%	31.66%	Maximum error (in %) in the operation

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