An Efficient Design Approach for Implementation of 2 bit Ternary Flash ADC Using Optimized Complementary TFET Devices

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***Abstract*—Recent studies have indicated that multilogic circuits in VLSI design helps in reducing the transistor count of circuits and increases the data transfer rate significantly. This paper presents an efficient design methodology for the implementation of a two bit ternary output Flash Analog to Digital Converter (ADC) utilizing Tunnel Field Effect Transistors (TFETs). Optimized SiGe TFET structures which have ON currents more than twice while OFF currents at least an order of magnitude lower than the standard 45 nm MOSFETs have been developed. These devices form the basic active elements for the proposed ADC. A new complementary TFET (CTFET) based comparator design is also proposed in the paper which has delays and power consumption lesser than the conventional CMOS based comparator design. An efficient methodology for directly designing logical functions with TFET devices, obtaining 2 bit ternary ADC output with a resolution of 50 mV and input quantized to 9 levels is illustrated in this paper. The proposed CTFET based ADC needs only 48 transistors to encode the comparator outputs to the required 2 bit ternary output which is significantly lower than the transistor count of 70 needed for the 2 bit ternary flash ADC designs available in literature. The performance of the CTFET based ternary ADC has been benchmarked with the same ADC circuit implemented with 45 nm CMOS technology. It has been demonstrated that the CTFET based ADC not only has delays much lesser than the corresponding CMOS based ADC but also consumes significantly lesser power and the overall decrease in Power Delay Product (PDP) has been shown to be 99.7%.**

I. Introduction

Recent research [1]–[6] have revealed that ternary logic significantly reduces the number of transistors required for implementation of various logical and arithmetical circuits, besides enabling faster data transfer. Ternary logic circuits can also be implemented with CMOS devices, however they consume large power. Recent studies [7]–[11] have demonstrated that TFETs with SiGe substrate and high-κ dielectric materials have higher I_{ON}:I_{OFF} ratio with better inverse subthreshold swing than CMOS, unlike earlier TFET designs [12]–[16]. Section II presents optimized SiGe TFET device structures which has I_{OFF} at least one order of magnitude lower than the MOSFETs while the I_{ON} is more than twice that of MOSFETs with the same width at the same technology node. A novel faster CTFET based Comparator design is presented in section III. The advantage of using a CTFET based NAND gate as a building block for ADC instead of CMOS based NAND gate is explained in section IV. A brief description of the methodology for implementing ternary flash ADC with the innovative CTFET devices is given in section V. Simulation results are shown in section VI. Furthermore, the performance of the TFET based ternary ADC has been benchmarked with 45 nm CMOS based ternary ADC in section VII.

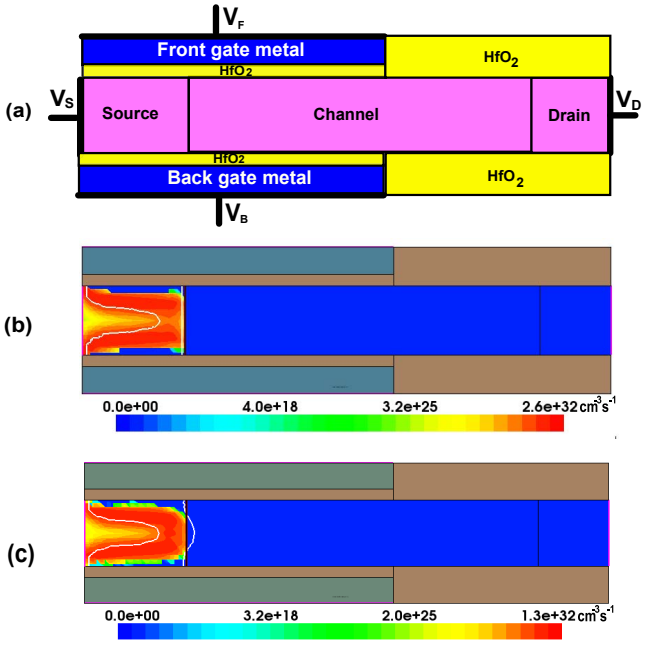

Fig. 1. (a) Schematic of the proposed TFET device. Band-to-band generation rate ($cm^{-3}s^{-1}$) throughout the lateral cross-section of 1 μm wide (b) NTFET and (c) PTFET devices under a symmetric bias of V_{DS}=V_{GS}=1 V.

II. Silicon Germanium TFET

The optimized SiGe TFET structure and the Band-to-Band (BtB) generation contour is depicted in Fig. 1. The device parameters for NTFET and PTFET are summarized in Table I. Device level synopsys® TCAD [17] simulations were used to obtain I_D-V_{DS}/I_D-V_{GS} and I_S-V_{SD}/I_S-V_{SG} characteristics of the NTFET and PTFET respectively, as shown in Fig. 2. All the device simulations reported in this work were carried out using the standard doping dependent mobility model, high

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TABLE I
PARAMETERS OF THE OPTIMIZED DEVICES USED

	NTFET		*PTFET*	
Region	*Material*	*Doping* (/cm^3)	*Material*	*Doping* (/cm^3)
Source	$Si_{0.1}Ge_{0.9}$	10^{20} P$^+$	$Si_{0.2}Ge_{0.8}$	10^{20} N$^+$
Channel	undoped Si	–	$Si_{0.2}Ge_{0.8}$	5×10^{17} P
Drain	Si	10^{20} N$^+$	$Si_{0.2}Ge_{0.8}$	5×10^{17} P
Gate	Al	–	Mo	–

field saturation model, SRH and Auger recombination models in addition to non-local Band-to-Band generation models. ITRS specifies 1 V to be the limit of biasing at the 45 nm technology node. We have followed the same regulation for all the simulations. The same biases were applied at the front and back gates to simulate symmetrical gate bias conditions. The C_{GS} & C_{DS} capacitances were extracted using AC analyses in TCAD. A look up table based verilog-A behavioral code has been formulated based on TCAD simulation results. As there are no standard SPICE models available for the TFET structures in circuit simulators [18], [19] at the time of this work, so circuit designs and performance analyses were evaluated in SPICE using the verilog-A behavioral code in cadence® EDA tool [20].

III. IMPROVED CTFET BASED STATIC COMPARATOR

A comparator is the first building block of the flash ADC which senses the input analog voltage and quantizes it into specified voltage levels. Comparators are formed by cascading a preamplifier with a latch [21]. The preamplifier compares the input signal with the reference voltage and generates the differential signal for the latch. The schematic of a conventional comparator and the proposed improved comparator is shown in Fig. 3. In case of the conventional comparator

TABLE II
COMPARISON OF THE PERFORMANCE OF CONVENTIONAL VS. IMPROVED COMPARATOR DESIGNS

Circuit parameter	*Conventional design*	*Improved design*
Power supply V_{DD} (V)	1	1
Average delay (ns)	2.3	1.6
Average power (μW)	29.8	13.6
PDP ($\times 10^{-14}$ J)	6.9	2.2
Decrease in PDP	68.1%	

designs, TFETs T_{10}, T_{11}, T_{13} & T_{14} form the latch while NTFETs T_9 & T_{12} receive differential gate input voltage from the preamplifier and accordingly drive the latch to the required digital states. In conventional design, either of the transistors T_9 or T_{12} has to bring about the change in the latch by sinking adequate current to flip the state of the latch and hence require greater gate bias. However, in the improved comparator, as both the cross connected inverters react to the differential input simultaneously, the net comparator response is much

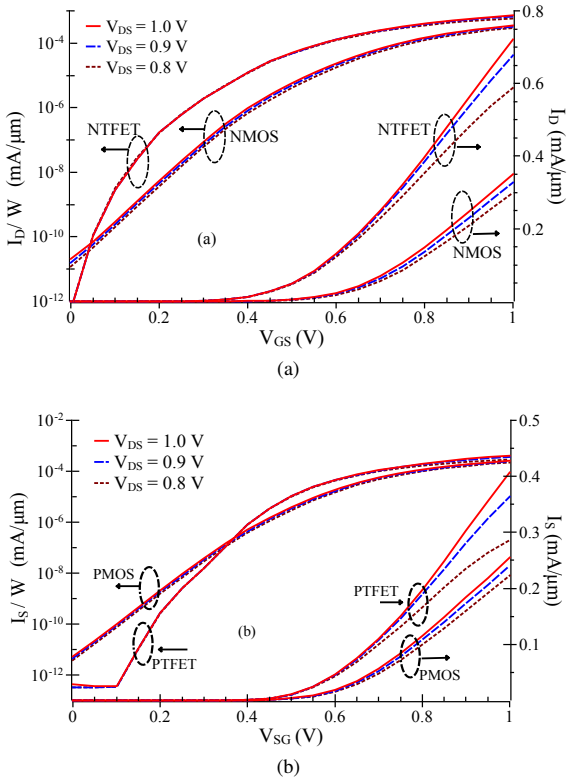


Fig. 2. Comparison of (a) I_D-V_{GS} characteristics of the symmetric NTFET vs. NMOSFET with increasing V_{DS} (b) I_S-V_{SG} characteristics of the symmetric PTFET vs. PMOSFET with increasing V_{SD} biases.

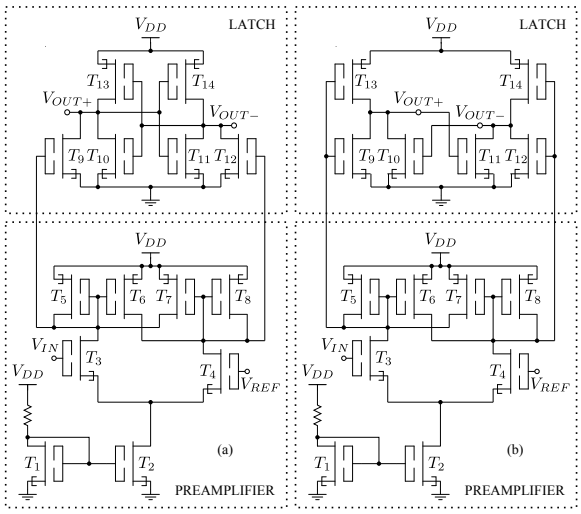


Fig. 3. Schematic of (a) Conventional comparator (b) Improved comparator

faster and the required dynamic power is considerably lower. The response of the two comparators to a sinusoidal input is shown in Fig. 4 and the summary of their performance is listed in Table II. The Power Delay Product (PDP) of the improved comparator is only $^1/_{3^{rd}}$ of the PDP of conventional

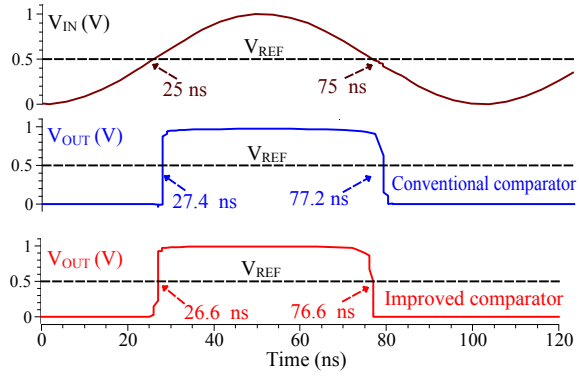


Fig. 4. Comparison of the delay characteristics in conventional vs. improved comparator designs.

TABLE III
COMPARISON OF THE PERFORMANCE OF 2 INPUT NAND GATE

Circuit parameter	*CMOS NAND*	*CTFET NAND*
Bias V_{DD} (V)	1	1
Rise time τ_{LH} (ps)	212	98
Fall time τ_{HL} (ps)	200	74
Avg delay (ps)	206	86
Static I_{LOW} (pA)	6.9	0.103
Static I_{HIGH} (pA)	9.5	0.063
Avg P_{static} (pW)	8.2	0.083
PDP ($\times 10^{-24}$ J)	1689	7.14
Improvement in PDP	99.6%	

comparator, with a significant 68% reduction in PDP.

IV. CTFET BASED NAND GATE FOR THE IMPLEMENTATION OF COMBINATIONAL BLOCK

The subsequent building block of the flash ADC is a NAND gate. Proposed CTFET NAND gate has delays less than half of the corresponding delays in CMOS NAND gate. In addition, the static power consumption of CTFET NAND gate is 2 orders lower than that of CMOS NAND gate. The performance plots are shown in Fig. 5 and summarized in Table III. Overall, there is a reduction of 99.6% of PDP on replacing the CMOS devices by TFETs in NAND gates.

V. DESIGN METHODOLOGY FOR THE IMPLEMENTATION OF 2 BIT TERNARY FLASH ADC

The schematic of the complete CTFET based 2 bit ternary flash ADC is shown in Fig. 6. The ternary ADC has to be so designed to receive analog input and provide ternary 2 bit output as given in Table IV. Half of the supply voltage $V_{DD}/2$ is considered as logic 1 and V_{DD} is taken as Logic 2. The analog input is first quantized into 9 discrete levels using 8 comparators. The next step is to design a combinational logic circuit to convert these 9 different quantized levels to

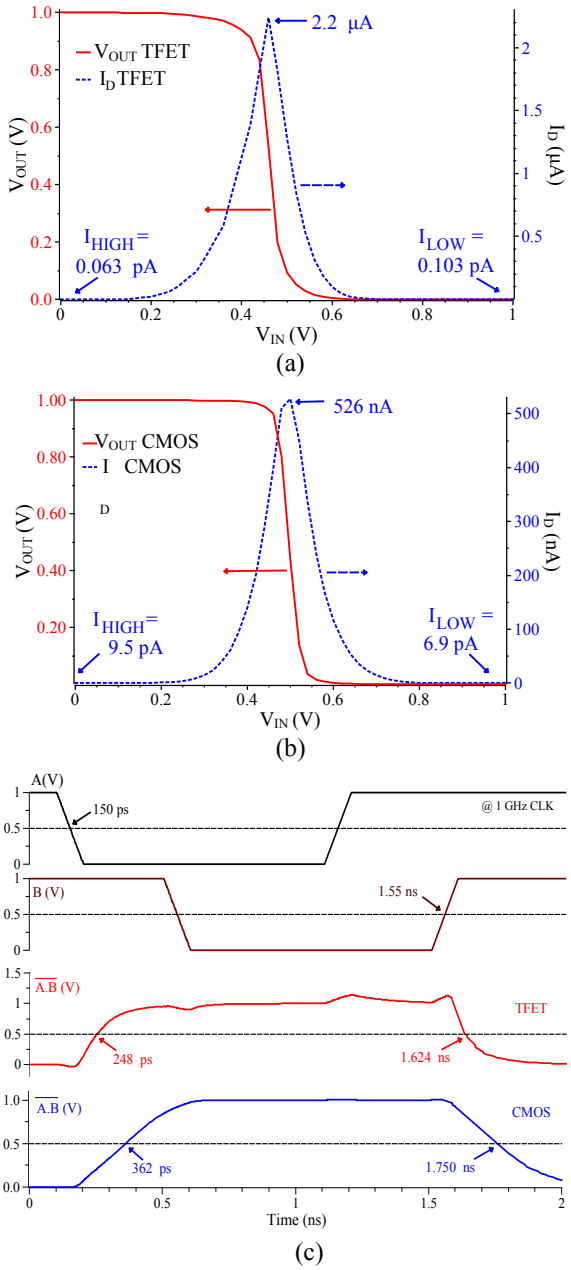
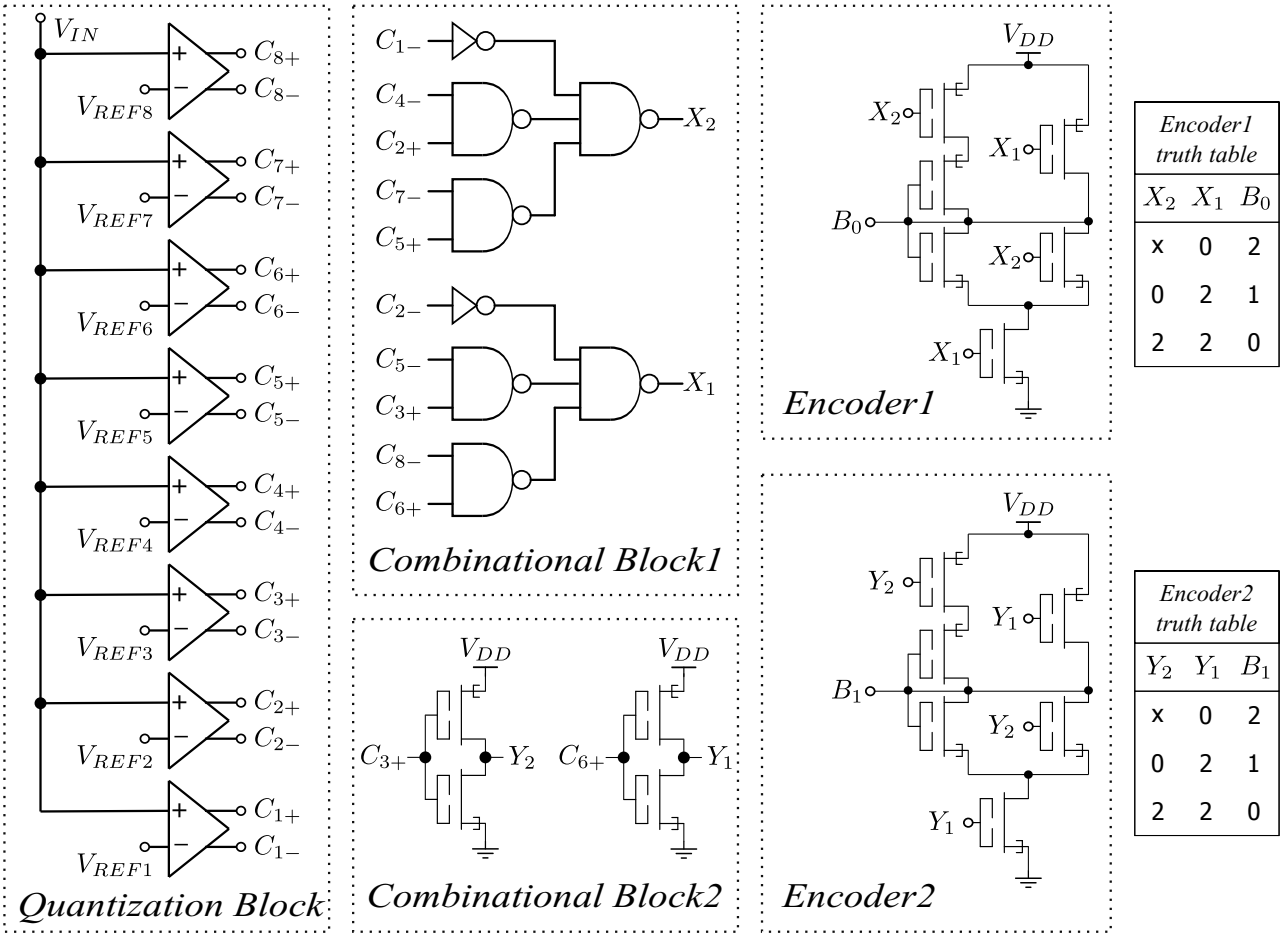


Fig. 5. Performance plots of 2 input NAND gate (a) Static power consumption of CTFET Ckt (b) Static power consumption of CMOS Ckt (c) Delay Comparison CTFET vs CMOS Ckt.

signals which can drive 2 ternary encoders. 2 independent encoders are required to generate 2 bit ternary digital output. The encoder generating LSB B_0 has been named *Encoder1* and its inputs have been designated as signals X_2 & X_1. Similarly, the encoder generating MSB B_1 has been named *Encoder2* and its inputs are Y_2 & Y_1. The truth table and schematic of *Encoder1* are shown in Fig. 6. The truth table for *Encoder2* would be exactly similar to *Encoder1* except that the inputs would be Y_2, Y_1 & output B_1. Truth table for

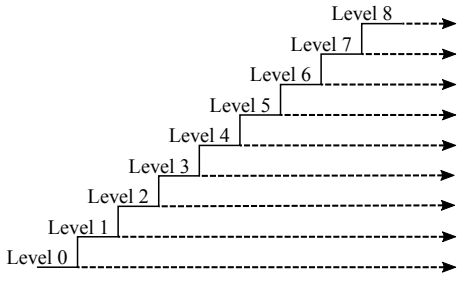


Encoder1 truth table		
X_2	X_1	B_0
x	0	2
0	2	1
2	2	0

Encoder2 truth table		
Y_2	Y_1	B_1
x	0	2
0	2	1
2	2	0

Fig. 6. Schematic of the CTFET based 2 bit ternary flash ADC.

TABLE IV
QUANTIZATION LEVELS AND EQUIVALENT TWO BIT TERNARY OUTPUT



Ternary output	
B_1	B_0
2	2
2	1
2	0
1	2
1	1
1	0
0	2
0	1
0	0

TABLE V
TRUTH TABLE FOR COMBINATIONAL BLOCK DESIGN

Comparator output							
C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	2
0	0	0	0	0	0	2	2
0	0	0	0	0	2	2	2
0	0	0	0	2	2	2	2
0	0	0	2	2	2	2	2
0	0	2	2	2	2	2	2
0	2	2	2	2	2	2	2
2	2	2	2	2	2	2	2

Encoder input			
Y_2	Y_1	X_2	X_1
2	2	2	2
2	2	0	2
2	2	x	0
0	2	2	2
0	2	0	2
0	2	x	0
x	0	2	2
x	0	0	2
x	0	x	0

Encoder output	
B_1	B_0
0	0
0	1
0	2
1	0
1	1
1	2
2	0
2	1
2	2

the design of combinational block with output of comparators as input variables is shown in Table V, in which, all the encoder input and output combinations for all the 9 possible comparator output states are indicated. The other combinations of comparator outputs are considered as don't care conditions, represented with the usual '$\times$' symbol. The novel ADC design proposed in this paper needs only 48 transistors to encode the comparator outputs to the required 2 bit ternary output which is significantly lower than the transistor count of 70 required for the 2 bit ternary flash ADC design reported in recent literature [22].

VI. Verification of The Proposed ADC Design

Circuit simulations were carried out by providing an input sweep from 0 to 1 V. V_{REF1} has been taken as 0.48 V and the quantization step size as 50 mV to generate 9 discrete quantized levels. The ternary output waveform, shown in Fig. 7, was verified to be matching with the desired truth table in Table V.

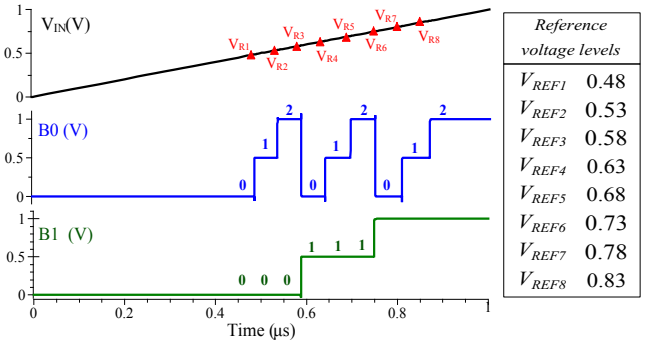


Fig. 7. Ternary ADC Output for Input Signal Sweep.

VII. Performance Benchmarking of the Proposed CTFET vs CMOS Ternary Flash ADC

The performance of the CTFET based ternary flash ADC was compared with the same ADC circuit using standard 45 nm CMOS devices. The optimized TFET channel length is 45 nm and hence the same technology node for CMOS has been used for benchmarking. The corresponding device widths have been kept same in both the circuits. On one hand, since our proposed TFETs have twice the I_{ON} of the corresponding MOSFETs, the delays of CTFET ternary flash ADC are much lower than the CMOS based ternary flash ADC. On the other hand, since the I_{OFF} of our proposed TFETs are at least one order lower than the corresponding MOSFETs, the power consumption in CTFET ternary flash ADC is significantly lower. The simulation results indicate that CTFET ternary ADC has an average delay of only 13.8 ns while CMOS based ternary ADC exhibits a delay of 22.3 ns. The results also indicate static power of only 0.26 nW in CTFET ternary flash ADC which is significantly lower than that of CMOS ternary flash ADC which consumes 51.7 nW. The overall PDP of CTFET ternary flash ADC is only 3×10^{-18} J which is merely 0.26% of the PDP of the standard 45 nm CMOS ternary flash ADC (found to be 1.15×10^{-15} J). Overall, the decrement in PDP due to the proposed CTFET based improved ternary flash ADC circuit is 99.7% as compared in Table VI.

VIII. Conclusions

The device and circuit level simulations have indicated that the optimized TFETs structures proposed in this paper have OFF currents at least an order lower than that of the standard 45 nm CMOS devices while having ON currents more than twice than the CMOS devices. The lower OFF currents lead to significant reduction of power consumption in CTFET based circuits while higher ON currents make CTFET based ternary flash ADC much faster in operation as compared to CMOS based ternary flash ADC. Overall, a reduction of 99.7% in PDP of CMOS ternary ADC has been achieved by replacing CMOS devices with the proposed optimized TFET devices. Furthermore, the proposed CTFET flash ADC requires only 48 transistors for its combinational logic where as 2-bit ternary ADC design available in current literature requires 70 transistors. Thus the proposed CTFET ADC saves chip area immensely. From device point of view, TFETs have steeper subthreshold slopes than the MOSFETs at the same technology node, hence they are much more efficient switches than the CMOS devices for low power digital applications.

TABLE VI
Comparison of the performance of CTFET vs. CMOS based ternary flash ADC

Circuit parameter	*CMOS*	*CTFET*
Power Supply V_{DD} (V)	1	1
Resolution (mV)	50	50
Reference Voltage Range (V)	0.48 - 0.83	0.48 - 0.83
Delay (ns)	22.3	13.8
Average Power (nW)	51.7	0.26
PDP ($\times10^{-15}$ J)	1.15	0.003
Decrease in PDP	99.7%	

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