2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID)

An Unified Charge Centroid Model for Silicon and Low Effective Mass III-V Channel Double Gate MOS Transistors

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***Abstract*—In this paper, we have analysed applicability of the charge centroid model used in industry standard BSIM-CMG compact model for III-V multi-gate transistors. It is observed that the existing model is unable to capture the charge centroid behaviour accurately for low effective mass channel materials. The lower effective mass and highly confined geometry enhance the quantum-mechanical effects and the charge centroid shows anomalous behaviour. By using a self-consistent Poisson-Schrödinger solver, the reason behind the anomalies is analysed in detail. A correction to the existing model is proposed to enable its usefulness for low effective mass channel materials. The proposed model is validated by comparing with the the results of a 1D self consistent Poisson-Schrödinger solver. The new model can accurately predict the charge centroid for silicon as well as low effective mass III-V channel double gate transistors of different dimensions and for different bias conditions.**

***Index Terms*—Charge centroid, quantum confinement, III-V, multi gate transistors, BSIM-CMG**

I. Introduction

The rapid increase in the demand of high speed and low power VLSI circuits has accelerated the introduction of unconventional device architectures like Multi-Gate FETs (MuGFETs) and Fully-Depleted SOI (FDSOI) transistors into CMOS technology domain. The integration of these complex MuGFETs with III-V channel materials to increase the electrostatic integrity and to facilitate low power operation [1]–[4], is currently under active research in several semiconductor industries and academia. Some recent experiments have successfully demonstrated the integration feasibility of these III-V MuGFETs [5], [6].

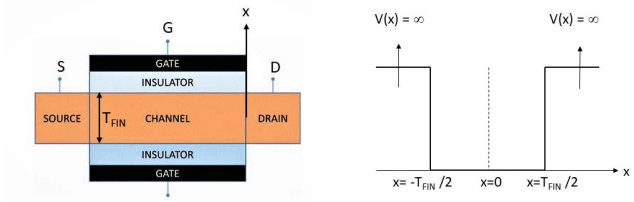
There are several reports on benchmarking the performance of III-V channel MuGFETs against its silicon counterpart [7]–[9]. These comparisons are mainly based on the device simulation results. However, the work related to the evaluation of circuit performance of III-V MuGFETs are limited due to lack of suitable compact models. The conventional circuit simulator models for MuGFETs like BSIM-CMG are developed as a solution of the Poisson equation with quantum mechanical effects added as correction factors [10], [11]. However, the low effective mass and highly confined geometry of III-V MuGFETs show uncommon quantum behaviour than the conventional silicon channel MuGFETs [12], [13]. Because of this, the applicability of quantum correction models (introduced specifically for silicon channel FETs) to the III-V MuGFETs is questionable. One such quantum correction model used in conventional BSIM-CMG model is the charge centroid correction.

Because of higher quantum confinement, the energy band splits into subbands and can no longer be considered as continuous in energy. So, the effect of subband wavefunction on the spatial distribution of inversion charges becomes prominent. The conventional charge sheet approximation is no longer valid and peak of the charge distribution shifts away from the oxide-semiconductor interface. This effect is generally taken care of by adding a correction factor to the oxide thickness based on the centroid of the inversion charge distribution [11], [14]. Note, the subband energy values primarily depend on geometrical (due to device dimensions) and electrical (due to band bending with the application of electric field) confinement. Therefore, the inversion charge centroid is also a function of the device geometry as well as applied bias. The charge centroid distribution being one of the important quantum mechanical effects in highly confined MuGFETs, it is necessary to address it accurately. However, to accurately calculate the charge centroid values for different device dimensions and applied bias, the coupled Poisson-Schrödinger (PS) equation needs to be solved self consistently. This method is computationally expensive and not suitable for circuit simulators. As an alternative approach, a semi-empirical model for inversion charge centroid can be used like BSIM-CMG. The charge centroid correction model in BSIM-CMG is mainly based on the work done by *Venugopalan et al.* [14].

In this work, we have analysed the applicability of the methodology described by *Venugopalan et al.* for low ef-

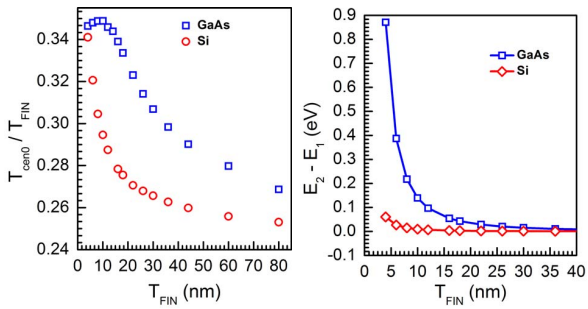
This work is supported by the Visvesvaraya PhD scheme by MeitY, Government of India and Indian Space Research Organization (ISRO) RESPOND project.

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00047



(a) (b)

Fig. 1: (a) Schematic representation of the double gate FET used in this work. Here, T_{FIN} is the body thickness. An insulator thickness of 1 nm (EOT) is used for all the simulations. (b) 1D potential well used to represent the double gate FET structure.



(a) (b)

Fig. 2: (a) The Normalized T_{cen0} as a function of T_{FIN} for GaAs and silicon channel DGFETs. The normalized T_{cen0} for GaAs channel DGFET remains constant for T_{FIN} less than 12 nm. (b) The subband energy difference between the ground state and the first excited state as a function of T_{FIN} for GaAs and silicon channel DGFETs. The difference between the subband energies increases at lower T_{FIN}. The subband energy difference between the ground state and the first excited state is almost 0.8eV for a 3nm thick GaAs channel DGFET.

fective mass III-V channel double gate field effect transistors (DGFETs). For simplicity, we will refer the model by *Venugopalan et al.* as the existing model hereafter. We have calculated the exact charge centroid values using an 1D self-consistent PS solver. We examined both geometrical and bias dependence of the charge centroid and found that the model proposed in [14] fails to predict the behaviour of charge centroid in III-V DGFETs. Alternatively, there are several models reported specifically for III-V DGFETs [15]–[18]. However, these models either use a constant charge centroid value or resort to the similar empirical equation proposed in [14]. In this paper, through 1D PS solver simulations, we identified the reason behind the failure of the existing model and proposed a correction to the existing model. The proposed model is validated by using the results from 1D PS solver and found to be accurate for different low effective mass III-V channel materials as well as for silicon DGFETs. The proposed model is, therefore, unified and can be used across DGFETs with different channel materials.

The rest of the paper is organised as follows. Details about the simulation setup and the charge centroid extraction are described in Sec. II. The reason behind the failure of the existing model for III-V DGFETs is dicussed in Sec. III. The new model is then proposed and is validated for different channel materials. The work is finally summarized in Sec. IV.

II. Simulation Setup

The DGFET device geometry used in this paper is schematically shown in Fig. 1a. InAs, $In_{0.53}Ga_{0.47}As$ and GaAs as channel materials with Al_2O_3 as the gate insulator is used for simulating the III-V DGFETs. The silicon with SiO_2 is used to simulate the conventional silicon channel DGFET. The material parameters are extracted from [19], [20]. Isotropic effective mass and 2D density of states (DOS) with Fermi-Dirac statistics are taken into account for the simulation. The simulations are done assuming negligible wavefunction penetration into the gate insulator.

Due to 1D confinement and assumption of negligible wavefunction penetration into the gate insulator, the DGFET structure can be modeled by a 1D infinite potential well (see Fig. 1b). The inversion charge centroid thickness (T_{cen}) with respect to the insulator-semiconductor interface are calculated as,

$$T_{cen} = \frac{T_{FIN}}{2} - \frac{\int_0^{T_{FIN}/2} n(x)xdx}{\int_0^{T_{FIN}/2} n(x)dx} \quad (1)$$

Here, T_{FIN} is the DGFET body thickness and $n(x)$ is the volume charge density. T_{cen} is numerically calculated using the $n(x)$ extracted from the 1D PS solver.

III. Model Description

A. Geometry Dependence

Fig. 2a plots the simulated (1D PS solver) T_{cen} normalized to T_{FIN} as a function of T_{FIN} for GaAs and silicon channel DGFETs. The T_{cen} values are extracted at $V_G \approx V_{FB}$ + 50 mV to eliminate the effect of bias voltage (V_G). Since only the geometry dependence is captured here, the centroid thickness is referred to as T_{cen0}. As shown in Fig. 2a, (a) The charge centroid moves away from the interface with reduction in T_{FIN}, (b) For a particular T_{FIN}, the charge centroid for GaAs DGFET is farther from the interface compared to that of Si DGFET and (c) The charge centroid remains constant for GaAs DGFET at low values of T_{FIN}. The reason for these differences can be understood by analysing the number of occupied subbands and the charge distribution profile in each subband.

The charge distribution profile (n(x)) in each subband mainly depends upon its wavefunction. According to the solution of 1D Schrödinger equation for an infinite potential well, the absolute value of ground state wavefunction is proportional to $cos^2(\pi x/T_{FIN})$ with maximum probability density at centre of the well. For a very thin semiconductor, the structural confinement causes the carrier to occupy only the first subband. This results in n(x) with a peak at centre of the channel and a higher value of T_{cen0} as per (1). With the increase in the fin thickness, the confinement reduces and the carrier starts occupying higher energy subbands. This causes

the charge distribution to flatten out and T_{cen0} reduces. For a thick fin, the subband merges to form quasi-continuum in energy leading to a more uniform charge distribution.

Fig. 2b shows the difference between ground state and first excited energy level for Si and GaAs DGFETs. As energy value of the nth subband ($E_n = n^2\pi^2\hbar^2/2m^*T_{FIN}^2$) is inversely proportional to the effective mass (m^*), the subband energy difference is smaller for the Si DGFETs in comparison to GaAs DGFETs. As a result for a Si DGFET, with increase in the fin thickness there is a gradual increase in the probability of occupation of higher energy subband. Therefore, the n(x) changes gradually from having peak at the centre of the channel to a more flat profile as shown in Fig. 3a, this results into a uniform decrease of the T_{cen0} as shown in Fig. 2a for Si DGFET. On the other hand, compared to a Si DGFET, the subband energy difference (at a particular T_{FIN}) for GaAs DGFET is much higher for $T_{FIN} < 12$ nm. This indicates the possibility of only first subband occupation and results in an overlapping n(x) profile for $T_{FIN} < 12$ nm, with peak at centre of the semiconductor fin as shown in Fig. 3b. The subband energy difference gradually decreases with increasing T_{FIN} above 12 nm, indicating higher subband occupation. As the n(x) doesn't change the T_{cen0} also remains constant for $T_{FIN} < 12$ nm and decreases gradually after that for GaAs DGFETs (see Fig. 2a).

The existing model captures the geometry dependence of T_{cen0} using the following equation [14],

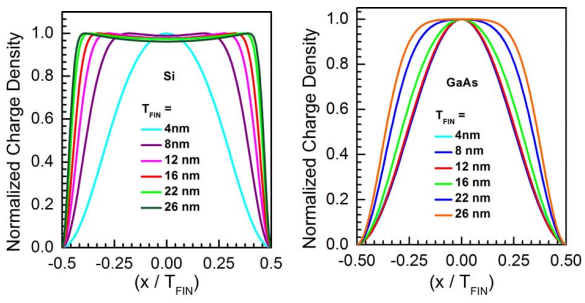
$$\frac{T_{cen0}}{T_{FIN}} = 0.25 + (0.351 - 0.25) * exp(-T_{FIN}/T_0) \quad (2)$$

Here, 0.351 and 0.25 are the asymptotic values of T_{cen0} for thin and thick fin respectively and T_0 is a model parameter. According to (2), starting from the asymptotic value of 0.351, the T_{cen0} decreases exponentially controlled by a single slope factor T_0. Fig. 4a shows the simulated and the modeled normalised T_{cen0} as a function of T_{FIN} for GaAs and silicon DGFETs. Since the existing model ignores the fact that for low m* channel material the channel charges tend to occupy only the first subband and the T_{cen0} remains constant for lower T_{FIN}, it fails to describe accurately the behaviour of T_{cen0} for GaAs DGFETs. In the case of GaAs DGFET, a single T_0 is not sufficient. We therefore propose a modification to (2) to capture the effect of constant T_{cen0} for lower T_{FIN} as,

$$\frac{T_{cen0}}{T_{FIN}} = 0.351 - (0.351 - 0.25)exp\left(-\frac{\frac{\alpha}{T_{FIN}} + \beta}{T_{FIN}}\right) \quad (3)$$

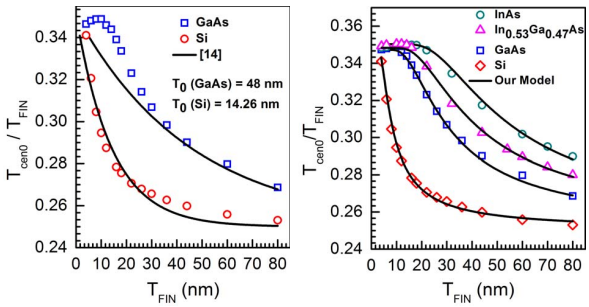
Here, α and β are the model parameters. In (3), the numerator $(\alpha/T_{FIN} + \beta)$ reduces to (α/T_{FIN}) for lower T_{FIN}. The exponential term drops rapidly and T_{cen0}/T_{FIN} saturate to 0.351 for lower T_{FIN}. While for larger T_{FIN}, $(\alpha/T_{FIN} + \beta)$ reduces to β and equation assumes the normal exponential form.

Fig. 4b compares the simulated T_{cen0} (as a function of T_{FIN}) with the model propoesed in (3) for GaAs, Si, $In_{0.53}Ga_{0.47}As$ and InAs channel DGFETs. As shown, the proposed model matches very well with the simulated data. The list of the



(a) (b)

Fig. 3: Normalized charge density per unit volume for, (a) Silicon DGFET and (b) GaAs DGFET with different T_{FIN}. The distance along the thickness of the channel is also normalized. Distribution of the charge density for silicon DGFET changes gradually from having a peak at the centre of the channel to a flat profile, while for GaAs DGFET the charge density distribution overlaps for T_{FIN} less than 12 nm.



(a) (b)

Fig. 4: Normalized T_{cen0} as a function of T_{FIN} for, (a) GaAs and silicon channel DGFETs and (b) For InAs, $In_{0.53}Ga_{0.47}As$, GaAs and silicon DGFETs. The symbols represent the 1D PS solver data. The solid lines in (a) represent existing model whereas the solid lines in (b) represent data from our model. The existing model fails to describe the T_{cen0} behaviour for GaAs DGFET whereas our proposed model shows an excellent agreement with the simulated data both for III-V and silicon channel DGFETs.

TABLE I: Parameters used for matching the model with 1D PS slover data

Channel Material	$\alpha(nm^2)$	$\beta(nm)$
InAs	1405	20
$In_{0.53}Ga_{0.47}As$	675	19.5
GaAs	425	12
Si	25.5	3.75

model parameters used for the matching is shown in Table I. It can be noted that compared to the existing model, the proposed model shows an excellent agreement even for the Si DGFETs. Therefore, (3) can be used to model the charge centroid for the low effective mass III-V as well as the Si channel materials. The proposed model is, therefore, unified and can be used for both Si and III-V channel materials by appropriately tunning parameters α and β.

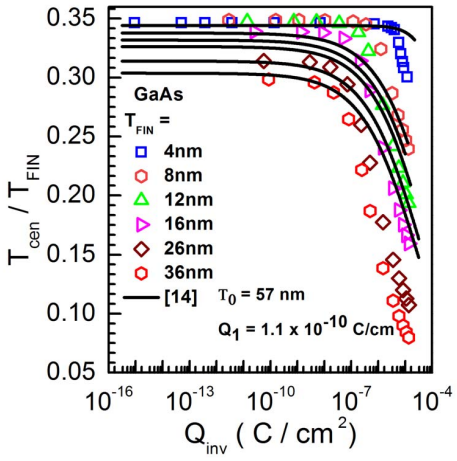


Fig. 5: Normalized T_{cen} as a function of the inversion charge density (Q_{inv}) for different T_{FIN}s for GaAs DGFETs. The symbols represent the 1D PS solver data. The solid lines represent the existing model. The existing model is unable to capture accurately the bias dependence of T_{cen} for GaAs DGFETs.

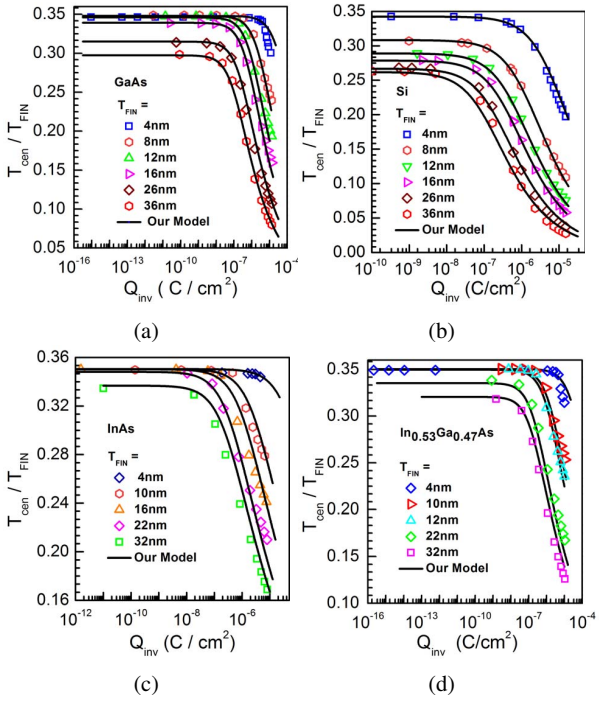


Fig. 6: Normalized T_{cen} as a function of inversion charge density (Q_{inv}) for (a) GaAs, (b) silicon, (c) InAs and (d) $In_{0.53}Ga_{0.47}As$ DGFETs. The symbols represent the 1D PS solver data. The solid lines represent the proposed model. The new model matches very well with the simulated data.

B. Bias Dependence

With increase in V_G, the channel charge increases thereby causing band bending at both the interfaces of the DGFET. The electric field also shifts the charge distribution peak towards the insulator-semiconductor interface and this results in decrease of T_{cen}. This effect has been modeled by [14] using the concept of critical charge density. It has been argued that the T_{cen} remains almost constant till a critical charge density Q_0, after which it starts to decrease. Using the concept of Debye screening length this Q_0 was modeled as a linearly decreasing function of T_{FIN} ($Q_0 = Q_1/T_{FIN}$, Q_1 is the model parameter). The bias dependence of T_{cen} has been captured in [14] using the equation,

$$T_{cen} = \frac{T_{cen0}}{1 + \left(\frac{T_{FIN} Q_{inv}}{Q_1}\right)^{\gamma}} \tag{4}$$

Here, T_{cen0} capture the geometry dependence of T_{cen}, given by (2), Q_{inv} is the inversion charge density, γ and Q_1 are the model parameters. Fig. 5 compares the T_{cen} vs Q_{inv} plot for GaAs DGFETs generated using the 1D PS solver with the existing model [14]. As shown, the existing model is unable to capture the bias dependence of T_{cen} for GaAs DGFETs. The T_{cen} value do decreases after some Q_0 as argued in [14]. But, instead of a linear dependence of Q_0 on T_{FIN}, the Q_0 shows a large change after T_{FIN} of around 12 nm.

The reason for this non-linear dependence (Q_0 vs. T_{FIN}) can also be attributed to the large difference between the subband energies in GaAs DGFETs due to low m*. As explained in section III-A, the charges tend to occupy only the first subband in GaAs DGFETs for $T_{FIN} < 12$ nm. As the spacing between two back-to-back subbands (in terms of energy) is higher in GaAs DGFETs, it requires higher bias or Q_0 to have an appreciable band bending in the channel. This results in a higher Q_0 for $T_{FIN} < 12$ nm. For $T_{FIN} > 12$nm, Q_0 drops gradually as more subbands are occupied by the charges. To capture this nonlinear change of Q_0 with T_{FIN}, the (4) is modified in the proposed model as follows,

$$Q_0 = \frac{Q_1 10^{\delta/T_{FIN}}}{T_{FIN}} \tag{5}$$

$$T_{cen} = \frac{T_{cen0}}{\left(1 + \frac{Q_{inv}}{Q_0}\right)^{\gamma}} \tag{6}$$

where, Q_1, δ and γ are the model parameters. Fig. 6 shows the simulated and the modeled T_{cen} as a function of Q_{inv} for GaAs, Si, $In_{0.53}Ga_{0.47}As$ and InAs channel DGFETs. The model parameters used to match our model with the 1D PS solver data are shown in Table II. It can be seen that the proposed model accurately captures/predicts the bias dependence of T_{cen} for both Si channel and III-V channel DGFETs.

TABLE II: Parameters used for matching the model with 1D PS slover data

Channel Material	γ	$\delta(nm)$	$Q_1(c/cm)$
InAs	0.199	5.5	6.75x10^{-13}
$In_{0.53}Ga_{0.47}As$	0.25	6.5	5.15x10^{-13}
GaAs	0.27	6.5	4x10^{-13}
Si	0.425	3.25	3.85x10^{-13}

IV. Conclusion

To summarize, the applicability of the charge centroid model used in BSIM-CMG compact model for low effective mass III-V channel DGFETs was systematically investigated. It was found that the existing models could not predict the charge centroid behaviour in case of III-V DGFETs accurately. The charge centroid for III-V DGFET shows anomalous behaviour and the reason behind this anomalous behavior was analyzed using the exact charge centroid values extracted from 1D Poisson-Schrödinger solver. The reason was attributed to the higher subband energy difference of low effective mass channel materials, which is ignored in the existing models. A modification to the existing model was proposed to extend its validity to low effective mass channel materials. The proposed model is verified for different DGFET body thickness, channel materials and found to be accurate. A single model equation was shown to fit the data for both III-V and Si channel DGFETs for a wide range of applied bias. The proposed model is, therefore, unified and can be used for DGFETs with both Si and III-V channel materials.

References

[1] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors," *Nature*, vol. 479, no. 7373, p. 310, 2011.

[2] K. J. Kuhn, "Considerations for ultimate cmos scaling," *IEEE transactions on Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012.

[3] J. A. Del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, 2011, doi: 10.1038/nature10677.

[4] M. K. Hudait and R. Chau, "Integrating III-V on silicon for future nanoelectronics," in *2008 IEEE Compound Semiconductor Integrated Circuits Symposium*, Oct 2008, pp. 1–2, doi: 10.1109/CSICS.2008.8.

[5] S. Ramesh, T. Ivanov, V. Putcha, A. Alian, A. Sibaja-Hernandez, R. Rooyackers, E. Camerotto, A. Milenin, N. Pinna, S. E. Kazzi, A. Veloso, D. Lin, P. Lagrain, P. Favia, N. Collaert, and K. D. Meyer, "Record performance Top-down $In_{0.53}Ga_{0.47}As$ vertical nanowire FETs and vertical nanosheets," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec 2017, pp. 17.1.1–17.1.4, doi: 10.1109/IEDM.2017.8268406.

[6] A. Vardi, L. Kong, W. Lu, X. Cai, X. Zhao, J. Grajal, and J. A. del Alamo, "Self-aligned InGaAs FinFETs with 5-nm fin-width and 5-nm gate-contact separation," in *Electron Devices Meeting (IEDM), 2017 IEEE International*. IEEE, 2017, pp. 17–6, doi: 10.1109/IEDM.2017.8268411.

[7] D. Lizzit, D. Esseni, P. Palestri, P. Osgnach, and L. Selmi, "Performance Benchmarking and Effective Channel Length for Nanoscale InAs, $In_{0.53}Ga_{0.47}As$ and sSi n-MOSFETs," *IEEE transactions on Electron Devices*, vol. 61, no. 6, pp. 2027–2034, 2014.

[8] M. Rau, E. Caruso, D. Lizzit, P. Palestri, D. Esseni, A. Schenk, L. Selmi, and M. Luisier, "Performance projection of iii-v ultra-thin-body, finfet, and nanowire mosfets for two next-generation technology nodes," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016, pp. 30.6.1–30.6.4.

[9] A. Pethe, T. Krishnamohan, D. Kim, S. Oh, H. S. P. Wong, Y. Nishi, and K. C. Saraswat, "Investigation of the performance limits of iii-v double-gate n-mosfets," in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, Dec 2005, pp. 605–608.

[10] N. Paydavosi, S. Venugopalan, Y. S. Chauhan, J. P. Duarte, S. Jandhyala, A. M. Niknejad, and C. C. Hu, "Bsimspice models enable finfet and utb ic designs," *IEEE Access*, vol. 1, pp. 201–215, 2013.

[11] Y. S. Chauhan, D. D. Lu, V. Sriramkumar, S. Khandelwal, J. P. Duarte, N. Payvadosi, A. Niknejad, and C. Hu, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. Academic Press, 2015.

[12] D. Jin, D. Kim, T. Kim, and J. A. del Alamo, "Quantum capacitance in scaled down III-V FETs," in *2009 IEEE International Electron Devices Meeting (IEDM)*, Dec 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424312.

[13] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur, and M. Rodwell, "Simulation of electron transport in high-mobility MOSFETs: density of states bottleneck and source starvation," in *2007 IEEE International Electron Devices Meeting*, Dec 2007, pp. 109–112, doi: 10.1109/IEDM.2007.4418876.

[14] S. Venugopalan, M. A. Karim, S. Salahuddin, A. M. Niknejad, and C. C. Hu, "Phenomenological compact model for qm charge centroid in multigate fets," *IEEE Transactions on Electron Devices*, vol. 60, no. 4, pp. 1480–1484, 2013.

[15] S. Mudanai, A. Roy, R. Kotlyar, T. Rakshit, and M. Stettler, "Capacitance compact model for ultrathin low-electron-effective-mass materials," *IEEE Transactions on Electron Devices*, vol. 58, no. 12, pp. 4204–4211, 2011.

[16] C. Yadav, J. P. Duarte, S. Khandelwal, A. Agarwal, C. Hu, and Y. S. Chauhan, "Capacitance modeling in iii–v finfets," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3892–3897, 2015.

[17] M. D. Ganeriwala, C. Yadav, N. R. Mohapatra, S. Khandelwal, C. Hu, and Y. S. Chauhan, "Modeling of charge and quantum capacitance in low effective mass iii-v finfets," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 6, pp. 396–401, 2016.

[18] A. S. Chakraborty and S. Mahapatra, "Surface Potential Equation for Low Effective Mass Channel Common Double-Gate MOSFET," *IEEE Transactions on Electron Devices*, vol. 64, no. 4, pp. 1519–1527, 2017, doi: 10.1109/TED.2017.2661798.

[19] J. Kim and M. V. Fischetti, "Electronic band structure calculations for biaxially strained Si, Ge, and III-V semiconductors," *Journal of Applied Physics*, vol. 108, no. 1, p. 013710, 2010, doi: 10.1063/1.3437655.

[20] J. Robertson and B. Falabretti, "Band offsets of high K gate oxides on III-V semiconductors," *Journal of applied physics*, vol. 100, no. 1, p. 014111, 2006, doi: 10.1063/1.2213170.