Ultra Low Power Digital Front-End for Single Lead ECG Acquisition

Sanket Thakkar and Biswajit Mishra*
VLSI and Embedded Systems Research Group, DA-IICT, Gandhinagar 382 007, India
*Email: {biswajit_mishra}@daiict.ac.in

***Abstract*—A low power single lead electrocardiogram front end acquisition system in $0.18\mu m$ CMOS process with supply voltage $0.5V$ is presented in this paper. The analog blocks in Low Noise Amplifier (LNA), filters and passive elements that performs amplification, DC offset cancellation is replaced by a Moving Average Voltage to Time Converter (MA-VTC) to get amplification and alias removal in the time domain. A digital feedback algorithm is used to cancel out the DC offset. The front-end structure is designed in the subthreshold region of MOS to reduce the power consumption in the circuit. The proposed architecture consumes $50nW$ of power with a gain of $670\mu s/V$.**

***Keywords*—All Digital Frontend Acquisition, Electrocardiogram, ECG, Nanowatt**

I. Introduction

Miniaturization in wearable devices for continuous health monitoring are gaining popularity. Such applications require signal processing where the challenge is to design very low power analog front end circuits. Low input referred noise, reconfigurable bandwidth, and programmable gain are required in the front end processing block to accommodate the weak signals and the high dynamic range [1].

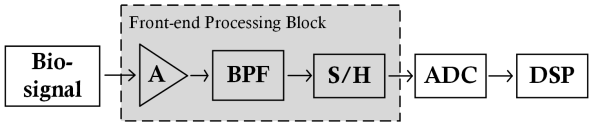

Fig. 1: Block Diagram of a Biomedical Acquisition System

As shown in Fig. 1, a biomedical acquisition system front end processing consists of analog blocks in front-end amplifier and filters that are power consuming units [2]. Examples of such systems have been discussed in [3] where the ECG front end converts frequency domain configuration to time domain. By doing so, certain analog blocks including the front end acquisition could be designed using digital circuits. The advantage of such circuits is the lowering of supply voltage that provides power advantage that is often a requirement and necessity for wearable devices.

In [4] authors have discussed an all digital front end acquisition system for an ECG system and advantages discussed are:

1) Amplification without a dedicated amplifier done in the time domain.
2) Eliminating DC offset voltage without any passive elements with digital feedback loop.
3) Aliasing effect is cancelled out by using a moving average filtering without the need of LPFs.

However the architecture in [4] suffers from a poor DC offset cancellation, low gain and is only useful for ECG applications. In this work, we have proposed the following:

1) Single lead ECG front end acquisition that can be extended to ExG (EKG, EOG, EEG, ECG, EMG) applications.
2) Overall gain is increased due to circuit optimization with lower power consumption.
3) The input variation adaptability and noise cancellation by a novel algorithm.
4) A novel decoding structure for controlling the digital to current converter for DC offset cancellation.

This paper is organized as follows: Section II presents the proposed architecture and its sub blocks. Moving Average Filtering and Offset cancellation technique are discussed in Section III and IV respectively. Section V presents the mathematical model. Simulation Results and Conclusion are discussed in Section IV and Section V respectively.

II. Proposed architecture

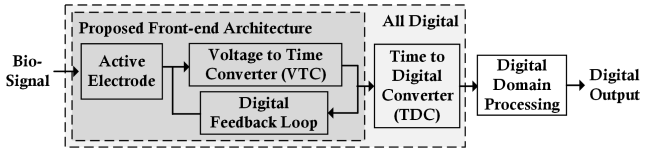

Fig. 2: Block Diagram of Fully Digital Biomedical (ECG) Acquisition System

The block diagram of the proposed digital front end architecture is shown in Fig. 2. The analog front-end is replaced using the digital block with an active electrode, Voltage to Time Converter (VTC), digital feedback loop and Time to Digital Converter (TDC). The output of TDC is digital signal which is further processed in digital domain.

As shown in Fig. 3, a millivolt ($\pm 5mV$) biosignal sensed by the active electrodes is given as an input to the VTC; where the output pulse delay changes according to the input voltage. The digital feedback loop induces offset cancellation technique which remove the input offset voltage according to the pulse delay of VTC.

This digital feedback loop consists of a control logic, a synchronous counter, a decoder with a priority scheme,

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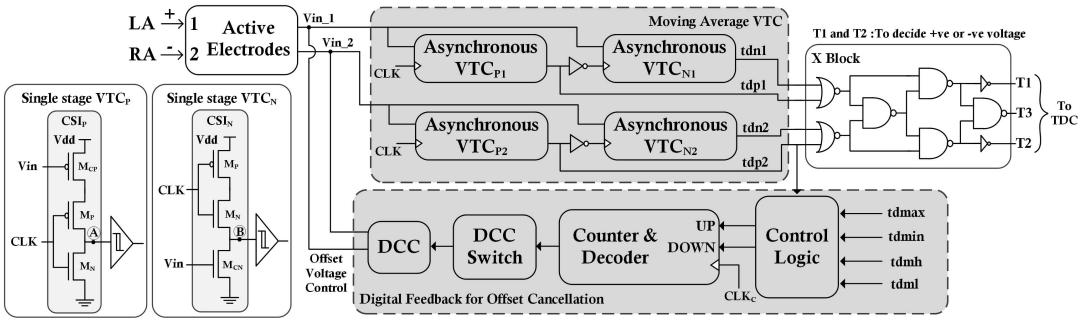

Fig. 3: Schematic of Proposed Front End Architecture

and a Digital to Current Converter (DCC), provides offset cancellation.

A. Single Lead ECG Architecture

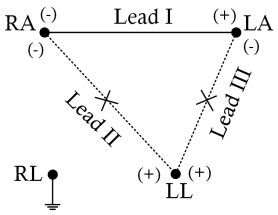

Fig. 4: 3-Leads & Einthoven's Triangle

Traditionally, 12 leads or 3 leads are used to study cardiac activity in the form of electrical signals [5]. The idea of a single lead carrying approximately same information is discussed in [6] where Lead II and Lead III can be ignored as shown in Fig.4.

B. Active Electrodes

In order to improve the sensitivity, a buffer circuit (opamp or a MOS transistor) is used as an active dry electrode [7]. A single MOS transistor exhibits better performance with respect to noise, CMRR and power consumption [7]. A MOS transistor as active electrode is considered (Fig. 5).

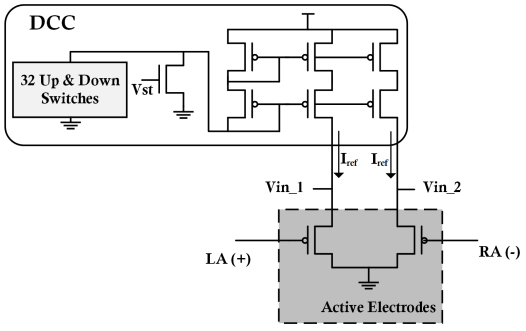

Fig. 5: PMOS as an Active Electrode

C. Voltage to Time Converter (VTC)

As shown in Fig. 3, a single stage VTC [8] is implemented as a combination of current starved inverter (CSI) and inverting Schmitt trigger (ST) circuit. VTC_P has PMOS and VTC_N has NMOS as controlling device. The Schmitt trigger circuit at the output of current starved inverter is used to enhance the rising and falling edge of the clock, which helps in reducing the jitter and power consumption. As the outputs of both inverter and schmitt trigger are inverting in nature, the output of VTC is in phase with the input voltage. In order to obtain more delay, the load capacitance which is the input capacitance of the schmitt trigger is required to be kept large enough by sizing the transistors. By doing so the delay of Schmitt trigger becomes negligible.

In order to get reasonable time domain amplification, 26 stages of VTC_P (positive VTC) and 17 stages of VTC_N (negative VTC) have been used in cascade respectively showing amplification in the time domain [9]. This technique is further enhanced in [4] as an anti-aliasing filter. As the VTC and filtering is performed in the same circuit, it is also called a Moving Average VTC (MA-VTC) generating a *sinc*-function for anti-aliasing. The different number of stages for VTC_P and VTC_N is to balance the delay.

D. Control Logic Block

To detect the offset, the control logic block compares the t_{dp} with four delays (offset cancellation delays *tdmax, tdmin, tdmh,* and *tdml*) with a digital Time Comparator (TC). The UP and DOWN signals are generated from the control logic and is fed to the counter. It is implemented using a negative edge triggered D flip-flop that has lower power consumption compared to analog voltage comparator.

E. Counter and Decoder

A 5-bit synchronous up-down counter is implemented where frequency is set 8× to 10× less than the reference clock (8 KHz). It is done in order to count a fixed number of samples after a time and later to settle down the input voltage level of VTC between the range -5mV to +5mV. Additionally, 5 to 32 bit decoder has been implemented which takes the input from the counter. Corresponding to the count of 0 to 15 (31 to 16), up1 to up16 (down1 to down16) signals are generated which

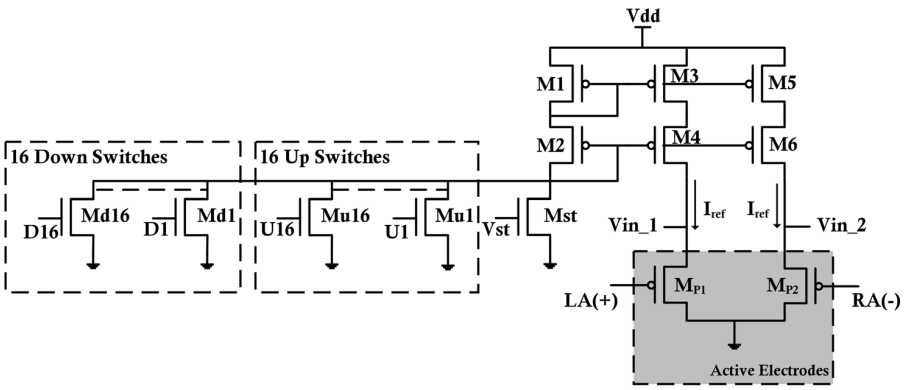

Fig. 6: Digital to Current Converter (DCC)

indicates that the input voltage of VTC is less than -5 mV (greater than +5 mV) and needs to be increased (decreased).

F. Digital to Current Converter (DCC)

Depending on the output of the decoder, the DCC decides the number of MOS that needs to be switched ON (OFF) in order to increase (decrease) the input voltage of the VTC. Effectively the DCC switch is responsible for generating the gate voltages for generating a reference current in the DCC. As shown in Fig. 6, the DCC consists of two voltages Vin_1 and Vin_2 at the output and are fed to the VTC_{P1} and VTC_{P2} blocks.

In order to control the voltage at the output of active electrodes, 32 transistor switches are used. Half of the transistors are used to decrease the current and rest are used to increase the current. This process results in decreasing and increasing the voltage at the output of the active electrodes respectively. Incrementing or decrementing in current requires either V_{GS} or the width of the transistors be changed. In the proposed design, the width of the transistors is changed as adjusting the V_{GS} to an exact value is difficult. The off current is taken into consideration while sizing the transistors. This is done to accommodate and observe single bit change that has a resolution of 3.125 mV.

III. Moving Average Filtering

To ensure the proper functioning of the asynchronous VTC, an antialiasing filter is employed. The low pass filter is used to remove aliasing effect [4] which functions both as VTC and anti-aliasing filter. As the VTC and filtering is done in the same circuit, it is called Moving Average VTC (MA-VTC) and consists of a chain of 26 VTC_P followed by a chain of 17 VTC_N, which generates a sinc function and performs anti-aliasing function.

As the clock passes through the first stage of VTC, a delay is generated proportional to Vin. At the end of the chain an overall delay proportional to Vin is obtained. The delay is either shortened or lengthened by the noise and overall summing of the delay cancels out the effect of the noise. This cancellation is more effective when the averaging takes place during whole clock period. Therefore at each sampled input, the delay of VTC_P and VTC_N is matched in such a way that a constant clock is generated at the output.

The circuit integrates the signal in a time window of duration Tclk. The sum of this integration period generated by the chain of $VTCs$, define the clock period and is given by,

$$H(t) = \frac{1}{T_S}\int_{t-T_S}^{t} V_{in}(\tau)d\tau \tag{1}$$

So, the system response (impulse response) is given as,

$$H(t) = \frac{1}{T_S}\int_{t-T_S}^{t} \delta(\tau)d\tau = u(t) - u(t-T_S) \tag{2}$$

Hence, the frequency response of above function is a *sinc* function. So, we can say MA-VTC perform anti-aliasing filtering.

IV. Offset cancellation technique

The DC offset voltage is generated due to the placement of biopotential electrodes. Thus it adds to non-linearity in the VTC characteristics and needs to be removed. For the offset cancellation technique, an oscillating algorithm *i.e.* voltage increases or decreases in steps and then stabilizing is employed. However, due to variation in input the algorithm at certain times fail [4]. To avoid this, we propose to remove the offset up to $\pm 50mV$.

A. Offset Cancellation Algorithm

As shown in the Fig. 7, the four different delays (tdmax, tdmin, tdmh, tdml) of VTC_P is divided into three regions R1, R2 and R3. Here the delays tdmax, tdmin, tdmh and tdml represents the delay at +5 mV, -5 mV, +1.5 mV and -1.5 mV input voltage respectively. The resolution of DCC is 3.125 mV and the maximum allowable input range is $\pm 5mV$. So, one bit change is reflected as a bias voltage Vb = (5-3.125) mV = 1.875 mV. To create a hysteresis in the delay line, the value of tdmh (tdml) should be less than Vb and is chosen to be 1.5 (-1.5) mV.

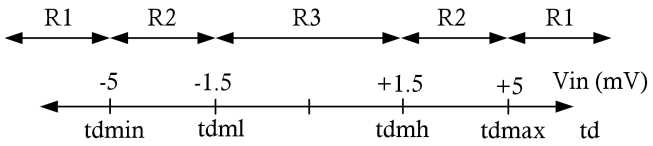

Fig. 7: Regions in the Characteristics of VTCp

Any DC offset that occurs, will be obtained in the R1 region. Our aim is to bring this delay value from R1 to R3 region in order to remove the offset voltage. A feedback system has been created which displaces the delay obtained in the R1 region into R2 region which is then further pushed into the correct R3 region. Due to fluctuations, if the delay value jumps directly from R1 to R3, bypassing R2 region then also the desired output is obtained in the proposed method.

Fig. 3 shows digital feedback for offset cancellation. Initially, the time comparator in control logic is used to compare the output delay of the VTC_P block, tdp with tdmax, tdmin, tdmh and tdml where tdmh and tdml are used to create hysteresis effect in order to avoid continuous switching. On the basis of this delay, a DOWN (UP) signal is set by the control logic if the delay is more (less) than the tdmax (tdmin) and fed to synchronous counter. The counter output is then applied to the decoder, which controls the DCC. At the output of DCC, current is generated according to the digital input which control the input voltage of the VTC_P and VTC_N. This process will continue until the circuit goes into R3 region. If this happens, the input voltage value lies within the tolerable range ($\pm 5mV$) of the circuit.

V. Mathematical Model

In this section, The delay model for VTC has been prepared in subthreshold region. From Fig. 3, the delay of a VTC (td) is the combination of two different delays, the delay of current starved Inverter (t_{CSI}) and the delay of schmitt trigger (t_{ST}).

$$td = t_{CSI} + t_{ST} \tag{3}$$

The input capacitance of Schmitt trigger is working as a load (C_L) for current starved circuit. In order to obtain more delay, the load capacitance is required to be kept large enough. So, the sizing of the transistors is kept large. This has an added favourable effect that the delay effect of Schmitt trigger becomes negligible.

The mathematical model has been developed with the certain assumptions, mentioned below:

1) The term $(1-e^{\frac{-|V_{DS}|}{V_t}})$ is ignored in the $eq.$ 4 as it close to 1. The on current I_D is given as:

$$I_D = I_0 \left(e^{\frac{|V_{GS}|-|V_{TH}|}{\eta V_t}}\right)\left(1-e^{\frac{-|V_{DS}|}{V_t}}\right) \tag{4}$$

where I_0 is the off current, η is the subthreshold slope factor, V_{GS}, V_{TH} and V_{DS} are the gate, threshold and drain voltage respectively.

2) Node A and B of VTC in Fig. 3 have full swing of 0 and V_{dd}. So, the delay of CSI_P and CSI_N is approximated to $t_{CSI_P} = \frac{C_L \times V_{dd}}{I_{DP}}$ and $t_{CSI_N} = \frac{C_L \times V_{dd}}{I_{DN}}$. where C_L is the total input capacitance of schmitt trigger and V_{dd} is the supply voltage.

With these assumptions, the current flowing through M_{CP} is,

$$\begin{aligned} I_{DP} =& I_0 \left(e^{\frac{Vdd-Vin-|V_{THp}|}{\eta V_t}}\right) \\ =& I_0 \left(e^{\frac{Vdd-|V_{THP}|}{\eta V_t}}\right)\left(e^{\frac{-Vin}{\eta V_t}}\right) \end{aligned} \tag{5}$$

So, the delay of CSI_P is,

$$\begin{aligned} t_{CSI_P} =& \frac{C_L \times V_{dd}}{I_0 \left(e^{\frac{Vdd-|V_{THp}|}{\eta V_t}}\right)} \left(e^{\frac{Vin}{\eta V_t}}\right) \\ =& \gamma_P \left(e^{\frac{Vin}{\eta V_t}}\right) \end{aligned} \tag{6}$$

From the Maclaurian expansion (ignoring higher order terms), $eq.$ 6 can be expressed as:

$$t_{CSI_P} = \gamma_P \left(1 + \frac{Vin}{\eta V_t}\right) \tag{7}$$

So, the total propagation delay of VTC_P and VTC_N from the $eq.$ 3 is given by,

$$\begin{aligned} tdp\_1 &= \gamma_P \left(1 + \tfrac{Vin}{\eta V_t}\right) + t_{ST}, \\ tdn\_1 &= \gamma_N \left(1 - \tfrac{Vin}{\eta V_t}\right) + t_{ST}, \end{aligned} \tag{8}$$

where, γ_P is the delay multiplying factor for VTC_P and $\gamma_P = \frac{C_L \times V_{dd}}{I_0\left(e^{\frac{Vdd-|V_{THp}|}{\eta V_t}}\right)}$ and $\gamma_N = \frac{C_L \times V_{dd}}{I_0\left(e^{\frac{-|V_{THn}|}{\eta V_t}}\right)}$ is the delay multiplying factor for VTC_N.

The $eq.$8 represent theoretical delay of a single stage VTC_P and VTC_N. The delay of asynchronous VTC_P and asynchronous VTC_N is nothing but $n1 \times tdp\_1$ (n1 = No. of stages of VTC_P) and $n2 \times tdn\_1$ (n2 = No. of stages of VTC_N) respectively.

$$\begin{aligned} td_{TDC} =& t_{dp1} - t_{dp2} \\ =& \gamma_P \left(\frac{|Vin_1 - Vin_2|}{\eta V_t}\right) \\ =& \delta(|Vin_1 - Vin_2|) \end{aligned} \tag{9}$$

where, δ is another delay multiplying factor given as $\delta = \frac{\gamma_P}{\eta V_t}$.

The delay difference of these asynchronous VTCs represent the averaging of the input signal in full clock cycle. The delay difference of two asynchronous VTC_P at the output represent the voltage difference of the input. So, the $eq.$ 9 represents the delay difference of the differential input and it is the input of TDC.

VI. Simulation results and discussion

The simulations for the proposed architecture were performed using $0.18\mu m$ CMOS physical models varying input voltage from $-5mV$ to $+5mV$.

A. Results of VTC_P and VTC_N

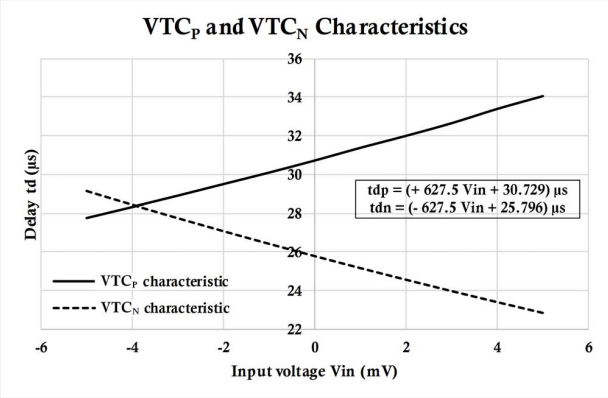

Fig. 8: Results of VTC_P and VTC_N Stages

The VTC_P and VTC_N characteristics for 26 stages and 17 stages respectively are as shown in Fig. 8. As can be seen in Fig.8, as Vin changes from $-5mV$ to $+5mV$, the delay of VTC_P and VTC_N are linear and close to $6.275\mu s$. So, the gain of VTC_P and VTC_N are said to be $+627.5\mu s/V$ and $-627.5\mu s/V$ respectively.

Due to linearity in delay, the input voltage can be predicted. The redundant delay difference of VTC_P and VTC_N shown from two equations (see inset Fig. 8) is removed by taking the delay difference of two MA-VTC.

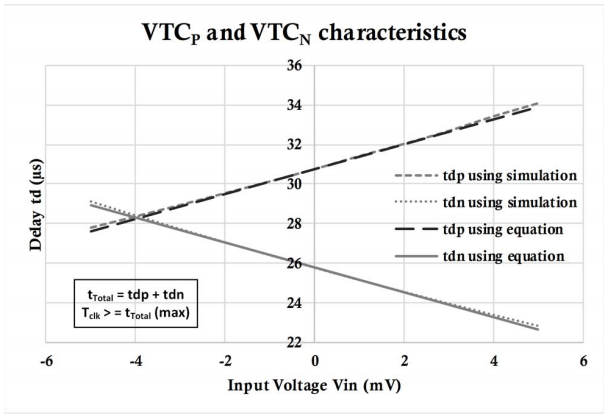

Fig. 9: VTC_P and VTC_N Characteristics using Simulation and Equation

When VTC_P blocks (26 stages of VTC_P) are followed by VTC_N blocks (17 stages of VTC_N), then the total propagation delay is the addition of the delays generated by the VTC_P and VTC_N blocks *i.e.* $t_{Total} = tdp + tdn$. The clock period should be slightly larger than the total max propagation delay from the equation (see inset Fig. 9).

The total propagation delay from the simulation is $56.92\mu s$. So, the maximum allowable clock frequency is approximately $8.5KHz$ which is well within the range of sampling frequency for such type of application (typically $\sim$ 0.5 KHz).

The results obtained from the equations are approximately same with the results obtained from the simulation as shown in Fig. 9.

B. Results of DCC

The digital feedback circuit of the front end architecture is designed to be in a sleep mode when there is no input offset voltage. The drain of the electrode is maintained at (0.2 V + Input voltage). The offset is always removed from the DCC so that the drain is always maintained at (0.2 V + Input voltage) even after the input of electrode is (offset + input voltage). From Fig. 10, It is observed that the value of Vin_1 and Vin_2 is (0.2V + Input voltage) at the absence of input offset. From Fig. 11, after the elimination of the offset of 50 mV the final Vin_1 and Vin_2 is (0.2 + Input voltage).

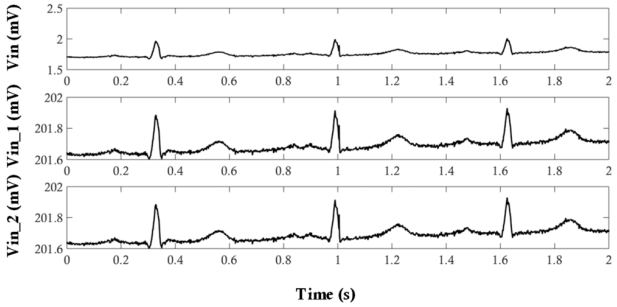

Fig. 10: The Output of DCC without Input Offset

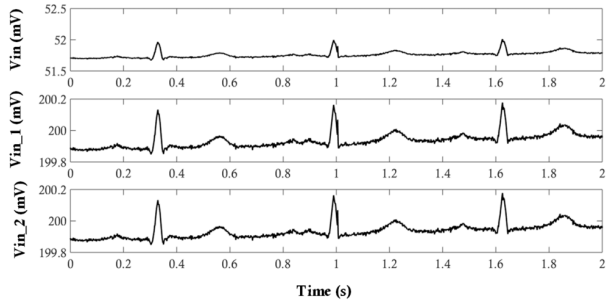

Fig. 11: The Output of DCC with +50 mV Input Offset

C. Mapping of Front-end output delay to input voltage

The front-end architecture has three signals at the output. Out of which two are required to decide the positive input voltage or negative input voltage. The third signal is input to the Time to Digital Converter (TDC). The linearity of the ECG front end output delay with respect to the input voltage can be observed as shown in Fig. 12. As the gain of the

TABLE I: Performance summary and comparison Results

Parameter	Proposed Work	[4]	[10]	[11]	[12]	[3]	[1]
Technology	$0.18\mu m$	$0.18\mu m$	$40nm$	$0.18\mu m$	$0.18\mu m$	$65nm$	$0.35\mu m$
Voltage Supply (V)	0.5	0.5	0.6	0.8	1	0.5	1
Architecture	Digital	Digital	Mixed	Mixed	Analog	Mixed	Analog
Gain	(627.5 (VTC), 670 (System)) $\mu s/V$	$176\mu s/V$	-	$35-47dB$	$34dB$	-	$45.6-60dB$
Power (W)	$50n$	$274n$	3.3μ	5.1μ (Amp), 384μ (TDC)	8.49μ	5.04μ	$450-895n$
Applications	ECG	ECG	ECG	ECG	ECG	Neural	ECG, EEG etc

digital front end is $670s/V$, the resolution of the ECG is $67ns/100V$. This can be captured with low power TDCs. For example, the TDC reported in [13], has a resolution of 586.4 ps consuming $32.5W$ and can be interfaced to convert the ECG front end output to a digital code and is left as a future work. The architecture presented here can be extended to ExG (ERG, EOG, EEG, ECG, EMG) where the lower and higher cutoff frequencies are fixed at $1Hz$ and $500Hz$ respectively and can be accommodated with the TDC [13] that is capable of capturing the $1\mu V$ change in ExG signals. It is also possible to obtain better accuracy of the acquisition circuit with higher resolution of the TDC consuming slightly higher power $(201.8ps, 315.5\mu W)$.

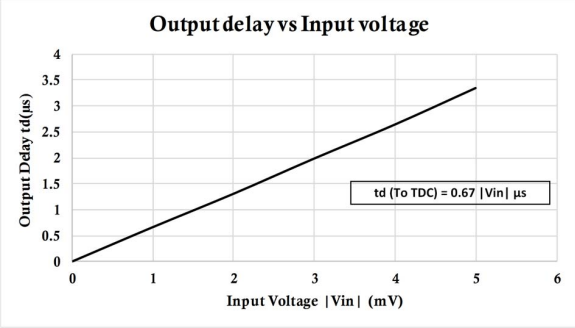

Fig. 12: Delay Output of the Front-End Architecture

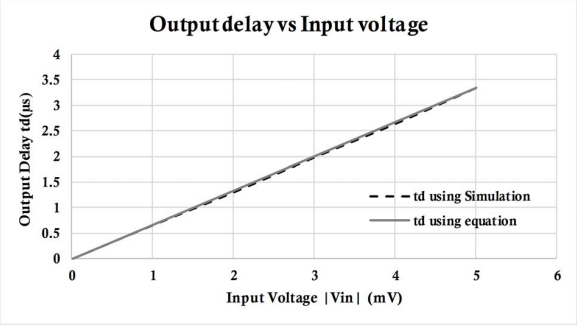

Fig. 13: Delay Output of Front-end Architecture (Simulation v/s Analytical Equation)

The results obtained from the equation are approximately same with the results obtained from the simulation as given in Fig. 13. The proposed circuit achieves a higher gain compared to [4]. In terms of power, our design is the lowest as compared to the reported literature shown in Table I.

VII. Conclusion

The proposed circuit focuses on the design that eliminates passive elements, LNA, and analog filters. A novel technique for offset cancellation has been used which reduces the offset voltage of $50mV$ to less than $5mV$. The design employs moving average in time domain and does not require dedicated antialiasing filter. The proposed architecture is implemented using 0.18- µm CMOS technology at 0.5 V supply consuming $50nW$ with a gain of $670\mu s/V$.

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