Design and Physical Implementation of Array Signal Processor ASIC for Sector Imaging Systems

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***Abstract*—In this paper, we present architecture, physical design, and implementation of Array Signal Processor (ASP) which performs phased array beamforming for sector imaging systems, such as RADAR, SONAR, Medical Ultrasound, Multiple-Input-Multiple-Output (MIMO) etc. The architecture is Cycle stealing DMA based delay and sum (DAS) with dynamic receive focus support. The processor supports 8 channels, operates up to 20 MHz sampling frequency and streams LVDS input data upto 280 Mbps (14 bit ADC). It supports up to 65 fps, 61 beams per frame to support a Field Of View (FOV) of 60 degrees with 1-degree lateral resolution. The dynamic receive focus supports a resolution of 64 samples per beam up to near field, and based on sampling frequency the resolution is achievable up to 1.2 mm. The physical design is targeted 180nm SCL™ technology, and we used CANENCE™ toolchain for physical design and Synopsis™ Prime Time (PT) for timing closure. The power consumption of the ASIC is 440mW and physical size is 5mm x 5mm. The package selected is 80 pin LQFN and accordingly,bonding diagram is designed.**

Keywords—Array Signal Processor, Phased array beamforming, dynamic receive focus, Cycle stealing DMA, Physical Design, Bonding Diagram.

I. Introduction

Array signal processing or beamforming (Fig.1) is a technique which is employed to focus the multitude of small transducer elements to a single focal point by providing suitable delay values to each transducer element. A sector imaging array (phased array) is a sequence of transducers which are equally spaced by $\lambda/2$, where $\lambda$is the wavelength of wave propagation.In dynamic receive focus beamformer, the receive focal points will change as a function of range. The propagation path of a beam is further divided into near-field range and far field range. The near-field range is the distance between the center element of the transducer array and the focal point where the beam is converged while transmitting a wave and it is called a focal zone. The beam divergence starting from the focal zone is called far field range. For an array geometry, the near field is calculated as $\mathbf{2D^2/\lambda}$, where D is the active aperture area and beyond $\mathbf{2D^2/\lambda}$ is far-field. The near-field backscattered signals are uniformly sampled by the dynamic receive focal points, that delivers high-quality focus over the entire near field. The far-field beamforming operation is performed by applying the propagation delay value to each transducer element. The delay resolution applied to each transducer element (channel) of the beamformer is the integer multiple of the sample period of ADC, is called coarse delay resolution, and the delay accuracy provided to each channel, less than the sample period is called fractional or fine delay resolution. To generate a fine delay, interpolation needs to be performed and the same can be implemented by the digital FIR filter by employing proper filter coefficients. The received ultrasound beam has main lobe width and side lobe levels, the side lobe levels are noises and can be suppressed by single window apodization.

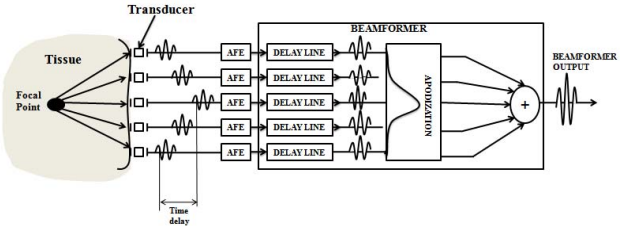

Fig. 1 Beamforming Technique.

This paper is outlined as follows. Section II describes the Array Signal Processor (ASP) architecture and FPGA emulation, III illustrates the physical design and implementation, section IV describes the results and discussions and finally section V the conclusions.

II. Array Signal Processor Architecture

The array signal processor architecture is designed to process the incoming echo signals from Analog Front End (AFE) by implementing the delay units (coarse delay and fine delay), apodization units and adder unit. The coarse delay unit is designed and developed by registered MUX with multi-bit shift registers and the fine delay unit is implemented by MMSE filter structure. The architecture also includes deserializer blocks, programmable and debuggable registers, custom JTAG debugs logic block and cycle stealing DMA Controller based on Quad SPI controller. Fig. 2 depicts the designed architecture with peripheral interfaces and Fig. 3 the detailed architecture.

The proposed ASP receives the signal conditioned LVDS data from AFE, samples at both edges at 280MHz bit clock generates a 14-bit sample and transformed into a 20MHz frame (sampling) clock domain. Since the design is for eight channels, eight LVDS deserializers are integrated into the ASP. To form a beam, the 8 channels LVDS data are deserialized, passed through a coarse delay (CD) and fine delay (FD) units, multiplied by apodization coefficients and summed to turn into a single output. The CD is integer multiples of the sampling period and FD is the fractional delay. The data path for the same is CD shift-registers followed by the multiplexer, a first order FIR filter, apodization unit, and summing unit. The coarse delay value can be used as the selection line of the multiplexer, which is

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stored in Course Delay register of each channel and loaded by QSPI controller from Flash. The fine delay is realized by the MMSE filter, the coefficients h0 and h1 for each channel is again stored at Fine Delay Coefficient registers and loaded by QSPI controller from flash memory. For each dynamic receive focal points, the coarse delay and fine delay registers are automatically loaded by the QSPI Controller from external flash. Hence the architecture optimizes the on-chip memory and QSPI Controller acts as cycle stealing DMA to load the delay values without disturbing the beamformer function (Fig.3). The FD filter output is multiplied by a 32-bit apodization register to reduce the side lobes. The filter coefficients and apodization values are represented in fixed-point data type. The bit growth due to the entire beamformer data path processing is upto 50 bits, and hence beamformer output is expanded upto 66-bits. Finally, the beamformer output is truncated to 16-bits without much loss of precision. Next subsections explain Design For Testability (DFT) scan chain insertion and FPGA Emulation of the designed ASIC.

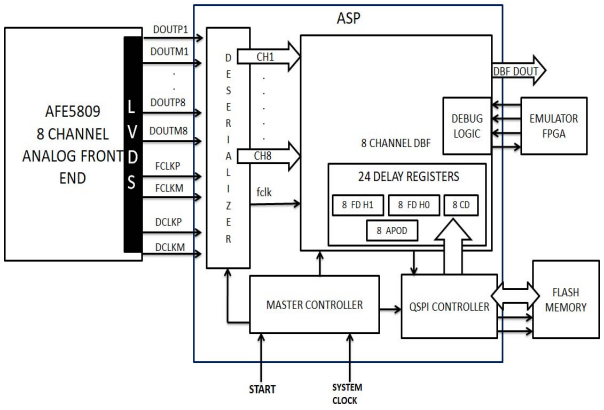

Fig. 2 Proposed ASP with peripherals

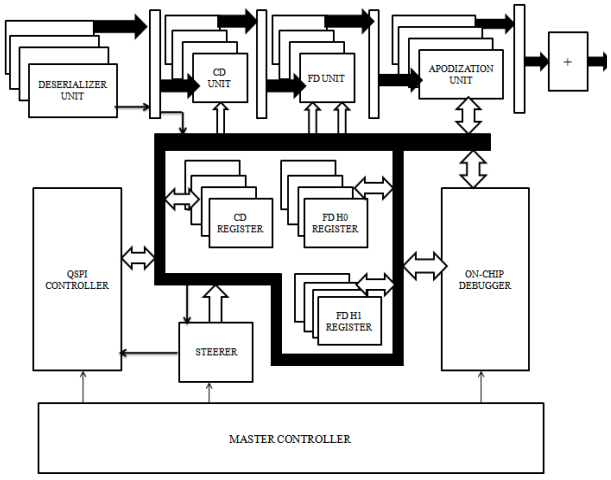

Fig. 3 Proposed ASP architecture

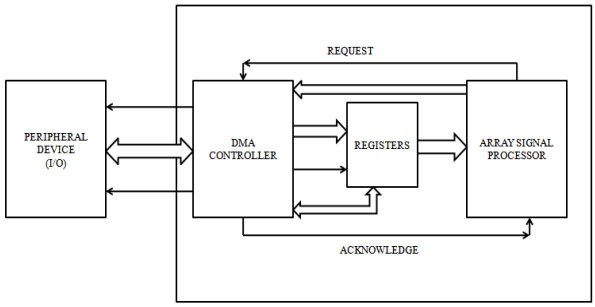

Fig. 3. Cycle stealing DMA data transfer

A. *Design For Testability*

Testability has become a critical concern in any processor design. DFT techniques provide measures to comprehensively test the manufactured chip for quality and coverage. The DFT techniques available today are Internal scan, Boundary scan, Memory BIST, Logic BIST, Scan Compression and OPCG et al. Among the miscellaneous DFT techniques, the proposed architecture exploits the internal scan insertion technique that replaces the basic D-Flip Flops with their equivalent flops and serially connecting the scan flops into scan chains. The same technique exploits the muxed scan flop as a replacement element.

The Fig.4.a shows the design without internal scan insertion and the Fig. 4.b shows the D-flops are replaced with muxed scan flops in the design. The scan flip-flops are linked together using the scan data input of the mux to form a scan chain that functions like a shift register in scan-shift mode. During scan-shift mode, test data can be shifted through the scan chains. Test data is shifted in through the scan-in pins and shift out through the scan-out pins.

The proposed processor has multiple clocks and mixed edge flops in design that rising edge and falling edge sensitive flops can be connected in the same chain with respect of the flop clocks by lock-up latches as shown in Fig.4.c. The proposed design has a total number of 238045 flip-flops which are connected in a single scan chain by the lock-up latch/flop.

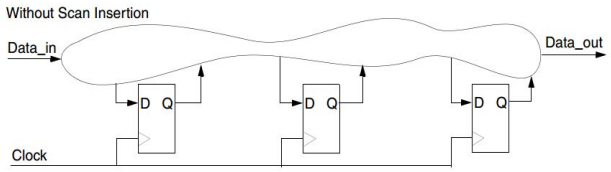

Fig. 4.a

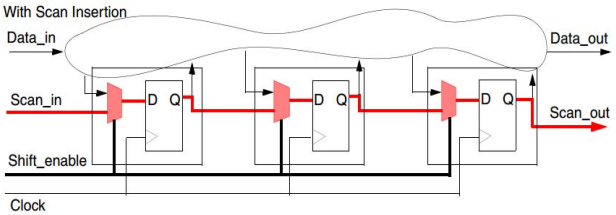

Fig. 4.b

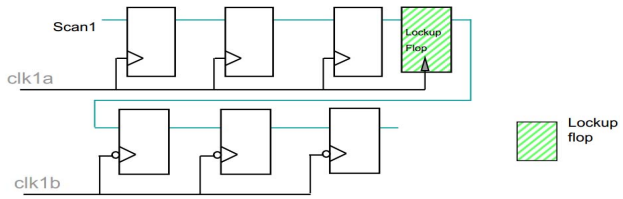

Fig. 4.c

B. FPGA Emulation

The ASP is emulated on FPGA targeting real-time medical ultrasound sector imaging applications, on the emulation set up depicted in Fig.5. The specification for the system emulation set up is shown in Table I. KC705 EVM is chosen for prototype/emulation due to its high-speed PCIe interface to stream the beamformed data to PC and FMC connector to interface high-speed LVDS lines and enough hardware resources to fit the architecture. Also, the EVM has external QSPI flash memory to store the delay values and apodization coefficients. The OPALKELLY XEM3001 FPGA module is employed as a JTAG off-chip debugger and transmit beamformer for the system. The data has been sent to PC through the high-speed communication interface called PCIe. To acquire data from test phantoms, we used a 128 channel custom sectored array, the array specification is shown in Table. II. As the signal wirings are custom, we designed a custom probe connector board (Fig. 6) to interface with pulsar (transmitter) board and master controller module. The probe connector board has programmable analog switches so that the board can be programmed via. SPI interface to select any 8 channels out of 128.

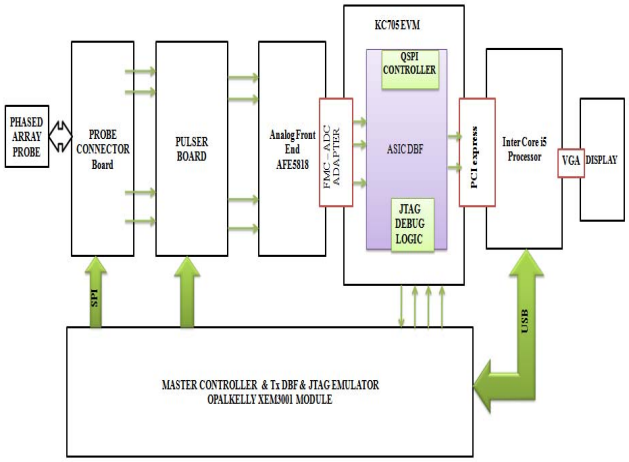

Fig. 5. FPGA Emulation System block diagram

TABLE I. SYSTEM SPECIFICATIONS

Parameter	Value
The speed of sound in tissue	1540m/s
Transducer center frequency	2.5MHz
Number of elements	8
FOV (Sector angle)	60 degree
Lateral Resolution	1 degree
Axial Resolution	1.2mm
Sampling frequency	40MHz
Focal points (Near field dynamic receive focus)	64 x 64 points
Depth	Max 30cm
Frame size	61 scan lines
Pulse Repetition Frequency	4KHz
Dimension of Active aperture area	5.27mm
Near field	8cm [$2D^2/\lambda$]

TABLE II. SECTORED ARRAY SPECIFICATIONS

Parameter	Value
Number of elements	128
Element pitch	0.17mm
Elevation Focus	80mm
Elevation Aperture	12.9mm
Sensitivity(Average)	-60±5dB
Centre frequency (-6dB, average)	2.5±0.5MHz
Relative Bandwidth (-6dB, average)	60±5%
-20dB Pulse Length (-20dB, average)	1.2±0.2 µsec

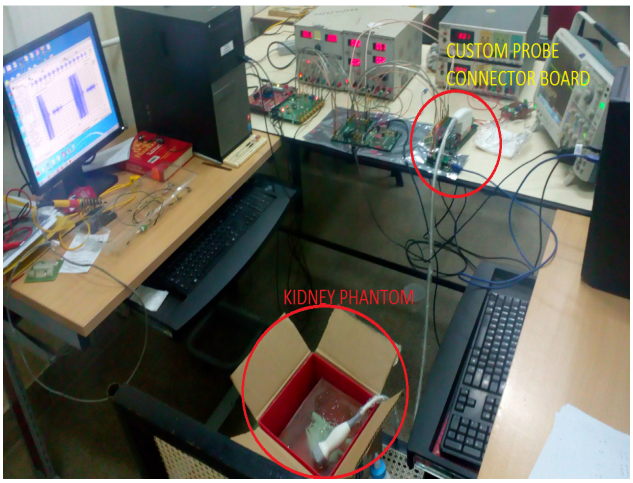

Fig. 6 FPGA Emulation set up

III. PHYSICAL DESIGN AND IMPLEMENTATION

In this section we describe the physical design and implementation steps followed for the proposed Array Signal Processor. The physical design flow followed is depicted in Fig.7. We used CADENCE™ Genus tool for RTL synthesis, Innovus tool for Place and Route, Voltus Tool for power (IR Drop) analysis, Virtuoso Layout editor tool for Design for Manufacturability (DFM), Mentor Graphics™ Calibre Tool for Physical Verification and Synopsys™ Prime Time tool for timing closure. We used Mentor Graphics™ ModelSim and CADENCE™ NcSim for Gate level and post layout verification of the ASIC.

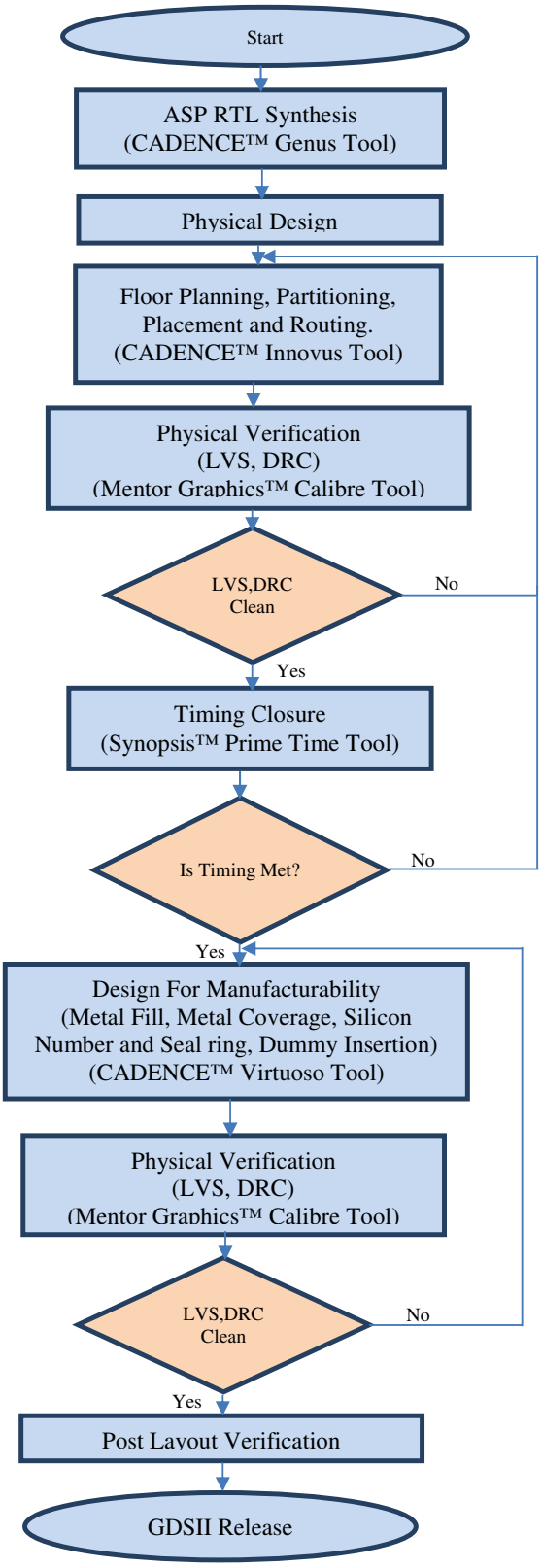

Fig.7 Physical Design Flow Followed for ASP

A. *Physical Design*

The inputs to physical design of the designed ASP is synthesized outputs (area, power and timing reports), which is an estimate of the physical parameters of the ASIC. We targeted SCL™ 180nm, 4 metal technology for synthesis and physical design. Table-III shows the synthesized result of the processor. Based on the area estimated, and fab requirements, the physical dimension of the chip die is decided as 5mm x 5mm. Based on the power and clock IOs, packaging availability, the number of IOs are round off to 80. The core and IO voltage selected is 1.8V and the current carrying capacity of the power IOs selected is 70mA. We have calculated the number of power IOs as four, based on the estimated power, current carrying capacity of power IO and core voltage. We have employed separate power pins for core and I/Os. The design has three clock domains, where the core operates at 20 MHz, LVDS I/O at 280 MHz and QSPI Flash Interface at 40MHz.

TABLE III

Area	1.6 Million Gates (NAND Area)
Power	440 mW
Frequency	
Clk_Sampling	20 MHz
Clk_IO	280 MHz
Clk_QSPI_Flash	40 MHz
Number of Ios	80
Packaging	80 pin LQFN

Once the physical parameters are decided, the physical design is initiated. Initially fixed the physical area with I/O pads.Then performed the floor planning and placement. Next stage power planning and power design is completed. Based on the current carrying capacity and fab design rules the power metal stripes are placed horizontally and vertically, so that power can be uniformly distributed across the chip. Once the power design is completed, power routing is performed and IR drop analysis is carried out. Once power is clean we performed, Clock Tree Synthesis (CTS) for all three clock domains and clock routing is completed. Once power and clock routing is completed, global and detailed routing is performed. During global routing the tool estimates, the best routing paths for interconnection and routing, and later in detailed routing complete chip routing will be performed.

B. *Physical Verification*

In any ASIC design flow, once physical design is completed, the next step is physical verification. The main steps in physical verification are Layout Versus Schematic (LVS) and Design Rule Check (DRC). The DRC performs, against the fab ruleset file and routed layout. The DRC violations are cleaned using layout editor (Virtuoso) tool. Once DRC violations are cleaned next step is LVS. Since inputs to the LVS tool (Calibre) is physical routed layout with power and ground, we generated Power Ground (PG) netlist using P&R tool (Innovus) .The inputs to LVS is PG netlist of

the processor and routed layout. Once LVS is clean, we performed Parasitic Extraction (PEX) using Calibre tool, which is compatible with Synopsis™ timing closure tool (Prime Time). Once PEX is completed, the PEX file and constraints written (Synopsis Design Constraints) by P&R Tool are fed as input to timing closure tool.

C. Timing Closure

The timing closure is the major sign off process in chip design flow. The inputs to the timing closure tool is post routed netlist without power and ground, and we used flat netlist for timing closure. The other inputs are PEX file with RC (path delay) and Cc (Coupling) extracted, and post routed constraints file. During timing analysis, all the clocks in the design need to be propagated to exhibit the actual clock network delays. The output of timing analysis tool is violations (set up, hold, max transitions, max capacitance, etc.) and the fixes for violations. The fixes for violations, need to be carried to P&R tool (Innovus) and need to perform the fixes and the same process need to continue, (Fig.7) till the required timing is met and there is no any violations. Once timing closure is completed next stage is Design for Manufacturability (DFM).

D. Design For Manufacturability

In Design for Manufacturability (DFM) stage, the reliability aspect of the ASIC is taken into consideration. In this stage we performed the metal fill, to fill the unused areas in design, to increase metal coverage etc. Metal coverage as per fab requirements is an important criteria for reliability and yield. Once metal filling is complete, next step is insertion of I/O fillers and later seal ring and silicon number. The seal ring need to be connected to ground, and it provides electrical shielding for the processor. The silicon number is required for chip identification by the fab. Once metal fill, insertion of seal ring and silicon number is complete, the next stage is dummy generation and fill. The dummy can be generated using Calibre Tool for the stream out GDSII file from P & R/Layout editor Tool. Once dummy metal is generated the same is inserted to layout using layout editor Tool (Virtuoso). The dummy metal is required for Chemical Metal Polishing (CMP) process. The DRC need to be carried out at each stage, and final DRC clean GDSII is released for fab. Fig.8 depicts the layout and Fig.9 the bonding diagram of the designed Array Signal Processor.

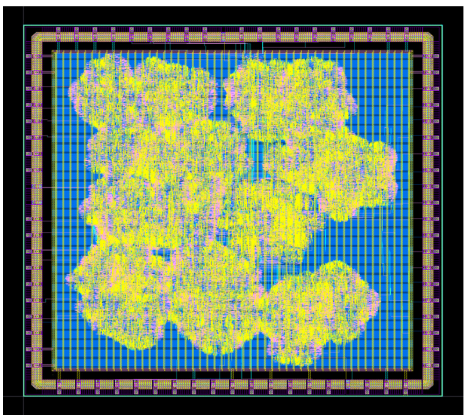

Fig.8 Layout of the ASP

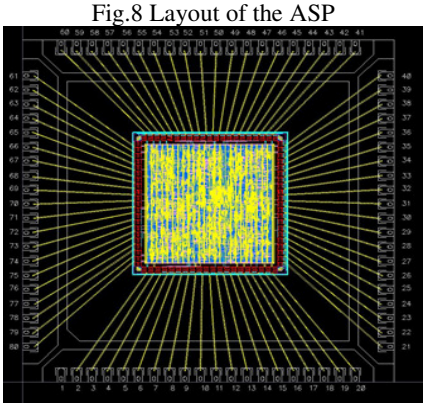

Fig. 9 Bonding Diagram of ASP

CONCLUSION

In this paper, we presented architecture and, FPGA prototype and physical design and implementation, of cycle stealing DMA Array Signal Processor. The architecture is optimized for internal memory, the pre-computed delay values are stored in external flash memory and loaded into the corresponding resisters for each dynamic focal points. The architecture is synthesized to SCL™ 180nm technology for estimating chip area and power consumption. It uses 22.75 mm^2(5mm x 5mm) chip area and dissipates 440mW of power. The FPGA emulation is performed and validated the design for real-time sector imaging applications. This paper comprehensively briefs the physical design flow for the designed ASP architecture, tool chain used in various stages of physical design towards chip tape out.

ACKNOWLEDGMENT

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REFERENCES

[1]. M. Karaman, E. Kolagasioglu,and A. Atalar, "A VLSI receive beamformer for digital ultrasound imaging," *[Proceedings] ICASSP-92: 1992 IEEE International Conference on Acoustics, Speech, and Signal Processing*, San Francisco, CA, 1992, pp. 657-660 vol.5.

[2]. M. Karaman and M. Kozak, "Digital beamforming using non-uniform oversampling delta-sigma conversion," *1999 IEEE Ultrasonics Symposium. Proceedings, International Symposium (Cat. No.99CH37027)*, Caesars Tahoe, NV, 1999, pp. 1279-1282 vol.2.

[3]. S. R. Freeman *et al*., "Heterodyning technique to improve performance of delta-sigma-based beamformers," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 46, no. 4, pp. 771-790, July 1999.

[4]. J. R. Talman, S. L. Garverick, and G. R. Lockwood, "Integrated circuit beamformer for high frequency array," *1999 IEEE Ultrasonics Symposium. Proceedings, International Symposium*

(Cat. No.99CH37027), Caesars Tahoe, NV, 1999, pp. 1235-1238 vol.2.

[5]. H. T. Feldkamper, R. Schwann, V. Gierenz and T. G. Noll, "Low power delay calculation for digital beamforming in handheld ultrasound systems," *2000 IEEE Ultrasonics Symposium. Proceedings, An International Symposium (Cat. No.00CH37121)*, San Juan, 2000, pp. 1763-1766 vol.2.

[6]. V. S. Gierenz, R. Schwann,and T. G. Noll, "A low power digital beamformer for handheld ultrasound systems," *Proceedings of the 27th European Solid-State Circuits Conference*, Villach, Austria, 2001, pp. 261-264.

[7]. Ho-San Han, Hye-Joung Park and Tai-Kyong Song, "A new architecture for ultrasound sigma-delta modulation beamformer," *2002 IEEE Ultrasonics Symposium, 2002. Proceedings*, 2002, pp. 1631-1634 vol.2.

[8]. Pei-Jie Cao, K. K. Shung, N. Karkhanis and Wo-Hsing Chen, "Design of a real-time digital beamformer for a 50MHz annular array ultrasound transducer," *2002 IEEE Ultrasonics Symposium, 2002. Proceedings,* 2002, pp. 1619-1622 vol.2.

[9]. K. Ranganathan, M. K. Santy, J. A. Hossack, T. N. Blalock and W. F. Walker, "Direct sampled I/Q beamforming: a strategy for very low cost ultrasound," *IEEE Symposium on Ultrasonics, 2003*, 2003, pp. 1863-1866 Vol.2. doi: 10.1109/ULTSYM.2003.1293277

[10]. B. G. Tomov and J. A. Jensen, "A new architecture for a single-chip multi-channel beamformer based on a standard FPGA," *2001 IEEE Ultrasonics Symposium. Proceedings, An International Symposium (Cat. No.01CH37263)*, Atlanta, GA, 2001, pp. 1529-1533 vol.2.

[11]. J. P. Stitt, R. L. Tutwiler and K. K. Shung, "An improved four-focal zone high-frequency ultrasound analog beamformer," *2002 IEEE Ultrasonics Symposium, 2002. Proceedings.* 2002, pp. 617-620 vol.1.

[12]. Pai-Chi Li and Jing-Jung Huang, "Dynamic focus control for imaging with two-dimensional arrays," *2001 IEEE Ultrasonics Symposium. Proceedings. An International Symposium (Cat. No.01CH37263)*, Atlanta, GA, 2001, pp. 1521-1524 vol.2.

[13]. Pai-Chi Li and Jing-Jung Huang, "Efficient dynamic focus control for three-dimensional imaging using two-dimensional arrays," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 49, no. 9, pp. 1191-1202, Sept. 2002.

[14]. K. Ranganathan and W. F. Walker, "A novel beamformer design method for medical ultrasound. Part I: Theory," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 50, no. 1, pp. 15-24, Jan. 2003.

[15]. K. Ranganathan and W. F. Walker, "A novel beamformer design method for medical ultrasound. Part II: Simulation results," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 50, no. 1, pp. 25-39, Jan. 2003.

[16]. B. Lam, M. Price,and A. P. Chandrakasan, "An ASIC for Energy-Scalable, Low-Power Digital Ultrasound Beamforming," *2016 IEEE International Workshop on Signal Processing Systems (SiPS)*, Dallas, TX, 2016, pp. 57-62