A Power Efficient Output Capacitor-Less LDO Regulator with Auto-Low Power Mode and Using Feed-forward Compensation

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***Abstract*— An output capacitor-less low-drop out (LDO) regulator using a feed-forward compensation is presented in this paper. The power stage; implemented using flipped-voltage-follower (FVF) stage along with the feed-forward compensation stabilizes the LDO for the entire range of load current and load capacitor. The LDO uses only 1pF of compensation capacitor and consumes quiescent current of 28µA in active mode and 3µA in low power (LP) mode. A load current sensor is used to sense ultra-low power and automatically switch to LP mode. The proposed LDO was implemented in TSMC-65nm for an input of 1.2 V, output of 0.9V to 1.1V and achieves settling time of <1µs with undershoot/overshoot of ~250mV for 10mA load current.**

Keywords—feed-forward compensation, flipped voltage follower, capless LDO, low power mode.

I. INTRODUCTION

Today's portable and handheld gadgets are powered by a power management IC (PMIC) which contains multiple switching and low dropout regulators (LDO) on a single chip. For instance, DA9068 [1], a PMIC from Dialog Semiconductor, contains 8 switching and 25 LDOs with LDOs supplying about 1/3rd of the total power requirement. Even though LDOs cater to smaller portion of power need, they may still outnumber switching regulators as seen in [1]. This is mainly due to large number of low power analog modules such as sensors, A/D-D/A converters, amplifiers, filters, clock generators, etc. Integrating such a large number of LDOs on a single chip requires smaller on-chip and off-chip area due to limited board space available on a mobile device. Moreover, depending upon the nature of the load, these LDOs should be capable of operating with wide range of load currents and output capacitors. With the reduction of the large decoupling capacitors, the transient response and the power supply noise rejection (PSR) of the LDO worsens. Transient response can be improved by increasing the slew rate of the error amplifier (EA) and the loop response. Whereas for improving PSR; a high gain and wide bandwidth of the loop is needed. Both these techniques of improving transient response and PSR lead to higher quiescent power in LDO.

Most commonly used compensation techniques for LDO are the Miller and Ahuja compensation [2]. However, these techniques are based on dominant pole compensation which reduces the bandwidth thus adversely affects the transient and PSR performance. Various feed-forward compensation techniques have been reported in the past [3, 5-8] but most of them suffers from large power and/or area penalty due to large number of stages and compensation capacitors.

In this paper, an improved feed-forward compensation (FF) based on Proportional-Integral-Derivative control (PID) has been proposed. This achieves good transient and PSR performance while consuming very low power and at a small silicon footprint. The proposed LDO also employs low power mode to reduce the quiescent current to 3µA in standby mode when load current goes below 20µA.

Section II elaborates on the details of the proposed compensation. The proposed architecture of LDO is discussed in Section III along with its circuit implementation. Simulation results are presented in Section IV followed by conclusion in Section V.

II. PROPOSED FEEDFORWARD (FF) COMPENSATION

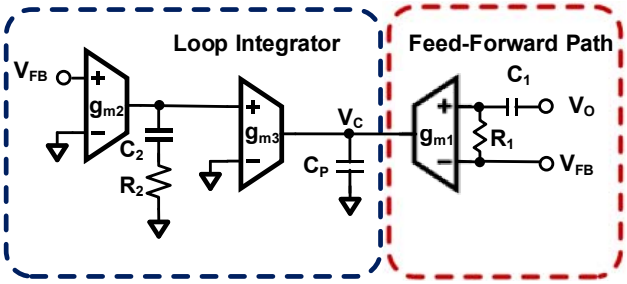

Fig. 1 Proposed Compensation Scheme.

Fig.1 illustrates the proposed feed-forward compensation with two stage amplifier and a feed-forward path. The transfer function from the LDO output to the control node is given as

$$\frac{v_c}{v_o}(s) = \frac{\beta g_{m2} g_{m3}}{C_P C_2} \frac{\left[(1+s/\omega_{z1})(1+s/\omega_{z2})\right]}{s^2\left(1+s/\omega_{p1}\right)} \quad (1)$$

Where, $\omega_{z1} = \left(\frac{g_{m1}}{\beta g_{m2} g_{m3} R_2}\right)\frac{1}{R_1 C_1}, \omega_{z2} = \frac{1}{R_2 C_2}$

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And, $\omega_{p1} = \frac{1}{R_1 C_1}, V_{FB} = \beta V_o, \beta = \frac{R_{FB1}}{R_{FB1} + R_{FB2}}$

Here in active mode, the error amplifier first stage output is kept dominant. The zero ω_{z1} is placed at lower frequencies to cancel the error amplifier output pole whereas ω_{z2} is used to cancel the LDO output pole $\omega_{p,out}$. This gives a single pole system with around 90° phase margin.

In low power mode, the dominant pole moves to lower frequencies and rises the DC gain keeping the UGB fixed. Due to lower quiescent current, the parasitic poles move to lower frequencies and reduce the phase margin.

III. Proposed LDO Architecture

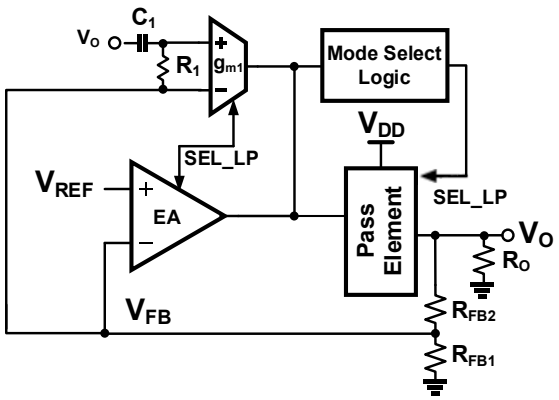

Fig. 2 Block Diagram of the proposed LDO with active and low power modes.

Fig.2 shows the block diagram of the proposed LDO. It is implemented using 2-stage error amplifier (EA), a FF compensator, a pass element and a mode select logic to switch between active and LP mode. As discussed in section II, the feed-forward path, g_{m1} was added to introduce a zero which cancels the EA output pole. This is followed by the pass element designed to cover wide range of load current and output capacitance.

The proposed LDO implements two modes of operation, active mode (AM) and low power (LP) mode which can be selected using an internally generated control signal SEL_LP. In AM, the loop operates with higher IQ and achieves a wide UGB. In LP mode, the IQ through the blocks is curtailed to save power.

The proposed feed-forward compensated LDO was designed in TSMC 65nm CMOS process to operate at V_{DD}=1.2V, V_O=0.9V-1.1V and I_{LOAD}=0-10mA. The operation was verified through simulation on cadence. Design details of each block are discussed below:

A. Error Amplifier (EA)

As shown in Fig 3, the EA is implemented using a conventional 2-stage error amplifier. A series RC compensation was used to compensate the LDO output pole. Operated at 0.8V reference, the EA consumes 3µA of IQ in AM and only 300nA in LP. The input differential pairs M_1-M_2 are scaled to 1/3rd of its size in the LP mode to retain good biasing in LP.

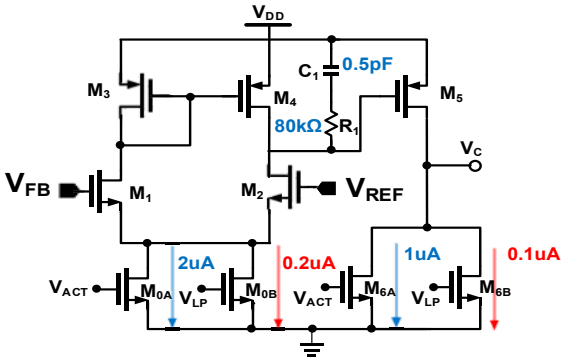

Fig. 3 Circuit Diagram of Error Amplifier.

B. Feed-forward Transconductor

A standard single stage transconductor was implemented using 8µA bias current in AM and 0.5µA in LP. The differential input transistors M_{F1}-M_{F2} are sized large to achieve maximum g_{m1}. A FF zero is realized with RC high-pass filter (R_1-C_1) and the transconductance, g_{m1}. In LP, the sizes of differential input transistors M_{F1}-M_{F2} are cut down to 1/2 of their original size.

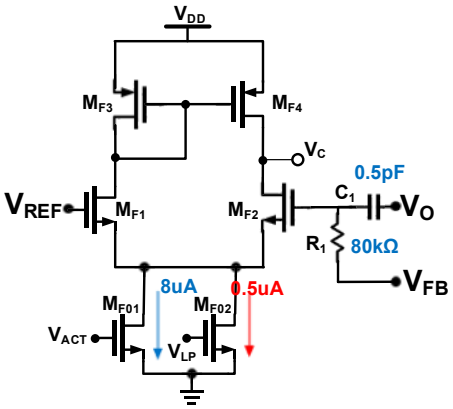

Fig. 4 Circuit diagram of the feed-forward transconductor.

C. Pass Element

As shown in Fig. 5, the proposed LDO uses flipped PMOS source follower widely known as flipped-voltage-follower (FVF) [4]. The FVF has a low output impedance and hence, it supports a wide range of output capacitance and load current.

The control voltage (V_C) generated from the compensator is applied to the PMOS source followers, M_{P_S}- $M_{P\_S\_LP}$. Due to the loop formed by the source follower and PFET driver, M_P, the output impedance reduces significantly pushing the output pole to higher frequencies. As the size of the source follower, M_{P_S}- $M_{P\_S\_LP}$ is small; it does not add any significant capacitance at control node, V_C and ensures overall stability of the loop. The FVF is biased with a 2µA current source.

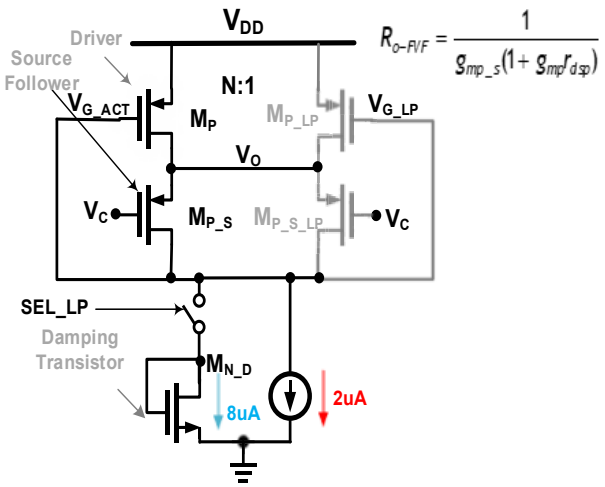

Fig.5 Circuit Diagram for the pass element.

At very light load currents and high output capacitance; poles at gate of MP and VO forms a complex pole pair close to the UGB. This leads to gain peaking in the magnitude bode plot and degrades the phase margin; rendering the loop unstable. Adding a small diode connected NMOS (MN_D) dampens the peak. The diode consumes a current of 10µA in active mode and 2µA in low power mode.

The maximum current through damping transistor (I_MN_D) is ensured to be 10µA or less under all the loading conditions in active mode. In low power mode, main pass-element branch (consists of MP, MP_S and MN_D) is disabled and low power pass-element branch (consists of MP_LP, and MP_S_LP) element branch remains activated which is sized 100 times (N=100) smaller than MP. Since the gate capacitance of MP_LP is reduced significantly, the complex pole problem does not arise in low power mode. The current in the pass element is reduced to just 2µA in low power mode.

D. Mode Control Logic

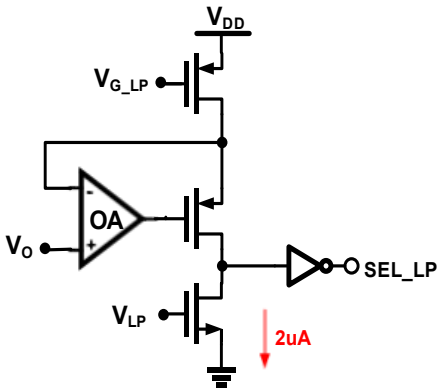

Fig.6 Circuit Diagram Auto-Mode Select Logic.

The circuit implementation of the mode control logic is shown in Fig.6. The pass element current is sensed and compared against a reference threshold current using a current comparator. The output of current comparator, SEL_LP, is used to activate and de-activate low power mode. The MP_LP current is sensed by the sense FET MS_LP having a scaling factor of 1/20th generating a gate voltage of VG_LP. The mode transition threshold is set at 50µA.

Operational amplifier (OA) is used in regulated cascode configuration to achieve accurate mirroring the sensed current. The OA consumes only 100nA of current in all operating modes. Overall, the auto-mode select logic block consumes 2.1µA in active mode and 100nA in low power mode. As the load current reduces below 50µA, the LP mode is activated saving 10x power than active mode.

IV. Results and Discussion

Stability of the proposed time-based LDO was verified across zero to 10mA load current and output capacitance of 1pF-100pF. It can be observed from Fig.7, the UGB remains around 2.1MHz and phase margin is about 90°. The phase margin reduces to 35° at higher load capacitance and zero load current in LP mode. This limits the capacitance which can be used at the output of LDO. The DC gain improves and the dominant pole shifts to lower frequencies in LP mode.

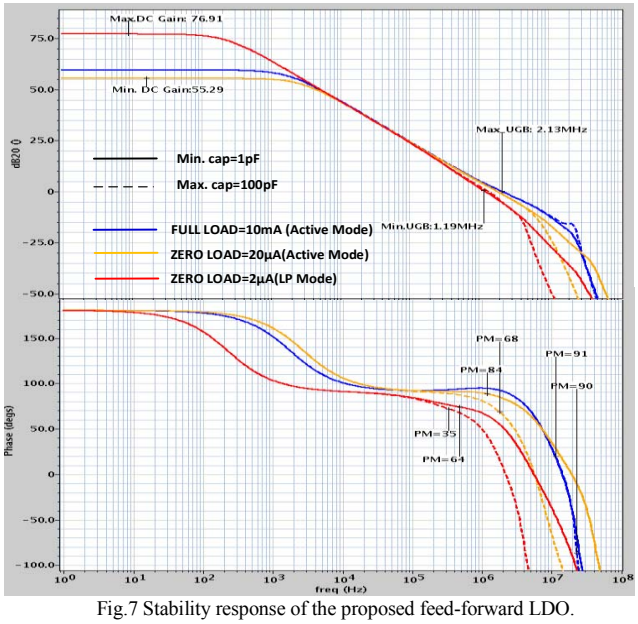

Fig.7 Stability response of the proposed feed-forward LDO.

Load transient response was simulated by applying a load step of 100µA↔10mA, with rise/fall=100ns as shown in Fig.8. In the mentioned load range, the LDO maintains the active mode of operation. The LDO is observed to be settling within 1µs with undershoot of < 250mV for a minimum output capacitance (1pF). The transient performance improves considerably with increase in output capacitance.

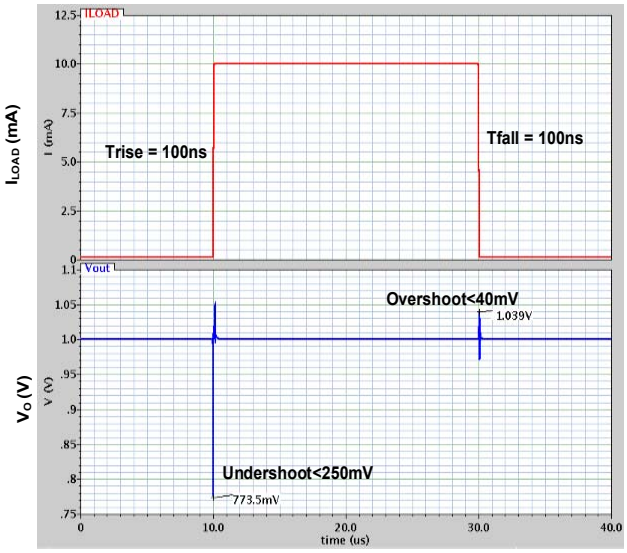

Fig.8. Load transient response of the proposed LDO.

Load transient response for different V_O is shown in Fig. 9. The lower limit for V_O is restricted by the lower common mode range of the amplifier and the higher limit by the supply. The transient response remains fairly same as in the 1V regulated output.

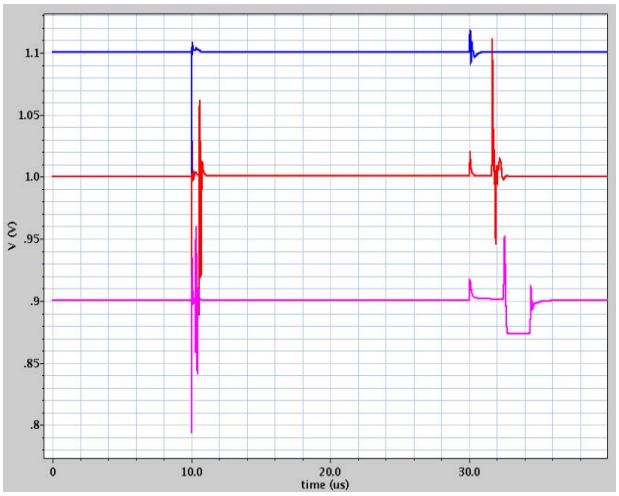

Fig. 9. Load transient response for V_O = 0.9V, 1.0V and 1.1V

Fig.10 shows the transition between active mode and low power mode. Overshoot and undershoot of ~110mV was observed in the output due to change in control voltage V_C during transition. However, output during mode transition settles in less than 1µs. It can be observed that LP mode IQ is ~3µA and ~28µA (excluding the load current of 1 µA in LP and 100µAin active mode)

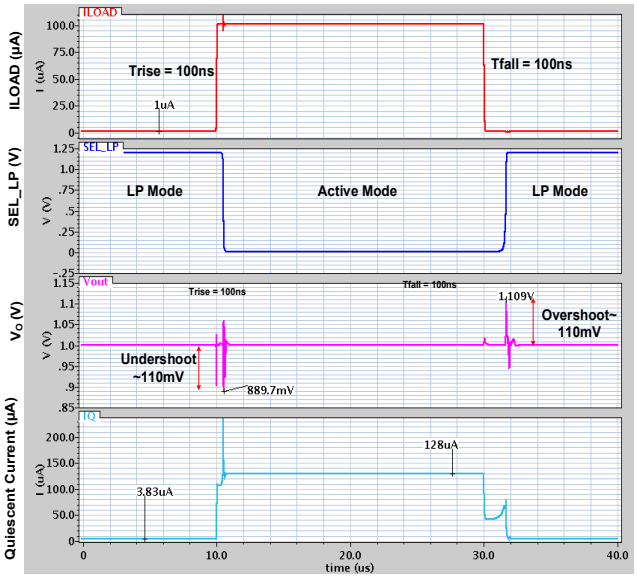

Fig. 10. Mode transition between active and low power mode at C_L=1pF

Fig.11 shows a slow transition between active mode and low power mode. The LP mode transition threshold is observed to be slightly above 50µ. Whereas, the active mode transition threshold is about 40µA. A hysteresis of 10µA is maintained to avoid any false triggering due to noise. The overshoot and undershoot of ~200mV and ~150mV was observed respectively in the output due to change in control voltage V_C during transition. However the output settles within 1µs.

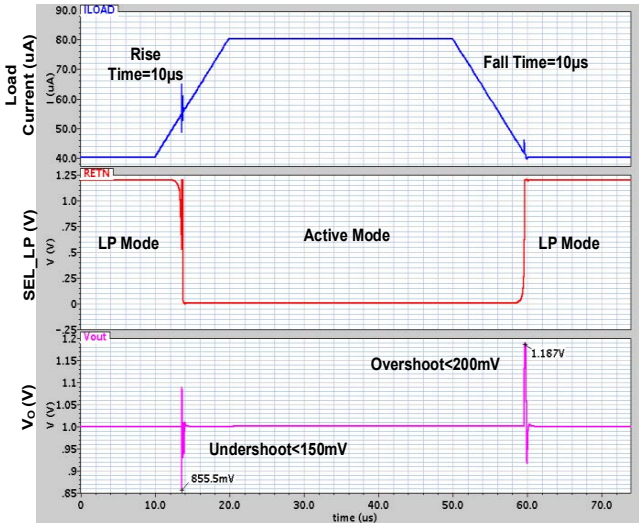

Fig. 11. Slow mode transition between active and low power mode at C_L=1pF

The PSR plot of the proposed LDO is shown in Fig.12. The PSR is more than 14dB at 1MHz under all load currents. The DC-PSR is more than 50dB making it suitable for application lower than 1MHz.

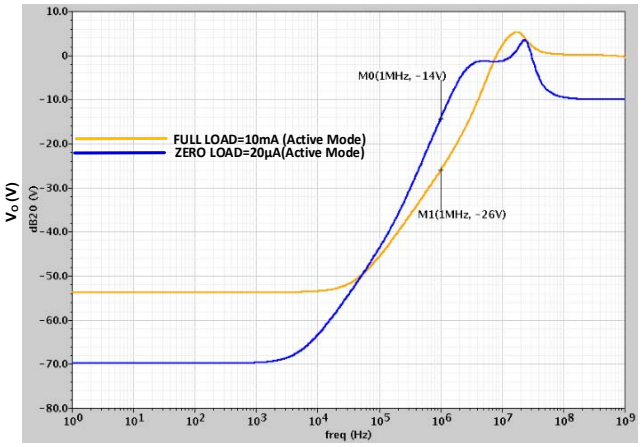

Fig. 12. PSR response for the LDO

Table-I provides the performance comparison of the proposed LDO with state-of-the art LDOs. The formula used to compare these LDOs is as follows:

$$FOM = \frac{C_C}{C_{L,\max}} \cdot \frac{\Delta V_O}{V_O} \cdot \frac{I_{Q,\max}}{f_{UGF}} \cdot \frac{1}{I_{L,\max}} .10^{12} \quad (2)$$

The FOM is a measure of quiescent current per unit load current, compensation to load capacitance; percent load transient regulation and speed (f_{UGB}). Table I compares state-of the art LDOs with the proposed work.

TABLE I. PERFORMANCE TABLE AND COMPARISON

Metrics	**This Work**	ISCAS'17 [5]	ISCAS'17 [6]	CICC'17[7]	MWSCAS' 17[8]
Technology	**65nm**	180nm	180nm	65nm	500nm
Vin/Vout	**1.2/ 0.9-1.1**	1.84/1.8	1.2/1	1.2/1	2/1.5
Overshoot/ Undershoot(mV)	**<250/40**	50/40	220/150	46/45	159/491
Settling Time (µs)	**<1**	4.6	3.6	1.2	>25
Current, I_Q (µA)	**28/3***	7	3	4.9	4.9
f_{UGB} (MHz)	**2.1**	0.1	0.5	8	0.29
$I_{L,max}$ (mA)	**10**	50	100	25	50
Comp./Load(pF) Cap ($C_C/C_{L,max}$)	**1/100**	10/100	2.5/10	10/240	14.3/ 100
FOM[1] (ps)	**3**	3.89	3.3	7.5	15.8

[1]Lower FOM value indicates better performance.

*Active/LP Mode

V. CONCLUSION

An output capacitor-less dual-mode LDO using feed-forward compensation is presented. The proposed LDO achieves bandwidth of 2.1MHz with total on-chip compensation capacitance of 1pF and quiescent current of 28µA in active mode. In low power mode, it consumes only 3µA. Designed in 65nm CMOS process with input voltage of 1.2V, it can regulate output from 0.9V to 1.1V with load current of 0-10mA and load capacitance of 0-100pF. Due to its low power, low silicon area and auto mode switch feature of the proposed LDO, it stands a suitable candidate for system level linear regulator applications.

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