A 0.8V V_{MIN} Ultra-Low Leakage High Density 6T SRAM in 40nm CMOS Technology using Repeated-Pulse Wordline Suppression Scheme

Ashish Kumar[1] , Mohammad Aftab Alam[2], G.S.Visweswaran[3]
[1]STMicroelectronics Pvt. Ltd., Greater Noida, India, [2]Zia Semiconductor Pvt. Ltd., [3]IIIT, Delhi, India
ashish.kumar@st.com, aftab@ziasemi.com, viswes@iiitd.ac.in

***Abstract*— A low Vmin 6T-SRAM is realized in 40nm CMOS technology using a 0.242um2 high density, ultra-low leakage memory cell. We could achieve the functional Vmin of SRAM to 0.8V using a Repeated-Pulse Wordline Suppression (RPWS) scheme. We could achieve a performance of 40MHz at 0.8V for a 512Kb capacity SRAM with 16K words of 32 bits width. Area and dynamic power overhead for the implementation is within 1% each when compared to a conventional WLUD scheme. Absolute area overhead of the scheme is 2% for the chosen instance.**

Keywords*— Low supply voltage, low leakage, SRAM, low Vmin, source bias, static noise margin, wordline underdrive, read assist, write assist.

I. INTRODUCTION

Low voltage functionality of SRAM is challenged due to reduced static noise margin (SNM) and write margin (WM). Variation of SNM and WM with supply voltage is illustrated in Fig.1. To ensure stability for a large SRAM array, we target a six-sigma qualification for SNM and WM. Six-sigma stability points are shown by dotted lines in Fig.1. SNM and WM fail to qualify six-sigma below 1.15 volts and 1.2 volts respectively. We have used a 0.242um2 high density 6T-SRAM cell in 40nm Ultra Low Power (ULP) CMOS technology. To enhance stability of the memory cell assist methods are used for read and write operations [1-4].

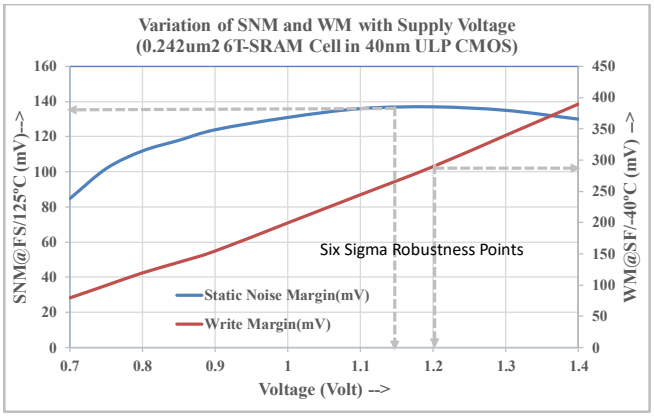

Fig.1 Variation of Static Noise Margin and Write Margin with Voltage. (0.242um2 High-Density Ultra-Low Leakage 6T-SRAM cell in 40nm ULP CMOS)

Wordline underdrive (WLUD) to enhance SNM of memory cell is commonly used. However, application of WLUD results in reduced cell current and loss of performance. WLUD also deteriorates the WM of memory cell. This work proposes the use of repeated pulse wordline suppression (RPWS) to gain on performance. In the proposed scheme, duration and magnitude of effective WLUD is reduced while achieving the similar stability when compared to a conventional scheme. This results in higher average cell current and thus higher bitline differential generated over a period of time. Impact on WM is also smaller with RPWS. To ensure write stability, bitline undershoot is used as a write assist.

II. DESCRIPTION OF THE PROPOSED SCHEME

Fig.2 illustrates the conventional as well as proposed RPWS scheme. In conventional WLUD scheme, a voltage of magnitude VDD-ΔV drives the wordline. Fig.3 illustrates the impact of WLUD on cell current at performance limiting PVT (SS/0.8V/-40°C). There is a strong dependency of cell current on wordline voltage. WLUD of mere 35mV reduces the worst-case cell current by 50 percent. In the proposed repeated pulse wordline suppression scheme, wordline is suppressed by using repeated pulses of ΔV', where ΔV' > ΔV. Thus there are intervals where wordline is at higher voltage VDD and cell current is much higher in these intervals. Cell is able to discharge effectively by a larger amount within wordline window.

Flipping mechanism of cell due to low SNM can be explained w.r.t Fig.2. When the wordline is activated, bitline discharges through PG_R (Fig.2). This flow of current through BLB-PG_R-PD_R is the cell current or read current of memory cell. Due to read current, node'0' rises and under unstable condition or low SNM condition, goes above the trip point of the facing inverter (PU_L and PD_L) resulting in flipping of the cell. This takes a finite amount of time 'T_{flip1}' for the cell to flip. RPWS takes advantage of this fact. If we are able to restore the flipping cell nodes to their original condition before they are flipped, we can ensure a flawless access. Repeated pulses are used to recover the stability of the cell before they flip as shown in fig.4(b), whereas Fig.4(a) is the normal wordline window without any read assist.

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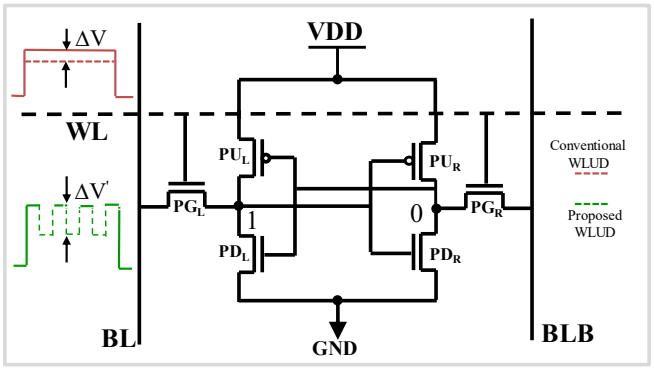

Fig.2. Wordline Underdrive applied in a 6T-SRAM Cell. Conventional and RPWS

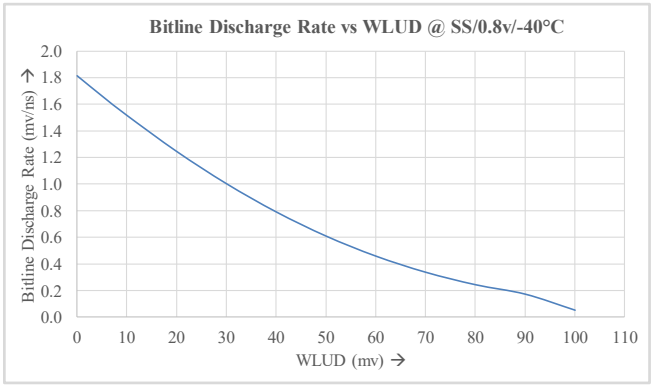

Fig.3. Impact of WLUD on bitline discharge rate.

Flipping time of the memory cell has a strong dependency on the word-line voltage. Wordline Underdrive increases flipping-time. On applying a WLUD of ΔV, flipping time increases to 'T_{flip2}' (Fig. 4(c)). This fact helps us to design a RPWS scheme in combination with WLUD scheme when stability of cell is extremely poor, resulting in a very small T_{flip} (flipping time). If the T_{flip} is very small, it becomes difficult to apply repeated pulses at higher frequency.

Fig.5 is a comparative illustration of the scheme. To ensure six-sigma stability of the SRAM cell, required WLUD

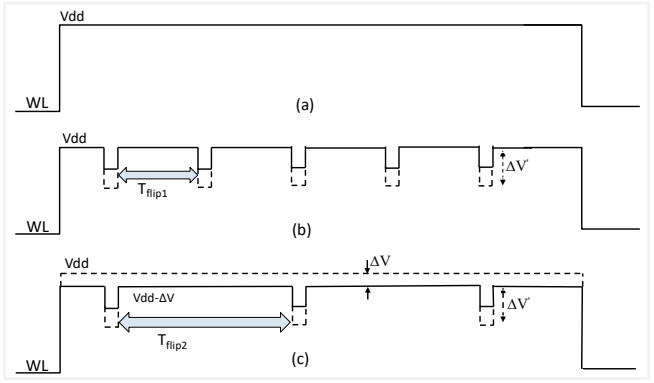

Fig.4 Proposed RPWS scheme Illustrated. (a) No WLUD applied. (b) RPWS applied without wordline underdrive. (c) RPWS with under driven wordline.

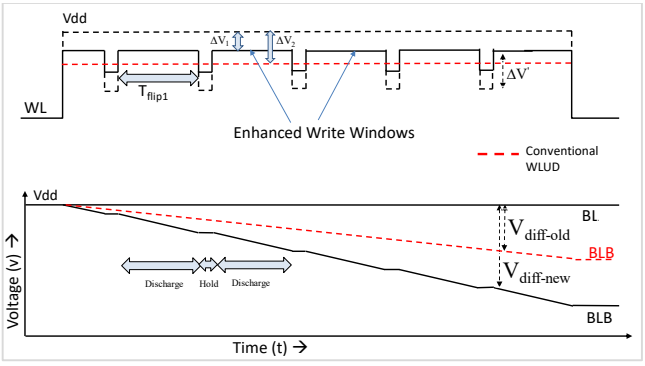

Fig.5. Illustration of Performance gain with RPWS. Bitline discharge is faster using RPWS.

in conventional scheme is ΔV_2. RPWS is implemented using a WLUD of ΔV_1 achieving similar stability. Pulses in RPWS are shown as dotted line to indicate that depth of these pulses can be modulated to optimize on stability and performance of memory.

Bitline discharge is faster with proposed scheme. Due to smaller WLUD used, higher wordline level is available between pulses and responsible for higher cell current. Higher wordline level available with the proposed scheme helpful during write operation as well. Enhanced write windows are shown in Fig.5. As illustrated, bitline discharge occurs as a combination of 'discharge' and 'hold' phases in the proposed scheme.

III. Results and Discussion

A repeated pulse wordline suppression (RPWS) scheme is proposed to enhance the read stability of the 6T SRAM-cell. RPWS is applied in combination with compensated WLUD [4]. Proposed scheme is validated using circuit level simulations in 40nm CMOS technology. Memory instance of 16K words and 32-bits is used to evaluate the effectiveness of the proposed scheme. Simulations are performed using silicon validated SPICE models. We could achieve a performance gain of approximately 30% using this scheme. Area overhead of the scheme is less than 1% for the chosen memory instance when compared to conventional WLUD scheme. Dynamic power overhead is within 1% compared to conventional scheme.

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