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A Model of Spurs for $\Delta\Sigma$ Fractional PLLs

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***Abstract*—In this brief, a model of spurs for fractional PLLs based on Delta-Sigma modulators is presented. The model predicts both fractional and reference spurs and is applicable for modulators of any order. The accuracy of the model is verified by using a conventional second-order modulator for a 2.4 GHz PLL. The results show fair match between the predicted and simulated values with maximum error of 7 dB. The derivation does not consider any spur cancellation or compensation technique.**

***Index Terms*—Phase-locked loop, fractional and reference spurs, spur model**

I. Introduction

Clock generation circuits are critical elements in communication systems. High speed data transmission/reception may require clocks of multiple frequencies and phases for modulation and demodulation. The task is well performed by PLL-based frequency synthesizers. Charge pump-PLL circuits are generally robust and can produce varying frequencies depending on a channel-select input. However, certain performance parameters like phase noise and spur generation need to be optimized for reliable carrier utility. High phase noise and spurious emissions by a system can hamper data transmission ongoing in adjacent frequency channels occupied by other systems. In this brief, we present a model to accurately predict magnitudes of spurs in conventional $\Delta\Sigma$-fractional PLLs (DSM-PLL).

In the next section, the model is presented and compared with a PLL utilizing a second order DSM. The brief ends with conclusions in section III.

II. Simplified Spur Estimation for $\Delta\Sigma$ PLL

The derivation presented here is based on two assumptions—(1) $f_{\rm ref} \ll I_{\rm CP}/(V_A C_1)$, and (2) DSM output is pseudorandom and predictable. Here, $f_{\rm ref}$ is the reference frequency, C_1 is the larger capacitor of the second order loop filter and V_A is the amplitude of control voltage. The loop filter is simplified to a single capacitor C_1 for ease of calculation. The in-band spurs will be minimally affected by this simplification; however, as the the resistor R_1 introduces a zero [1], the out-of-band spurs need to be augmented by

$$S_{\rm LF} = 20\log_{10}\frac{C_1}{\sqrt{2}C_2}\ \text{dB} \tag{1}$$

The control voltage waveform is approximated into ramp sections near the rising edges of the reference and divided signals, and flat sections in the intermediate positions. The durations of the ramping edges are considered low compared to the flat sections according to the assumption (1). The flat segments are equally spaced i.e. their corresponding voltage differences are assumed equal. Let V_k be the voltage of the kth flat segment of $V_{\rm ctrl}$, T_k be the period of VCO output when $V_{\rm ctrl} = V_k$, and Δt_k be the duration of the ramp waveform preceding at the start of V_k. Then T_k and Δt_k are related as

$$(N + A_k)\,T_k = T_{\rm ref} \pm \frac{\Delta t_k}{2} \pm \frac{\Delta t_{k+1}}{2} \tag{2}$$

where $T_{\rm ref} = 1/f_{\rm ref}$ and $N + A_k$ is the frequency divider modulus that causes $V_{\rm ctrl}$ to be equal to V_k. The sign of Δt_k will depend on whether the ramp signal is rising or falling pertaining to the location of the divided signal edge compared to the reference edge. The voltages V_k are then represented as

$$V_{k+1} = V_k \pm \frac{I_{\rm CP}}{C_1}\Delta t_{k+1} \tag{3}$$

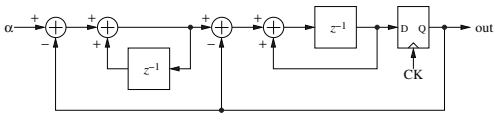

Fig. 1. Second order DSM for $\alpha = 3/4$

TABLE I
Parameters of 2.4 GHz PLL

Parameter	Value
Reference frequency $f_{\rm ref}$	40 MHz
Loop bandwidth	2 MHz
Integer division ratio N	60
Fractional division ratio α	3/4
CP currents $I_{\rm UP}$ and $I_{\rm DN}$	510 μA and 500 μA
PFD delay $t_{\rm PFD}$	930 ps
VCO gain $K_{\rm VCO}$	$2\pi \times$ 100 MHz/V
Loop filter	(15 kΩ + 23 pF) ‖ 1.25 pF

Also, it can be proved that the average of the output frequencies at different control voltages equals $f_{\rm out}$.

$$\sum_{k=1}^{n}\frac{1}{T_k} = \frac{n(N+\alpha)}{T_{\rm ref}} \tag{4}$$

where $\alpha = m/n$, $nT_{\rm ref}$ being the period of the control voltage. Substituting equation (2) in (4), Δt_k are determined, which when used in equation (3) will determine the control voltage $V_{\rm ctrl}$. Then the relative magnitude of ith fractional spur will be

$$S(i) = \frac{nK_{\rm VCO}}{2i\omega_{\rm ref}}\frac{2}{nT_{\rm ref}}\left[\left\{\int_0^{nT_{\rm ref}} V_k \sin\left(i\frac{\omega_{\rm ref}}{n}t\right)dt\right\}^2 + \left\{\int_0^{nT_{\rm ref}} V_k \cos\left(i\frac{\omega_{\rm ref}}{n}t\right)dt\right\}^2\right]^{1/2} \cdot 10^{S_{\rm LF}/20} \tag{5}$$

$V_{\rm ctrl}$ is constructed as follows—

- The voltage domain is divided into equally spaced levels. Each of V_k will occupy these levels.
- A_k can be either 0 or 1. The sequence having highest aggregation of either 0 or 1 is determined. Start from the beginning of that sequence.
- The V_k associated with the first 0 in the entire sequence is assigned the highest level. The next levels are assigned to the next 0's.
- The last 1 in the sequence is assigned the next level. The preceding 1's are assigned the remaining levels from the end to the beginning.
- The intermediate regions will constitute the ramp signals.

Charge pump nonideality attributes to the mismatch between the up and down currents leading to reference spurs at multiples of $f_{\rm ref}$ away from $f_{\rm out}$. A PLL utilizing a second order DSM [2], shown in Fig. 1, is used to verify the magnitude of spurs due to this nonideality. The parameters of the PLL are shown in table I. The control voltage approximation is shown in Fig. 2. It is divided into two waveforms represented as $V_{\rm c1}$ and $V_{\rm c2}$. $V_{\rm c1}$, constructed following the above procedure, contributes to fractional spurs, while $V_{\rm c2}$ is used to calculate the reference spurs. Now, $V_{\rm c2}$ is approximated into a

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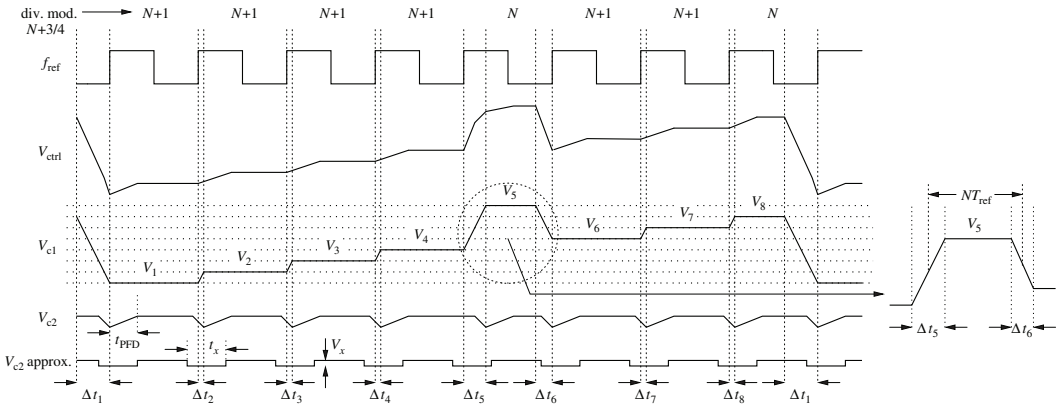

Fig. 2. Approximated control voltage 2nd order DSM and $\alpha = 3/4$

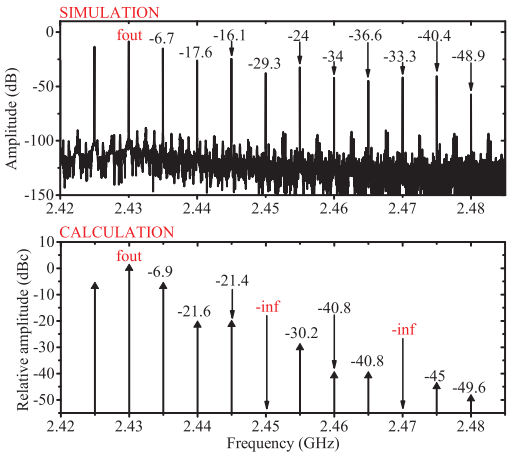

Fig. 3. Fractional spurs comparison for the PLL with 2nd-order DSM and $\alpha = 3/4$

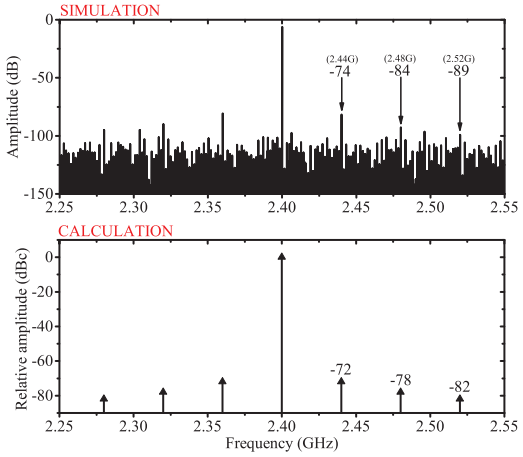

Fig. 4. Reference spurs comparison for the integer PLL

rectangular wave with peak-to-peak amplitude V_x which denotes a voltage such that the area under V_x is same as the area under the triangular wave of duration t_x. Following this convention, t_x and V_x can be expressed as,

$$t_x = t_{\mathrm{PFD}} \frac{I_{\mathrm{UP}}}{I_{\mathrm{DN}}}, \quad V_x = \frac{1}{2C_1} \left(I_{\mathrm{UP}} - I_{\mathrm{DN}}\right) t_{\mathrm{PFD}} \tag{6}$$

The Fourier expansion of V_{c2} will furnish the relative magnitudes of the reference spurs. As seen from Fig. 2, V_{c2} will have period of $8f_{\mathrm{ref}}$. The reference spurs are evaluated using t_x and V_x from (6) and substituting them in the following equation.

$$S_{\mathrm{int}}(i) = \frac{K_{\mathrm{VCO}}}{2i\omega_{\mathrm{ref}}} \frac{2}{T_{\mathrm{ref}}} \left[\left\{ \int_0^{t_x} V_x \sin\left(i\omega_{\mathrm{ref}} t\right) dt \right\}^2 + \left\{ \int_0^{t_x} V_x \cos\left(i\omega_{\mathrm{ref}} t\right) dt \right\}^2 \right]^{1/2} \cdot 10^{S_{\mathrm{LF}}/20} \tag{7}$$

Comparison of fractional and reference spurs obtained through simulation and calculation are shown in Fig. 3 and Fig. 4 respectively. The maximum deviation between the results appears to be 7 dB.

Finally, we state that, though analytical models for reference spurs due to CP current mismatch exist [3] [4], a model for predicting fractional spurs is sparsely existing. The work presented in [5] presents one such model. Though the referred model predicts the spurs with high accuracy, we believe the model presented here is simpler and equally accurate. However, to be noted that, though lower order binary modulators produce smaller spurs, still, higher order multistage modulators are used today as their noise shaping characteristics are superior. In this case, the procedure for constructing V_{ctrl} will require further investigation.

III. Conclusion

The analysis presented here is simple and produces fairly accurate values of spur magnitudes. Maximum deviation between simulated and measured values seems to be 7 dB which may be related to the exponentially decaying nature of the control voltage and larger rise and fall times of the up and down signals in real circuits. Nonetheless, the calculations using the model fairly complies with the simulated results.

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