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Large dynamic range Readout Integrated Circuit for Infrared Detectors

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***Abstract*—Infrared (IR) thermal imaging is an emerging technology with promising industrial, scientific, space and medical applications. In general ROICs are made of using standard silicon technology to collect signals from the Infrared detectors arrays. Typical detector arrays are made on wafers of compound semiconductors, which are then bump bonded to silicon ROICs. ROIC circuit design of direct injection with correlated double sampling (CDS) has been proposed and implemented to meet the readout noise. The large charge handling has been achieved through optimum use of metal oxide semiconductor (MOS) capacitor. CDS removes the correlated noise by subtracting reset noise, offset from the signal. The performance of most of the infrared focal plan arrays (FPAs) are limited by large dark current.This then appears as an offset voltage in the ROIC output. This reduces the actual dynamic range of the ROIC. The offset resulting from dark current can be removed through a proposed skiming circuit which subtracts a preset current from the input current before integration. We have used a current mirror circuit for offset removal. An external off-chip trimming resistor has been provided for adjusting the trimming current. We have archived charge handling capacity of 11M$\bar{e}$, readout noise of $<$ 397 electrons and low power of $<$ 128 mW with in pixel size of 30 μm$\times$30 μm of 320$\times$256 ROIC.**

***Keywords*-Readout integrated circuit (ROIC), detectors, direct injection (DI), snapshot, Array, Semiconductor Laboratory (SCL), million electron (M$\bar{e}$), focal plane array (FPA).**

I. Introduction

The absorption of an IR photon by the detector sensitive material generates an electron-hole pair which is separated by the internal electrical field of the photodiode. The photodiodes are electrically coupled to the readout circuit by direct injection and the charges generated by the absorption of IR photons during the integration time are stored in the capacitance of the Read Out Integrated Circuit (ROIC)[1], [2], [3], [4], [5]. At the end of the integration time, the charge stored in the capacitance is transferred to a charge-voltage conversion amplifier. Several multiplexers operating simultaneously allow the transfer of the signals from the amplifiers to the outputs. Fig. 1 shows basic block diagram of principle of the IR detection.

The IR detector are hybridised on a silicon readout circuit. For critical applications like space readout circuit typically used in a snapshot configuration ie all pixels are sampled at the same time. The simultaneous integration of charges

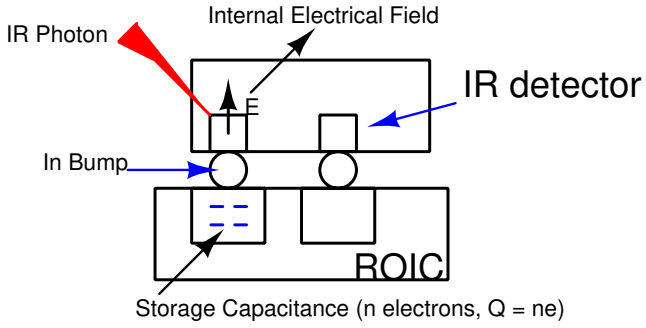

Figure 1. Principle of infrared detectors

during read-out of a previous frame is known as integration while read IWR mode. Large dynamic range ROIC requires high value of integration capacitors/pixel. Where as accuracy demands for large active circuit/pixel like implementation of CDS etc and demands for high resolution for imaging application requires small pixel size. It leads to a complex design constraints on ROIC design for IR detectors. traditionally IR detectors noise are subtracted after digitization which results into the integration of noise and demands large integration capacitor/pixel to improve charge handling capacity. We have proposed a pixel level 'skimming' feature for subtraction of dark offset current. Detector's dark current eats into the useful dynamic range of the ROIC. Circuitry for subtracting dark current has been added in this design which extends the useful dynamic range of the ROIC. We have archived charge handling capacity of 11M$\bar{e}$, readout noise of $<$ 397 electrons and low power of $<$ 128 mW with in pixel size of 30 μm$\times$30 μm of 320$\times$256 ROIC.

II. Typical ROIC Operation

The ROIC circuit consists of unit cells for charge integration and charge to voltage conversion, timing and control circuits, signal processing stages, pixel voltage multiplexers, and amplification stages as illustrated in Fig. 2.

Each unit cell integrates the photo-current from the detector connected to its input and the resulting charge is converted to an equivalent voltage. The voltage output of the unit cell is then multiplexed into a serial stream through

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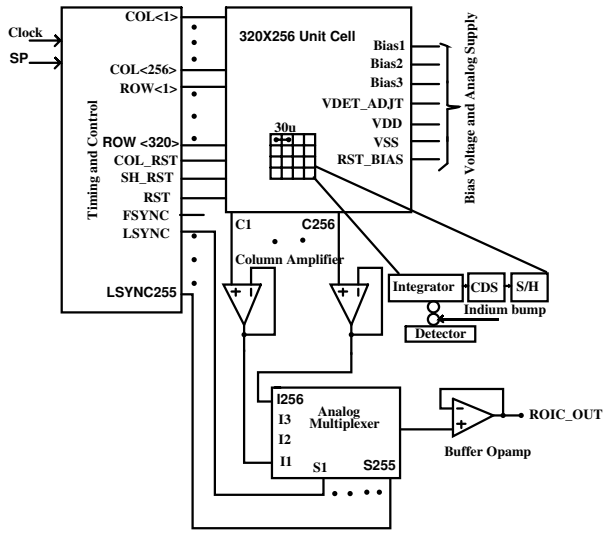

Figure 2. Basic Sub-modules of ROIC ASIC

a column amplifier, multiplexer and output buffer. In order to support the snapshot mode operation, each ROIC pixel also requires a sample and hold circuit to hold the pixel output value of the last frame in order to free up the rest of the circuit to perform the next integration, while the output is waiting to be read. The input stage is known as the 'unit cell'and it includes an integration stage, a signal conditioning CDS stage and the sample and hold stage.

The pixel area is dependent on the size and resolution of detector array and cannot be changed. The noise of ROIC can be reduced with pixel level CDS implementation at the cost of area and charge handling capacity. Due to space constraints, charge handling capacity and noise performance are difficult to meet simultaneously for all topologies.

For example our design goal for charge handling capacity is >5 M$\overline{\text{e}}$ or Q = 800 fC. The value of integration capacitance required for handling this charge is given by:

$$C = \frac{Q}{V} = \frac{800\text{fC}}{1\text{V}} = 800\text{fF}$$

Linearity of the integration capacitor is important for over all linearity of the ROIC. However, the use of most linear metal insulator metal (MIM) capacitors will need an area of approximately 800 μm^2. Since the pixel size is 30 $\mu m \times 30$ $\mu m = 900 \mu$m^2, the capacitor will occupy 88% of the pixel area. Thus it is not feasible to implement both CDS and signal processing stages simultaneously. The proposed work includes additional features of skimming. We have used MOS capacitor to achieve large charge handling capacity for further improvement of charge handling capacity within 30 μm $\times$ 30 μm pixel size.

Other submodules of the ROIC include timing and control circuitry which uses two external digital signals: the master clock and the start pulse. These two signals are used to generate internal timing and control signals for the ROIC operation. These timing signals are used by the unit cells to manage the sequence of operations required to integrate the detector current. The column amplifier stage is used for buffering the output of the pixel and to drive the multiplexed column bus.

III. Proposed ROIC architecture

The basic function of a ROIC unit cell is to integrate the detector current and convert this signal to a voltage level. The integration and reading of a unit cell is controlled by the timing and control circuit. When the integration cycle is followed by a read out operation, this is known as integrate then read mode operation. In this mode of integration, half the frame time is used for reading the pixel information. Since there is no readout during the integration phase, there is no switching activity in the circuit. This eliminates noise due to digital signals. However, during the reading cycle, integration is stopped which misses the integration of useful information during readout time. Critical operations like military and space applications require continuous acquisition of data. The read-while-integration mode supports continuous integration and simultaneous reading. In this mode of integration, reading cycle of a particular frame goes in parallel with the next integration cycle. In order to support this operation, a sample and hold circuit is required to hold the pixel voltage for the entire read cycle. The signal from the hold capacitor is then read out during the next integration cycle. An amplifier stage is used before the sampling stage to drive the sampling capacitor. A correlated double sampling (CDS) stage can be introduced just before the sampling capacitor for readout noise optimization.

Fig. 3 shows the implemented Direct injection(DI) unit cell with a CDS stage. Direct Injection topology provides stable detector bias but suffers in low illumination conditions due to low injection efficiency [1], [6], [7]. During the reset phase, the negative terminal of the CDS stage MOS capacitor C_2 is reset to ground and the positive terminal of capacitor C_2 samples correlated noise and offset voltage as shown Fig. 3. In the integration phase, noise and offset is subtracted from the integrated value. Thus the output voltage ΔV depends only on the integrated signals. This ΔV is transferred to the hold capacitor C_3 as switch SH_TR turns ON.

For a particular frame rate, this ΔV is proportional to the detector current and hence the output voltage should be a linear function of the input current. Correlated double sampling (CDS) has been implemented to improved the dynamic range. We have optimized the size of the integration capacitor through a parallel combination of Metal Oxide semiconductor (MOS) capacitor. The MOS capacitor adds non-linearity due to its inherent structure. However it provides nearly four-times the capacitance per unit area. The

dynamic range of MOS capacitor has been adjusted through appropriate biasing in saturation region so that the overall linearity of MOS capacitor increased. The skimming circuit is a simple current mirror circuit of 500:1 ratio. The dark signal noise has been removed through SKIM transistor M_3 at pixel level. The off chip resistor value need to select once to calibrate detector dark noise.

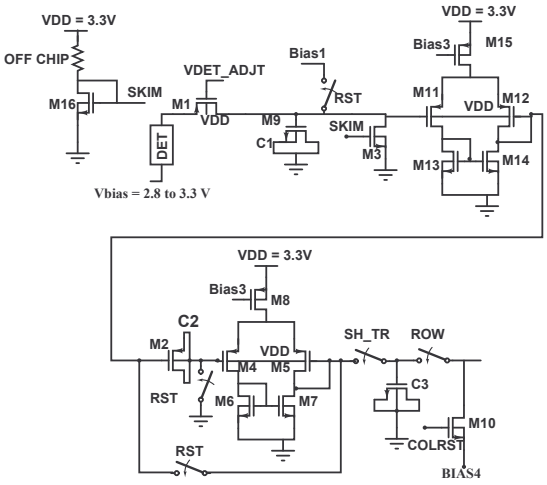

Figure 3. Proposed DI architecture

Typically source follower amplifier stage is used for charge to voltage conversion. The gain of source follower stage is just less than 1. Due to large variation of threshold voltages in the selected process, the source follower output voltage range is reduced. A buffer stage (M_{11} - M_{15}) has been implemented to improve the dynamic range. However it requires additional power.

We have optimized the pixel dynamic range with a unity gain buffer as shown in Fig. 4. The trade off study shows that increase in pixel power consumption is very small and will meet system specifications, but the dynamic range is increased considerably.

The gain between the detector node V_{DE} and the correlated double sampling (CDS) circuit input node A is close to unity. However it is difficult to get large charge handling capacity within a pixel size of 30μm $\times$ 30 μm.

In order to support the snapshot mode of operation, the signal from the last integration needs to be sampled and held before reseting the integration capacitor to start the integration of the next frame. The signal from the previous frame is stored temporally, and will be read out sequentially by the multiplexer. The key characteristics of the sample and hold (S/H) circuit are its settling time and droop rate. The settling time of S/H is governed by the time required to charge or discharge the hold capacitor C_3. However constraints resulting from droop rate require a high value of hold capacitor to meet the system requirement of 14 bit accuracy. The droop rate of the Hold capacitor depends on the capacitor leakage current. For MIM/MOS capacitor, the leakage current in 0.18 μm process has been computed through simulation. For the selected technology, capacitor leakage is 0.125 mV/pF/ms. In order to have uniform pixel response this droop should be less then 1 LSB. For pixel rate of 100 Hz, the last pixel will be read out 10ms later than the first one. This requires the S/H capacitor size to be C_3 = 2.5 pF, which can not be accommodated in the available space of the unit cell. However, the pixel to pixel variation caused by droop rate can be calibrated. The value of hold capacitor has been chosen based on the available area for the capacitor with in the 900 μm^2 pixel size. Since a MOS capacitor provides nearly four-time the capacitance per unit area, C_3 = 400 fF has been implemented using MOS capacitors.

The performance optimization of one ROIC parameter is feasible at the cost of performance degradation in other parameters. Hence a trade off is required. Following are the proposed steps for the ROIC unit cell design.

1) Maximize the integration, hold and CDS capacitor value.
2) Choose the RESET voltage (Bias1) based on optimum swing at the integration node.
3) Compute the I_{bias} limit of buffer amplifier
4) Compute the bias current I_{bias} limit based on bandwidth requirement.
5) Finalize bias current I_{bias}.
6) Compute the (W/L) for M_1,M_2,M_3,M_4 and M_5 based on current and swing requirements.
7) Estimate the thermal noise and flicker noise component contributed by the input stage transistor M_1.
8) Select (W/L) for RESET switch.
9) Select (W/L) for sample and hold transfer switch.
10) Select (W/L) of the five transistor opamp

The pixel opamp is required to drive the S/H capacitive load of 400 fF. The input voltage range of the pixel opamp has been finalized based on the input voltage range of signal. The design specifications of the pixel opamp are given in Table. I

Table I
GOAL SPECIFICATION OF PIXEL OPAMP

Parameters	Specifications
DC Gain (dB)	>30
Unity Gain Bandwidth product (KHz)	600
Settling time (us)	<15.5
Slew rate (V/μ s)	0.26
Equivalent input noise (nV/Hz)	56
Load capacitor (fF)	>400
Power (μ W)	< 1

A large hold capacitor value reduces the voltage droop and minimizes pixel to pixel photo response variation. The

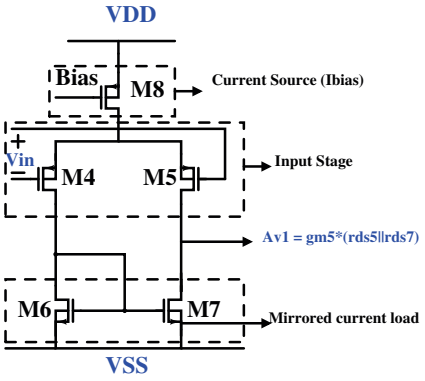

Figure 4. Unit cell Opamp (pMOS as input stage)

sample and hold capacitor also decides the dynamic range. Dur- ing charge transfer to the column amplifier, the input voltage depends on the sample and hold capacitance and long wire parasitic capacitor of the large array. Hence, in order to increase the sample and hold capacitor value, a 1.8V MOS capacitor with a thinner insulator is a better choice since it has twice the capacitance per unit area as compared to 3.3V MOS capacitors. Hence 1.8V MOS capacitors have been used. The performance of most of the quantum detectors is limited by large dark current.This then appears as an offset voltage in the ROIC output. This reduces the actual dynamic range of the ROIC. This IR signal represents the small temperature change from the target to detector. The voltage swing on the integration capacitor for Without skimming is:

$$\Delta V = \frac{(I_{\text{noise}} + I_{\text{signal}}) \times t_{int}}{C_{int}} \tag{1}$$

If skimming is included the relationship simply becomes

$$\Delta V = \frac{(I_{\text{noise}} + I_{\text{signal}} - I_{\text{skim}}) \times t_{int}}{C_{int}} \tag{2}$$

If we assume that 100% of the background noise is subtracted the above equation shows us that we can integrate for a large time without saturating the integration capacitor and the signal being integrated is mainly from the IR signal.

$$\tau_{int} = \frac{\Delta V \times C_{int}}{I_{\text{signal}}} \tag{3}$$

There are two methods for current skimming circuit. The first is simple and uses a bias voltage on the gate of MOS-FET and the second method uses an external resistor, PMOS current buffer and a current mirror. Using a current mirror provides better sensitivity for temperature variations and is low noise. We have added novel circuit using pixel level skimming circuit by transistor M_3. The skimming current has been controlled through off-chip resistor and a large size on chip transistor M_6. The offset resulting from dark current can be removed through a skimming circuit, which subtracts a pre-set current from the input current before integration. A simple current mirror circuit has been used for offset removal. An external off-chip trimming resistor has been provided for adjusting the trimming current. It further improves the dynamic range.

IV. Pixel Level Simulation Results

This unit cell design layout has been designed through Metal 1 and Metal 2 to make easy interconnection at chip level. As per the proposed ROIC optimization methodology given in [8], the size of the CDS capacitor has been optimized for noise requirements and for well capacity requirements. Rest of the available area is given to the sample and hold capacitor to minimize droop and voltage reduction due to charge sharing. The pixel layout and the area distribution among the different capacitors is shown in Fig. 5 and Fig. 6 respectively.

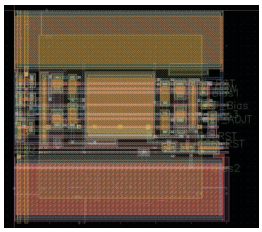

Figure 5. Layout of a Pixel

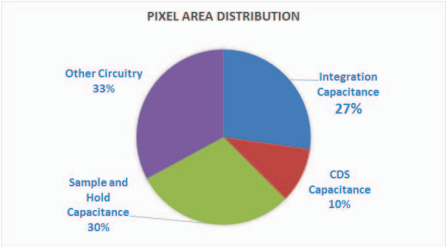

Figure 6. Area Distribution

Fig. 6 shows that 2/3rd of the area has been used by the three capacitors. The simulated results across all process corners, with 3% VDD variation and from -55°C to 60°C shows 99.99% linearity. Also the increase in static power is within the specification for typical case and slightly more at higher temperature mainly due to the variation of VDD. However, in operating condition ROIC is never required to operate above room temperature. (In fact, its typical usage is at liquid nitrogen temperature).

Table II
PIXEL DESIGN AND SIMULATION RESULTS

Parameters		Post Layout Simulation
Input Current@100 Hz(pA)		0.1-170
Maximum current@5kHz (nA)		8.2
Well capacity (MeV)		10.5
Noise (e^-)@300K		322
power (nW)	max	1594
	typ	752
	min	194

In Fig. 7, the output voltage from post layout simulation for different input currents and the corresponding linearity plot is shown.

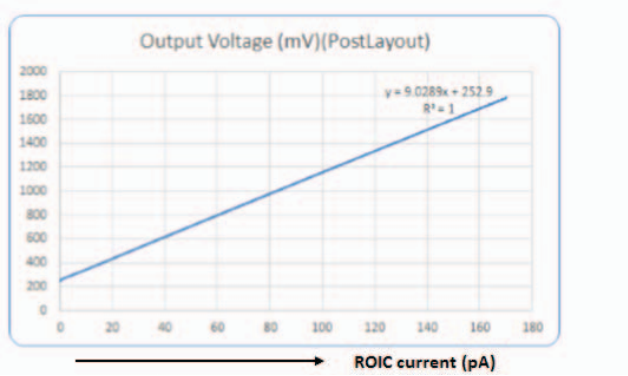

Figure 7. Postlayout simulated linearity of ROIC Pixel output

V. INTEGRATED PERFORMANCE OF 320×256 READOUT INTEGRATED CIRCUIT

The timing and control signals are also important for the performance of a ROIC. In general for large area array detectors, pixels are sequentially selected and the pixel information is transferred to ROIC output after necessary processing.The sequence of operations is initiated by timing and control circuit. The traditional approach [9] of sequential reading of pixel information leads to comparatively higher power dissipation in column amplifiers. We have proposed low power design technique [10] and an efficient implementation of the unity gain column amplifier. which reduced column amplifier power budget to 20mW.

We have further optimized through the clock disable operations for the group of shift registers which are not used in the selected window. It will reduce maximum power for the smallest window. However power requirements for the readout of full frame 320 × 256 pixels will remain same. This requires to use separate clocks for separate group of flip flops. A window can be selected in multiples of 16, all 16 flip flops in a block are clocked with the same clock. The implemented concept is shown in Fig. 8

Here depending on the address bits, a particular group of 16 flip flops are clocked. So the ring counter is driven by a

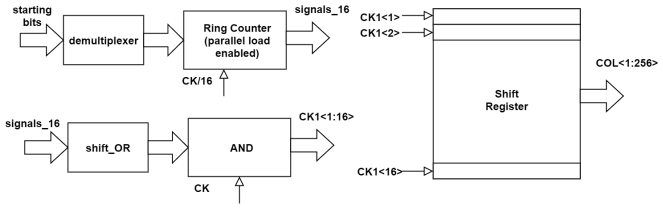

Figure 8. Power optimized Architecture for column and Row signals

divided by 16 clock. We have first delayed the ring counter output of divide by 16 signals by single master clock. The output of this delayed signal is then logical AND with input gives signals high for 17 clock period. The one additional clock period is to ensures operation of last column of a group. the timing and control circuit has been optimized through delayed selection of the column amplifier stage.

The proposed Direct Injection (DI) ROIC of 320×256 array with skimming circuit and correlated double sampling techniques has been implemented in SCL 180 nm process as shown in in Fig. 9. Post layout simulation shows that this large area array provides a charge handling capacity of 11M$\bar{e}$, readout noise of $<$ 500 $\bar{e}$ and low power of $<$ 150 mW at room temperature. Design is also simulated at liquid Nitrogen temperature using developed models. Table III shows postlayout simulation performance of ROIC.

Table III
320×256 ROIC POST LAYOUT SIMULATION PERFORMANCE

Parameters	Simulation	Simulation
	@300K	@ 77K
Pixel Pitch (μw)	30	30
Well capacity (M$\bar{e}$)	11.2	11.2
Noise ($\bar{e}$)	523	397
Power/pixel (μw)	1.4	0.9
ROIC Power (mW)	150	110
Lowest Input Current (pA)	2	1
Frame rate	100-5KHz	100-5KHz
Pixel Rate (Mpps)	10	10
Linearity (%)	99.99	99.99
Windowing	Smallest window size 1×48	
SKIMMING	$>$1 pA	$>$0.5 pA

The output amplifier needs to operate at a pixel rate of up to 10 Mega pixel per second (Mpps). Hence unity gain bandwidth of $>$95 MHz has been implemented for meeting 14 bit accuracy requirements of ROIC and drive off-chip load of 25 pF.

VI. CONCLUSION

Area array ROIC of 320×256 pixels is designed in 180 nm, 3.3V compatible CMOS process from Semi Conductor Laboratory (SCL), INDIA. The novel skimming circuit and low ROIC power design technique has been proposed and post-layout simulation results have been given in this paper.The proposed circuit is ideal for the development of

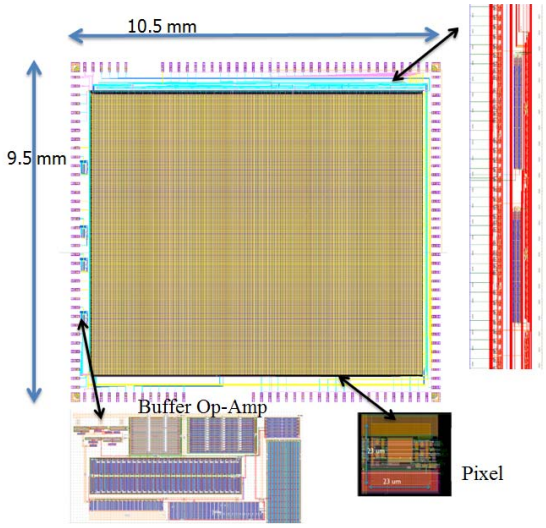

Figure 9. Integrated ROIC Chip for 320×256 array size

Table IV
ROIC PERFORMANCE COMPARISON

ROIC Parameters	This Work	[11]	[12]	[13]	[14]
Array size	320×256	8×10	64×64	1024×1024	128×128
Pixel size (μm^2)	30×30	30×30	50×50	30×30	30×30
Input cell	DI	CTIA	CMI	CTIA	CTIA
Input Current (Nominal Range)	1 pA to 10nA	10 pA to 10nA	1 nA to 50nA	1 nA	5 nA
Charge handling capacity (M$\overline{e}$)	10	2	280	NA	2.75
Frame rate	0.1 to 5 KHz	110 Hz	110 Hz	NA	NA
Pixel rate	5 MHz	3 MHz	2 MHz	10 MHz	2 MHz
Integration type	snapshot	snapshot	NA	NA	NA
Power/pixel	900 nW	2.2 μW	NA	NA	NA
Readout noise @300K ($\overline{e}$)	523	6373	2978	NA	NA
Temperature	77 to 310K	77 to 300K	300K	300K	300K
Linearity (%)	99.9	99	NA	99	99
Windowing	Smallest window size 32×48	-	-	NA	NA

large dynamic range infrared focal plane array. This design is currently under fabrication.

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REFERENCES

[1] J.L. Vampola, "Readout electronics for infrared sensors," in *Infrared and Electro-Optical Systems Handbook, edited by W.D. Rogatto, Billingham, Washington*, 1993, p. Ch. 3.

[2] Francisco Serra-Graells et al, "Low-power and compact cmos aps circuits for hybrid cryogenic infrared fast imaging," *IEEE Transaction on Circuits and SystemsII Express Briefs*, vol. 54, no. 12, DEC. 2007.

[3] Jozef Piotrowski and Antoni Rogalski, "New generation of infrared photodetectors," *Sensors and Actuators A: Physical*, vol. 67, no. 1-3, pp. 146–152, 1998.

[4] Antonio Rogalski, *Infrared Detectors*, Actuators A: Phys, second edition, 2010.

[5] A Rogalski P Martyniuk, "Quantum-dot infrared photodetectors: Status and outlook," *Progress in Quantum Electronics*, vol. 32, pp. 89120, 2008.

[6] Kruer D. Scribner, M and J. Killiany, "Infrared focal-plane array technology," *Proc. IEEE*, vol. 79, pp. 66 – 85, 1991.

[7] S-W Han and E Yoon, "Area-efficient correlated double sampling scheme with single sampling capacitor for CMOS image sensors," *electronics letters*, vol. 42, no. 6, pp. 335–337, 2006.

[8] H. S. Gupta, A. S. K. Kumar, M. S. Baghini, S. Chakrabarti, and D. K. Sharma, "Design of high-precision roic for quantum dot infrared photodetector," *IEEE Photonics Technology Letters*, vol. 28, no. 15, pp. 1673–1676, Aug 2016.

[9] H S. Gupta, A S K. Kumar, S. Chakrabarti, S. Paul, R.M. Parmar, D R M. Samudraiah, M S. Baghini, and D K. Sharma, "Design of large dynamic range, low-power, high-precision ROIC for quantum dot infrared photo-detector," *Electronics Letters*, vol. 49, no. 16, pp. 1018–1020, 2013.

[10] Hari Shanker Gupta, Pranoy Datta, Maryam Shojaei Baghini, AS Kiran Kumar, and Dinesh K Sharma, "Low power configurable readout integrated circuit for infrared detector," 2018.

[11] Yi-Chuan; Shieh Hsiu-Li Sun, Tai-Ping; Lu, "A novel readout integrated circuit with a dual-mode design for single and dual-band infrared focal plane array," *Infrared Physics Technology*, vol. 60, September. 2013.

[12] HalukKulah and Tayfun Akin, "A current mirroring integration based readout circuit for high performance infrared fpa applications," *IEEE Transaction on Circuits and SystemsII: Analog and digital Signal Processing*, vol. 50, no. 4, April. 2003.

[13] L. Xie et al., "Readout circuit with novel background suppression for long wavelength infrared focal plane arrays," *Int. J. Electron*, vol. 98(2), pp. 207–222, 2011.

[14] Wenlong Ma et al, "A high speed snap-shot mode readout circuit for QWIP IR FPAs," in *Industrial Electronics and Applications, 2009. ICIEA 2009. 4th IEEE Conference on*, 2009, pp. 1012–1015.