

Instance	Design unit	Design
ha_tb	ha_tb	Modul
uut	ha	Modul
#INITIAL#15	ha_tb	Proce
#vsim_capacity#		Capac

Name	Value	Kind	Mo
a	1	Regis...Inte	
b	1	Regis...Inte	
carry	St1	Net	Inte
sum	St0	Net	Inte

Processes (Active)

Name	Type (filtered)
#INITIAL#15	Initial

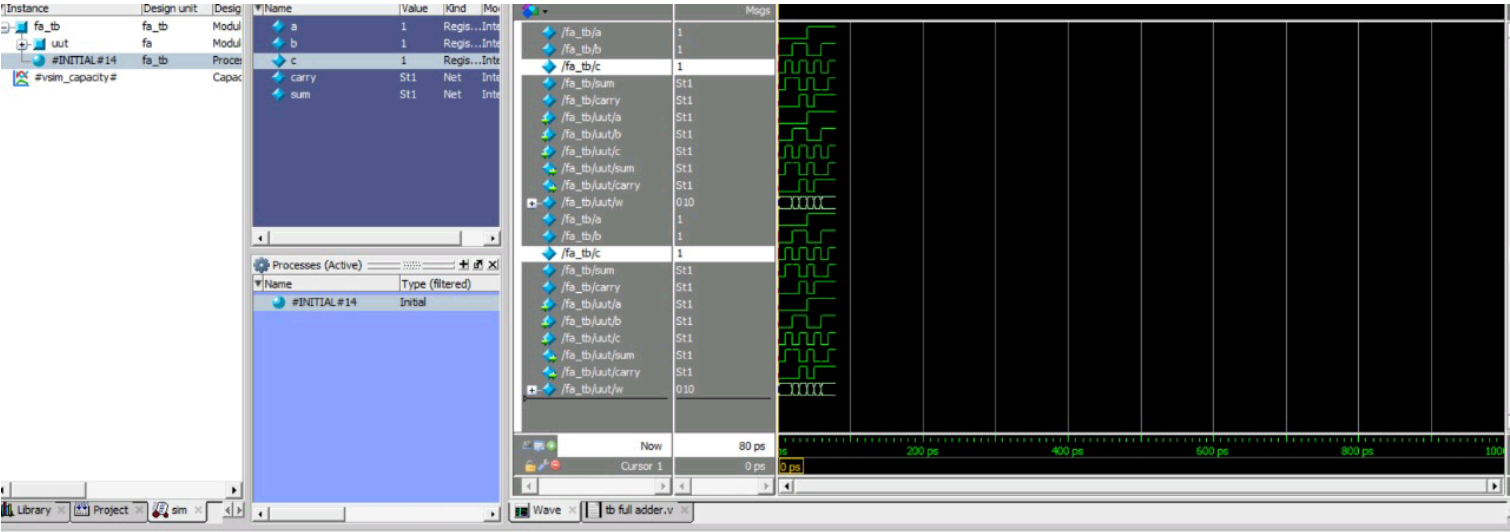
	Msgs
/ha_tb/a	1
/ha_tb/b	1
/ha_tb/sum	St0
/ha_tb/carry	St1
/ha_tb/uut/a	St1
/ha_tb/uut/b	St1
/ha_tb/uut/sum	St0
/ha_tb/uut/carry	St1

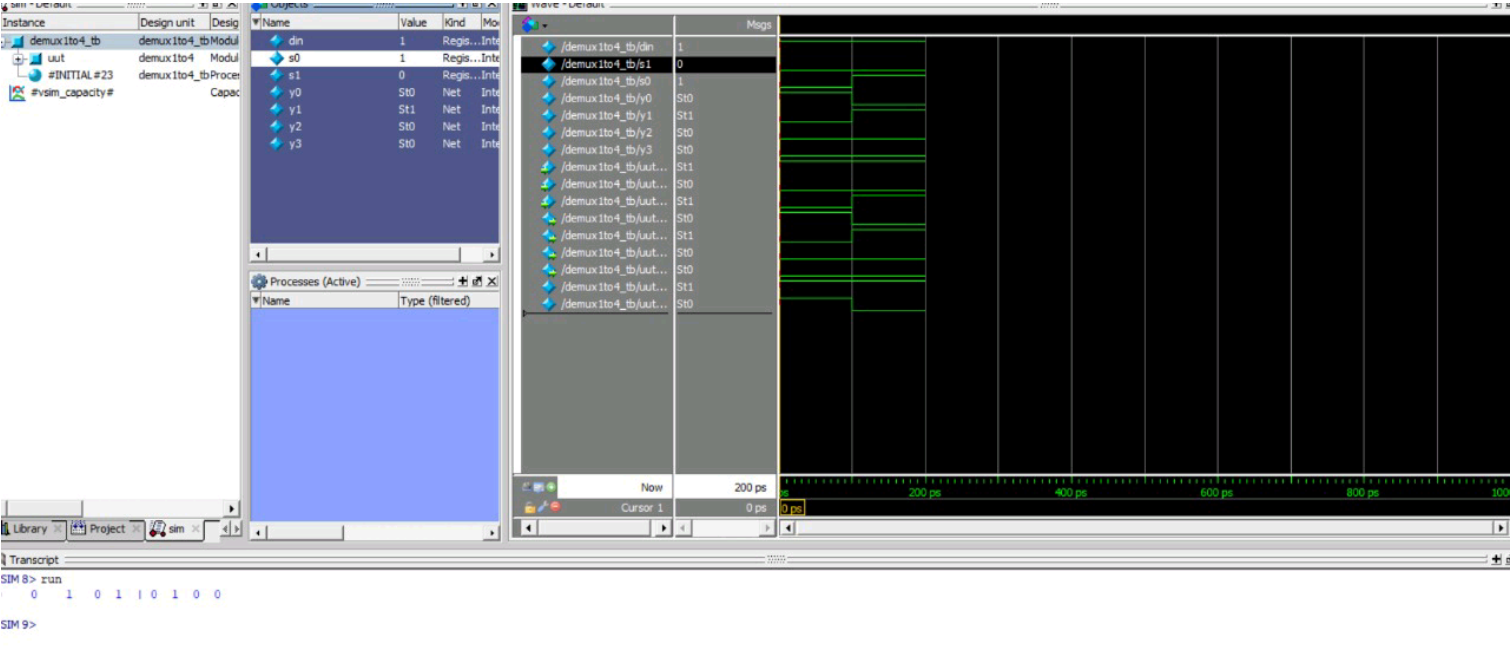
Now40 ps

Cursor 10 ps2 ps

200 ps400 ps600 ps800 ps

Wave tb_half adder.v





sim - Default

Instance	Design unit	Design
encoder2to4_tb	encoder2to...	Modul
uut	encoder2to4	Modul
#vsim_capacity#	Capac	

Objects

Name	Value	Kind	Mo
dn	0000	Pack...	Inte
y	00	Net	Inte

Processes (Active)

Name	Type (filtered)
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Wave - Default

	Msgs
/encoder2to4_tb/dn	0000
/encoder2to4_tb/y	00
/encoder2to4_tb/u...	0000
/encoder2to4_tb/u...	00

Now

Cursor 1

300 ps

80 ps

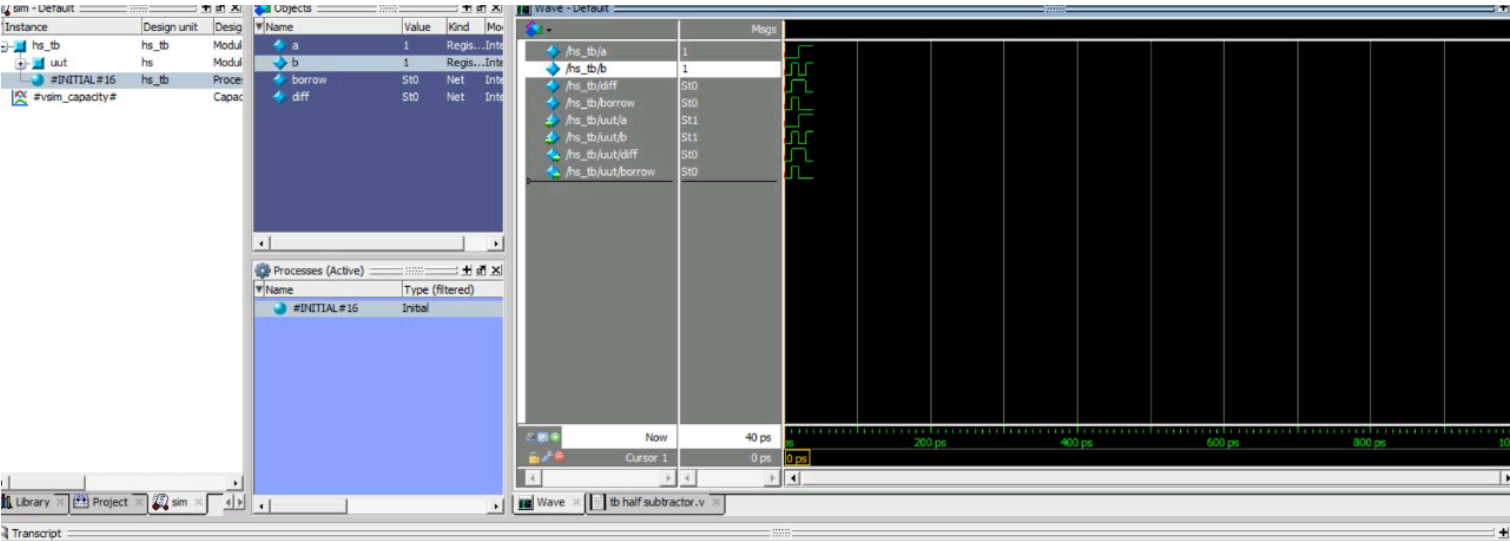
80 ps 200 ps 400 ps 600 ps 800 ps 1000 ps

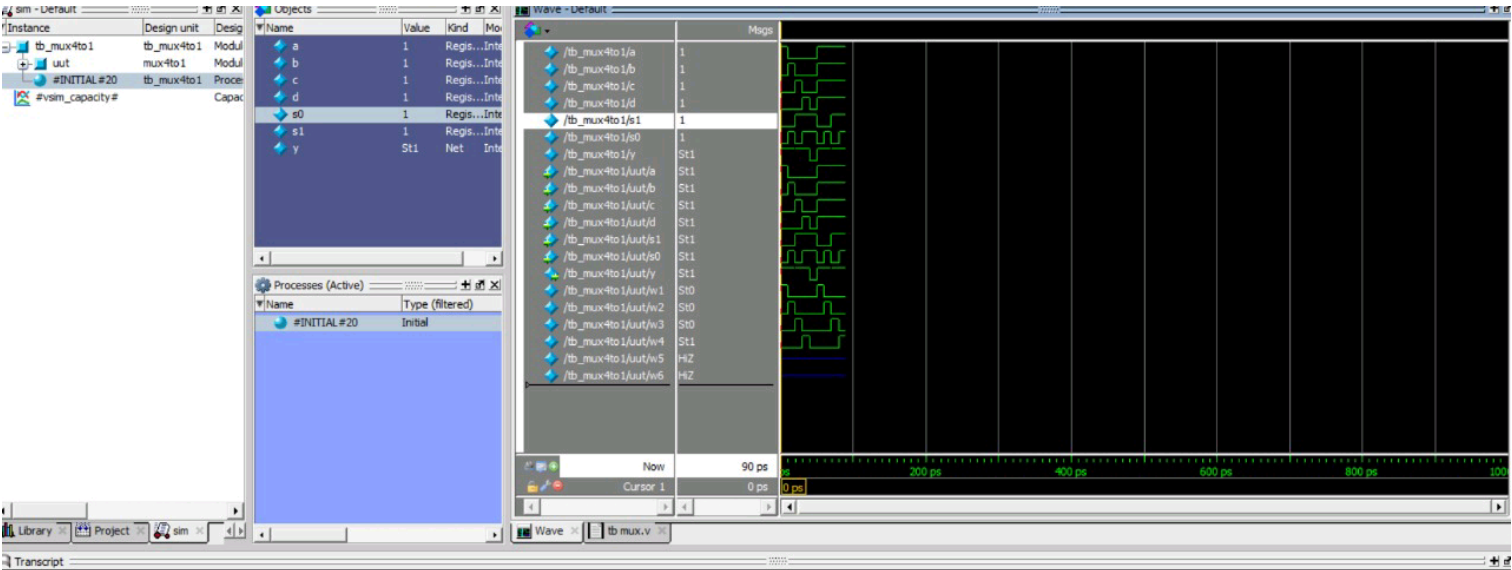
Transcript

Break in Module encoder2to4_tb at C:/modelsim 1/tb encoder.v line 27

IM 9> run

IM 9>





Transcript

```
# 1
# Break in Module tb_mux4to1 at C:/modelsim 1/tb_mux.v line 48
#SIM 10>
```