Compiler Assignment

Phase 1

Team Members:

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Step 2:

i) source (.c) to binary (executable)

Binary code that can be executed directly on the CPU

CMD: clang test.c -o testExecutable

Input File: test.c

Output File: testExecutable

ii) source (.c) to object file (.o)

Intermediary files generated in the compilation process

```
    Vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ clang -c test.c -o test0bject.o
    Vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ ll total 32 drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 01:57 ./ drwxrwxr-x 5 vagrant vagrant 4096 0ct 11 2022 ../ -rw-rw-r- 1 vagrant vagrant 331 Nov 5 2020 test.c -rwxrwxr-x 1 vagrant vagrant 15632 Nov 6 01:57 testExecutable* -rw-rw-r- 1 vagrant vagrant 1280 Nov 6 01:57 test0bject.o
```

CMD: clang -c test.c -o testObject.o

Input File: test.c

Output File: testObject.o

iii) source (.c) to machine assembly (.s)

Human-readable form of machine instructions that can be executed on the CPU.

```
• vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ clang -5 test.c -o testAssembly.s
• vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ ll
total 36
drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 01:57 ./
drwxrwxr-x 5 vagrant vagrant 4096 Oct 11 2022 ../
-rw-rw-r-- 1 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r-- 1 vagrant vagrant 2099 Nov 6 01:57 testAssembly.s
-rwxrwxr-x 1 vagrant vagrant 15632 Nov 6 01:57 testExecutable★
-rw-rw-r-- 1 vagrant vagrant 1280 Nov 6 01:57 testObject.o
```

CMD: clang -S test.c -o testAssembly.s

Input File: test.c

Output File: testAssembly.s

iv) source (.c) to LLVM bitcode (.bc); source (.c) to LLVM IR (.II)

LLVM bitcode files enable platform-independent optimizations.

```
vagrantQubuntu-mantic:-/src/compiler_project/CS201-F23-Template/test/phase1$ clang -emit-llvm -c test.c -o testBitcode.bc
vagrantQubuntu-mantic:-/src/compiler_project/CS201-F23-Template/test/phase1$ ll
total 40
drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 01:59 ./
drwxrwxr-x 5 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r-- 1 vagrant vagrant 2099 Nov 6 01:57 testAssembly.s
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r- 1 vagrant vagrant 15632 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r- 1 vagrant vagrant 1280 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r- 1 vagrant vagrant 1280 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r-- 1 vagrant vagrant 1280 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r-- 1 vagrant vagrant 1280 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r-- 1 vagrantvagrant 2488 Nov 6 01:57 testBitcode.bc
-rw-rw-rw-r-- 1 vagrantvagrant 4096 Nov 6 01:59 ./
drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 01:59 ./
drwxrwxr-x 5 vagrant vagrant 4096 Nov 6 01:59 ./
drwxrwxr-x 1 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r-- 1 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:57 testAssembly.s
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
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-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 250 Nov 6 01:57 testBitcode.bc
-rw-rw-r-
```

CMD: clang -emit-llvm -S test.c -o testIR.ll

Input File: test.c

Output File: testIR.ll

v) LLVM IR (.II) to LLVM bitcode (.bc)

```
vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ llvm-as testIR.ll -o testBitcodeFromIR.bc
vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ ll
total 48
drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 02:01 ./
drwxrwxr-x 5 vagrant vagrant 4096 Oct 11 2022 ../
-rw-rw-r- 1 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r- 1 vagrant vagrant 2099 Nov 6 01:57 testAssembly.s
-rw-rw-r- 1 vagrant vagrant 2488 Nov 6 01:59 testBitcode.bc
-rw-rw-r- 1 vagrant vagrant 2488 Nov 6 02:01 testBitcodeFromIR.bc
-rwxrwxr-x 1 vagrant vagrant 15632 Nov 6 01:57 testExecutable*
-rw-rw-r- 1 vagrant vagrant 2957 Nov 6 01:59 testIR.ll
-rw-rw-r- 1 vagrant vagrant 2957 Nov 6 01:57 testExecutable*
-rw-rw-r- 1 vagrant vagrant 1280 Nov 6 01:57 testObject.o
```

CMD: Ilvm-as testIR.II -o testBitcodeFromIR.bc

Input File: testIR.II

Output File: testBitcodeFromIR.bc vi) LLVM bitcode (.bc) to LLVM IR (.II)

```
vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ llvm-dis testBitcode.bc -o testIRFromBC.ll
vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ ll
total 52
drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 02:01 ./
drwxrwxr-x 5 vagrant vagrant 4096 0ct 11 2022 ../
-rw-rw-r-- 1 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r-- 1 vagrant vagrant 2099 Nov 6 01:57 testAssembly.s
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:59 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 02:01 testBitcodeFromIR.bc
-rwxrwxr-x 1 vagrant vagrant 15632 Nov 6 01:57 testExecutable*
-rw-rw-r-- 1 vagrant vagrant 2957 Nov 6 01:59 testIR.ll
-rw-rw-r-- 1 vagrant vagrant 2965 Nov 6 02:01 testIRFromBC.ll
-rw-rw-r-- 1 vagrant vagrant 1280 Nov 6 01:57 testObject.o
```

CMD: llvm-dis testBitcodeFromIR.bc -o testIRFromBC.ll

Input File: testBitcodeFromIR.bc

Output File: testIRFromBC.II

vii) LLVM IR (.II) to machine assembly (.s)

```
vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ llc testIR.ll -o testAssemblyFromIR.s
vagrant@ubuntu-mantic:~/src/compiler_project/CS201-F23-Template/test/phase1$ ll
total 56
drwxrwxr-x 2 vagrant vagrant 4096 Nov 6 02:02 ./
drwxrwxr-x 5 vagrant vagrant 4096 0ct 11 2022 ../
-rw-rw-r-- 1 vagrant vagrant 331 Nov 5 2020 test.c
-rw-rw-r-- 1 vagrant vagrant 2099 Nov 6 01:57 testAssembly.s
-rw-rw-r-- 1 vagrant vagrant 2097 Nov 6 02:02 testAssemblyFromIR.s
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 01:59 testBitcode.bc
-rw-rw-r-- 1 vagrant vagrant 2488 Nov 6 02:01 testBitcodeFromIR.bc
-rwxrwxr-x 1 vagrant vagrant 15632 Nov 6 01:57 testExecutable*
-rw-rw-r-- 1 vagrant vagrant 2957 Nov 6 01:59 testIR.ll
-rw-rw-r-- 1 vagrant vagrant 2965 Nov 6 02:01 testIRFromBC.ll
-rw-rw-r-- 1 vagrant vagrant 1280 Nov 6 01:57 testObject.o
```

CMD: Ilc testIR.II -o testAssemblyFromIR.s

Input File: testIR.II

Output File: testAssemblyFromIR.s

Step 3:

Running the opt on HelloPass without any changes.

```
This is Multiplication

216 = load 132, 132a ×24, align 4

217 = load 132, 132a ×35, align 4

This is Store

219 = load 322, 332a ×35, align 4

This is Load

220 = sob nows 132 ×19, 3

Op Code:sub

This is Load

231 = load 322, 132a ×35, align 4

This is Load

232 = sob nows 132 ×19, 3

Op Code:sub

This is Store

Problem 126

227 = load 322, 312a ×5, align 4

This is Load

233 = add nows 132 ×22, 1

Op Code:add

This is Addition

226 = load 322, 132a ×5, align 4

This is Load

237 = load 322, 132a ×5, align 4

This is Load

238 = sdiv 32 ×24, align 4

This is Load

258 = sdiv 322 ×24, align 4

This is Load

259 = sdiv 322 ×24, align 4

This is Load

250 = sdiv 322 ×24, align 4

This is Load

271 = load 322, 132a ×24, align 4

This is Load

272 = load 322, 33a ×22, align 4

This is Load

273 = load 322, 33a ×22, align 4

This is Load

274 = load 322, 33a ×22, align 4

This is Load

275 = load 322, 33a ×22, align 4

This is Load

377 = load 322, 33a ×22, align 4

This is Load

378 = load 322, 33a ×22, align 4

This is Load

379 = load 322, 33a ×22, align 4

This is Load

370 = load 322, 33a ×22, align 4

This is Load

371 = load 322, 33a ×22, align 4

This is Load

371 = load 322, 33a ×22, align 4

This is Load

372 = load 322, 33a ×22, align 4

This is Load

373 = sdiven said ×222, 1

This is Load

374 = load 322, 13a ×24, align 4

This is Load

375 = load 322, 13a ×24, align 4

This is Load

378 = load 322, 31a ×24, align 4

This is Load

378 = load 322, 31a ×24, align 4

This is Load

379 = load 322, 31a ×24, align 4

This is Load

370 = load 322, 31a ×24, align 4

This is Load

370 = load 322, 31a ×24, align 4

This is Load

371 = load 322, 31a ×24, align 4

This is Load

378 = load 322, 31a ×24, align 4

This is Load

379 = load 322, align 4

370 = load 322, align 4

371 = load 322, align 4

371 = load 322, align 4

371 = load 322, align 4

372 = load 322, align 4

373 = alica 322, align 4

374 = alica 322, align 4

375 = alica 322, align 4

377 = load 322, align 4

378 = alica 322, align 4

379 = alica 322
```

After Modification to HelloPass to print the predecessors and successors

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