**Homework Assignment #5**

***Due Date: 12/6, 11:59 p.m. This is a hard deadline as we will post the solution after the deadline. Please submit via Blackboard. For all questions, please note that you need to show the steps how you obtain your result and please do NOT just provide the final answer.***

***Please name your submission file starting with “LastName\_FirstName\_HW5”.***

**Q1. (15 points)** Please briefly explain the difference among symmetric multiprocessors (SMP) architecture, distributed shared memory (DSM) multiprocessors architecture, and distributed-memory multicomputers architecture.

**Q2. (10 points)** What is false sharing? Please give an example to illustrate it.

**Q3**. **(20 points)** The simple, multicore multiprocessor illustrated in the below figure represents a commonly implemented symmetric shared-memory architecture. Each processor has a single, private cache with coherence maintained using the snooping coherence invalidate protocol. Each cache is direct-mapped, with four blocks each holding two words. To simplify the illustration, the cache-address tag contains the full address, and each word shows only two hex characters, with the least significant word on the right. The coherence states are denoted M, S, and I (Modified or Dirty, Shared, and Invalid).

Assume the initial cache and memory state as illustrated in Figure 1. Assume a sequence of one or more CPU operations of the form:

P#: <op> <address> [<value>]

where P# designates the CPU (e.g., P0 ), <op>  is the CPU operation (e.g., read or write), <address>  denotes the memory address, and <value>  indicates the new word to be assigned on a write operation. Treat each action below as independently applied to the initial state as given in this figure. What is the resulting state (i.e., coherence state, tags, and data) of the caches and memory after the given action? Show only the blocks that change; for example, P0.B0: (I, 120, 00 01)  indicates that CPU P0 ’s block B0  has the final state of I, tag of 120, and data words 00 and 01. Also, what value is returned by each read operation?

a. P0: read 120 (note address 120 hashed to block B0 for all processors).

b. P0: write 120 <-- 80

c. P3: write 120 <-- 80

d. P1: read 110

e. P0: write 108 <-- 48

![A picture containing diagram

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Figure 1. Multicore multiprocessor.

**Q4.** **(10 points)** Please name one advantage of the directory based cache coherence systems over the snoopy cache systems.

**Q5. (10 points)** What are the two main types of hardware threading? Please briefly explain the main difference between them.

**Q6. (10 points)** What is a “pipeline flush” and when does it occur?

**Q7. (10 points)** Please draw a diagram to show what the 3-D torus interconnect topology with 27 nodes looks like.

**Q8. (15 points)** A ***mesh of trees*** is a network that imposes a tree interconnection on a grid of processing nodes. A  mesh of trees is constructed as follows. Starting with a  grid, a complete binary tree is imposed on each row of the grid. Then a complete binary tree is imposed on each column of the grid. The below figure illustrates the construction of a 4 x 4 mesh of trees. Assume that the nodes at intermediate levels are switching nodes. Please determine the bisection width, diameter, and total number of switching nodes in a  mesh.

Diagram

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Figure 2. The construction of a 4 x 4 mesh of trees: (a) a 4 x 4 grid, (b) complete binary trees imposed over each row (nodes added are switching nodes), (c) complete binary trees imposed over each column (nodes added are switching nodes), and (d) the complete 4 x 4 mesh of trees.

THE END.