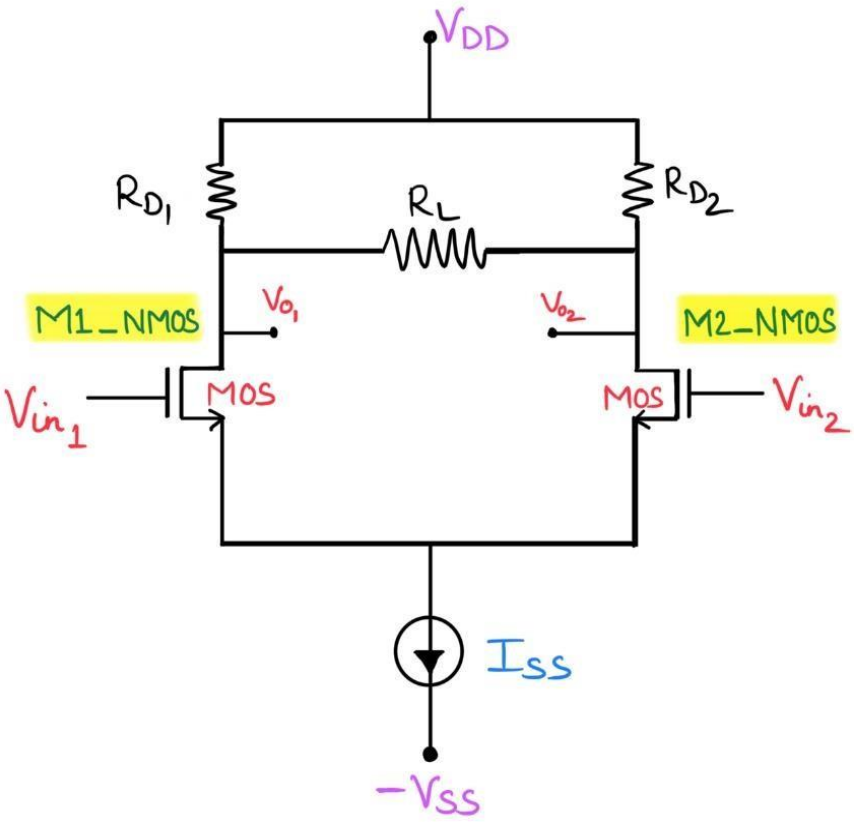
ECN 102 End Term Projects

(Questions specified in the pdf defines group number in the Excel sheet)

Submission Date 17/06/23

GROUP 1-10

Ques 1-10: For a given Differential Amplifier, both NMOS transistors are perfectly matched. Thedevice parameters for both MOSFETs are:



- $\mu nCox$ = 50$\mu A/V$ 2 & (W/L) = 0.5 (for both NMOS device)
- Kn = 0.5*$\mu nCox$ (W/L) = 50e-6.
- Kp = 2Kn
- $Vth1$ = $Vth2$ = 1V
- $Vin1$ = $Vin2$ $(but\ opposite\ in\ phase)$

Consider a sinusoidal waveform of:

a) Amplitude = 10mV

b) Frequency = 20KHz

- V_{th1} = Threshold Voltage of NMOS (M1).
- V_{th2} = Threshold Voltage of NMOS (M2).

- V_{DD} = 5V
- V_{SS} = 5V

Dot Model Statement: - [.model mos nmos (Vto=1V KP=100e-6)]

Derive and Calculate the Differential gain of the Amplifier shown above.

Alsovalidate the results with the LT-Spice simulation.

Groups	$R_{D_1} = R_{D_2}$ (KΩ)	R_L (KΩ)	I_{SS} (mA)
1	5	08	0.6
2	6	10	0.8
3	7	12	1.0
4	8	14	1.2
5	9	16	1.4
6	10	18	1.6
7	11	20	1.8
8	12	22	2.0
9	13	24	2.2
10	14	26	2.4

GROUP 11-25

11) Draw the minimum CMOS transistor network that implements the functionality of Boolean equation F= ((A+B) C + D)'. You can assume both the original and complemented versions of each literal are available as gate inputs.

12) Draw the minimum CMOS transistor network that implements the functionality of Boolean equation F= (A (B C + D))'. You can assume both the original and complemented versions of each literal are available as gate inputs.

13) Draw the minimum CMOS transistor network that implements the functionality of Boolean equation F= (A + (B' + CD)')'. You can assume both the original and complemented versions of each literal are available as gate inputs. F= (A + (B' + CD)')' = (A + B(CD)')' = (A + B (C' + D'))'

14) Draw the minimum CMOS transistor network that implements the functionality of Boolean equation F= (A' + B'C). You can assume both the original and complemented versions of each literal are available as gate inputs. F = (A' + B'C) = ((A' + B'C)')'= (A (B'C)')' = (A (B + C'))'

15) Implement the given Boolean function F= [((CD) +B) A]' and analyse the waveform in LT spice.

16) Implement the given Boolean function F=(AB)' since F= [AB(A+B)]' on simplification results in F=(AB)' and analyse the waveform in LT spice.

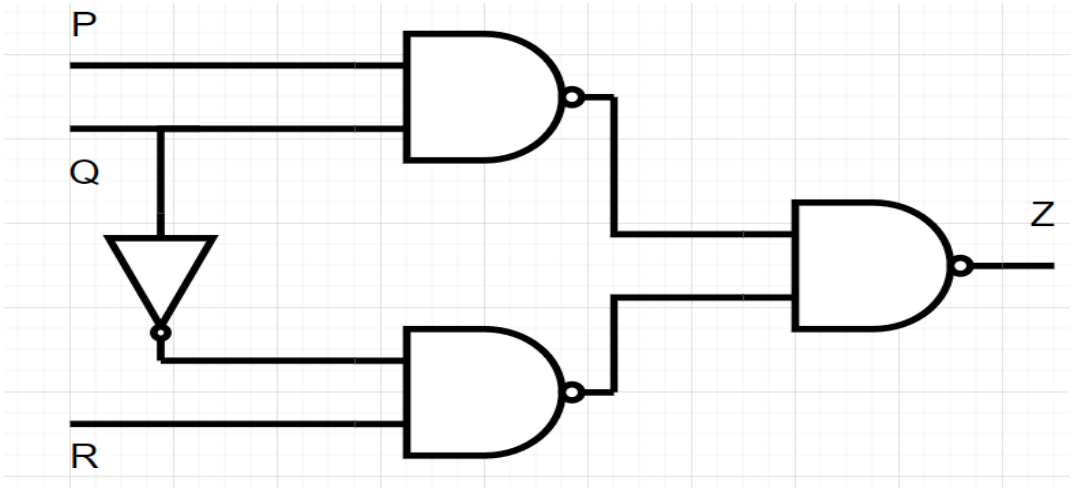
17) Implement the given Boolean function F= ((C'+D') B) +A and analyse the waveform in LT spice.

18) Implement the given Boolean function F= (A+D+C) (B+E) and analyse the waveform in LT spice.

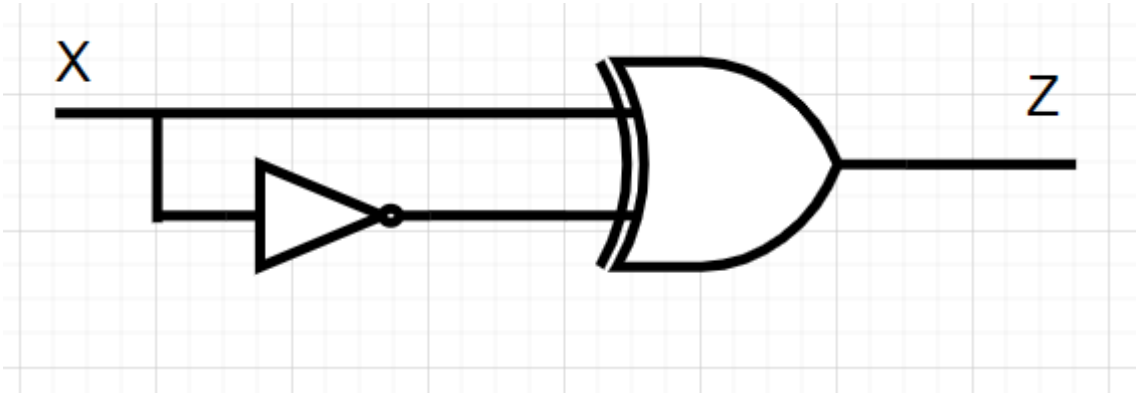
19)Implementation of OR Gate using minimum 2 input NAND gate.

20)Implement 3-input NAND gate using minimum 2-input NAND gate.

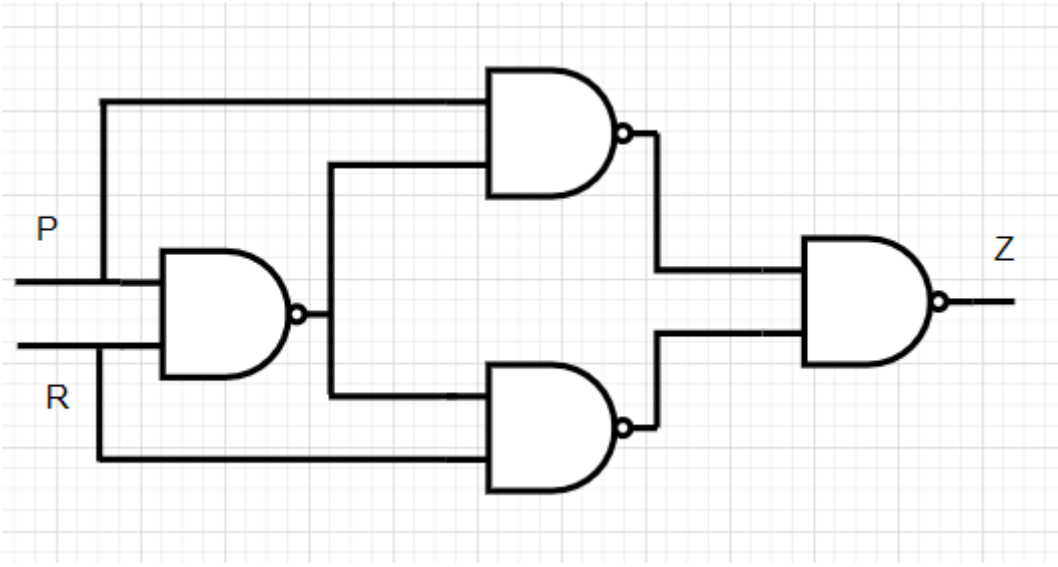
21) Simplify the below circuit and find out the Boolean function at output Z. simulate the circuit using CMOS transistor and verify the Output Z with the waveform in LT spice.



22)Simplify the below circuit and determine the logic function at output Z. simulate the circuit using CMOS transistor and verify the Output Z with the waveform in LT spice.



23)Simplify the below circuit and find out the Boolean function at output Z. simulate the circuit using CMOS transistor and verify the Output Z with the waveform in LT spice.



24) Simulate and analyse 5 stage CMOS inverter-based Ring oscillator and explain the output waveform of Ring oscillator in brief. Initialize one node of ring oscillator. (.ic (0)).
(Given Vdd=1.8, wp= 1.8u, wn=0.6u.)

25) Simulate and analyse 17 stage CMOS inverter-based Ring oscillator and explain the output waveform of Ring oscillator in brief. Initialize one node of ring oscillator. (.ic (0)). (Given Vdd=1.8, wp= 1.8u , wn=0.6u.)

26) Design a positive clamper circuit with biasing voltage that shifts the sinusoidal signal 10sinwt to completely positive part where a signal swings between Vmax= 23 V to Vmin = 3V using Lt-spice. Now apply the clamped waveform to CMOS inverter and observe the output.

27) Design a clipper circuit where we can get the output of sinusoidal signal 13sinwt as 10sinwt using LT spice. Pass the resultant waveform to CMOS inverter circuit and observe the output.

28) Design a negative clamper circuit with biasing voltage by taking 10sinwt and a rectangular pulse as input. Apply the resulting outputs to CMOS inverter circuit.

29) Design a circuit which first clips the positive part of the waveform and then clamps the resultant waveform completely to the positive part. Pass the resultant waveform to CMOS inverter circuit and observe the output.

30) Design a circuit which completely clips the negative part of the waveform and then clamps the resultant waveform completely towards the negative part. Pass the resultant waveform to CMOS inverter circuit and observe the output.

31) Design a 3 by 8 Decoder using NAND gates in Lt-spice.

32) Design a 3 Input NAND and NOR gate using Multiplexer in Lt-spice.

33) Design a 3 by 8 Decoder using NOR gate in Lt-spice.

34) Design an 8 by 3 priority encoder in Lt spice.

35) Design 4:1 mux using logic gates.

36) Design 1:4 Demux using logic gates.

37) Design Half adder using logic gates.

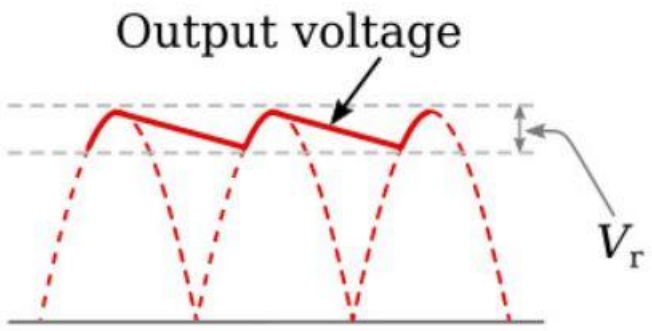
38) Design Half subtractor using logic gates.

39) Design Full adder using logic gates.

40) Design D flip flop using logic gates.

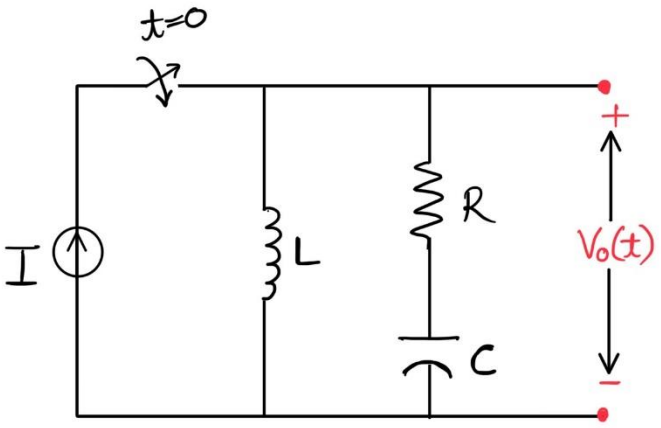
################ **GROUP 41-50** ###############

41) Design a full wave rectifier on LTspice with output as shown below with ripple voltage, V_r = 0.15V, and input is a sine wave of 5V amplitude, f_{in} = 1KHz. Explain the design steps followed to obtain the given output voltage.
42) Design Full adder using logic gates.
43) Design D flip flop using logic gates.
44) Design a full wave rectifier on LTspice with output as shown below with ripple voltage, V_r = 0.25V, and input is a sine wave of 6V amplitude, f_{in} = 3KHz. Explain the design steps followed to obtain the given output voltage.
45) Design a full wave rectifier on LTspice with output as shown below with ripple voltage, V_r = 0.2V, and input is a sine wave of 5V amplitude, f_{in} = 6KHz. Explain the design steps followed to obtain the given output voltage.
46) Design a full wave rectifier on LTspice with output as shown below with ripple voltage, V_r = 0.15V, and input is a sine wave of 6V amplitude, f_{in} = 4KHz. Explain the design steps followed to obtain the given output voltage.
(Hint: The ripple voltage is given by the expression, $V_r = \frac{V_O}{\pi f_{in} RC}$, V_O is output voltage)



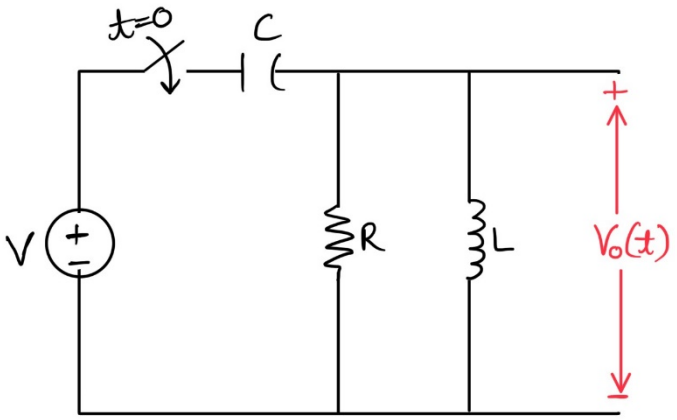
47) Design a RLC circuit shown below on LTspice such that the output voltage is having a damping ratio (ζ): 0.25, damping frequency (ω_d): 2 rad/sec. Explain the design steps followed. Assume that the amplitude of current source for t ≥ 0 sec is 1A.

48) Design a RLC circuit shown below on LTspice such that the output voltage is having a damping ratio (ζ): 0.15, damping frequency (ω_d): 1 rad/sec. Explain the design steps followed. Assume that the amplitude of current source for t ≥ 0 sec is 2A.



49) Design a RLC circuit shown below on LTspice such that the output voltage is having a damping ratio (ζ): 0.15, damping frequency (ω_d): 2 rad/sec. Explain the design steps followed. Assume that the amplitude of voltage source for t ≥ 0 sec is 1V.

50) Design a RLC circuit shown below on LTspice such that the output voltage is having a damping ratio (ζ): 0.25, damping frequency (ω_d): 1 rad/sec. Explain the design steps followed. Assume that the amplitude of voltage source for t ≥ 0 sec is 2V.



Hint: After solving for output voltage V_0, compare the obtained differential equation,

$D^2 + K_1 * D + K_2 = 0$ with $D^2 + 2\zeta\omega_n * D + {\omega_n}^2 = 0$, where damping frequency,

$\omega_d = \omega_n\sqrt{1 - \zeta^2}$ and find out the required values of R,L,C.

(Note: Instead of using a switch, try to give the input as a pulse signal with some finite delay(where the input is 0A/0V) and keep the ON period (T_{ON}) very large where the input amplitude is the value given in the question)

For Doubt Refer to Below TA

- Group 1-10: TA- Narendra Singh.
- Group 11-25: TA- Ravi Singh.
- Group 25-40: TA- Abhishek Goel.
- Group 41-50: TA- Jaya.