Tutorial 5: "Pipeline"

Q1: 3 staged Pipeline, delay 10, 20 and 40 ns. Assume no delay extra and no hazards. Assuming one instruction fetched every cycle, total execution time for 100 instructions?

Q2: 4 stage pipeline (5, 6, 11, 8 ns), 1 ns for register in between. Speed UP with and without pipeline.

Q3: 5 stage pipeline, F, D, FO, E, WO with 5 ns, 7 ns, 10 ns, 8 ns and 6 ns delays respectively. After each stage, pipeline register with delay 1 ns. We have a program:

I1, I2, I3, I4, I5…….I9

Instruction I3 is the only branch instruction, and its branch target is I7. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is?

Q4: 5 stage pipeline, register read is performed in EX stage, EX stage takes 1 cycle for ADD and 2 for MUL. Ignore pipeline register latencies. Consider below seq of instruction -

ADD, MUL, ADD, MUL, ADD

From the second instruction, all are data dependent on previous one, what is speed up with operand forwarding over without. [Draw Phase Diagram for both]

Q5: Pipelined System with 5-stage, IF, ID, FO, E and WB, each take 1 clock for any instruction except E stage. E stage takes 1 clock cycle for ADD and SUB instructions,3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Tell number of clock cycles system will take with and without operand forwarding?

Note: FO, is preferred to be performed just before E stage.

For below instructions:

Instruction	Meaning of instruction
I0 :MUL R2 ,R0 ,R1	R2 ¬ R0 *R1
I1 :DIV R5 ,R3 ,R4	R5 ¬ R3/R4
I2 :ADD R2 ,R5 ,R2	R2 ¬ R5+R2
I3 :SUB R5 ,R2 ,R6	R5 ¬ R2-R6

Q6: X1: Processor operating at 2GHz, 5 stage pipeline, CPI = 1, no pipeline hazards. We have a program P1, 30% instructions are branch, control hazard incur 2 cycle stalls for every branch. X2: processor operating at 2GHz but it has a Branch Prediction Unit, eliminates stalls for correct prediction. For wrong predictions no saving and no additional stalls. No structural and data hazards. BPU accuracy 80 %, speedup by X2 over X1

Q7: Non-Pipelined Processor, 5 clock cycle to complete an instruction with 2.5 GHz processor freq.

Now we are making a 5-stage pipeline, 2 GHz (due to pipeline overheads) processor operating freq.

The program we wish to run has 30 % memory, 60% ALU and the rest of the branch. 5% memory instructions cause stalls of 50 clock cycles each due to some reason and 50 % branch instructions cause stalls of 2. No stall for ALU, speed up??

Q8:
Q9:
Q10: