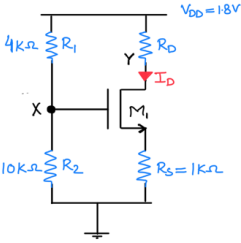


a.) Determine the bias current of M_1, shown in the figure above.

Given :-

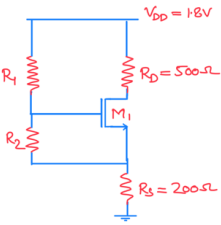
$V_{th} = 0.5V$
$\mu_n C_{ox} = 100\,\mu A/V^2$
$W/L = 5/0.18$

b) What is the maximum allowable value of R_D for M_1 to remain in saturation.

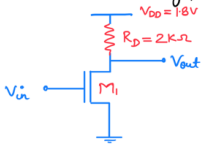
c.) Assume M_1 is in saturation and $R_D = 2.5K\Omega$, Now compute

(i) Maximum allowable value of W/L
(ii) Maximum allowable value of R_S with $W/L = 5/0.18$.

2.) Consider a circuit depicted in figure 2.1, where $W/L = 20/0.18$. Assuming the circuit flowing through R_2 is $1/10^{th}$ of I_{D_1}. Calculate the values of R_1 and R_2 so that $I_{D_1} = 0.5mA$.



3.) In the Common-Source stage, $W/L = 30/0.18$.



(i) What gate voltage yields a drain current of 0.5mA? (Verify that M_1 operates in saturation)

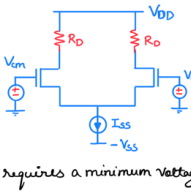
(ii) With such a drain bias, Calculate the voltage gain of the stage.

(iii) Assume, voltage gain of 5 with $W/L \leq 20/0.18$ Determine the required value of R_D, if the power dissipation must not exceed 1mW

4.) For a MOS differential pair with a common mode voltage (V_{cm}) applied as shown in the fig 4.1

Given :-

- $V_{DD} = V_{SS} = 1V$
- $(W/L)_1 = (W/L)_2 = 12.5$
- $\mu_n C_{ox} = 0.4mA/V^2$
- $V_{th} = 0.5V$
- $I_{SS} = 0.2mA$
- $R_D = 10K\Omega$



Assume current source (I_{SS}) requires a minimum voltage of 0.4V to operate properly

Calculate :-

a.) Find V_{GS} for each transistor.
b.) For $V_{cm} = 0$, find
(i) V_S
(ii) I_D
(iii) V_D
c.) What is the highest permitted value of V_{cm} for which M_1 and M_2 are in saturation?

5.) For the given MOS differential pair, both MOSFET are perfectly matched and following are the device parameters for both MOSFETs

- $V_{DD} = V_{SS} = 5V$
- $V_{th} = 0.5V$
- $\mu_n C_{ox}(W/L) = 4mA/V^2$
- $R_D = 6K\Omega$

Calculate Small Signal differential gain ?