ECN 104 – Digital Logic Design (Spring 2023)

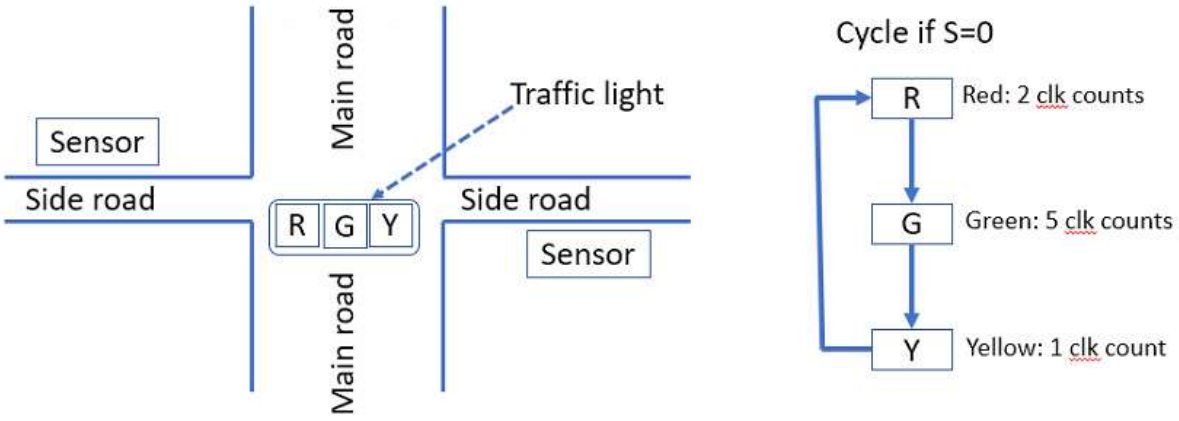
Tutorial 7 & 8 (Combined)

Full Marks – 40

Please solve this tutorial at least partially before coming to the tutorial session, since this is combined for two tutorials. You won't be able to finish it within 1hr of the in-class tutorial.

Question 1 10 Marks

The intersection in front of the ECE/CSE department at IIT Roorkee requires a new traffic light system. You have to design a digital logic for the traffic light to be placed on the main road. The system has three lights: Red, Green, Yellow. There are sensors on the side road that detects if any vehicle is approaching the intersection. If a vehicle is detected it provides a signal S=1 (else S=0)



Design the logic such that

a. The traffic light cycles from red to green to yellow and back to red continuously, ***as long as S=0***. It should stay red for 2 clock counts, green for 5 clock counts and yellow for 1 clock count.
b. If S=1, while the signal is green, it should go to yellow at the next clock trigger. If S=1, while the signal is either yellow or red, it should have no effect.

(a) Draw the state diagram. Define all your outputs, inputs and state variables. [5]

(b) Design the complete synchronous logic. You can use D-flip-flops, mux, demux, decoder etc. as black-boxes. Show all steps. [5]

Question 2: 5 Marks

Design a synchronous sequential circuit that can generate a signal with a frequency 3 times lower than the clock frequency. The output duty cycle need not be 50%.

Question 3: 5 Marks

Design a 2-bit synchronous sequential circuit that can count UP or DOWN depending on the input control signal. Show all steps.

Question 4: 5 Marks

What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?

Question 5: 5 Marks

Draw the logic diagram of a four-bit register with four D flip-flops and four 4 × 1 multiplexers with mode selection inputs s1 and s0. The register operates according to the following function table. (Follow the universal shift register structure)

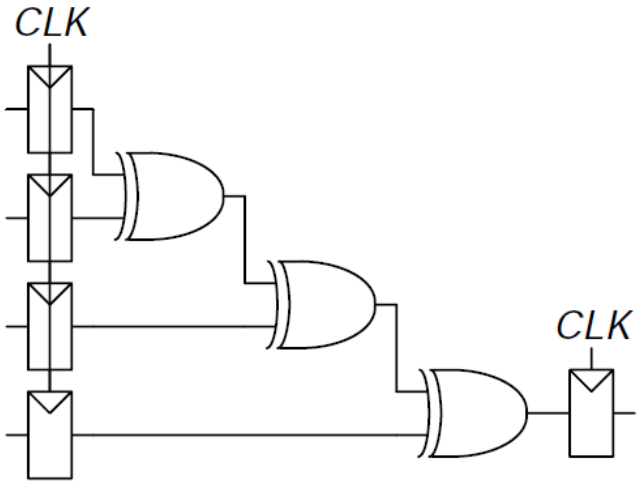
s_1	s_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

Question 6: 5 Marks

Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.

Question 7: 5 Marks

Calculate the maximum clock frequency that the following circuit can correctly operate at.



Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. Ignore the impact of clock skew.