Literatures Review About Spintronics

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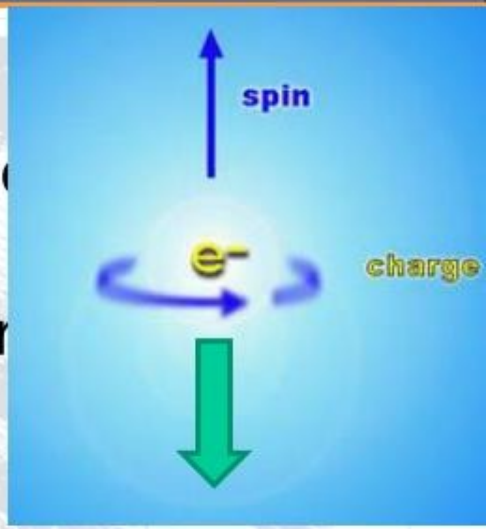
Apr. 10th

Main Papers

- Glenn Zorpette, The quest for the spin transistor. IEEE Spectrum. Vol. 38, Issue 12
- Claude Chappert, Albert Fert, Frederic Nguyen Van Dau, The emergence of spin electronics in data storage. Nature Materials 6, 813-823 (2007)
- Shoji Ikeda, Jun Hayakawa, Young Min Lee, Fumihiro Matsukura, Yuzo Ohno, Takahiro Hanyu, Magnetic tunnel junctions for spintronic memories and beyond. IEEE Transactions on Electron Devices, Vol. 54, issure 5, pp. 991-1002
- Daughton, J.M. Magnetic tunneling applied to memory. J. Appl. Phys. 81, 3758-3763
- Shoun Matsunaga, Jun Hayakawa, Shoji Ikeda, Katsuya Miura, Haruhiro Hasegawa, Tetsuo Endoh, Hideo Ohno, Takahiro Hanyu, Fabrication of a nonvolatile full adder based on logic-in-memory architecture using magnetic tunnel junctions. App. Phys. Express 1 (2008) 091301

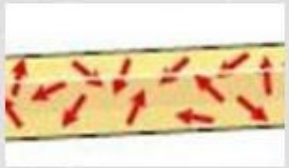
What is spintronics?

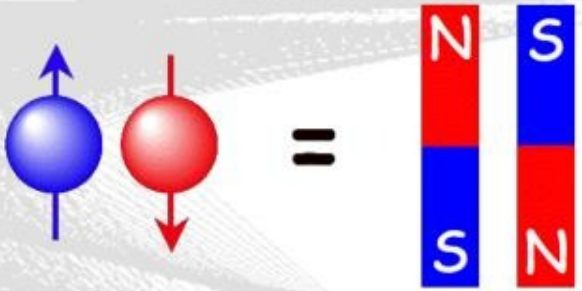


- **Spin**
  - The root cause of magnetism, intrinsic prope
    subatomic particles (fermions & bosons)
  - The angular momentum carried by an electr
    spin down
- **Spintronics**
  - Exploits the intrinsic spin of electrons, associated magnetic moment as well as charge in solid-state devices
  - Using spin to control the movement of charge
  - Using spin itself to store and process data without need to move charge at all
  - **Low power (change spin is 1/60 power of move it)**
  - **Non-volatility**

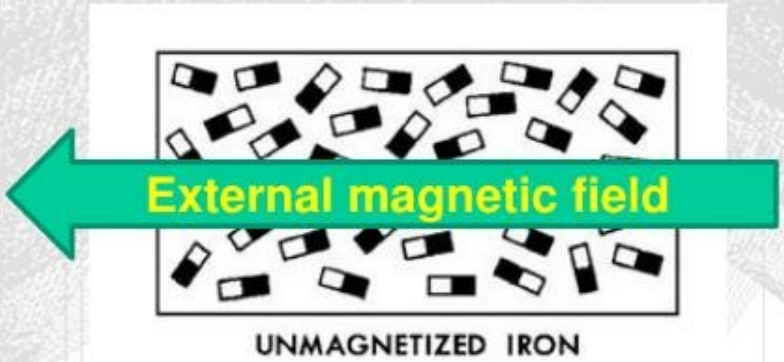
The Story Behind

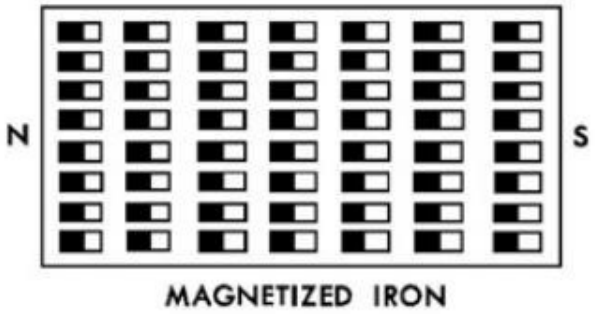
- **Spin->Magnetism**
  - Ordinary materials





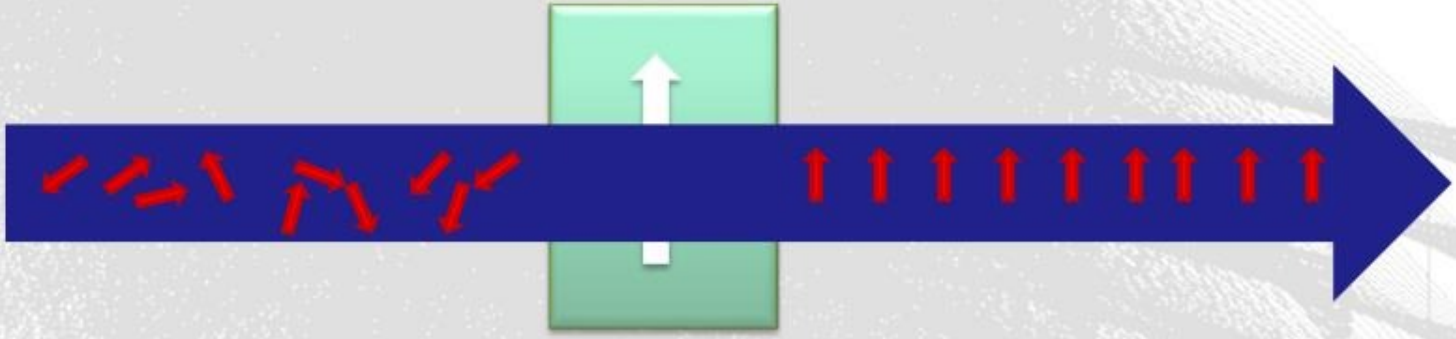
  - Ferromagnetic materials



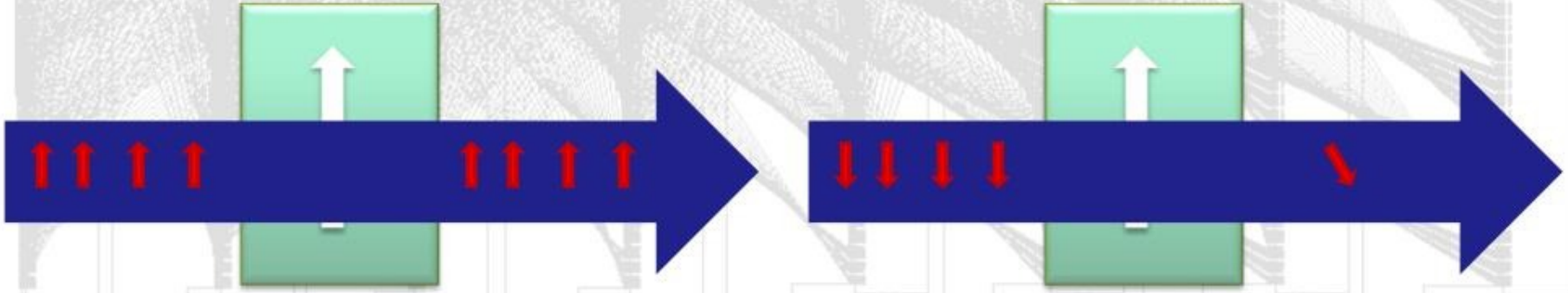


The Story Behind

- Ferromagnetic Materials' Role
  - Spin Polarizer

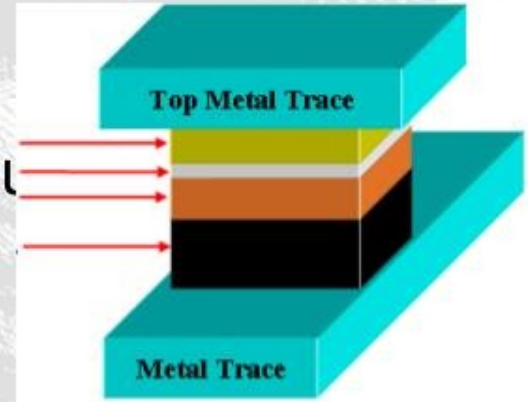


  - Spin Filter



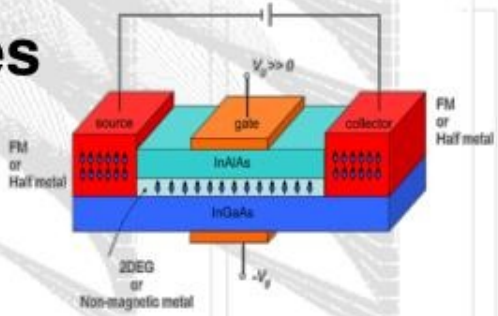
Spintronics Devices

- **Metal-based spintronics devices**
  - Ready for commercial product (successfu
    good yield, less process variation)
  - Used as memory devices in MRAM
  - Strong candidate for universal memory
  - logic design?



MTJ

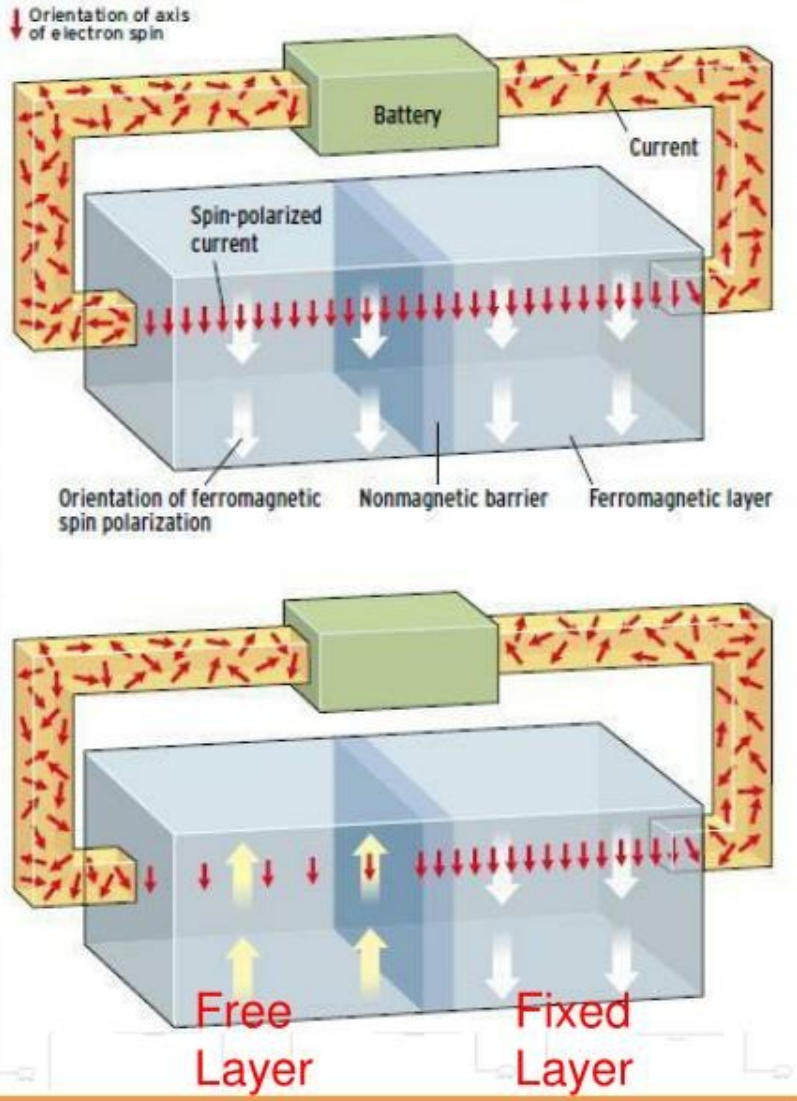
- **Semiconductor-based spintronics devices**
  - Build on semiconductor materials
  - Extra degree of freedom
  - No working devices has been reported…



Spin-FET

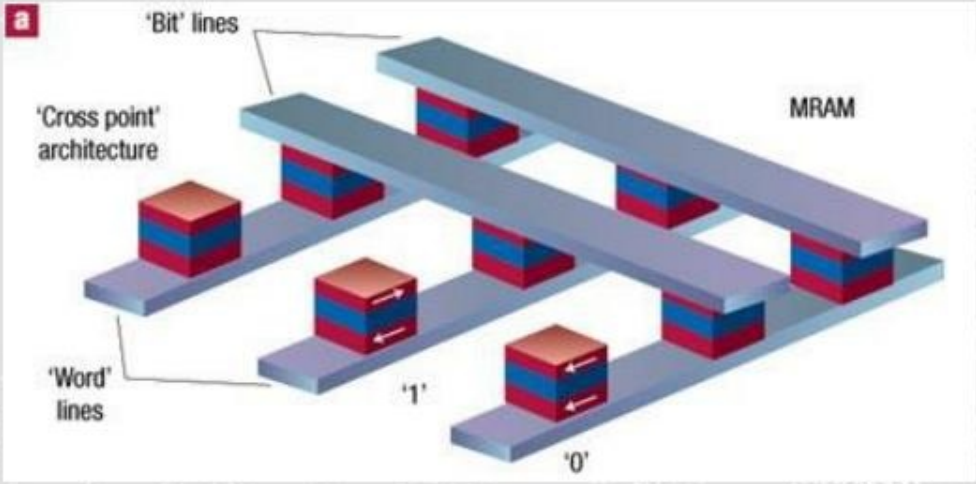
Magnetic Tunnel Junction

- **MTJ**
  - Two layers of ferromagnetic material separated by an extremely thin non-conductive barrier.
  - Parallel -> Low resistance
  - Anti-parallel -> High resistance
  - Speed? Power? Area? How to change data?



MRAM

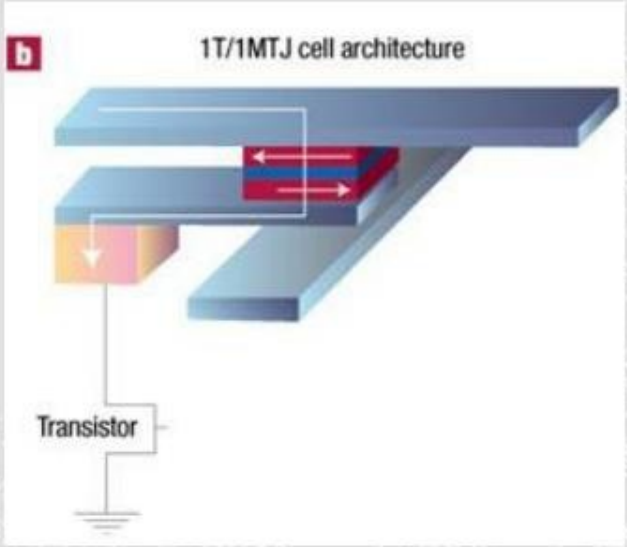
- **Cross-point Architecture**



  - The binary is recorded on the two opposite orientations of the magnetization of MTJ, which are connected to the crossing points of two perpendicular arrays of parallel conducting lines.
  - In principle, very high density
  - In practice, not good for fast reliable reading/writing

MRAM

- **1T-1MTJ**

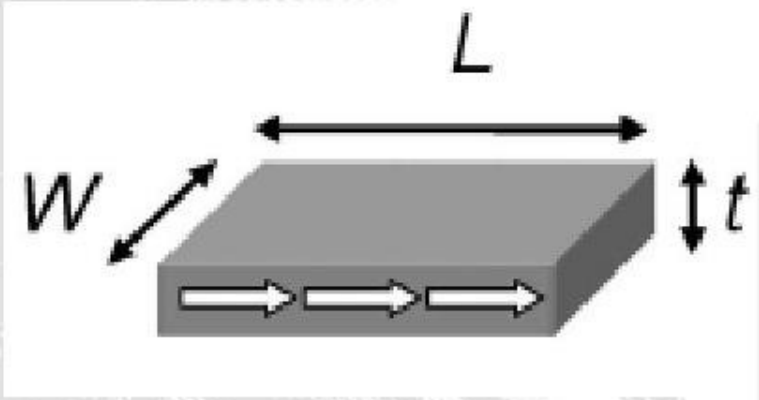


  - To remove the unwanted current paths around the direct one through the MTJ cell addressed for reading
- **Big Problem**
  - Current for writing can not be scaled down as dimension scales down

Writing Current

- **Magnetic Field Required to Switch The Free Layer (Hsw)**

$$Hsw = CM_s t/W + Hk$$

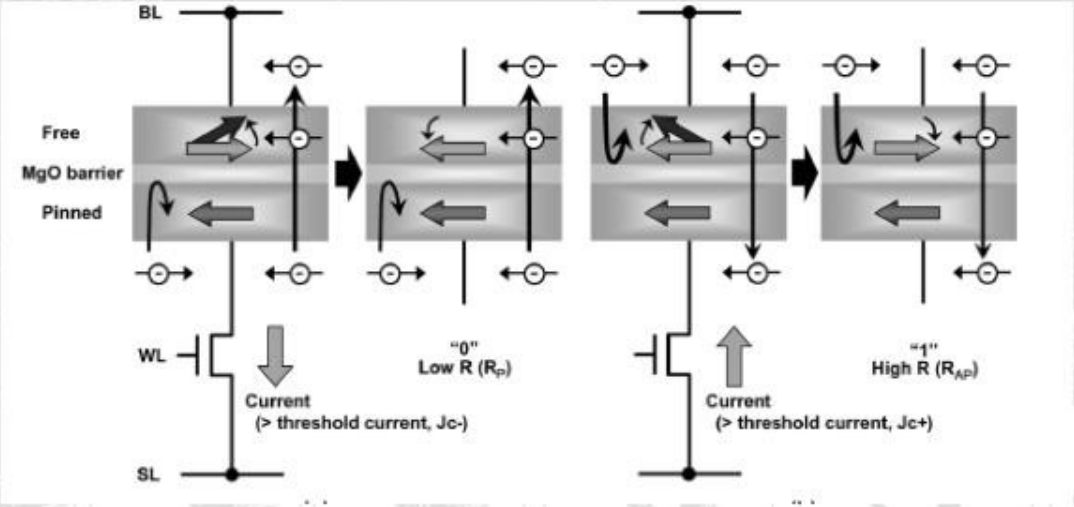


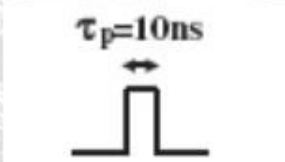
  - t, free layer thikness
  - w, free layer width
  - Ms, saturation magnetization
  - C, coefficient

  - No much room for reducing t, so Hsw increases with reduction of W.
  - Current need to generate Hsw also increases

Spin Torque Transfer

- **Predicted in 1996**
  - The magnetization orientation of a free magnetic layer could be controlled by direct transfer of spin angular momentum from a spin-polarized current.
- **Observed first in 2000**





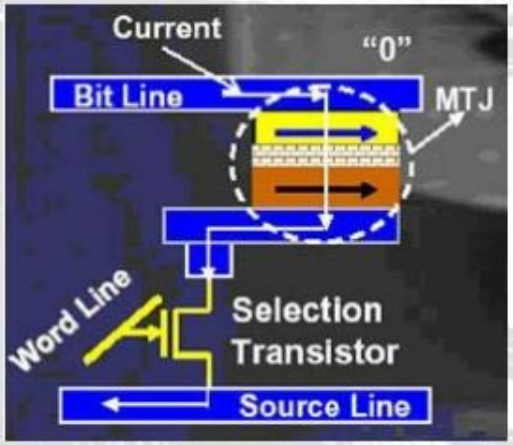
$J = I_{TMR} / A$
(A : Junction area)

Jc =5.8A/cm^2
(100uA/100nm gate width)
T_p = 2-10 ns

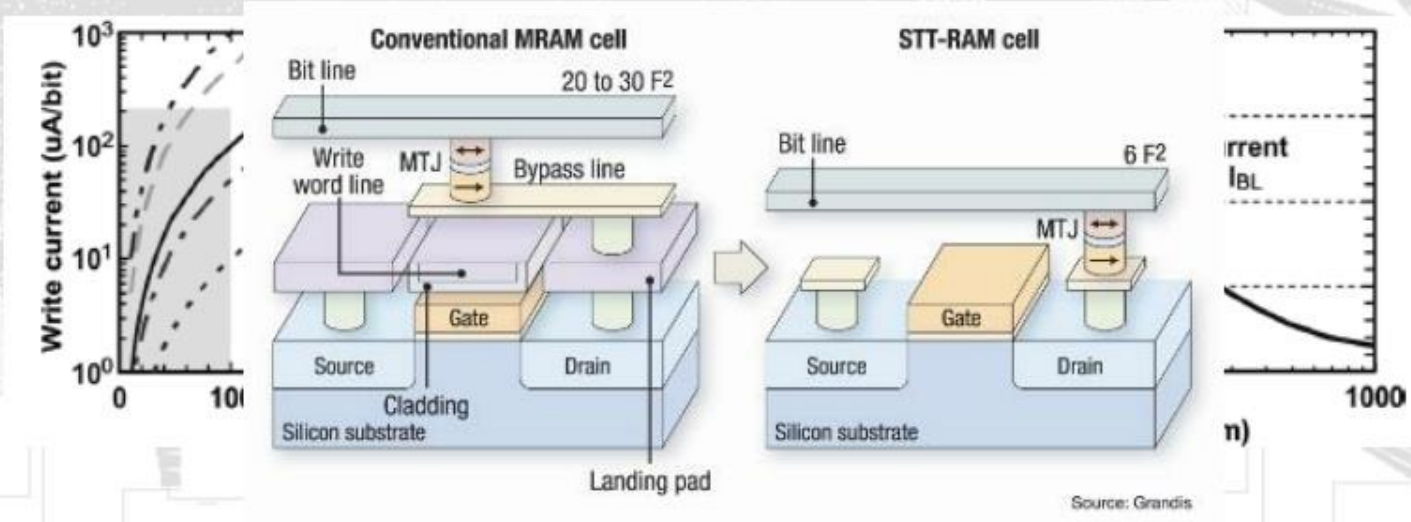
  - Current direction pushes the free layer to either have parallel or anti-parallel spin

STT-RAM

- **STT-RAM**
  - Remove the data line
  - Writing current is proportional to cell size



- **STT-RAM vs. MRAM**



STT-RAM

- **1T-4MTJ**

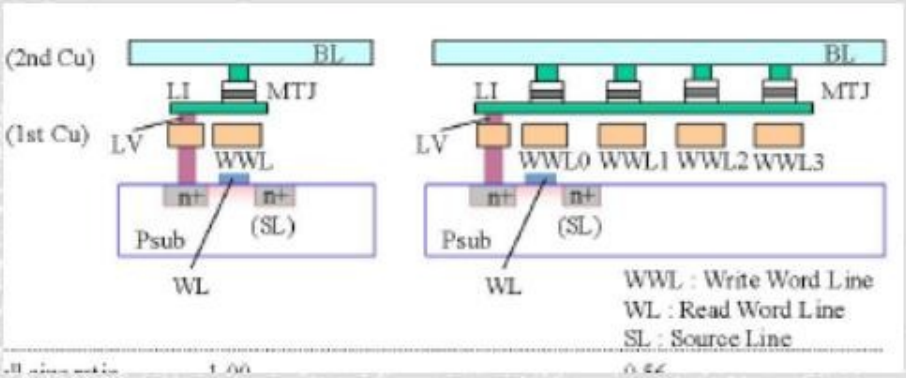


Table 1 Technology features of 1Mb-MRAM test chip.

Technology	130nm CMOS, 4Level Cu technology 1T – 4MTJ memory cell
Cell size	3.24 μm^2 / 4 bit
MTJ size	0.26 x 0.44 μm^2
Core Size	1.431 x 2.820 = 4.04 mm^2
Supply Voltage	1.5 V only
Organization	64K word x 16 bit
Operating Frequency (read/write)	50MHz@4 cycle 2nd read time=15.0nsec

- Some one also proposed 1T-2MTJ and 1T-4MTJ structure to increase density.
- All these cases increased density at expense of smaller signal amplitude (smaller noise margin) and slower read.

Comparison

	Standard MRAM (90 nm)*	DRAM (90 nm)†	SRAM (90 nm)†	SMT-MRAM (90 nm)*	FLASH (90 nm)†	FLASH (32 nm)†	SMT-MRAM (32 nm)*
Cell size (μm^2)	0.25 256 Mb/cm	0.25 256 Mb/cm	1–1.3 64 Mb/cm	0.12 512 Mb/cm	0.1 512 Mb/cm	0.02 2.5 Gb/cm	0.01 5 Gb/cm
Read time	10 ns	10 ns	1.1 ns	10 ns	10–50 ns	10–50 ns	1 ns
Program time	5–20 ns	10 ns	1.1 ns	10 ns	0.1–100 ms	0.1–100 ms	1 ns
Program energy per bit	120 pJ	5 pJ Needs refresh	5 pJ	0.4 pJ	30–120 nJ	10 nJ	0.02 pJ
Endurance	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$ read, $>10^{6}$ write	$>10^{15}$ read, $>10^{6}$ write	$>10^{15}$
Nonvolatility	yes	no	no	yes	yes	yes	yes

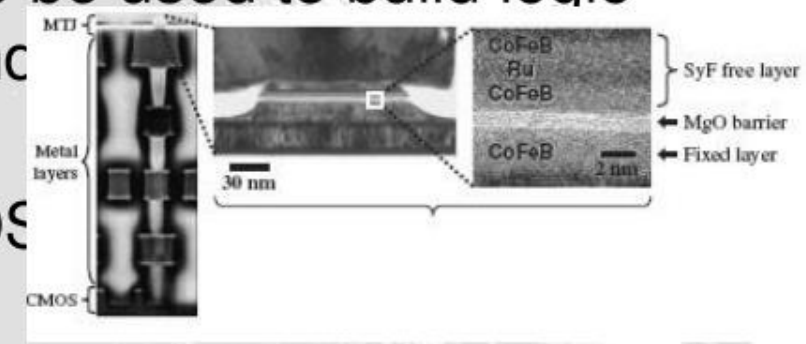
Source:-IBM

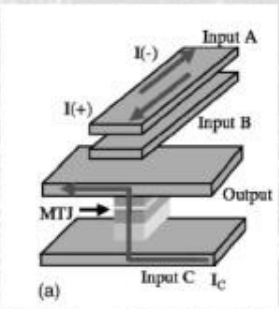
35Billion $

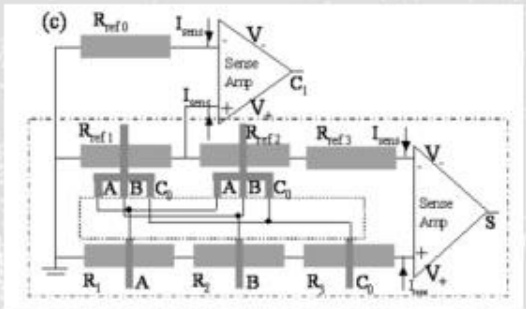
Ajey Jacob, Intel

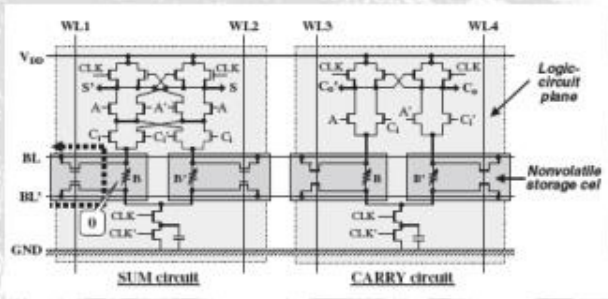
MJT for Logic Design

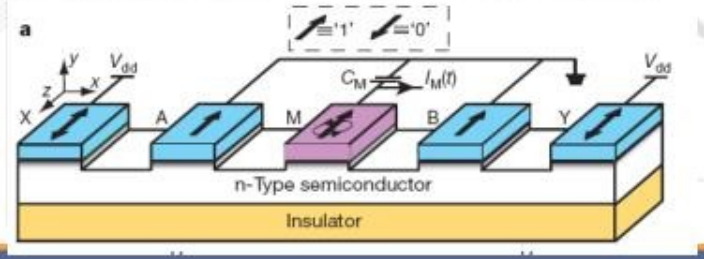
- **Why MTJ?**
  - Any memory device can also be used to build logic circuits, in theory at least, and
  - It is CMOS friendly
  - It can sitting on top the CMOS functional interconnect





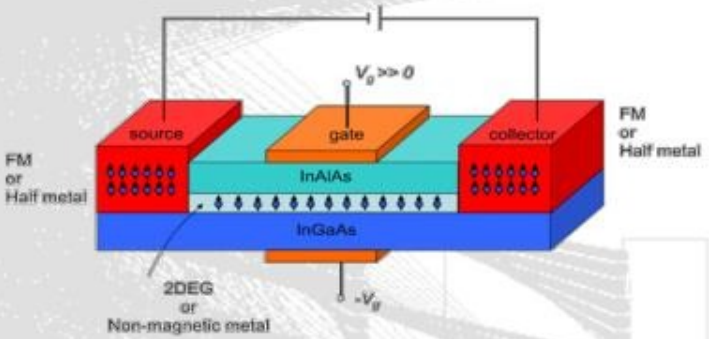






Semiconductor-Based Spintronics Devices

- **Spin-FET**
  - Extra degree of freedom
  - Resonant tunneling
  - Polarized laser beam

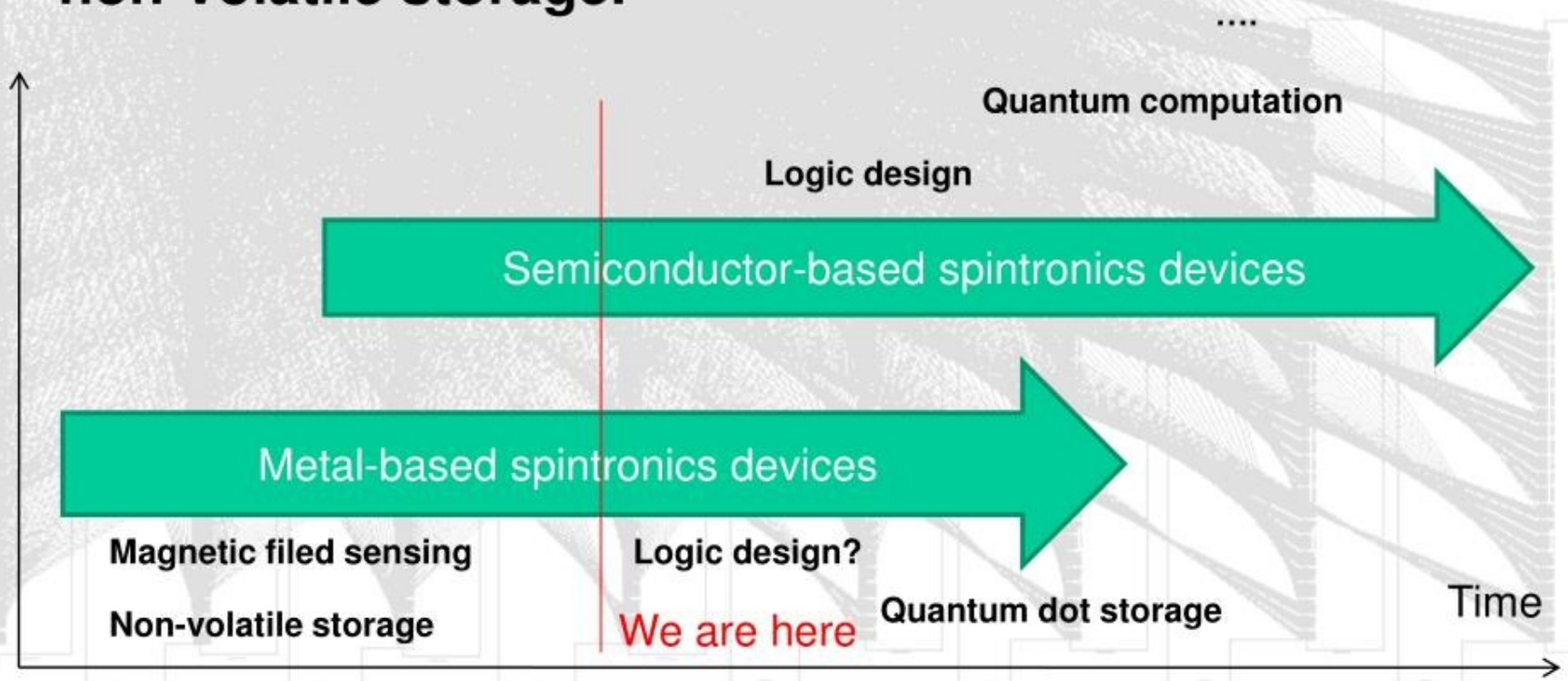


Spin-FET

- **Why no working Spin-FET?**
  - Spin injection rate is so low
  - Electrons will lose its spin direction when pass through the interface of metal and semiconductor due to the mismatch of conductivity
  - Injection of spin-polarized current in hybrid ferromagnetic-semiconductor systems at room temperature is being constantly improved

Where are we?

- **Till now, spintronics is realized only in all-metallic systems for applications in magnetic field sensing and non-volatile storage.**




Thanks