ECN 104

Digital Logic Design

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Question 1

- Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is:

(A) 0,1,3,7,15,14,12,8,0

(B) 0,1,3,5,7,9,11,13,15,0

(C) 0,2,4,6,8,10,12,14,0

(D) 0,8,12,14,15,7,3,1,0

Question 2

- A binary operation is defined by the following truth table, which of the below is true about the operator?

(A) Both commutative and associative

(B) Commutative but not associative

(C) Not commutative but associative

(D) Neither commutative nor associative

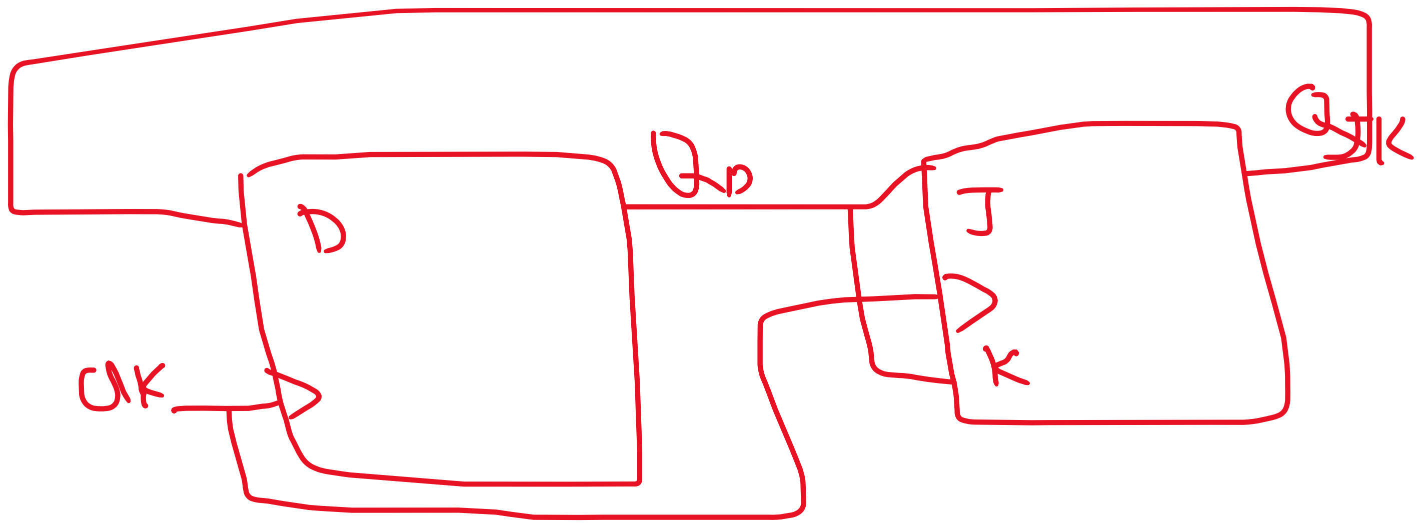
p	q	$p \neq q$
0	0	0
0	1	1
1	0	1
1	1	0

Commutative: A (op) B = B (op) A

Associative: A (op) [B (op) C] = [A (op) B] (op) C

Question 3

- Consider the following circuit:



- Initially, Qd = 1, Qjk = 0. What is the sequence that is generated (including the initial state) at the output Qjk

(A)0110110… (B) 0100100… (C) 011101110…

(D) 011001100…

Question 4

- Calculate the total propagation time of a 4-bit binary adder.

Question 5

- Given the function $F = P' + QR$, where F is a function of three Boolean variables P, Q and R. Which one of the below are the correct representation(s) of F?

$$F = \sum 4,5,6$$

$$F = \sum 0,1,2,3,7$$

$$F = \prod 4,5,6$$

$$F = \prod 0,1,2,3,7$$

Question 6

- Find the total number of prime implicants of the function $f(w, x, y, z) = \sum 0,2,4,5,6,10$

Question 7

Consider the Boolean operator # with the following properties: $x\#0 = x$, $x\#1 = \bar{x}$, $x\#x = 0$ and $x\#\bar{x} = 1$. Then $x\#y$ is equivalent to

(A) $x\bar{y} + \bar{x}y$

(B) $x\bar{y} + \bar{x}\bar{y}$

(C) $\bar{x}y + xy$

(D) $xy + \bar{x}\bar{y}$

Question 8

The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is __________ .

Question 9

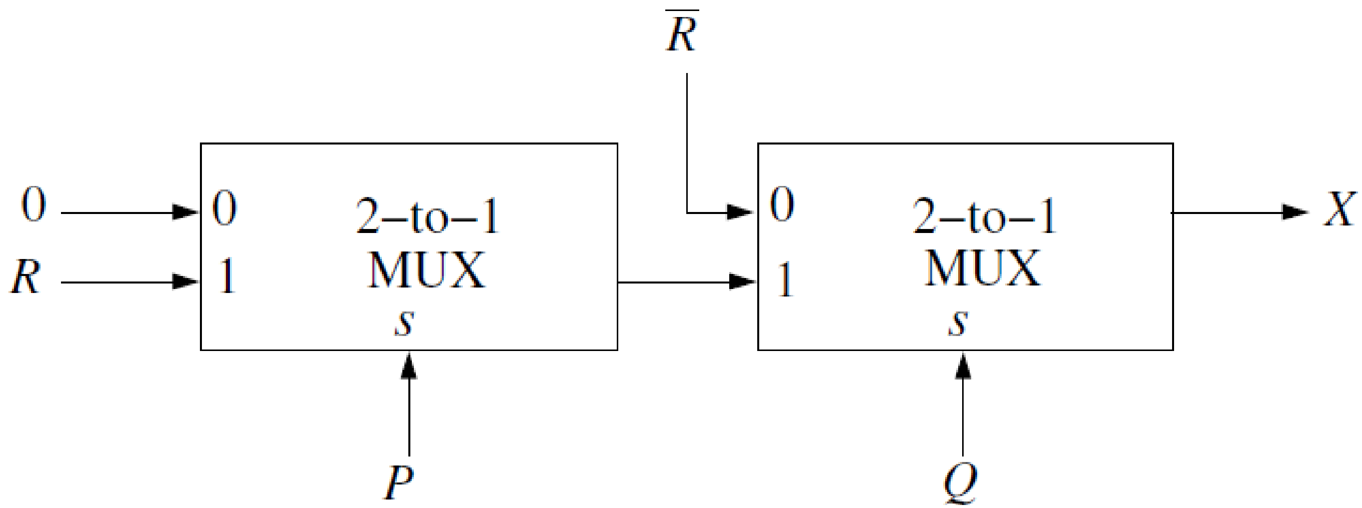
We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is __________ .

Question 10

A processor can support a maximum memory of 4 GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least ___________ bits.

Question 11

Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



The minimal sum of products form of the output X is

(A) $\bar{P}\bar{Q}+PQR$

(B) $\bar{P}Q+QR$

(C) $PQ+\bar{P}\bar{Q}R$

(D) $\bar{Q}\bar{R}+PQR$

Question 12

Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is __________ .

Question 13

Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and $\oplus$ is the XOR operator. Which one of the following must always be **TRUE**?

(A) $x_1 x_2 x_3 x_4 = 0$

(B) $x_1 x_3 + x_2 = 0$

(C) $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$

(D) $x_1 + x_2 + x_3 + x_4 = 0$

Question 14

Let X be the number of distinct 16-bit integers in 2's complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation.

Then $X - Y$ is ___________ .

Question 15

When two 8-bit numbers $A_7 \cdots A_0$ and $B_7 \cdots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a **ripple-carry adder**, the sum bits obtained are $S_7 \cdots S_0$ and the carry bits are $C_7 \cdots C_0$. An overflow is said to have occurred if

(A) the carry bit C_7 is 1

(B) all the carry bits $(C_7, \cdots, C_0)$ are 1

(C) $(A_7 \cdot B_7 \cdot \overline{S_7} + \overline{A_7} \cdot \overline{B_7} \cdot S_7)$ is 1

(D) $(A_0 \cdot B_0 \cdot \overline{S_0} + \overline{A_0} \cdot \overline{B_0} \cdot S_0)$ is 1

Question 16

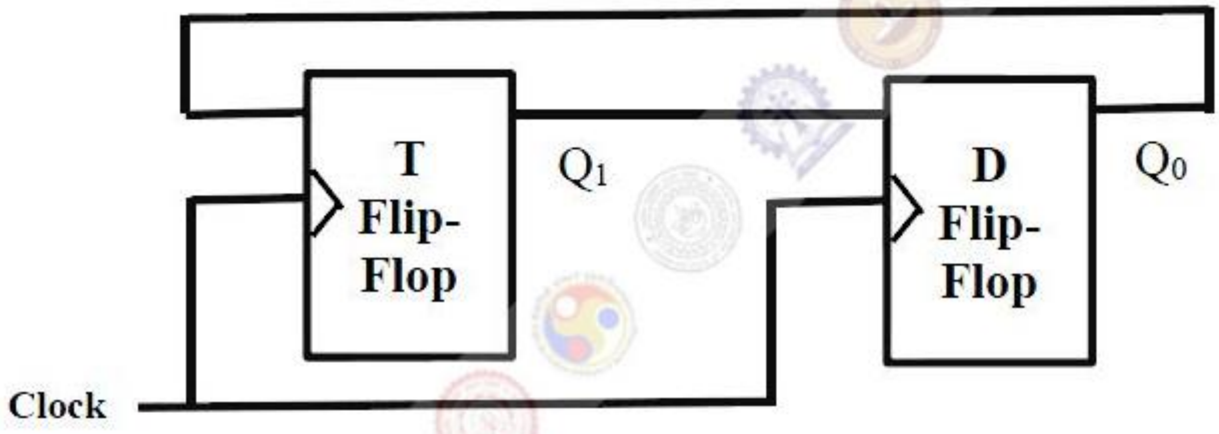
Consider the Karnaugh map given below, where X represents "*don't care*" and blank represents 0.

$dc \backslash ba$	00	01	11	10
00		x	x	
01	1			x
11	1			1
10		x	x	

Assume for all inputs (a, b, c, d), the respective complements ($\overline{a}, \overline{b}, \overline{c}, \overline{d}$) are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is ________________.

Question 17

Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

(A) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 00 respectively

(B) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 01 respectively

(C) $Q_1 Q_0$ after the 3rd cycle are 00 and after the 4th cycle are 11 respectively

(D) $Q_1 Q_0$ after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

Question 18

If w, x, y, z are Boolean variables, then which one of the following is INCORRECT?

(A) $wx + w(x + y) + x(x + y) = x + wy$
(B) $\overline{w\bar{x}(y + \bar{z})} + \bar{w}x = \bar{w} + x + \bar{y}z$
(C) $(w\bar{x}(y + x\bar{z}) + \bar{w}\bar{x})y = x\bar{y}$
(D) $(w + y)(wxy + wyz) = wxy + wyz$

Question 19

Given $f(w,x,y,z) = \sum_m(0,1,2,3,7,8,10) + \sum_d(5,6,11,15)$, where d represents the *don't-care* condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of $f(w,x,y,z)$?

(A) $f = (\bar{w} + \bar{z})(\bar{x} + z)$

(B) $f = (\bar{w} + z)(x + z)$

(C) $f = (w + z)(\bar{x} + z)$

(D) $f = (w + \bar{z})(\bar{x} + z)$

Question 20

Consider a binary code that consists of only four valid codewords as given below:

$$00000, 01011, 10101, 11110$$

Let the minimum Hamming distance of the code be p and the maximum number of erroneous bits that can be corrected by the code be q. Then the values of p and q are

(A) p=3 and q=1
(B) p=3 and q=2
(C) p=4 and q=1
(D) p=4 and q=2

Question 21

The next state table of a 2-bit saturating up-counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expressions for T_1 and T_0 are

(A) $T_1 = Q_1 Q_0,\quad T_0 = \bar{Q}_1 \bar{Q}_0$

(B) $T_1 = \bar{Q}_1 Q_0,\quad T_0 = \bar{Q}_1 + \bar{Q}_0$

(C) $T_1 = Q_1 + Q_0,\quad T_0 = \bar{Q}_1 + \bar{Q}_0$

(D) $T_1 = \bar{Q}_1 Q_0,\quad T_0 = Q_1 + Q_0$

Question 22

Let $\oplus$ and $\odot$ denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT CORRECT?

(A) $\overline{P \oplus Q} = P \odot Q$

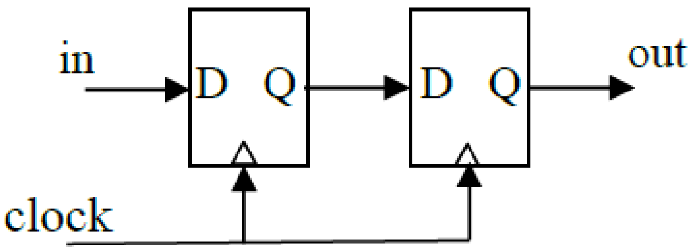
(B) $\bar{P} \oplus Q = P \odot Q$

(C) $\bar{P} \oplus \bar{Q} = P \oplus Q$

(D) $(P \oplus \bar{P}) \oplus Q = (P \odot \bar{P}) \odot \bar{Q}$

Question 23

Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.



The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of “in” is _____.

Question 24

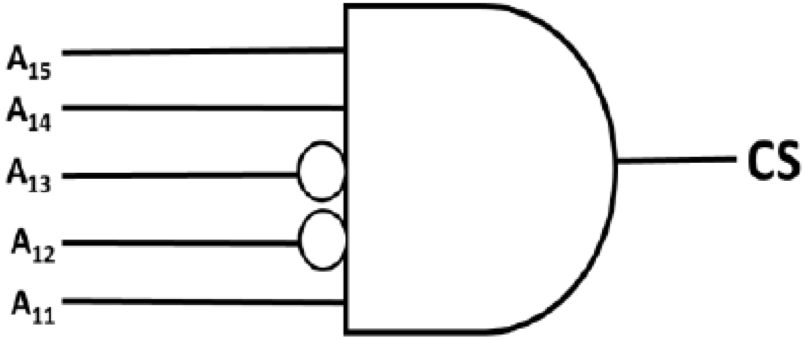
Consider the minterm list form of a Boolean function F given below.

$$F(P,Q,R,S) = \sum m(0,2,5,7,9,11) + d(3,8,10,12,14)$$

Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is ______.

Question 25

The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0. What is the range of addresses (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?



(A) C800 to CFFF

(B) CA00 to CAFF

(C) C800 to C8FF

(D) DA00 to DFFF

Question 26

Consider Z = X – Y, where X, Y and Z are all in sign-magnitude form. X and Y are each represented in n bits. To avoid overflow, the representation of Z would require a minimum of:

(A) n bits
(B) $n - 1$ bits
(C) $n + 1$ bits
(D) $n + 2$ bits

Question 27

What is the minimum number of 2-input NOR gates required to implement a 4-variable function expressed in sum-of-minterms form as $f = \sum (0, 2, 5, 7, 8, 10, 13, 15)$? Assume that all the inputs and their complements are available. Answer: ________________.

Question 28

In 16-bit 2's complement representation, the decimal number −28 is:

(A) 1111 1111 0001 1100

(B) 0000 0000 1110 0100

(C) 1111 1111 1110 0100

(D) 1000 0000 1110 0100

Question 29

Which one of the following is NOT a valid identity?

(A) $(x \oplus y) \oplus z = x \oplus (y \oplus z)$

(B) $(x + y) \oplus z = x \oplus (y + z)$

(C) $x \oplus y = x + y$, if $xy = 0$

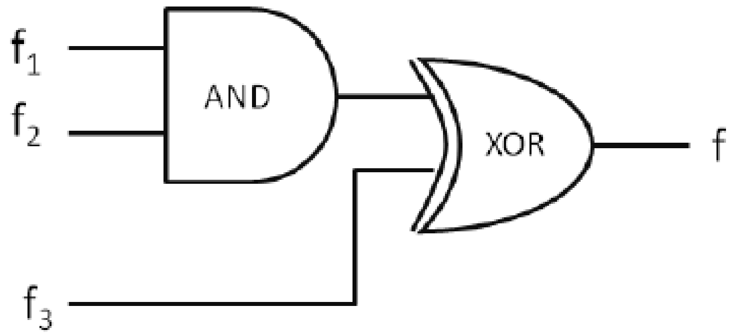
(D) $x \oplus y = (xy + x'y')'$

Question 30

Consider three 4-variable functions f_1, f_2, and f_3, which are expressed in sum-of-minterms as

$$f_1 = \sum (0, 2, 5, 8, 14), \qquad f_2 = \sum (2, 3, 6, 8, 14, 15), \qquad f_3 = \sum (2, 7, 11, 14)$$

For the following circuit with one AND gate and one XOR gate, the output function f can be expressed as:



(A) $\sum (7, 8, 11)$
(B) $\sum (2, 7, 8, 11, 14)$
(C) $\sum (2, 14)$
(D) $\sum (0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$

Question 31

If there are m input lines and n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of $m + n$ is ____ .

Question 32

Suppose we want to design a synchronous circuit that processes a string of 0's and 1's. Given a string, it produces another string by replacing the first 1 in any subsequence of consecutive 1's by a 0. Consider the following example.

Input sequence:	00100011000011100
Output sequence:	00000001000001100

A *Mealy Machine* is a state machine where both the next state and the output are functions of the present state and the current input.
The above mentioned circuit can be designed as a two-state Mealy machine. The states in the Mealy machine can be represented using Boolean values 0 and 1. We denote the current state, the next state, the next incoming bit, and the output bit of the Mealy machine by the variables s, t, b and y respectively.
Assume the initial state of the Mealy machine is 0.

What are the Boolean expressions corresponding to t and y in terms of s and b?

$t = s + b$
$y = s\,b$

$t = b$
$y = s\,b$

$t = b$
$y = s\,\overline{b}$

$t = s + b$
$y = s\,\overline{b}$

Question 33

Consider a Boolean function $f(w, x, y, z)$ such that

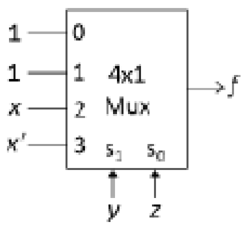
$$\begin{aligned} f(w,0,0,z) &= 1 \\ f(1,x,1,z) &= x+z \\ f(w,1,y,z) &= wz+y \end{aligned}$$

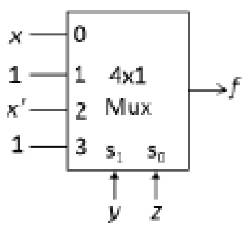
The number of literals in the minimal sum-of-products expression of f is __________.

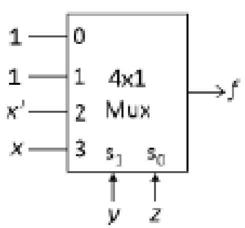
Question 34

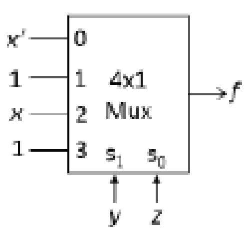
Which one of the following circuits implements the Boolean function given below?

$$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6,\ \text{where } m_i \text{ is the } i^{th} \text{ minterm.}$$









Question 35

Consider the following Boolean expression.

$$F = (X + Y + Z)(\overline{X} + Y)(\overline{Y} + Z)$$

Which of the following Boolean expressions is/are equivalent to $\overline{F}$ (complement of F)?

$(\overline{X} + \overline{Y} + \overline{Z})(X + \overline{Y})(Y + \overline{Z})$

$X\overline{Y} + \overline{Z}$

$(X + \overline{Z})(\overline{Y} + \overline{Z})$

$X\,\overline{Y} + Y\,\overline{Z} + \overline{X}\,\overline{Y}\,\overline{Z}$

Question 36

Assume that a 12-bit Hamming codeword consisting of 8-bit data and 4 check bits is $d_8d_7d_6d_5c_8d_4d_4d_3d_2c_4d_1c_2c_1$, where the data bits and the check bits are given in the following tables:

Data bits							
d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1
1	1	0	x	0	1	0	1

Check bits			
c_8	c_4	c_2	c_1
y	0	1	0

Which one of the following choices gives the correct values of x and y?

x is 0 and y is 0.

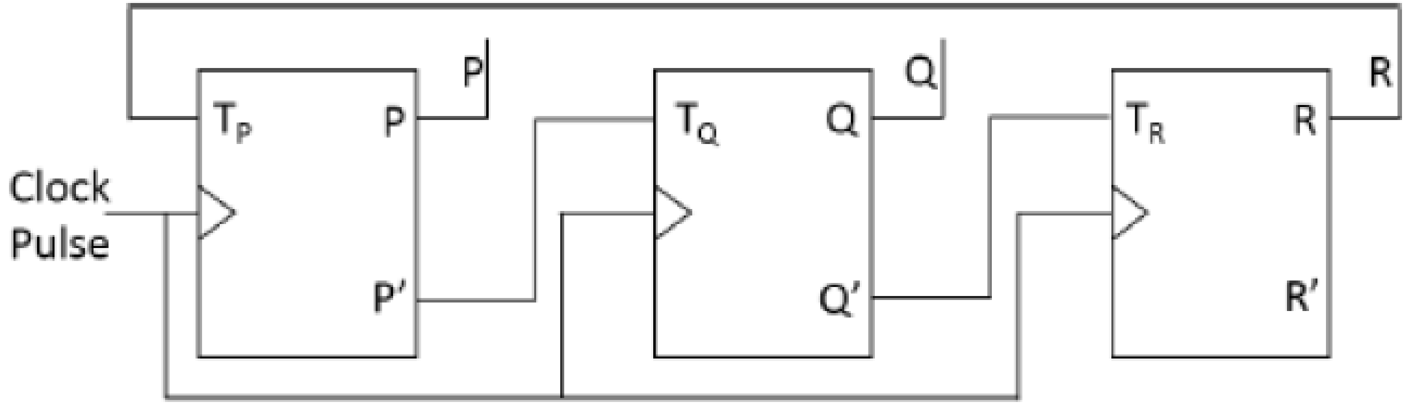
x is 0 and y is 1.

x is 1 and y is 0.

x is 1 and y is 1.

Question 37

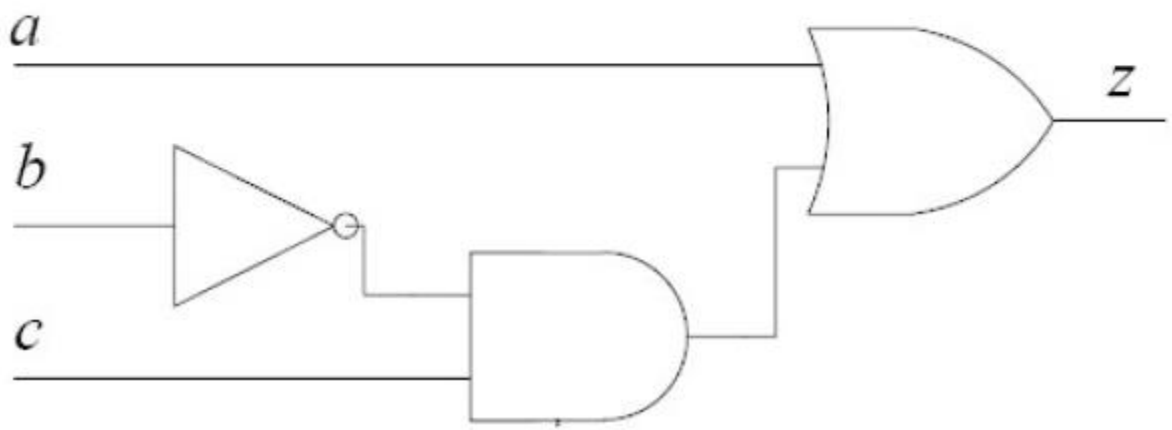
Consider a 3-bit counter, designed using T flip-flops, as shown below:



Assuming the initial state of the counter given by PQR as 000, what are the next three states?

Question 38

Consider the Boolean function $z(a, b, c)$.



Which one of the following minterm lists represents the circuit given above?

$z = \sum(0, 1, 3, 7)$

$z = \sum(1, 4, 5, 6, 7)$

$z = \sum(2, 4, 5, 6, 7)$

$z = \sum(2, 3, 5)$

Question 39

Let the representation of a number in base 3 be 210. What is the hexadecimal representation of the number?

Question 40

A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The minimum number of select lines needed for the multiplexer is ___________.

Question 41

Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. For the operation R1+R2, which one of the following values of R1 and R2 gives an arithmetic overflow?

R1 = 1011 and R2 = 1110

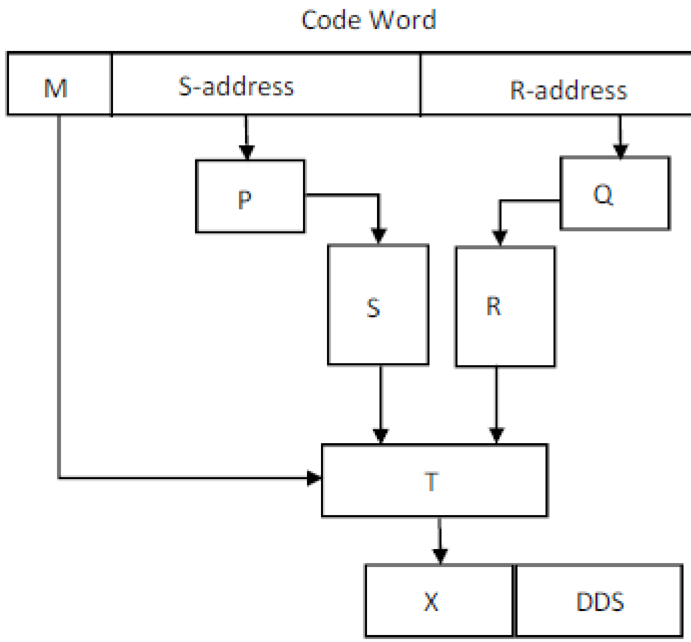
R1 = 1100 and R2 = 1010

R1 = 0011 and R2 = 0100

R1 = 1001 and R2 = 1111

Question 42

Consider a digital display system (DDS) shown in the figure that displays the contents of register X. A 16-bit code word is used to load a word in X, either from S or from R. S is a 1024-word memory segment and R is a 32-word register file. Based on the value of mode bit M, T selects an input word to load in X. P and Q interface with the corresponding bits in the code word to choose the addressed word. Which one of the following represents the functionality of P, Q, and T?



P is 10:1 multiplexer;	Q is 5:1 multiplexer;	T is 2:1 multiplexer
P is $10:2^{10}$ decoder;	Q is $5:2^{5}$ decoder;	T is 2:1 encoder
P is $10:2^{10}$ decoder;	Q is $5:2^{5}$ decoder;	T is 2:1 multiplexer
P is 1:10 de-multiplexer;	Q is 1:5 de-multiplexer;	T is 2:1 multiplexer