Department of Electronics and Communication, IIT Roorkee

ECN 104 – Digital Logic Design. End-term Exam, Spring 2023

Full Marks = 60; Time: 3 hours

Question 1 – 10 Marks

(a) Which is the gate ideally suited for bit comparison? Write down the correct option(s): (P) Two input XNOR (Q) Two input XOR (R) Two input NAND (S) Two input NOR. [1 Mark]

(b) If both NMOS and PMOS transistors of CMOS logic design are in OFF condition, the output is: (P) 1 or Vdd or HIGH state (Q) 0 or ground or LOW state (R) High impedance, Z or floating state (S) None of these [1 Mark]

(c) Draw the circuit for an inverter using TTL. [1 mark]
How many additional transistors are required for this TTL-inverter compared to a CMOS inverter? Why are so many transistors required? [1 mark]

(d) Why is CMOS preferred over TTL? [1 mark]

(e) How a monostable multi-vibrator is different from an astable multi-vibrator? Explain by drawing input/output waveforms. [1 Mark]

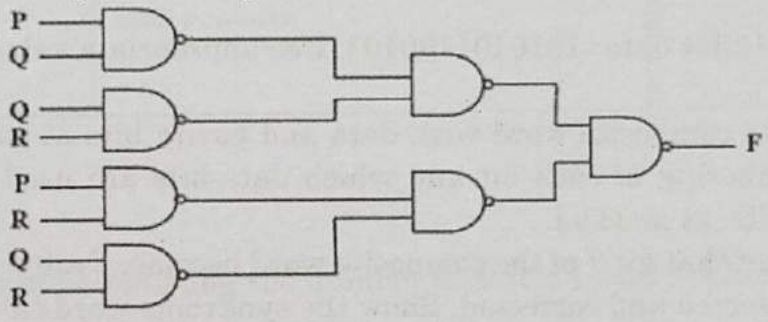
(f) Implement the function Y = (a+b)(c+d) using NOR-NOR network using minimum number of 2-input NOR gates. [1 Mark]

(g) Consider the equation $(43)_X = (Y3)_8$ where X and Y are unknown. How many solutions are possible? [2 Marks]

(h) Which logic gates are known as universal gates and why? [1 Mark]

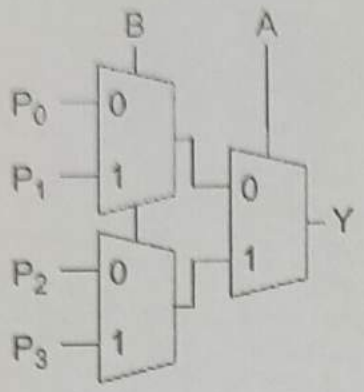
Question 2 – 7 Marks

(a) What is the Boolean expression for the output **F** of the combinational logic circuit of NAND gates given below: [2.5 Marks]



(b) Minimize the Boolean function $F(A,B,C,D) = \Sigma m$ (0, 1, 2, 5, 7, 8, 9, 10, 13, 15) [2.5 Marks]

(e) Consider below circuit. Let $P_0 = P_3 = 0$. Let $P_1 = P_2 = 1$. A and B are binary numbers. As you know, there are four combinations of A and B values. The value of Y will be equal to which of the following operations? Hint: make a truth-table of above circuit and then see which operation is achieved. Clearly show your solution steps. [2 Marks]



(P) AND(A,B)

(Q) OR(A,B)

(R) NOR(A,B)

(S) NAND(A,B)

(T) XOR(A,B)

(U) none of these

Question 3 – 6 Marks

(a) Implement the function $F(P,Q,R,S,T) = (P+Q)S + (R+T)\bar{S}$ using two 2:4 decoders. Assume the decoders have *enable* input. You may use extra OR gates. [3 Marks]

(b) Design a priority encoder that takes a 4 bit input A[3:0] and produces one two bit output Y[1:0] that denote the position of the first non-zero MSB in the input combination. Y should be zero if none of the input bits are one. Write down the truth table of the circuit and derive the minimized logic equations needed to implement this circuit. [3 Marks]

Question 4 – 5 Marks

(a) How many parity check bits must be included with the data word to achieve single error correction and double-error detection when the data word contains 390 data bits. [0.5 Mark]

(b) We have a 13-bit data: 1010101100101. Use appropriate value of k parity bits to protect the data.

i. Show the composite word with data and parity bits at suitable location. Also show the numbering of each bit and which data-bits are used for computation of which parity bits. [2 marks.]

ii. Assuming that bit 7 of the composite word becomes faulty, show how the error in this bit is detected and corrected. Show the syndrome word calculation clearly. [2 mark.]

iii. Add an extra parity bit to detect double-errors. Assume that 2nd and 5th bit of the composite word become faulty. Show how the double error is detected. [0.5 mark.]

Question 5 – 8 Marks

(a) What coding style (behavioral/dataflow/structural/hybrid etc.) does the code snippet below represent and why? What digital logic system does this code represent (Assume *halfadd* entity is already defined as a half-adder) ? [1 mark]

```
...
...
label1: halfadd port map (a=>a, b=>b,sum=>s1, carry=>s2);
label2: halfadd port map (a=>s1, b=>cin, sum=>sum, carry=>s3);
cout<=s3 OR s2;
...
```

(b) Write a behavioral version of the code in (a). Keep port names (i/o) same as in (a). Entity/Architecture declarations are not required. [3 marks]

(c) What does the following codes represent? [2 marks]

(i)
```
component abcd
  port( in1, in2: in std_logic;
        output: out std_logic);
end component;
```

(ii)
```
port (inp1: in std_logic_vector(7 downto 0);
```

(d) What is the difference between the codes for D-flipflops given below. (clk is the clock input and D is the data input. Q is the output)? [2 marks]

```
...
...
process(clk,reset)
  if (reset='1') then
    Q<=0;
  elsif(clk'event and clk='1')
    Q<=D;
  endif
end process
...
```

```
...
...
process(clk)
  if reset='1' then
    Q<=0;
  elsif(clk'event and clk='1')
    Q<=D;
  endif
end process
...
```

```
...
...
process(clk)
  if(clk'event and clk='1')
    if (reset='1') then
      Q<=0
    else
      Q<=D;
  endif
end process
...
```

Question 6 – 8 Marks

(a) Show the state table after reducing the number of states in the table below. [1 mark]

	Next state		Output	
Present State	x=0	x=1	x=0	x=1
p	t	v	1	0
q	r	t	0	1
r	s	q	1	1
s	p	u	0	0
t	s	q	1	0
u	t	v	1	0
v	r	t	0	1

(b) Design a detector which detects 1011 pattern in a binary string. For example,

Input : 101101100101101

Output: 000100000000100

You have to show the finite state machine state diagram, then assign binary encoding to each state, then state table, then show the overall circuit clearly showing the input to each flip-flop and the output signal. You can use either D or JK flip-flop. [Hint: Observe the example input and output carefully. As soon as one bit is detected that breaks the pattern, the circuit should return to the initial state and restart the search. Similarly, once 4 desired bits are detected, the circuit returns to the initial state and restarts the search from the next input bit.] [4 marks]

(c) Generate the pattern: 0, 1, 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15. You can either use a "4-bit binary counter with parallel load", or design the full circuit using multiple flip-flops of your choice. [1 marks]

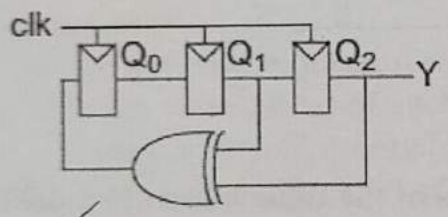
(d) A sequential circuit has 2 JK flip-flops, two inputs x and y and one output z. The input and output equations are:

$J_A = Bx'+By'$ $K_A = Axy$ $J_B = Ax+By$ $K_B = A+B$ $z = Axy+ Bx'y$

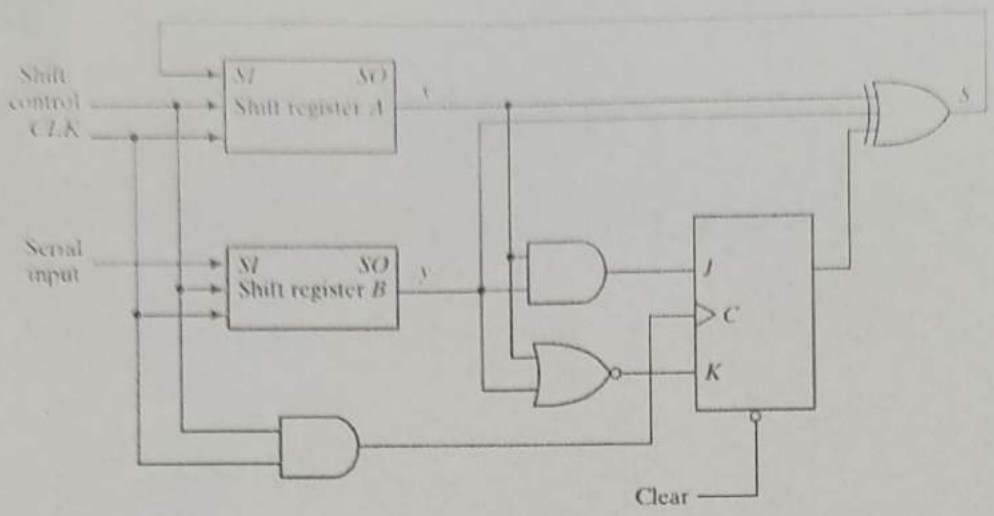
(i) Show the circuit diagram of the circuit. [1 mark] (ii) Show the state table. [2 mark]

Question 7 – 8 Marks

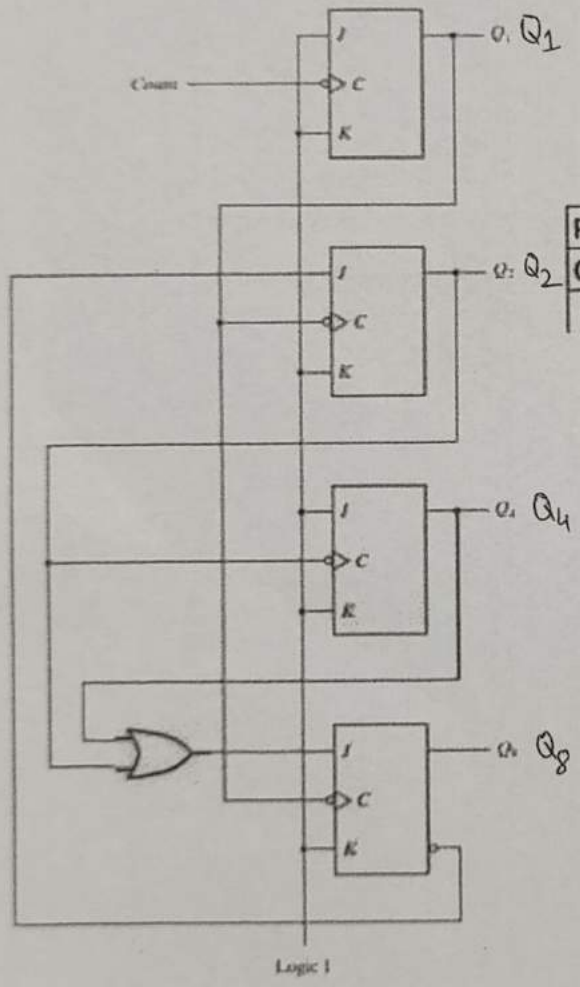
(a) Consider the circuit below, where all the 3 flip-flops are D flip-flops. Initially, a value of 1 is stored in each of the flip-flops. In other words, the register initially stores the value 111. Show the sequence of value on each clock pulse, till you see the same value (111) again. [2 marks]



(b) Consider the serial adder design below. Register A holds the binary number 1101 and register B holds 1001. The carry flip-flop is initially set to 1. List the binary values in register A and the carry flip-flop after each shift. [2 mark]



(c) Consider the ripple-counter shown below. Starting from the state 0000 (i.e., all the flip-flops store 0), show the subsequent states. That means show the state table showing the value of all flip-flops, each time when "Count" signal comes. You have to show till you again see the state 0000. (You have to show your answer by filling out the given table) [4 marks]



Present State (t)				J-K inputs						Next State (t+1)			
Q8	Q4	Q2	Q1	J1	K1	J2	K2	J4	K4	J8	K8	Q8	Q4	Q2	Q1
0	0	0	0												

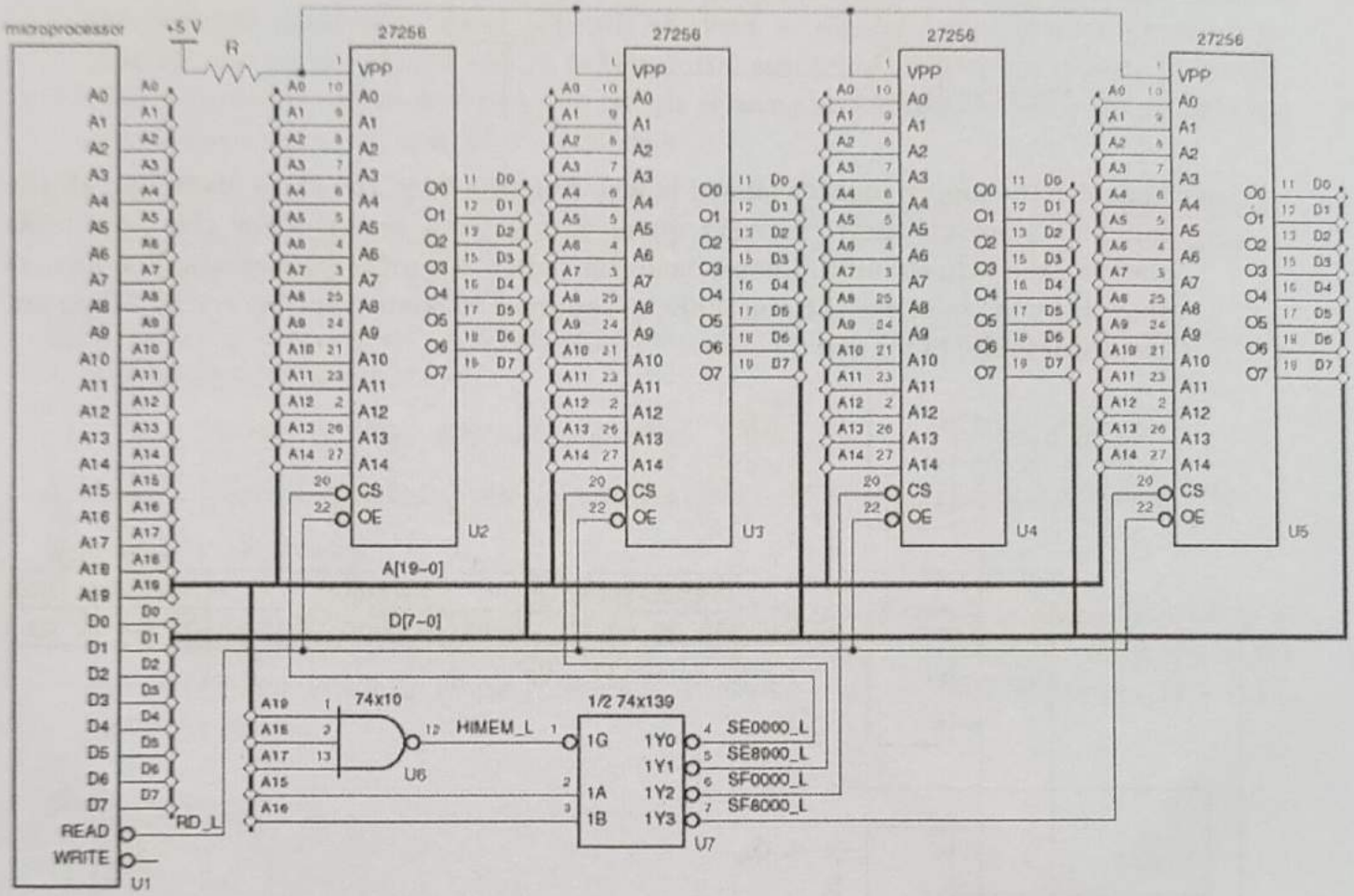
Question 8 – 8 Marks

(a) Consider a full-adder with three inputs A, B and C. Its outputs are Sum and Cout. Show the programming table of PLA that implements this full-adder. [4 Marks]

(b) Given a 128x8 ROM chip with an enable input, show the external connections required to construct a 512x16 ROM with eight chips and a decoder. [4 Marks]

OR

Find the memory address range of each memory chip placed in the circuit below:



All necessary explanations are required for mentioning the address range. [4 Marks]