Tutorial 4 ECN-104

1. Design all logic gates using NAND gate only in VHDL.
2. A. Write some VHDL code using an if statement that implements the following logic function: F OUT(A, B, C) = AB'C'+BC
   B. Write some VHDL code using case statement that implements the following logic function: F OUT(A, B, C) = AB'C'+BC
3. A. Create a truth table for 4-to-1 multiplexer and derive the expression for output.
   B. Write VHDL code for a 4-to-1 multiplexer using dataflow modeling along with the testbench.
   C. Write VHDL code for a 4-to-1 multiplexer using behavioral modeling along with the testbench.
   D. Write VHDL code for 4-to-1 multiplexer using 2-to-1 multiplexer. Write the testbench to validate the design.
4. Write a VHDL code for BCD to Excess 3 code converter.
5. Write a VHDL code for generating a clock signal of 1Hz.
6. Using the VHDL code below, draw the synthesized circuit.

```
library IEEE;
use IEEE.std_logic_1164.all;
entity Design_VHDL is
port (
 A,B: in std_logic_vector(1 downto 0);
 Out1: out std_logic;
 Out2: out std_logic;
 Out3: out std_logic
 );
end Design_VHDL;
architecture D_structural of Design_VHDL is
signal tmp1,tmp2,tmp3,tmp4,tmp5, tmp6, tmp7, tmp8: std_logic;
-- temporary signals
begin
 tmp1 <= A(1) xnor B(1);
 tmp2 <= A(0) xnor B(0);
 Out2<= tmp1 and tmp2;

 tmp3 <= (not A(0)) and (not A(1)) and B(0);
 tmp4 <= (not A(1)) and B(1);
 tmp5 <= (not A(0)) and B(1) and B(0);
 Out1 <= tmp3 or tmp4 or tmp5;


 tmp6 <= (not B(0)) and (not B(1)) and A(0);
 tmp7 <= (not B(1)) and A(1);
 tmp8 <= (not B(0)) and A(1) and A(0);
 Out3 <= tmp6 or tmp7 or tmp8;
end D_structural;
```