555 Timer

555 timer can be used for many applications.

A sample of these applications includes monostable and astable multivibrators, dcdc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control devices, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.

The timer basically operates in one of two modes:

astable (free-running) multivibrator

monostable (one-shot) multivibrator

Astable operation

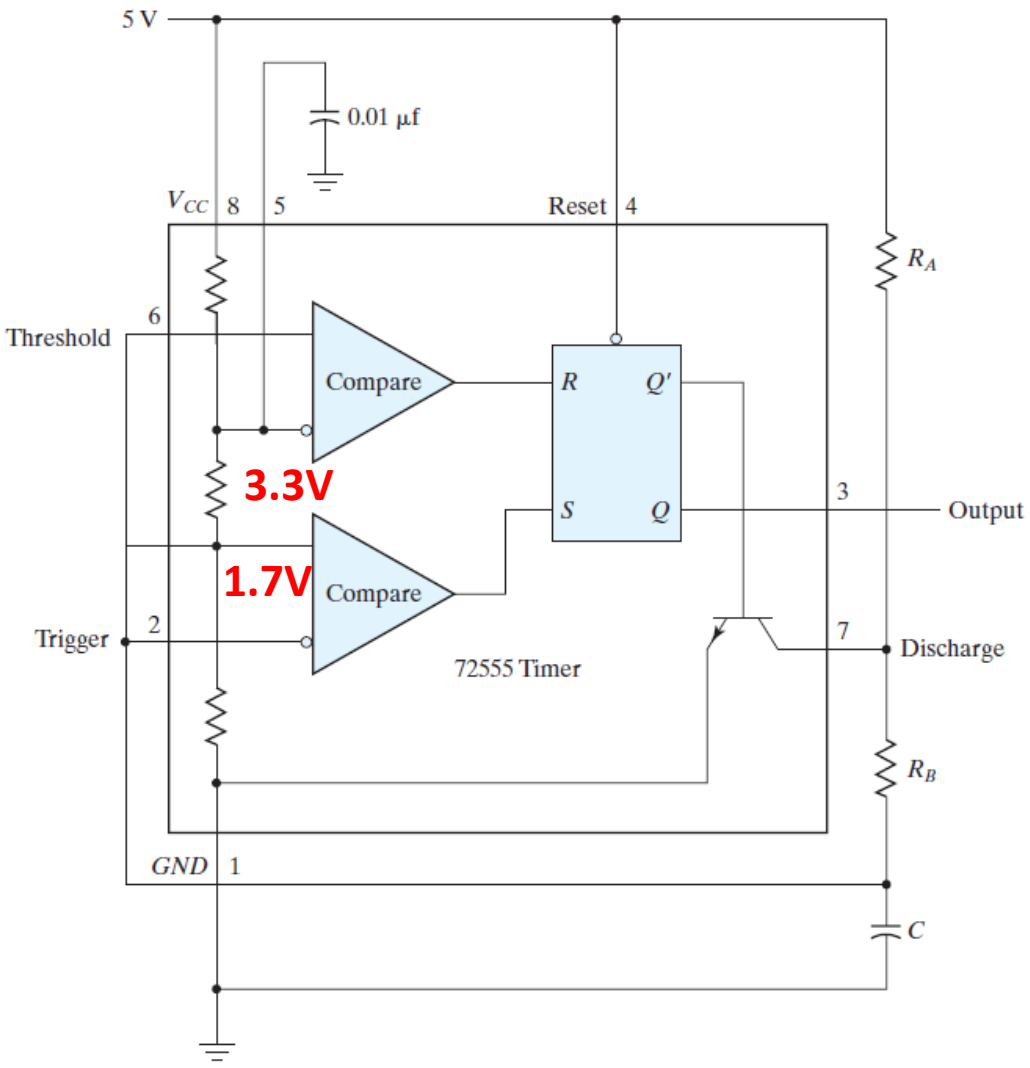
Timer

The circuit consists of two voltage comparators, a flip-flop, and an internal transistor.

The voltage division from *VCC* = 5 V through the three internal resistors to ground produces 2/3 and 1/3

of *VCC* (3.3 V and 1.7 V, respectively) into the fixed inputs of the comparators.

The timer circuit produces accurate time delays controlled by an external RC circuit

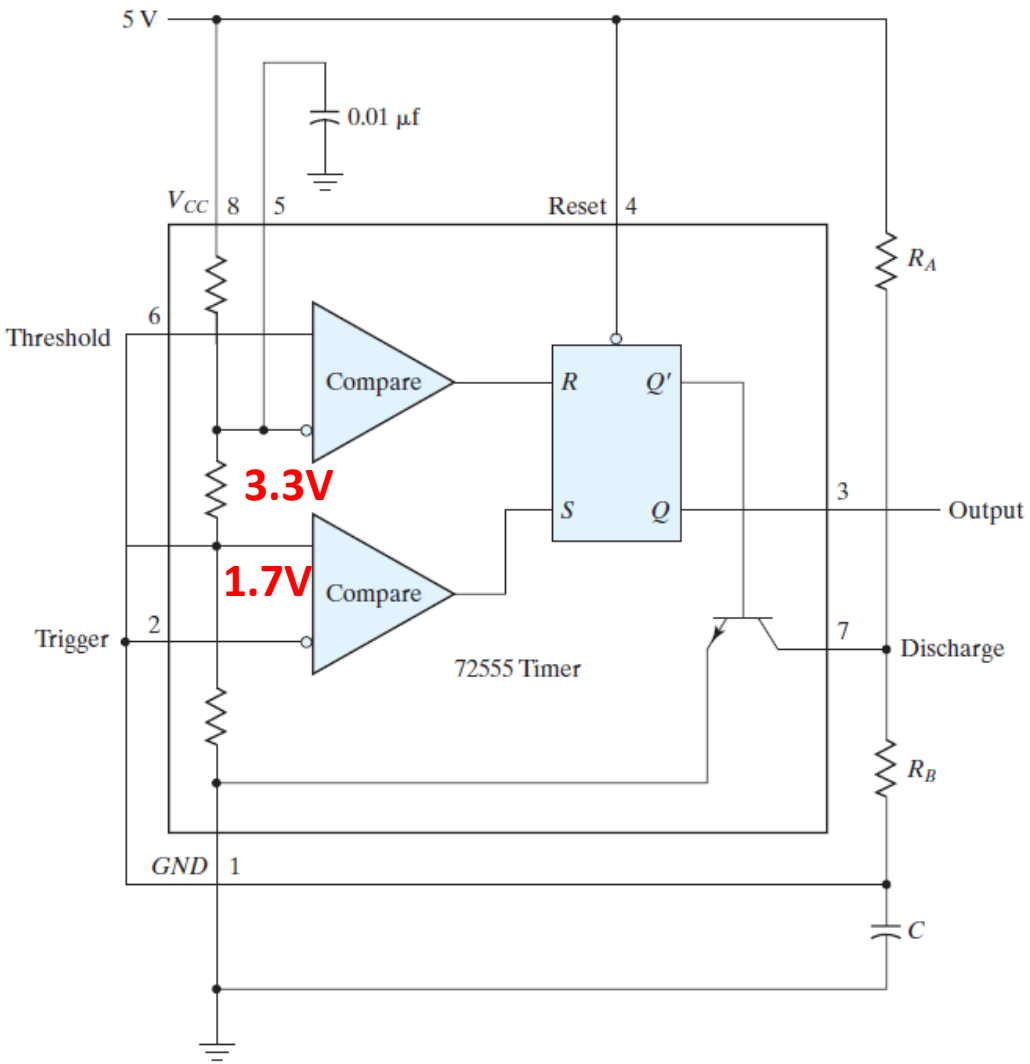


When threshold input at pin 6 goes above 3.3 V, upper comparator resets the flip-flop and the output goes low (0 V)

When trigger input at pin 2 goes below 1.7 V, the lower comparator sets the flip-flop and the output goes high to about 5 V.

When output is low, Q' is high and the base–emitter junction of the transistor is forward biased.

When the output is high, Q' is low and the transistor is cut off.



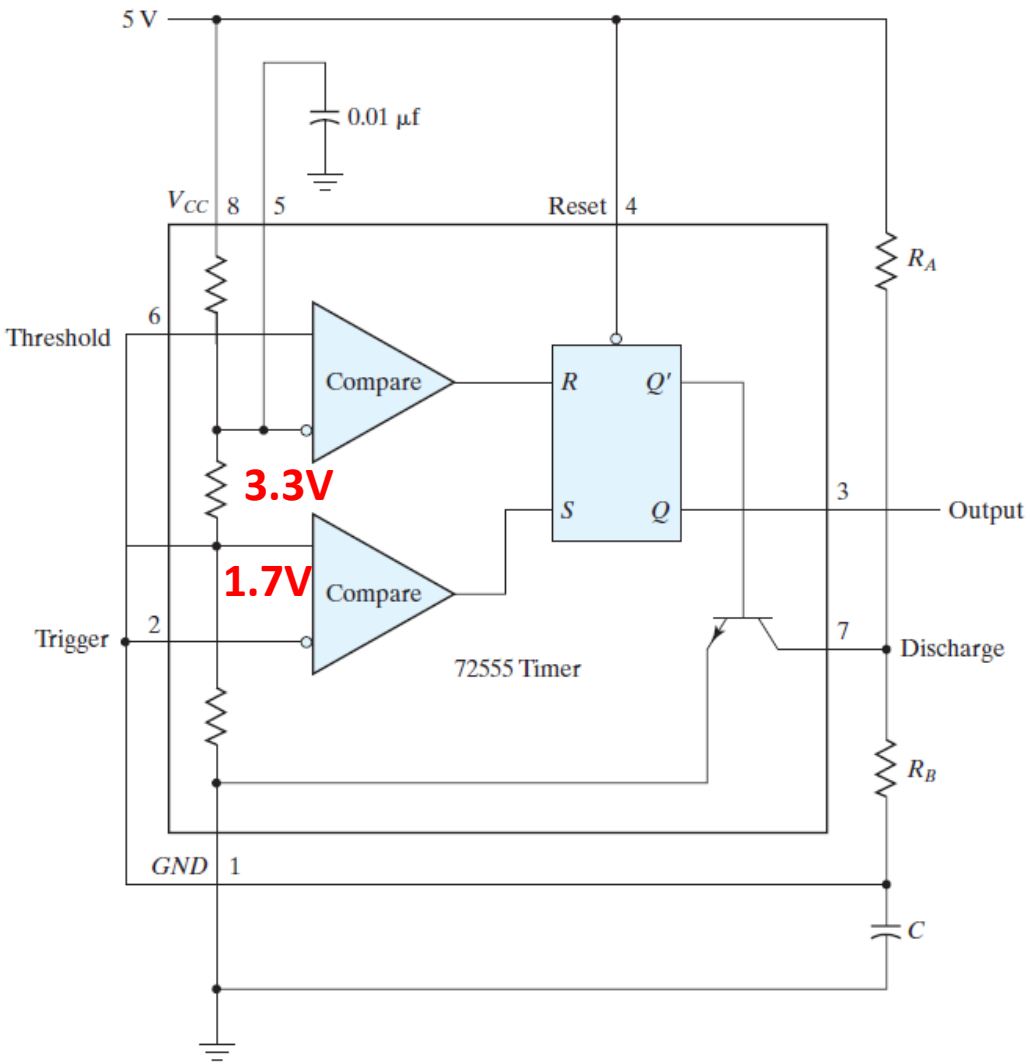
When transistor is cut-off, capacitor C charges through resistors R_A and R_B

When transistor is forward-biased and conducting, capacitor discharges through R_B.

When the charging voltage across capacitor C reaches 3.3 V, the threshold input at pin 6 causes the flip-flop to reset and the transistor turns on.

When the discharging voltage reaches 1.7 V, the trigger input at pin 2 causes the flip-flop to set and the transistor turns off.

Output alternates between two levels.



Summary

Vc =0	R=0, S=1, Q=1, Q'=0, NPN is off.
Vc charges to above 1/3V_{CC}	R=0, S=0, Q=1, NPN is off
Vc charges above 2/3Vcc	R=1, S=0, Q=0, Q'=1, NPN is ON, Vc starts discharging
Vc discharges below 2/3Vcc	R=0, S=0, Q=0, Q'=1, NPN is ON
Vc discharges below 1/3Vcc	R=0, S=1, Q=1, Q'=0, NPN is off.

Timing

The output remains high for a

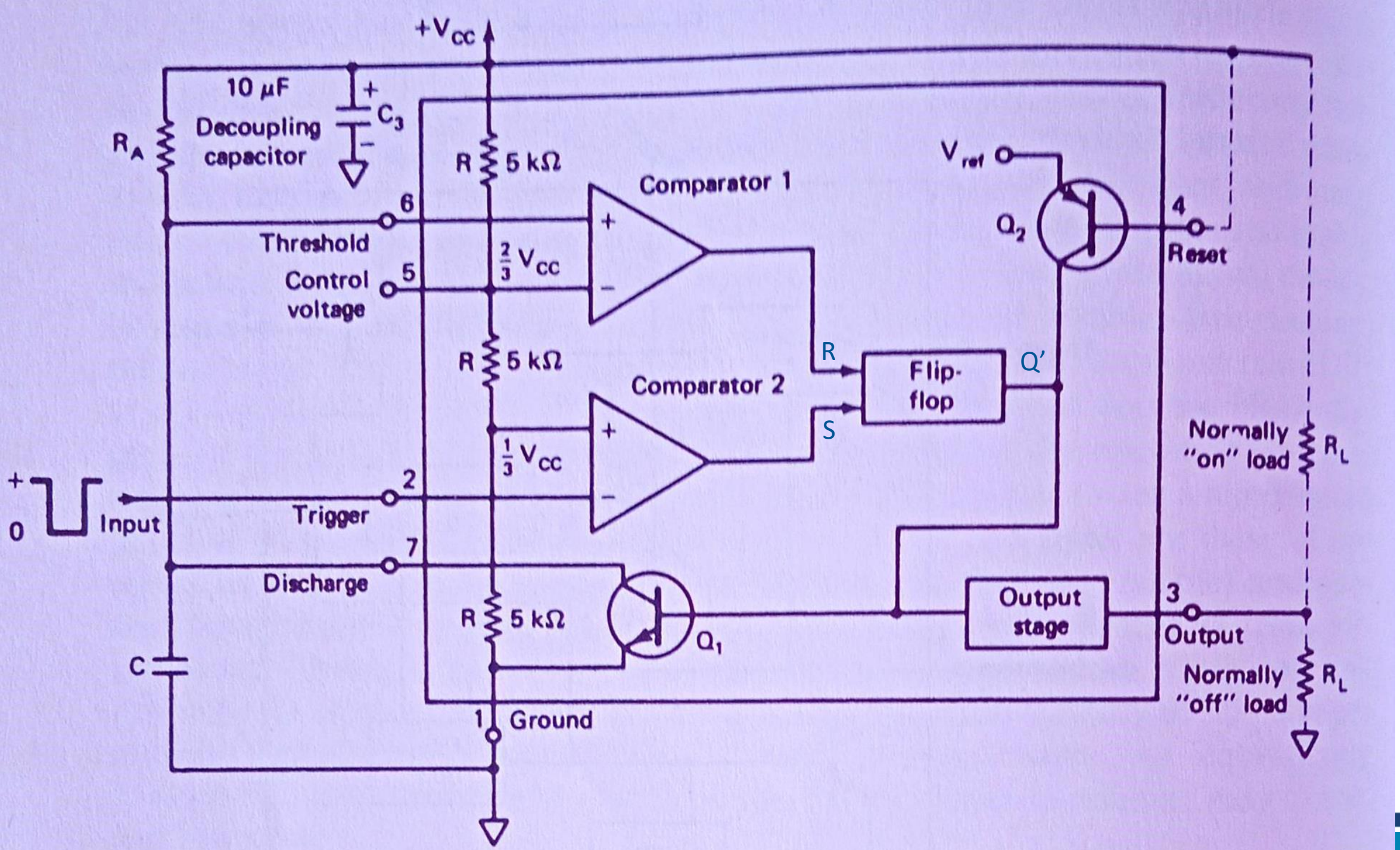
duration equal to the charge time. This duration is determined from the equation

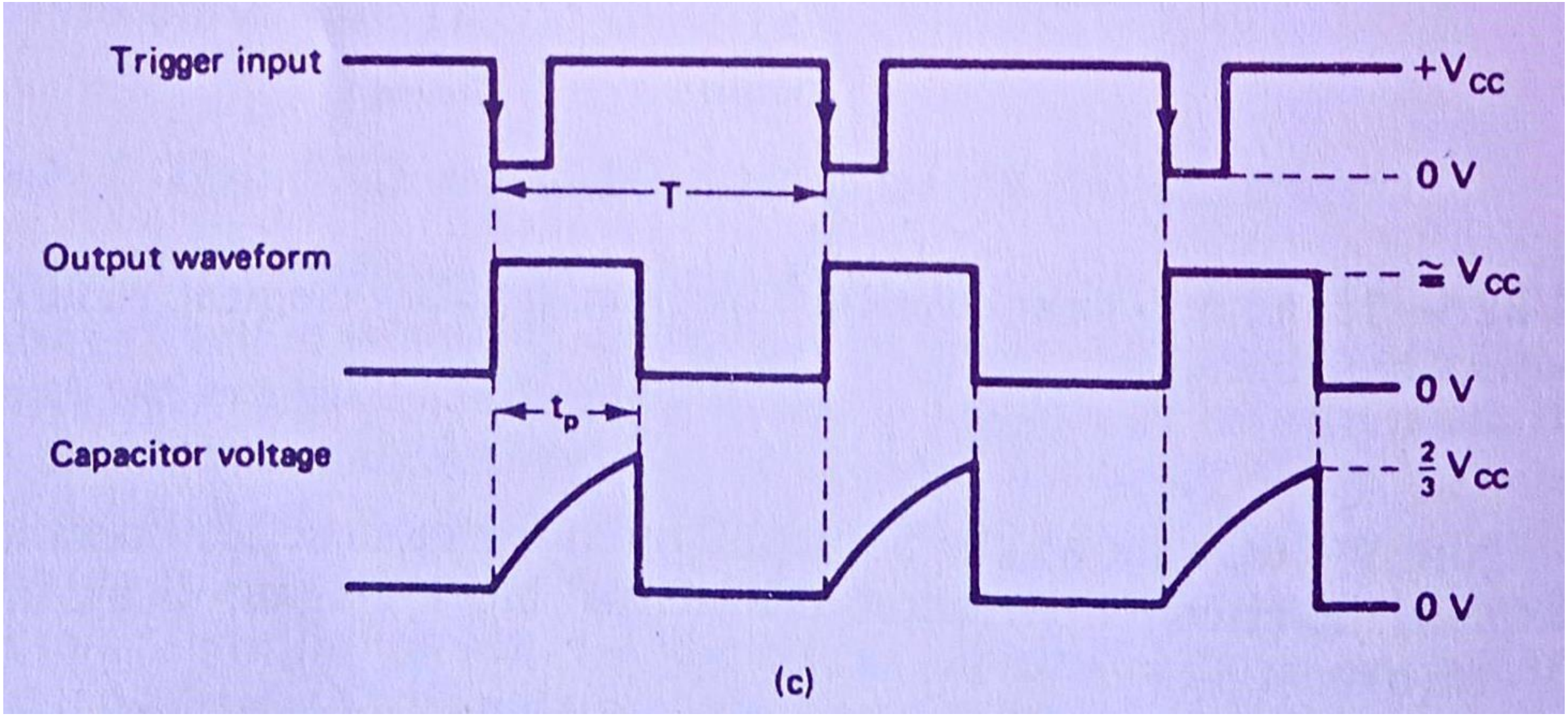
$$tH = 0.693(R_A + R_B)C$$

The output remains low for a duration equal to the discharge time. This duration is determined from the equation

$$tL = 0.693R_BC$$

Monostable operation


+Vcc
10 μF
Decoupling capacitor
C3
RA
R 5 kΩ
Vref
Comparator 1
Q2
4
Reset
6
Threshold
2/3 Vcc
5
Control voltage
R 5 kΩ
R
Q'
Flip-flop
Comparator 2
S
1/3 Vcc
Normally "on" load
RL
2
Trigger
Input
7
Discharge
R 5 kΩ
Output stage
3
Output
Q1
C
Normally "off" load
RL
1
Ground


Trigger input
+Vcc
0 V
T
Output waveform
≅ Vcc
0 V
tp
Capacitor voltage
2/3 Vcc
0 V
(c)

Explanation

When output (Q) is zero, Q'=1, transistor is forward-biased and capacitor is grounded. Capacitor voltage is zero. Top-input to comparator 1 is also zero. S=0, R=0. Trigger is at Vcc (5V).

When trigger of 0V is applied, output of comparator 2 is 1, so S=1, R=0, Q=1, Q'=0. Transistor is cut-off and capacitor starts charging.

Very soon after this, trigger is removed (i.e., trigger is changed to Vcc). R=0 and S=0, so, flip-flop value is maintained.

When capacitor voltage goes above 2/3Vcc, comparator 1 outputs 1, so R=1, and S=0, so flip-flop is reset. Q'=1 and Q=0. So, transistor is forward-biased and capacitor is grounded, so its voltage suddenly drops to zero.