ECN 104 Tutorial 4
Spring 2023
Full Marks = 20

Question 1:
Design a circuit that generates a parity bit from a 3-bit input. The generated parity bit P should be logic 1 if the number of 1s in the input code is odd and logic 0 if the number of 1s in the input code is even.

(a) From the above statement, write down the truth table. 2 Marks
(b) Create the output logical expression in minimized form using K-map. 2 Marks
(c) Draw the gate-level circuit diagram. 2 Marks

Question 2:
What is the difference between a full adder and a half adder? Design a full adder circuit with only NAND gates, keeping the number of gates minimum. 1+3 Marks

Question 3:
Implement the function $F(A, B, C, D) = \sum(0,1,5,7,8,13,14)$ using multiplexers. 2 Marks

Question 4:
Implement a 16x1 multiplexer using two 8x1 and one 2x1 multiplexer. 2 Marks

Question 5:
Design a half subtractor circuit with inputs x and y and outputs Diff and Borrow. x and y are 1 bit.

2 Marks

Question 6:
An 8x1 multiplexer has inputs A, B and C connected to the selection inputs S2, S1 and S0. The data inputs are connected as follows: I1=I2=0; I3=I5=I7=1; I0=I4=D and I6=D'. Determine the function implemented by this circuit. 4 Marks