ECN 104 – Digital Logic Design

Spring 2023

Mid-term exam, Full Marks = 30, Time: 1.5 hrs

*Note the following equivalent notations for max-term/min-term representations:

Minterm: $\sum(0,2,3) = m_0 + m_2 + m_3 = \sum m(0,2,3)$

Maxterm: $\prod(4,5,6) = M_4 M_5 M_6$

Show all steps in your answer.

Question 1 – 8 Marks

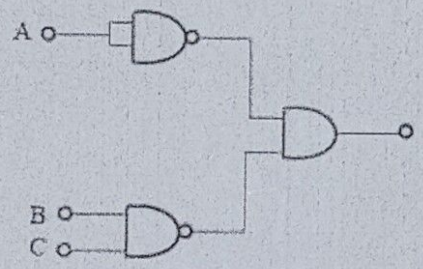
(a) Choose the correct option: A particular number is written as 132 in radix-4 representation. The same number in radix-5 representation is:
(A) 158 (B) 118 (C) 110 (D) 98 *1 Mark*

(b) A bulb in the staircase has two switches, one on the ground floor and the other on the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches, irrespective of the state of the other switch. The logic of switching on the bulb resembles: (A) AND gate (B) OR gate (C) XOR gate (D) NAND gate *1 Mark*

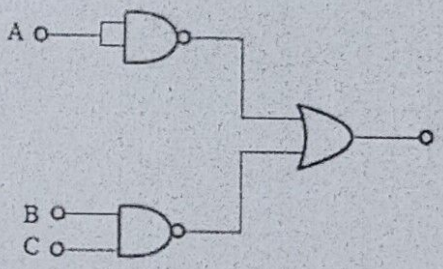
(c) Find the complement of the function $x'y'z' + x'y'z$ using DeMorgan's theorem. *1 Mark*

(d) Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in the figure ? *2 Marks*

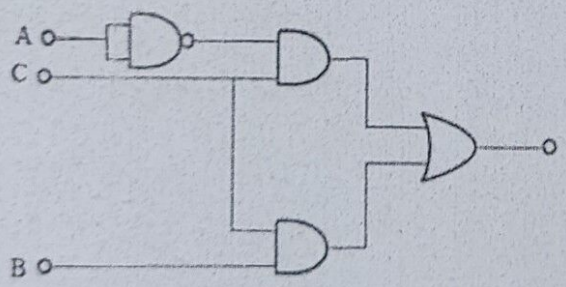
C \ AB	00	01	11	10
0	1	1		
1		1	1	



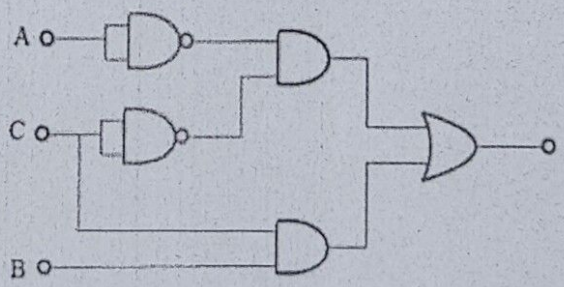
(P)



(Q)



(R)



(S)

(e) Express the function $F(x, y, z) = \sum(1,2,4,5)$ in POS form. *1 Mark*

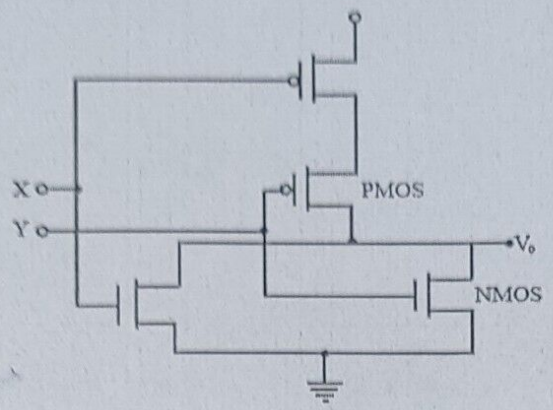
(f) Express the function $F(x, y, z, w) = \prod(0,1,3,4,7,11)$ in SOP form. *1 Mark*

(g) What is the 2's complement form of the number 01101000 ? *1 Mark*

Question 2 – 5 Marks

(a) Draw the minimum CMOS transistor network that implements the functionality of Boolean equation $F = (\bar{A} + \bar{B}C)$. You can assume both the original and complemented versions of each literal are available as gate inputs. *2.5 Marks*

(b) A CMOS implementation of a logic gate is shown in the following figure. Write the Boolean logic function realized by the circuit. *2.5 Marks*



Question 3* – 5 Marks

Implement the function $F(x, y, z, w) = \prod(2,3,5,9,14)$ using a multiplexer only, use minimum size multiplexer. You may use additional NOT gates only; no other gates are allowed.

Question 4* – 6 Marks

Minimize the following Boolean function using K-map -

$$F(A, B, C, D) = \Sigma m\,(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma m\,(0, 2, 14)$$

Implement the simplified logic using the NAND-NAND network. You can assume both the original and complemented versions of each input variable are available to you. *4+2 Marks*

Question 5 – 6 Marks

(a) Implement a T-flipflop using a D-flipflop. Show your steps. *2 Marks*

(b) Implement a sequential circuit to generate the sequence as 00→01→10→00. If the 11 state appears, the circuit should move to 10 state. Use JK-flipflops for this design. Is this sequential circuit a Moore or a Mealy type? *3.5+0.5 Marks*