Modern Computer Architecture

Debiprasanna Sahoo
Assistant Professor
Department of Computer Science and Engineering
Indian Institute of Technology Roorkee

The Core/CPU

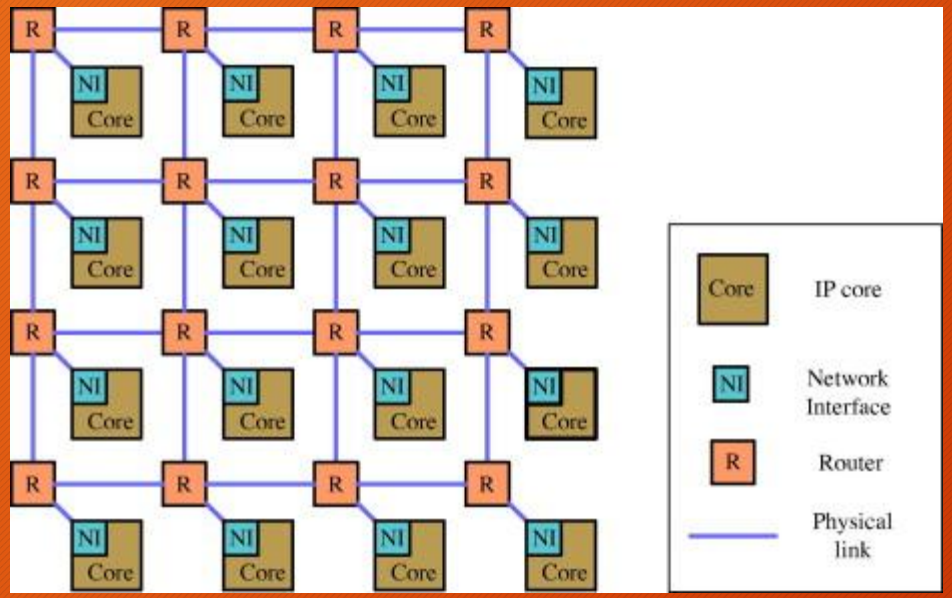
Instruction handling unit	Data handling unit (load store unit)	Register Set	Execution Unit	Control Unit
• Reading instruction • Decoding instruction	• Reading memory • Writing memory	• Reading registers • Writing registers	• Arithmetic and logic unit • Floating point unit • Integer unit	• Hardwired Controlled • Micro-programmed Controlled

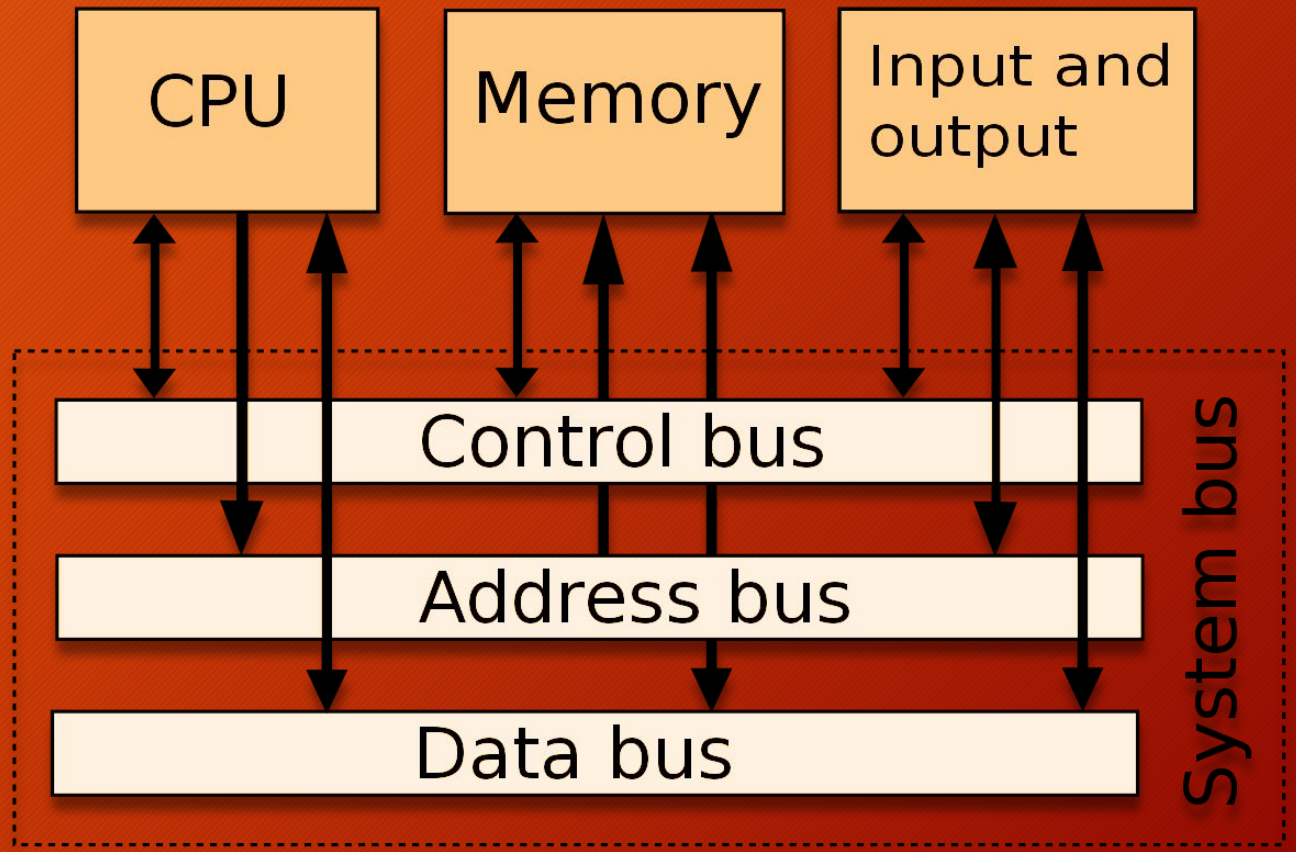
The Memory

Main Memory	Secondary Storage	Cache Memory (8KB to 64 MB)
• Typically, embedded boards ~ 2/4 GB, Mobile ~ 4/8/16 GB, Laptops/Desktops ~ 8/16/32 GB, Workstations ~ 64/128 GB, Servers ~ 128GB/2TB • OS-controlled allocation • Hardware-controlled access	• TBs now for laptops, desktops, workstations, servers • OS-controlled allocation/access	• Hardware-controlled allocation/access

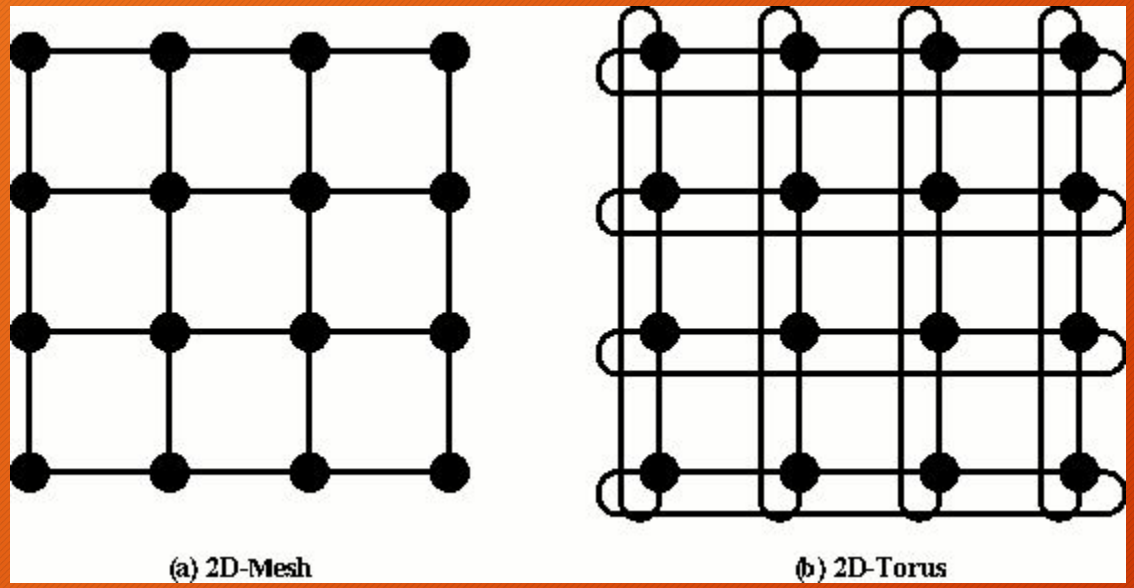
Buses and Interconnects

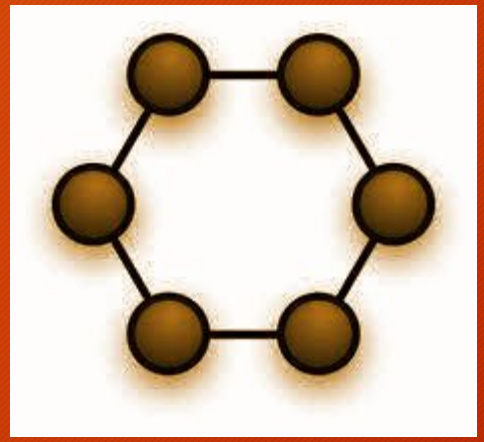
- Connects different units
- Transfers control signals
- Transfers address
- Transfers data

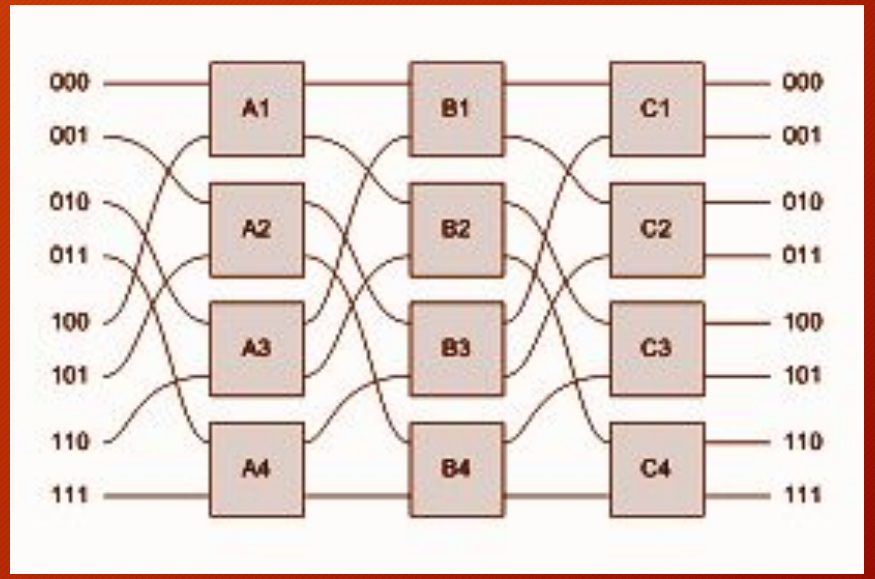




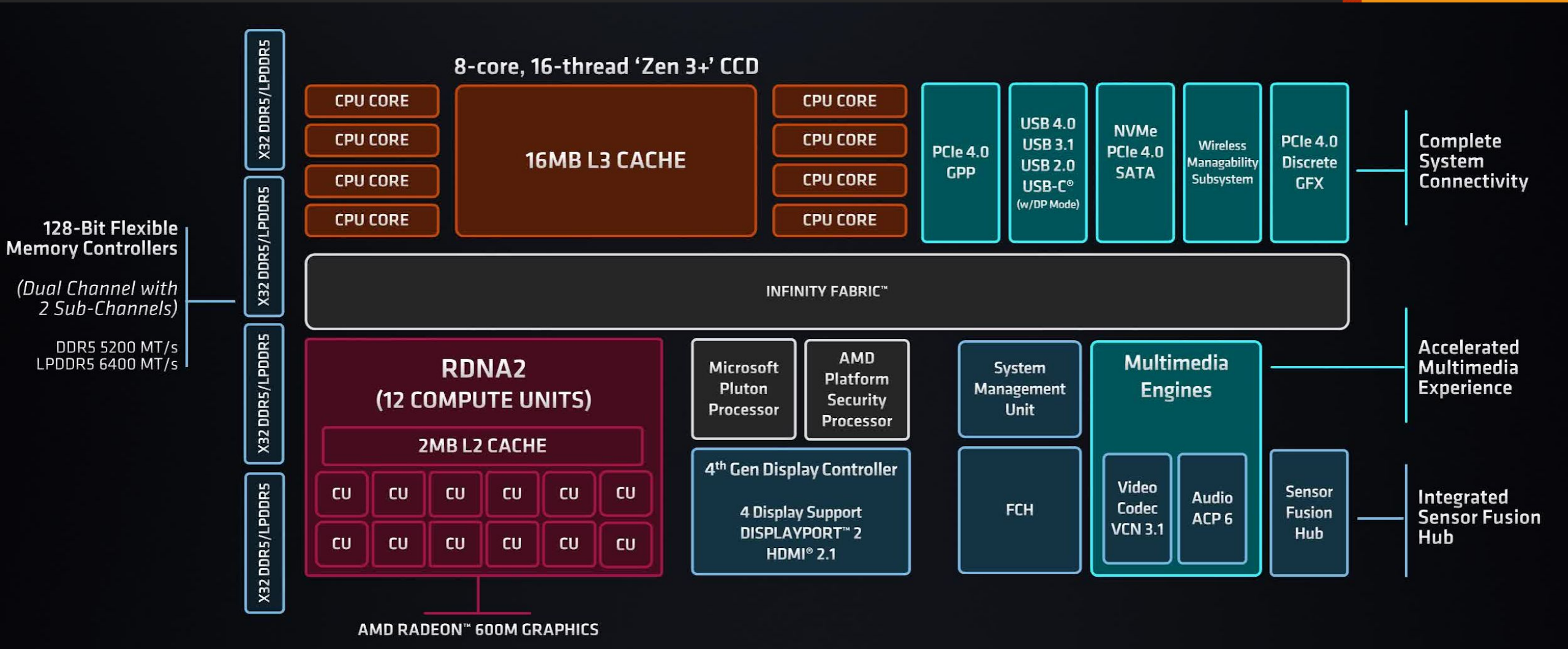
Multi-core Processors: Interconnection Network







System-on-chip (AMD Zen 4 Architecture)



System-on-chip (Intel)

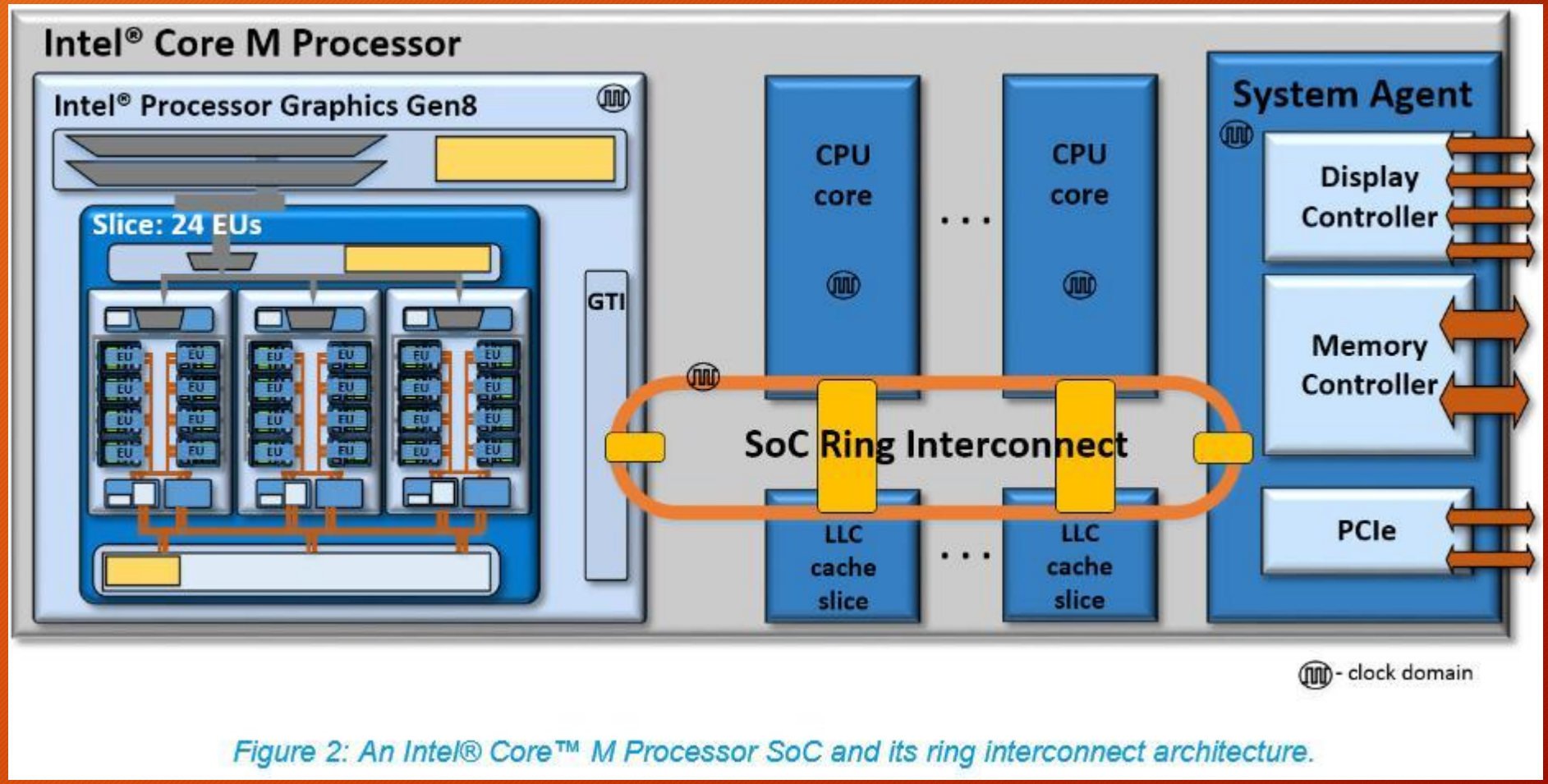


Figure 2: An Intel® Core™ M Processor SoC and its ring interconnect architecture.

Graphics Processing Unit

System-on-chip (AMD RDNA GPU)