INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

# System Software
# CSN-252
# Introduction

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## SIC/XE

- **Data formats** (additional)

  – 48-bit floating-point data

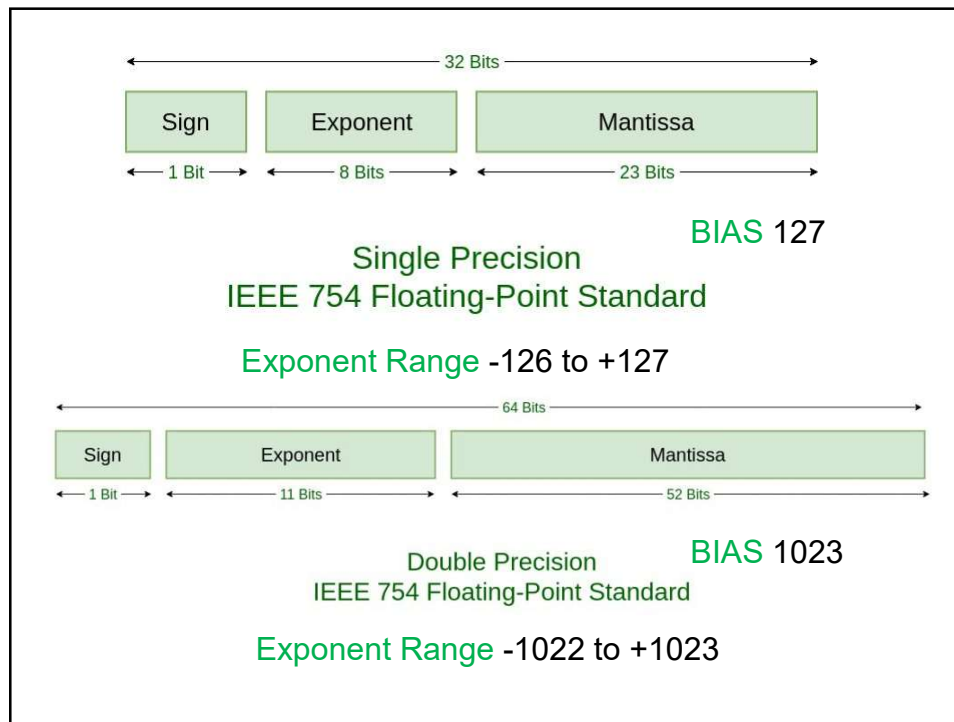  – Value of the fraction is between 0 and 1 (normalized?)

| 1 | 11 | 36 |
|---|----|----|
| s | exponent | fraction |

- Exponent – between 0 and 2047 (bias 1024)
- Zero: all bits are 0

$(.125)_{10} = (.001)_2 = .1 \times 2^{-2}$

e =

f =

32 Bits

| Sign | Exponent | Mantissa |
|------|----------|----------|

1 Bit      8 Bits      23 Bits

BIAS 127

**Single Precision**
**IEEE 754 Floating-Point Standard**

Exponent Range -126 to +127

64 Bits

| Sign | Exponent | Mantissa |
|------|----------|----------|

1 Bit      11 Bits      52 Bits

BIAS 1023

Double Precision
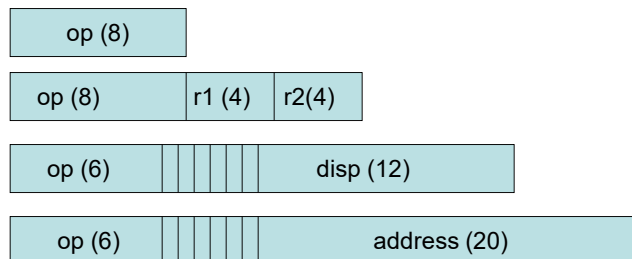IEEE 754 Floating-Point Standard

Exponent Range -1022 to +1023

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**Float Point Numbers**

$4.89 = .100111000111101011100001010001111010 * 2^3$

$= 0 \quad 10000000011 \quad 100111000111101011$
$100001010001111010$

- Instruction Formats (Four)
  - Instructions that do not reference memory at all (1 & 2)
  - Instructions that use relative addressing (3)
  - Instruction format with 20-bit address field (4)

| op (8) |
|---|

| op (8) | r1 (4) | r2(4) |
|---|---|---|

| op (6) | | | | | | | disp (12) |
|---|---|---|

| op (6) | | | | | | | address (20) |
|---|---|---|

- flags n, i, x, b, p, e
- All SIC instructions end in 00 (opcode) that is, if bits n and i are both 0, then bits b, p and e are considered to be part of address field

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- e = 0 means format 3
- e = 1 means format 4
- Relative addressing modes available for Format 3 instructions
  - b = 1, p = 0 (Base Relative) TA = (B) + disp
  - b = 0, p = 1 (PC Relative) TA = (PC) + disp
  - b = 0, p = 0 (direct addressing) TA = disp
  - b = 1, p = 1 ?
- Any of the above addressing modes can be combined with indexed addressing (x = 0 or 1)
- i = 1, n = 0 (immediate addressing)
- i = 0, n = 1 (indirect addressing)
- i = 1, n = 1 (simple addressing)

| Simple | 1 1 0 0 0 0 | Op c | disp | (TA) | D |
|---|---|---|---|---|---|
| | 1 1 0 0 0 1 | +Op m | addr | (TA) | 4 D |
| | 1 1 0 0 1 0 | Op m | (PC) + disp | (TA) | A |
| | 1 1 0 1 0 0 | Op m | (B) + disp | (TA) | A |
| | 1 1 1 0 0 0 | Op c, X | disp + (X) | (TA) | D |
| | 1 1 1 0 0 1 | +Op m, X | addr + (X) | (TA) | 4 D |
| | 1 1 1 0 1 0 | Op m, X | (PC) +disp +(X) | (TA) | A |
| | 1 1 1 1 0 0 | Op m, X | (B) +disp + (X) | (TA) | A |
| | 0 0 0 - - - | Op m | | (TA) | D |
| | 0 0 1 - - - | Op m, X | | (TA) | D |

| Indirect | 1 0 0 0 0 0 | Op @c | disp | ((TA)) | D |
|---|---|---|---|---|---|
| | 1 0 0 0 0 1 | +op @m | addr | ((TA)) | 4 D |
| | 1 0 0 0 1 0 | Op @m | (PC) + disp | ((TA)) | A |
| | 1 0 0 1 0 0 | Op @m | (B) + disp | ((TA)) | A |
| Immediate | 0 1 0 0 0 0 | Op #c | disp | TA | D |
| | 0 1 0 0 0 1 | +op #m | addr | TA | 4 D |
| | 0 1 0 0 1 0 | Op #m | (PC) + disp | TA | A |
| | 0 1 0 1 0 0 | Op #m | (B) + disp | TA | A |

| Address | Value |
|---|---|
| | . |
| | . |
| 3030 | 003600 |
| | . |
| | . |
| 3600 | 103000 |
| | . |
| | . |
| 6390 | 00C303 |
| | . |
| | . |
| C303 | 003030 |
| | . |
| | . |
| | . |
| | . |

(B) = 006000
(PC) = 003000
(X) = 000090

Instructions

032600
03C300
022030
0310C303

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**Instruction Set**

- instructions to load or store new registers

- Instructions to perform floating point arithmetic

- Register-register instructions

- Special supervisor call instruction