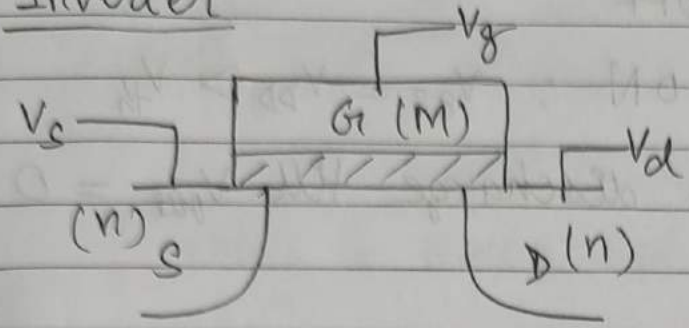
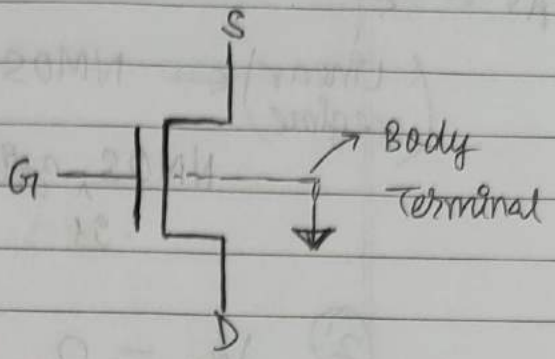
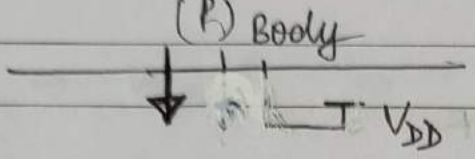
# CMOS Logic Gates

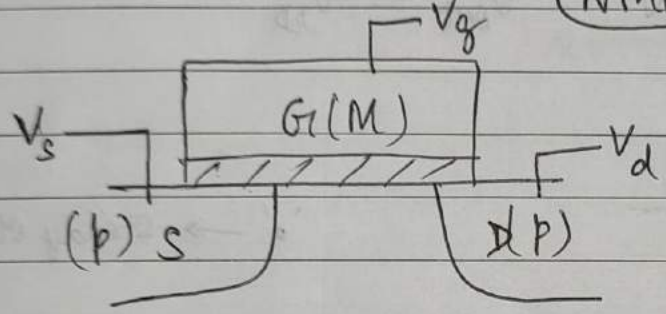
## Inverter

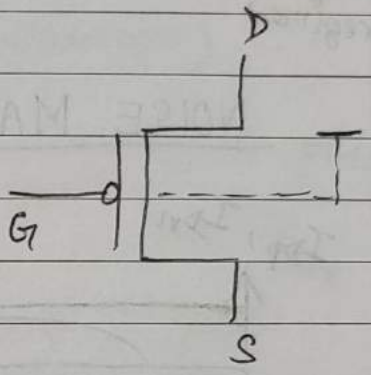


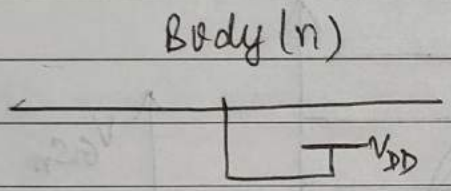




NMOS

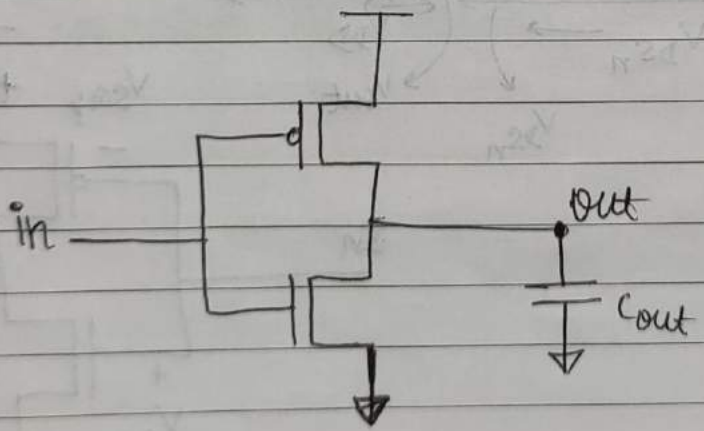



PMOS

## CMOS :-



① $V_{in} = V_{dd}$ , $V_{out} = 0$

PMOS → OFF

NMOS → ON ; $V_{gs} = V_{DD} > V_{th}$

(Linear regime) ← As $V_{ds} = 0$

NMOS is going to discharge till $V_{out} = 0$

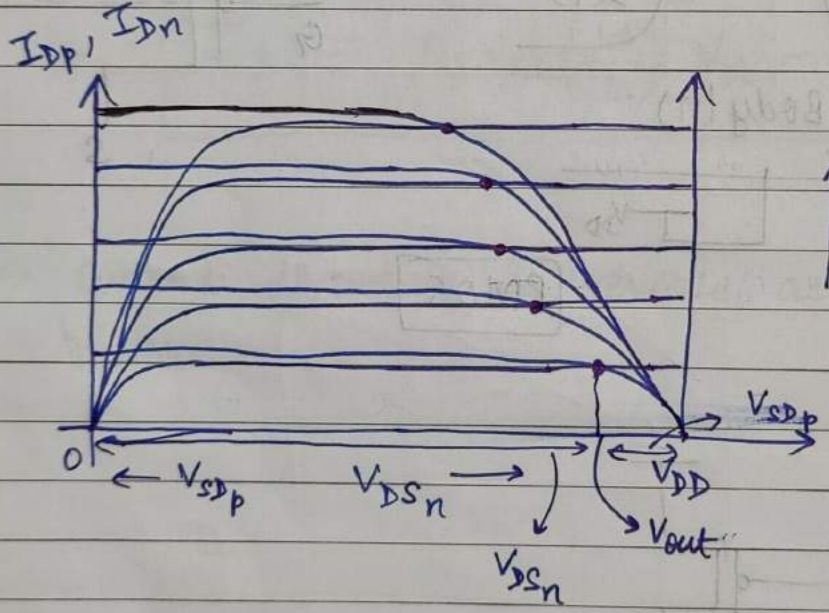
② $V_{in} = 0$

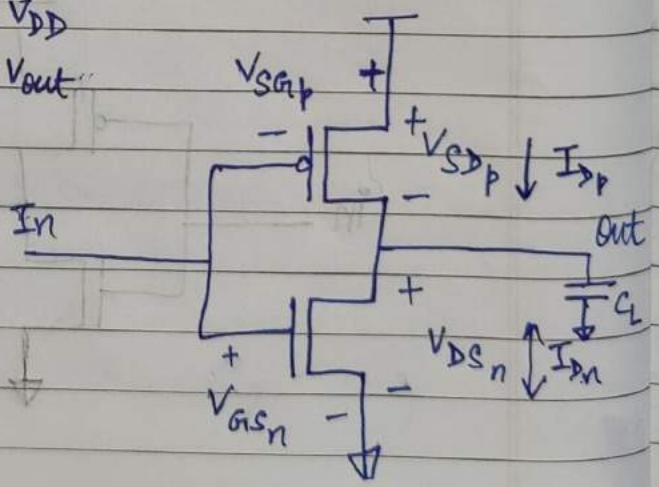
~~(Linear regime)~~ ← NMOS → OFF

(Linear regime) ← PMOS → ON $V_{out} = V_{DD}$

## NOISE MARGIN

'.' → steady state pts



$$V_{SD_p} + V_{DS_n} = V_{DD}$$

If $V_{in} = \frac{V_{DD}}{2}$ and $V_{out}$ has settled at it's steady state value

PMOS & NMOS both are ON.

$V_{in} \uparrow \Rightarrow V_{GSn} \uparrow \Rightarrow I_{D_n} \uparrow \Rightarrow V_{out} \downarrow \Rightarrow V_{DS_n} \downarrow$

$V_{SGp} \downarrow \quad I_{D_p} \downarrow \quad V_{SD_p} \uparrow$

$\longleftarrow$ after a while $\longrightarrow$

($C_L$ discharges) $\Downarrow$

Finally,

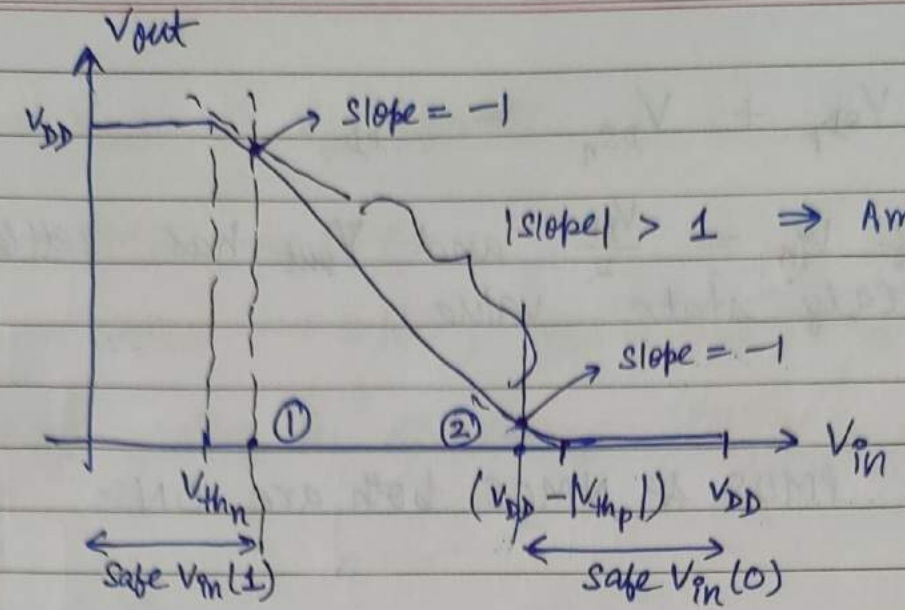
$I_{D_p} = I_{D_n}$

↑ steady state

As $V_{in} \uparrow \Rightarrow V_{out} \downarrow$ and $I_{D_p} = I_{D_n}$

when $V_{in} = 0$, $V_{out} = V_{DD}$

→ Because gate of MOSFET acts as capacitor, we use capacitor for $V_{out}$.




If $|\Delta(\text{Input})| >> |\Delta(\text{Output})| \Rightarrow$ we are safe

Otherwise, we are in trouble.

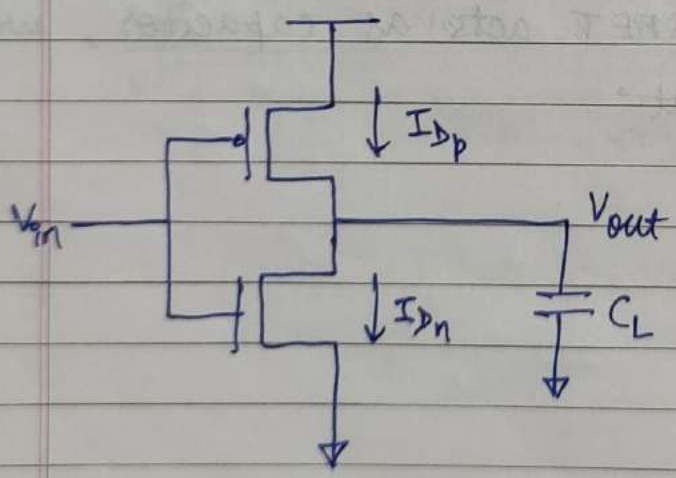
① $\longrightarrow$ $V_{IL}$ : $0 - V_{IL} \longrightarrow$ Logic 0

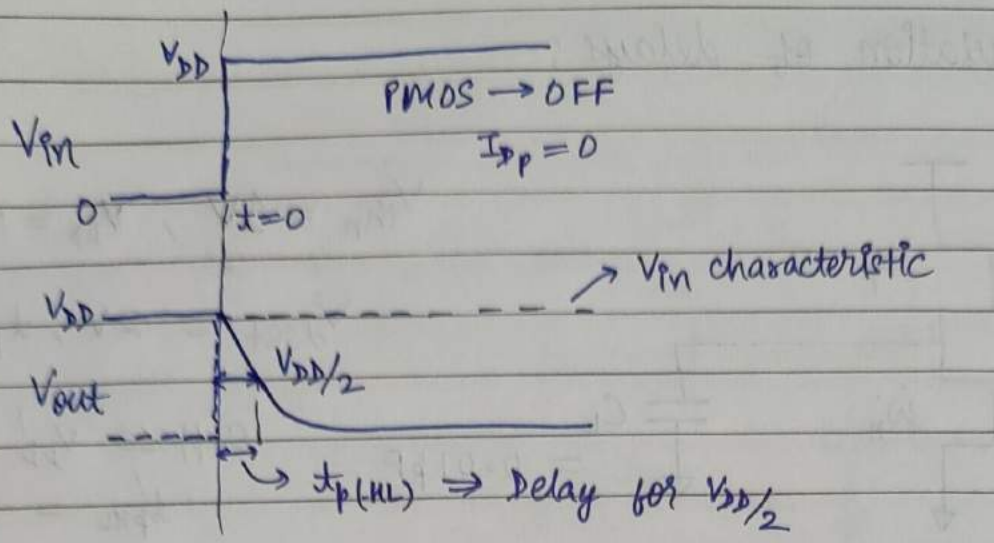
② $\longrightarrow$ $V_{IH}$ : $\underbrace{V_{IH} - V_{DD}}_{\text{Range}} \longrightarrow$ Logic 1

} Noise margin

$0 - V_{IL} \Rightarrow$ Noise Margin Low

$V_{IH} - V_{DD} \Rightarrow$ Noise Margin High

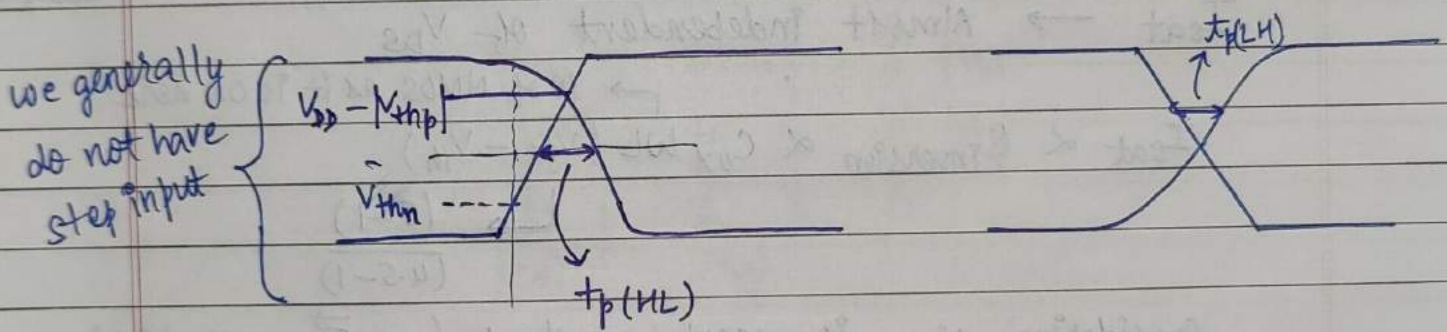





At t = 0,

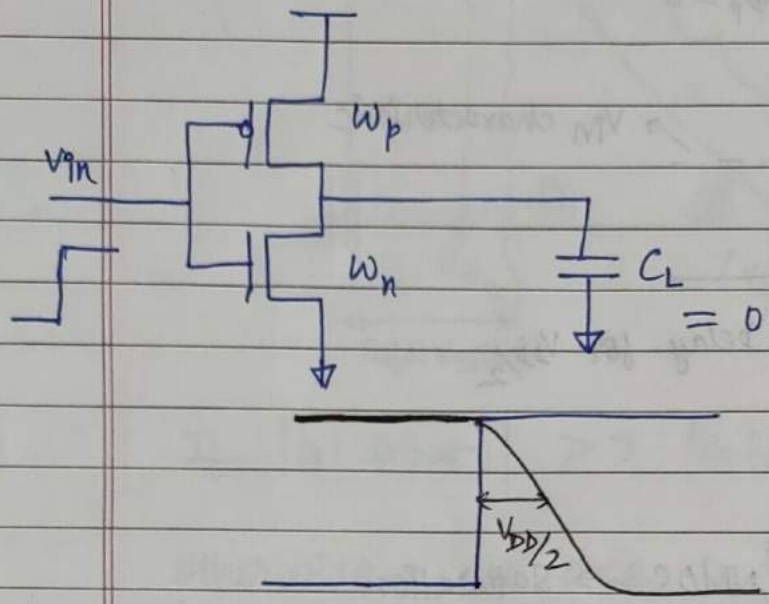
$V_{GS_n} = V_{DD}$ } NMOS → saturation
$V_{DS_n} = V_{DD}$ }

After $t = \Delta t$, $V_{DS} \downarrow$ ⇒ Constant $R_N$




* Indirectly, clock frequency / signal is dependent on delay of logic gates.

# Calculation of delays :-




$V_{thn} = 1V$, $V_{DD} = 5V$

$V_{dsat} = 2V$, $t_{pHL} = 50ps$

Suppose $V_{DD}' = 4.5V$

$t_{pHL}' = ?$

$$t_{pHL} = \frac{\Delta Q}{I_{sat}} = \frac{C_L\left(V_{DD} - \frac{V_{DD}}{2}\right)}{I_{sat}}$$

$$\Delta Q = \frac{2.5}{2.25} = \frac{10}{9}$$ } Factor by which $\Delta Q$ changes

$I_{sat} \rightarrow$ Almost independent of $V_{DS}$

$\rightarrow$ W of NMOS as it is ON here

$I_{sat} \propto Q_{inversion} \propto C_{ox} WL (V_{gs} - V_{th})$

$\hookrightarrow \frac{(5-1)}{(4.5-1)}$

considering $v_d$ is nearly constant (as $\vec{E}$ = very high)

$I_{sat}$ changes by factor $\left(\frac{5-1}{4.5-1}\right)$

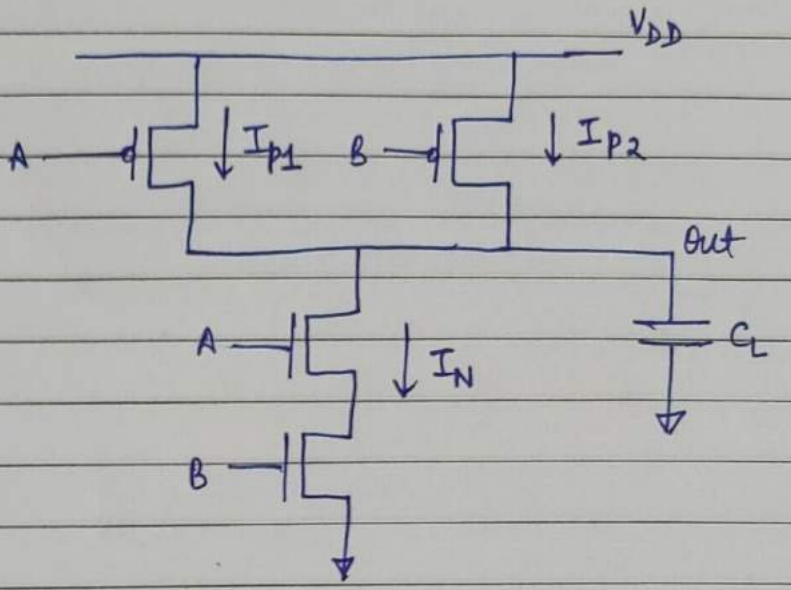
Hence, we can see factor by which $t_{pHL}$ changes.

* If $W_n \rightarrow 2W_n$ & $W_p \rightarrow 2W_p$, $t_{pHL} \rightarrow \frac{t_{pHL}}{2}$

As $I_{sat} \rightarrow 2 I_{sat}$

$$\frac{t_{pHL}(4.5V)}{t_{pHL}(5V)} = \frac{\Delta Q(4.5)}{\Delta Q(5)} \times \frac{I_{sat}(5)}{I_{sat}(4.5)}$$

## NAND




| A | B | Out |
|---|---|---|
| 0 | 0 | 1 ($V_{DD}$) |
| 0 | 1 ($V_{DD}$) | 1 ($V_{DD}$) |
| 1 ($V_{DD}$) | 0 | 1 ($V_{DD}$) |
| 1 ($V_{DD}$) | 1 ($V_{DD}$) | 0 |

## NOR