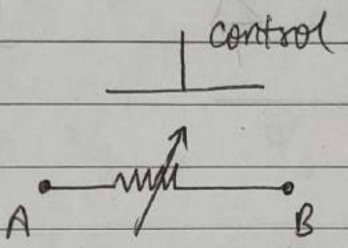
MOSFET

Transistor ⟶ Voltage-controlled switch
⟶ Amplifier

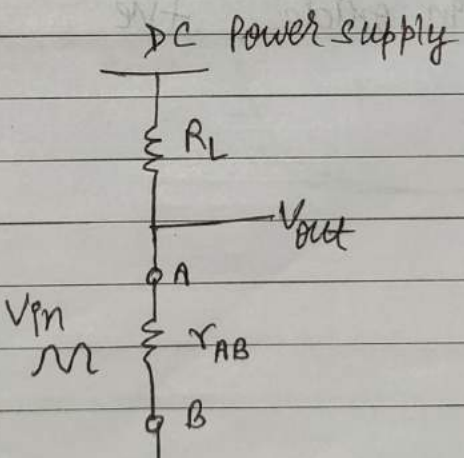
Trans - Resistor ⇒ Transistor

BJT ⟶ Current controlled



— Switch ⇒ Binary logic

Voltage controls resistance

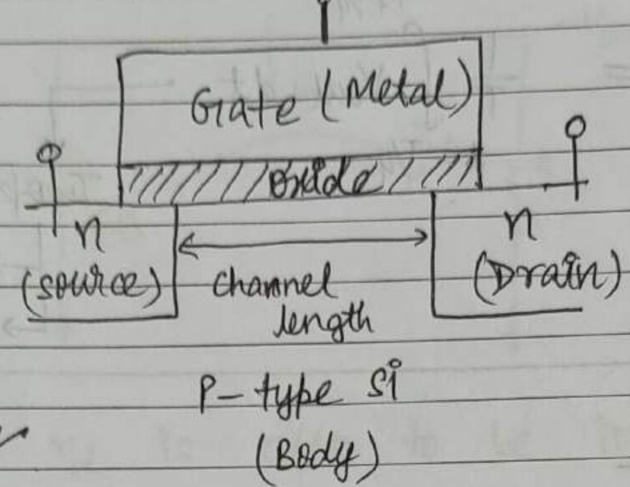


$r_{AB} \uparrow \Rightarrow V_{out} \uparrow$

controlled by V_{in}

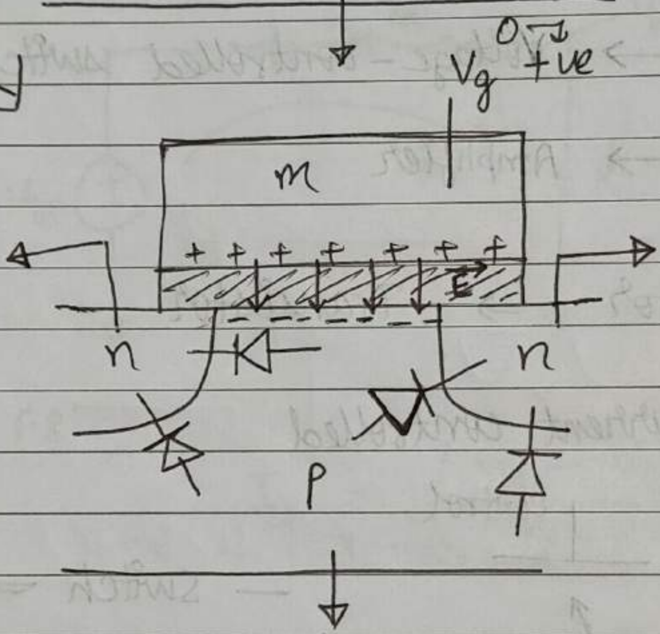
Amplifier

Structure of MOSFET



Oxide ⇒ Dielectric

Ideal oxide
⇓
No charges inside oxide

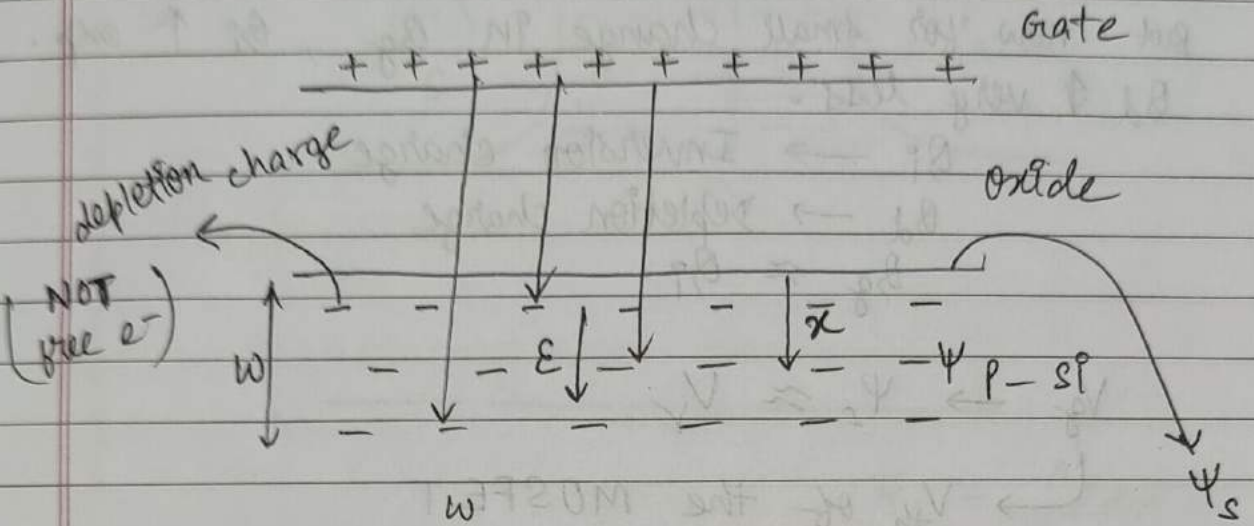


These diodes are zero biased
⇓
No current

As there is p.d., there will be $\vec{E}$ but its magnitude will remain same in oxide. As there are no charges in oxide, +ve

If +ve voltage ↑, width of −ve charge increases

⇒ ~~Det~~ Depletion Region width in ~~body~~ silicon ↑



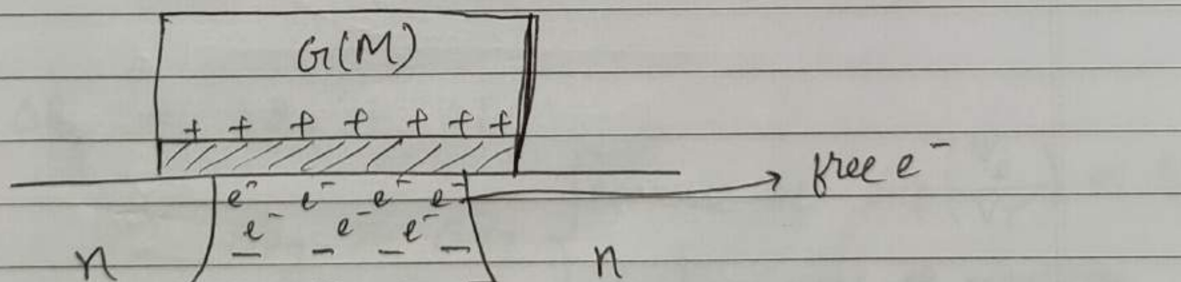
$$\psi_s = \int_{x=0}^{w} \mathcal{E}\, dx$$

Potential at Si − SiO_2 interface

$$\psi < \psi_s$$

If voltage is ↑, ψ at each layer in P−Si ↑ .

For certain V_g, $\psi_s \geq$ Barrier potential (cut-in voltage)



The free e^-s in channel $\longrightarrow$ Inversion charge

$$Q_g = Q_d + Q_i$$

But now for small change in Q_g, $Q_i \uparrow$ exp.
$Q_d \uparrow$ very less.

$Q_i \longrightarrow$ Inversion charge

$Q_d \longrightarrow$ Depletion charge

$Q_g \approx Q_i$

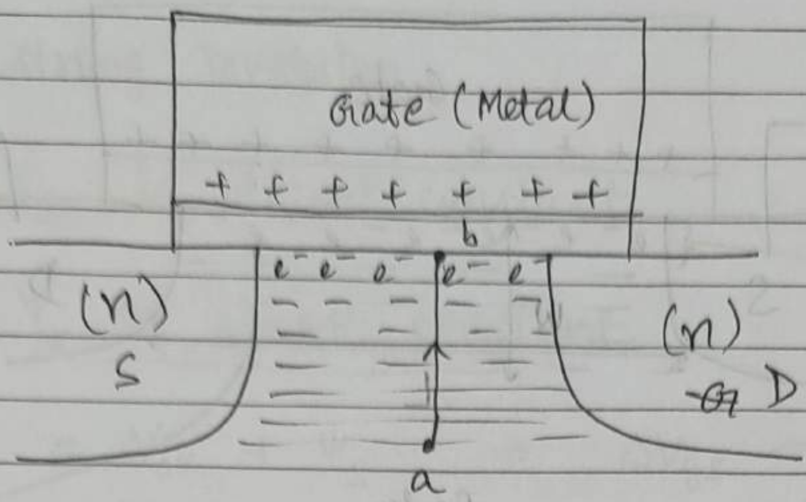
$V_g \rightarrow \Psi_s \approx V_r$

$\hookrightarrow V_{th}$ of the MOSFET

$$V_g = \varepsilon_{ox} \, t_{ox} + \Psi_s$$

If thickness of oxide $\uparrow \Rightarrow V_{th} \uparrow$

If doping density $\downarrow \Rightarrow V_{th} \downarrow$



$$\Psi_s = \int_a^b \mathcal{E}\, dx$$

free
Electron charge at interface → Inversion charge

If $V_g \uparrow$ → Q_d increases slightly

→ small increase in Ψ_s

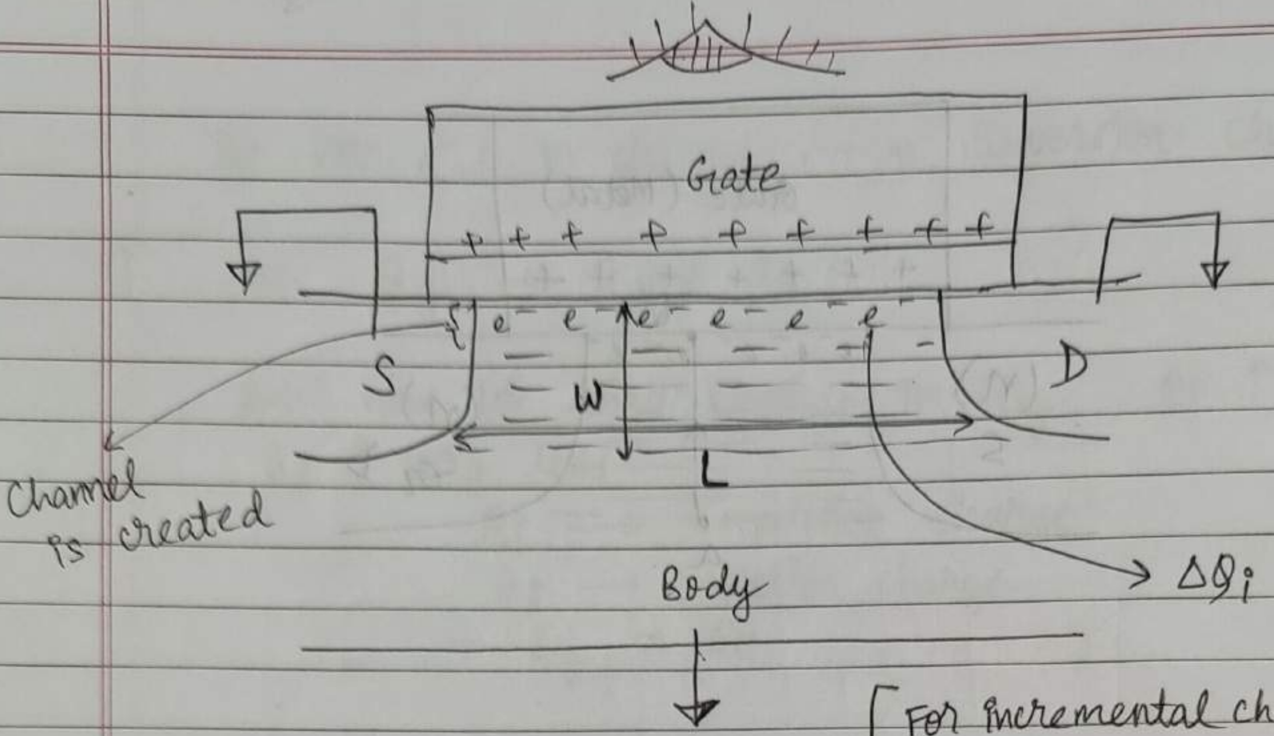
⇓

Exponential increase in Q_i

$$\Delta Q_g = \Delta Q_d + \Delta Q_i$$

$\Rightarrow \Delta Q_g \approx \Delta Q_i$ { Because of $\exp\left(\frac{\Psi_s}{V_T}\right) \propto Q_i$

↳ excess minority conc. ~~charge~~



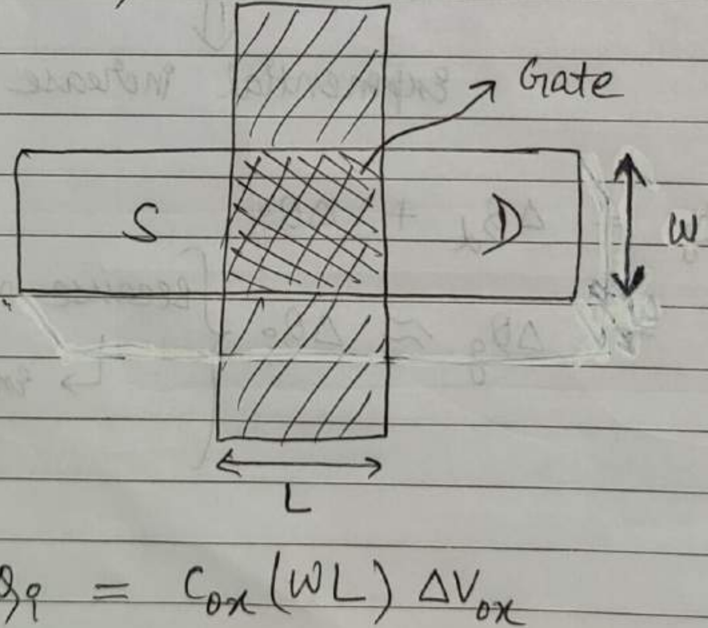
$\Delta Q_g \approx \Delta Q_i$

[For incremental charge, it behaves as capacitor]

$$C_{ox} \text{ (per unit area)} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}$$

$\cancel{\Delta Q_i = C_{ox} \in C_{ox}}$

From top-view,



$$\Delta Q_i = C_{ox}(WL)\,\Delta V_{ox}$$

After strong inversion,

→ Q_d is almost constant

→ Ψ_s is almost constant

$$V_{gs} = V_{ox} + \Psi_s \Rightarrow \Delta V_{gs} \approx \Delta V_{ox}$$

$$\Delta Q_i = C_{ox} WL \Delta V_{gs}$$

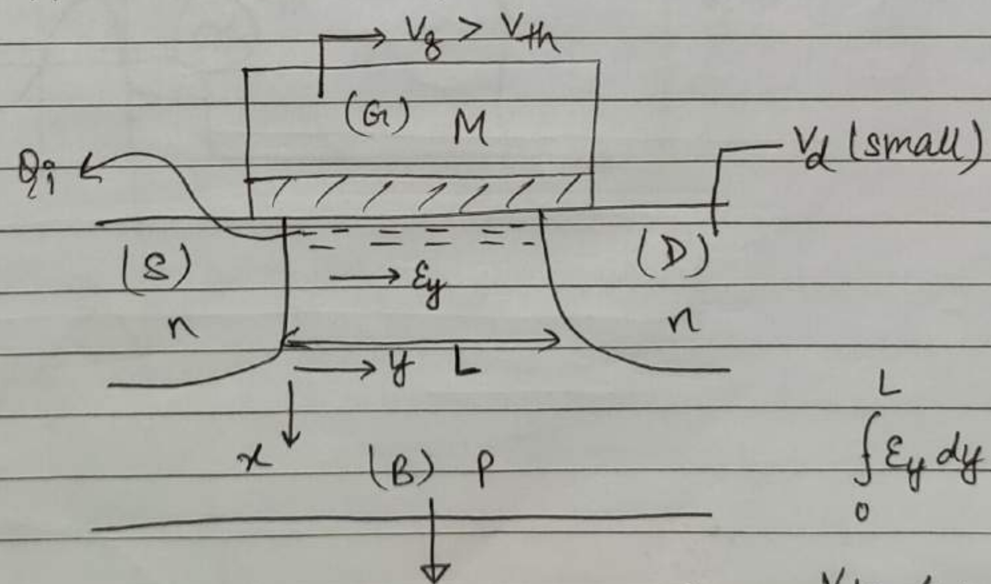
<u>Threshold Voltage</u>

$$\Psi_s = V_r \longrightarrow V_{gs} = V_{th}$$

$$\Delta Q_i = C_{ox} \Delta V_{gs} \quad \text{(Per unit area)} \quad [C/cm^2]$$

$$V_g = V_{th} \longrightarrow Q_i = 0$$ (Because it is just forward biased)

$$Q_i = C_{ox} (V_{gs} - V_{th}) \quad \text{(Per unit area)}$$



$$\int_0^L \varepsilon_y \, dy = V_{ds}$$

$$\varepsilon_y \approx \frac{V_{ds}}{L}$$ (for small values of V_{ds})

per unit area

$$J = Q_i \cdot V_d = (\mu_n \mathcal{E}_y) Q_i$$

$$= \mu_n \left(\frac{V_{ds}}{L}\right) C_{ox} (V_{gs} - V_{th})$$

$$I_D = Q_i \cdot V_d \cdot W$$

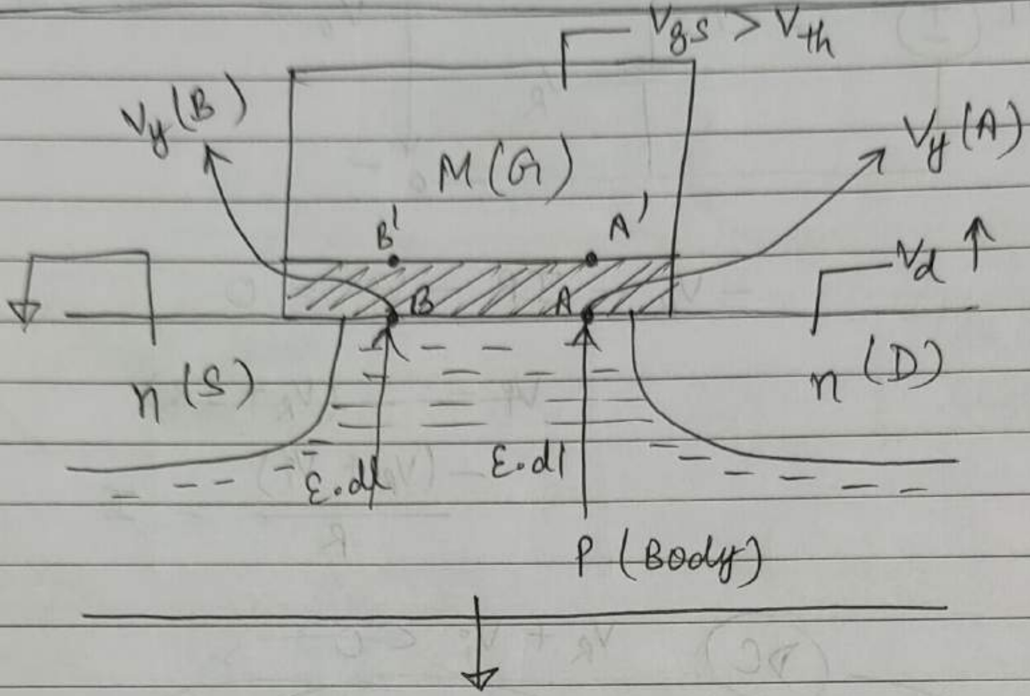
$$= (\mu_n \mathcal{E}_y) Q_i \cdot W$$

$$\boxed{I_d = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{gs} - V_{th}) V_{ds}}$$ (Linear Regime)

We assume Q_i is same everywhere in b/w source & drain. Hence, $\mathcal{E}_y \approx \frac{V_{ds}}{L}$ (As current is same everywhere)

Now V_{ds} is not small

~~Open Circuit Test~~ $\Rightarrow$ No longer Linear Regime



$$V_y(A) > V_y(B)$$

$$\Rightarrow \int_A \varepsilon \cdot dl > \int_B \varepsilon \cdot dl$$

As depletion ions are fixed ε_A can't be different than ε_B

$\Rightarrow$ Depletion Region (A) > Depletion Region (B)

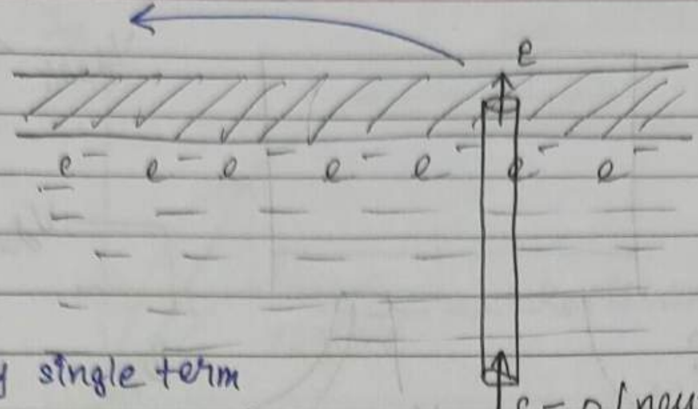
But $\int_{A'} \varepsilon \cdot dl = \int_{B'} \varepsilon \cdot dl$

$$\Rightarrow \underset{(A \cdot A')}{V_{ox}} < \underset{(B \cdot B')}{V_{ox}}$$

$$\Rightarrow \underset{(A - A')}{\varepsilon_{ox}} < \underset{(B - B')}{\varepsilon_{ox}}$$

Channel is very long $\Rightarrow E_y$ is very small

$\Rightarrow$ Neglect horizontal component



$\mathcal{E} \propto Q_{cyl.}$

$\mathcal{E} = 0$ (neutral region)

In flux, only single term

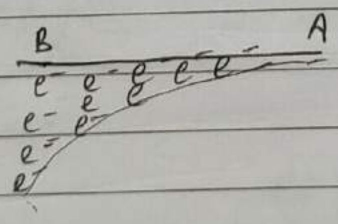
$\Rightarrow \mathcal{E}_{ox}(ds) \propto Q_{total}$

$$\underset{(A)}{Q_{cyl.}} < \underset{(B)}{Q_{cyl.}} \quad \left[\text{As } \mathcal{E}_{ox\,(A)} < \mathcal{E}_{ox\,(B)}\right]$$

$$\left.\begin{aligned} &(Q_i + Q_d)_A < (Q_i + Q_d)_B \\ &\text{But we know, } (Q_d)_A > (Q_d)_B \\ &(Q_i)_A < (Q_i)_B \end{aligned}\right\} \text{Magnitude-wise}$$

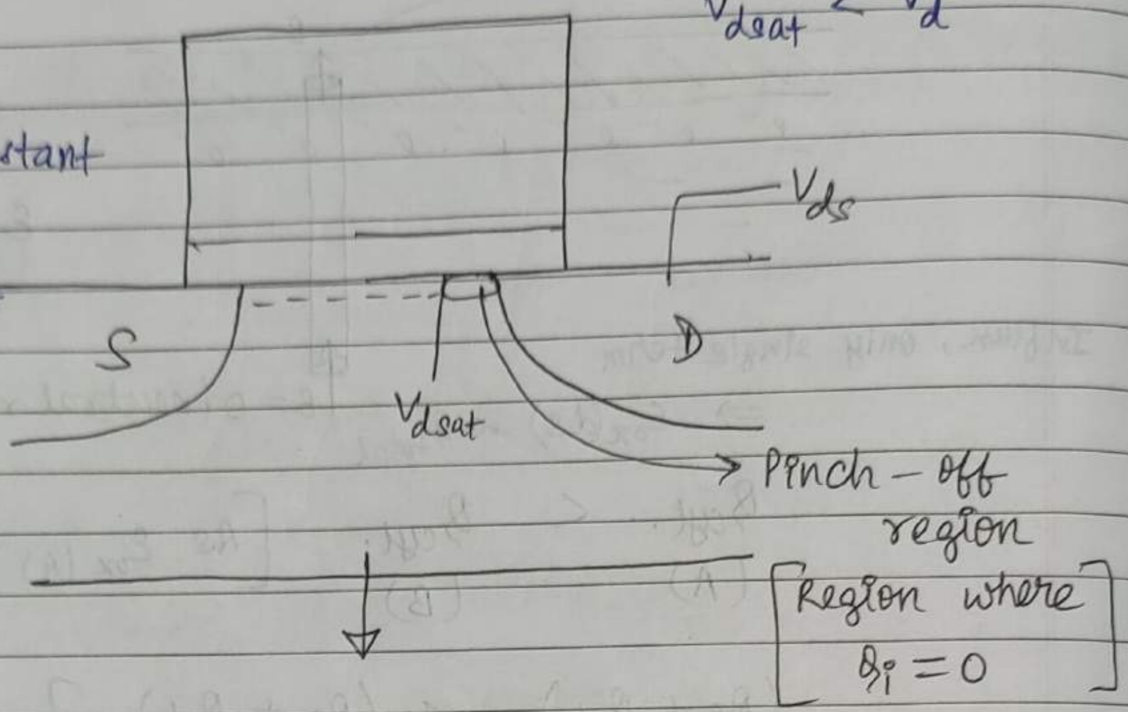
As $V_d \uparrow$, $(Q_i)_A \downarrow$ $\Rightarrow$ At some V_d, $(Q_i)_A = 0$

But even then current will flow due to $\vec{\mathcal{E}}$.



$$\frac{V_d - V_{dsat}}{x} = \text{constant}$$

x → length of Pinch-off

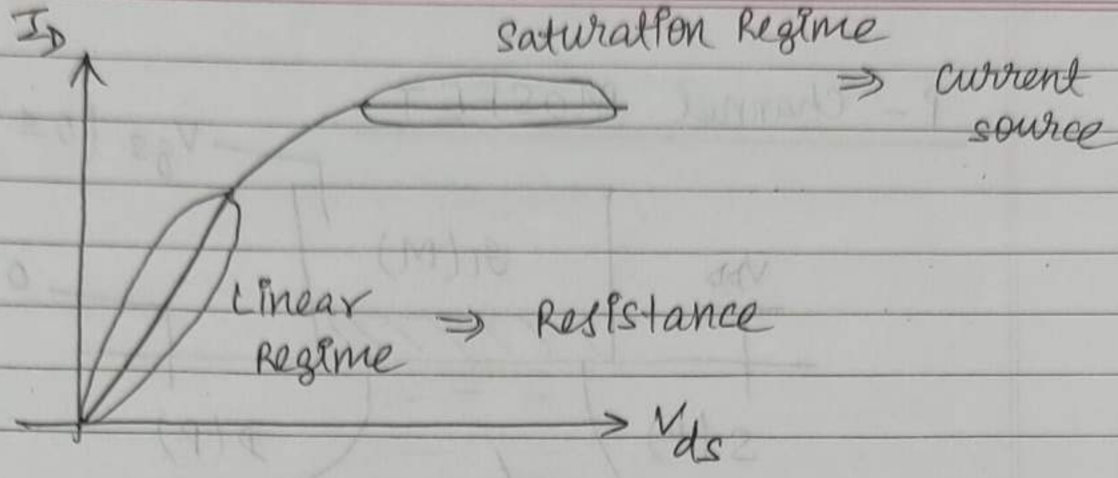


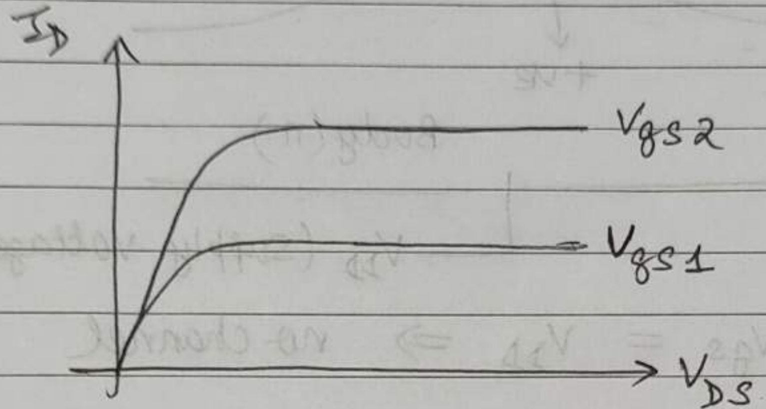
If $V_d \uparrow$, pinch-off region increases in length but again ends at V_{dsat}.

→ Pinch-off region extends slowly with V_{ds}

→ I_D flows due to $\mathcal{E}$-field profile from S to pinch-off point

↳ $V_{DS} \uparrow$, I_D is almost constant

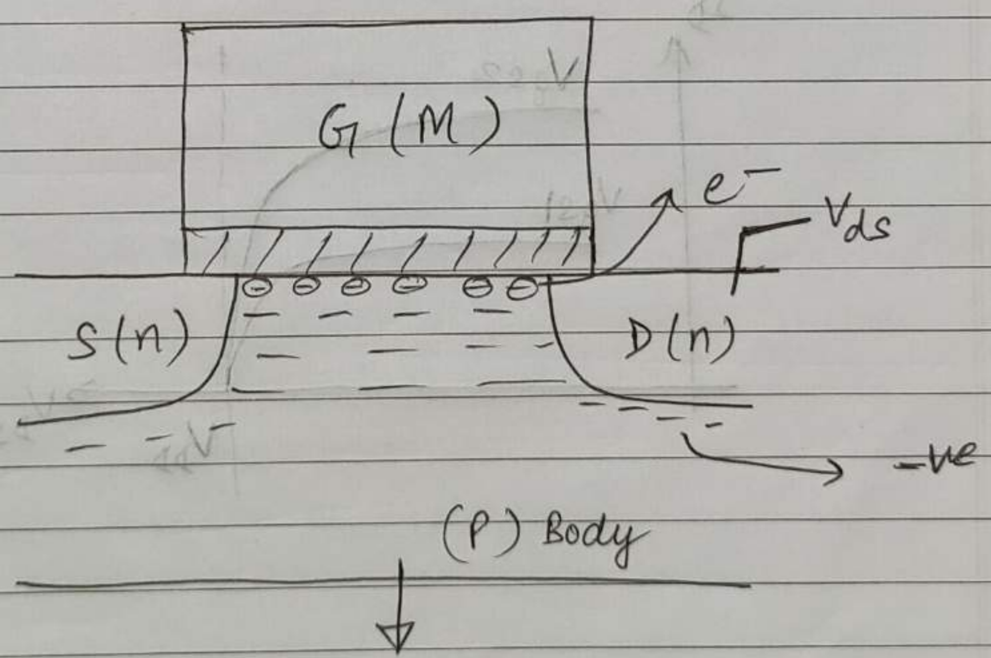




$V_{gs2} > V_{gs1}$

{ Because for higher V_{gs}, higher Q_i }

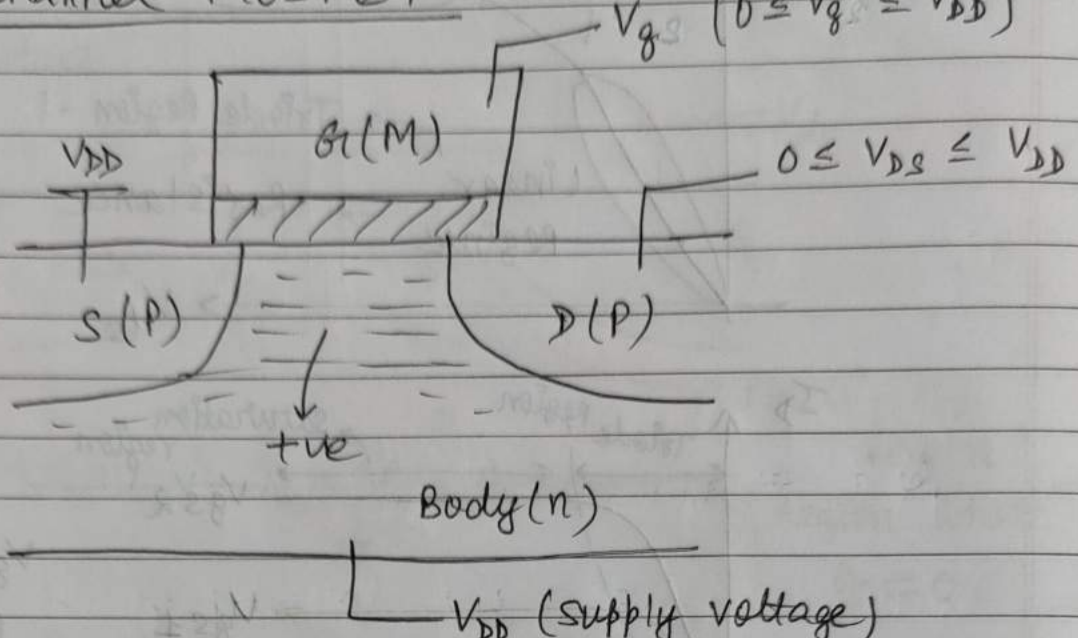
N-Channel Device



NOTE :

Gate offers only a capacitance (No resistance)

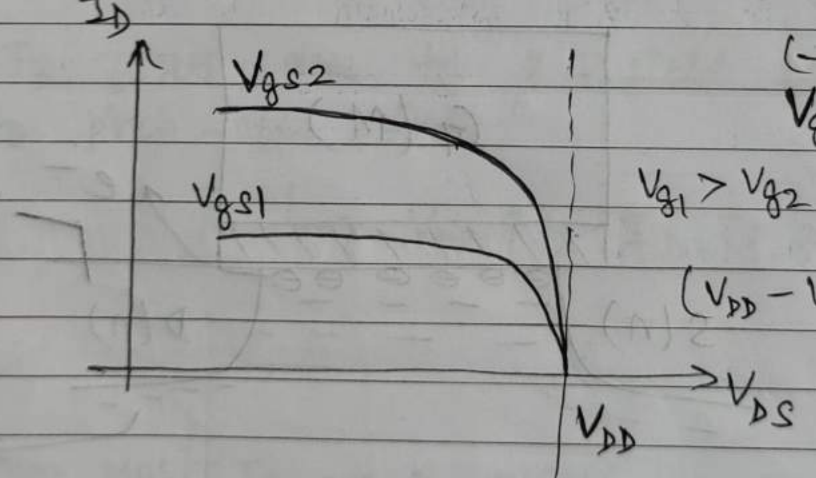
P – Channel MOSFET



when $V_{gs} = V_{DD} \Rightarrow$ no channel

when $V_{gs} \downarrow \Rightarrow$ channel formed

& +ve charge carrier $\uparrow$



(−ve) > (−ve)

V_{gs1} V_{gs2}

$V_{g1} > V_{g2}$ $\cancel{V_{g1} > V_{g2}}$

$\Downarrow$

$(V_{DD} - V_{g1}) < (V_{DD} - V_{g2})$

PMOS

$$V_{gs} = V_g - V_s = \overset{(G)}{V_g} - \overset{(S)}{V_{DD}} \longrightarrow (-ve)$$

$$V_{ds} = V_d - V_s = V_d - V_{DD} \longrightarrow (-ve)$$

As $V_g \downarrow$ from V_{DD} to 0, at some value, channel is formed.

$$Q_i = -C_{ox}(\overset{(-ve)}{V_{gs}} - \overset{(-ve)}{V_{thp}})$$

$$(or) \quad Q_i = C_{ox}[V_{DD} - V_g - |V_{thp}|]$$

$$\cancel{I_D = \mu_p C_{ox}} \qquad I_D = \mu_p \frac{|V_{DS}|}{L} Q_i W$$

$$\boxed{I_D = \mu_p C_{ox}\left(\frac{W}{L}\right)\left[V_{DD} - V_g - |V_{thp}|\right]}$$

⇒ current direction is reverse as compared to that in NMOS