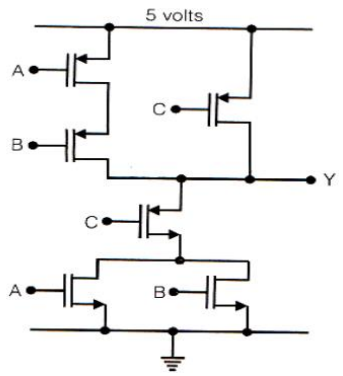
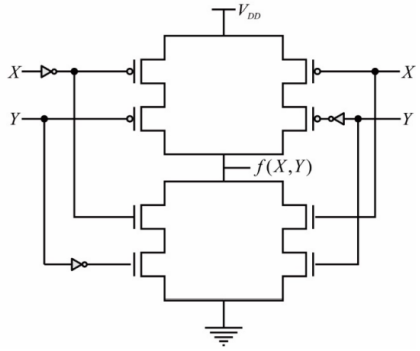
Tutorial-3

Question 1: Find out the expression for the output (Y)



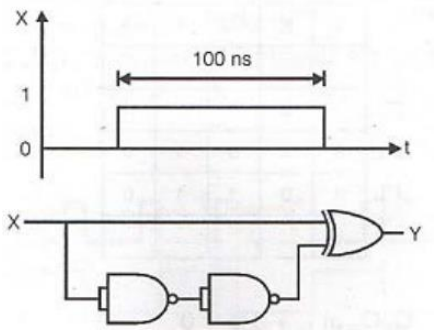
Question 2: The logic function f (X, Y) realized by the given circuit is?



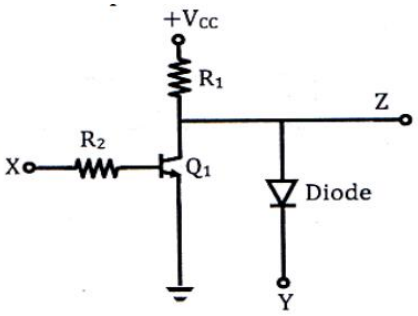
Question 3: Using Kmap, convert the following standard POS expression into a minimum POS expression, a standard SOP expression, and a minimum SOP expression.

$(\overline{A}+\overline{B}+C+D)\ (A+\overline{B}+C+D)\ (A+B+C+\overline{D})\ (A+B+\overline{C}+\overline{D})\ (\overline{A}+B+C+\overline{D})\ (A+B+\overline{C}+D)$

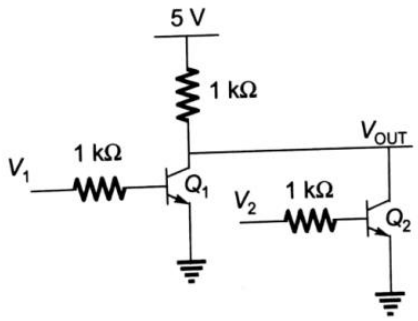
Question 4: The digital circuit shown in the figure is fed with the waveform X (also shown). All gates have an equal propagation delay of 10ns. What will be the waveform of the output (Y)?



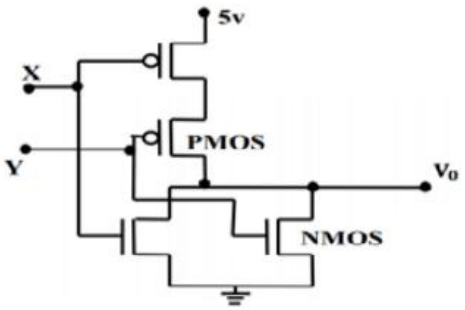
Question 5: In the circuit shown below, Q_1 has negligible collector –to –emitter saturation voltage and the diode drops negligible voltage across it number forward bias. If V_{cc} is +5V, X and Y are digital signals with 0 Vas logic 0 and V_{cc} as logic 1, then the Boolean expression for Z is?



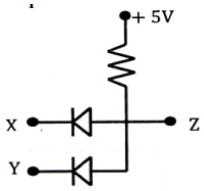
Question 6: The logical gate implemented using the circuit shown below where V_1 and V_2 are inputs (with 0V as digital 0 and 5V as digital 1). Find out the values of output (V_{OUT}) for different inputs.



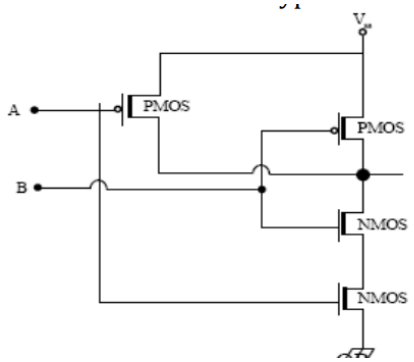
Question 7: A CMOS implementation of a logic gate is shown in the following figure. Which logic gate it represents?



Question 8: The diodes in the circuit shown are ideal. A voltage of 0V represents logic 0 and +5V represents logic 1. The function Z realized by the circuit for inputs X and Y is?



Question 9: The figure is a logic circuit with inputs A and B and output Y. V_{ss} = + 5 V. What type of logic circuit is this?



Question 10: Minimize the following Boolean function- F (A, B, C, D) = ∏ (0,1,2,4,5,7,10,15) using the Max terms reduction technique in K-map. Convert the POS expressions into reduced SOP expressions.