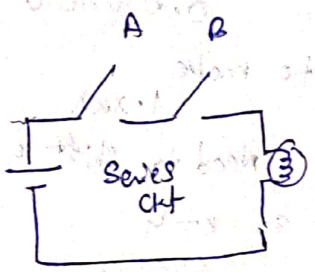
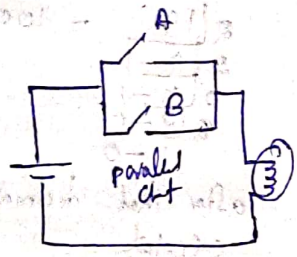
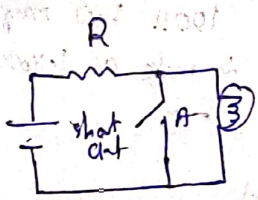
Digital electronics



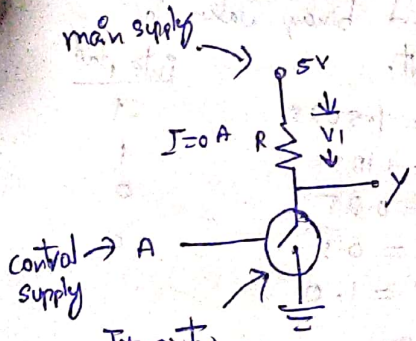
if A AND B are ON, then Bulb is ON



if A OR B is ON, Bulb is ON

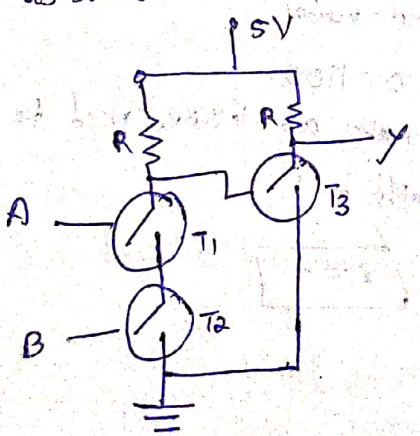


if A is ON, B is OFF
if A is OFF B is ON



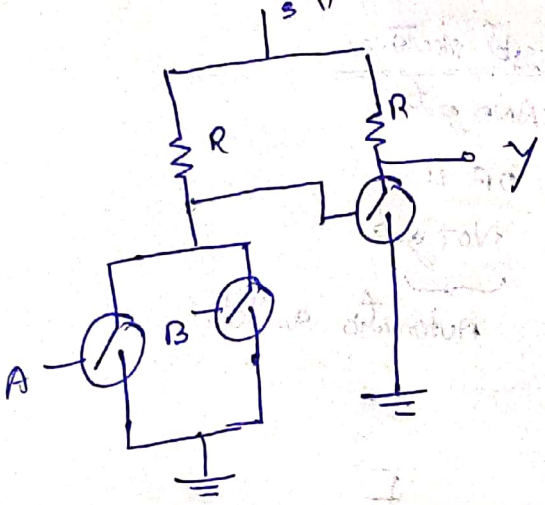
if A=0, Y=1
A=1, Y=0

$Y = V - V_1$ ($V_1 = {}^{0}_{0}$ X P1)
$= 5 - 0$
$Y = 5$

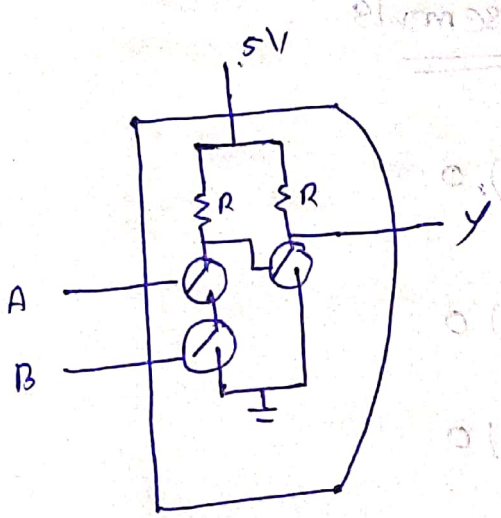


if A=B=0, then T3 will get 5V
then it turned ON Y=0. (bcz it is GND)

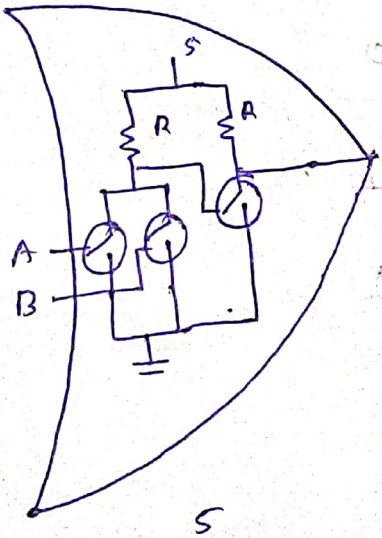
A	B	Y
0	0	0
5V	0	0
0	5V	0
5V	5V	5V



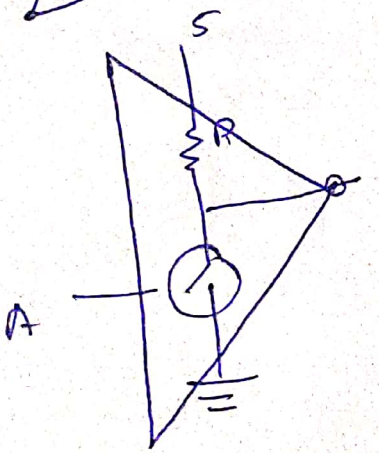
A	B	y
5V	0	5V
0	5V	5V
0	0	0V
5V	5V	5V



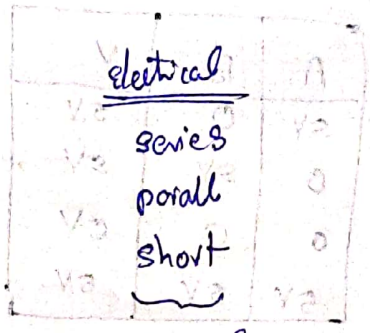
⇒ AND gate



= OR gate



= NOT gate



Electrical

series

parall

short

manual switches

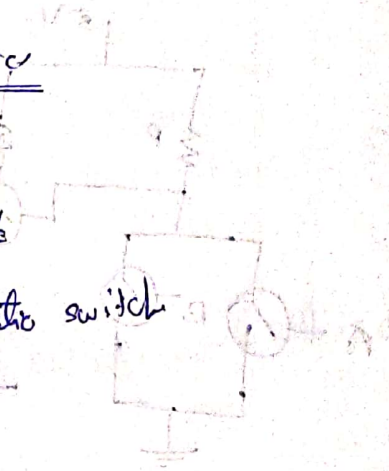
Digital electronics

AND gate

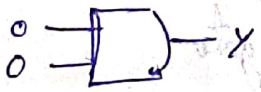
OR "

NOT gate

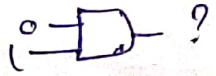
Automatic switch



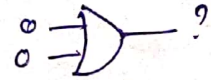
Fundamental Assessements

①  A) 0

②  A) 0

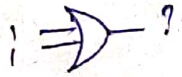
③  A) 0

④  A) 1

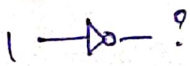
⑤  A) 0

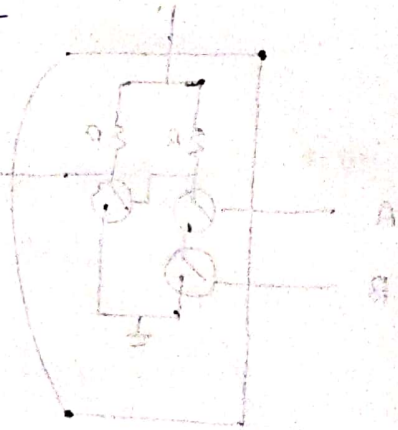
⑥  A) 1

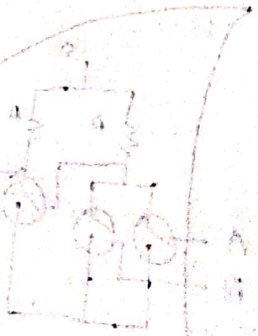
⑦  A) 1

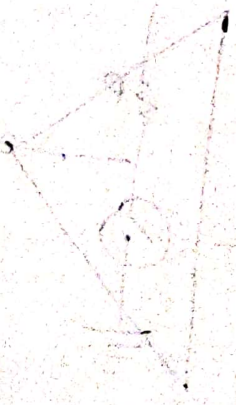
⑧  A) 1

⑨  A) 1

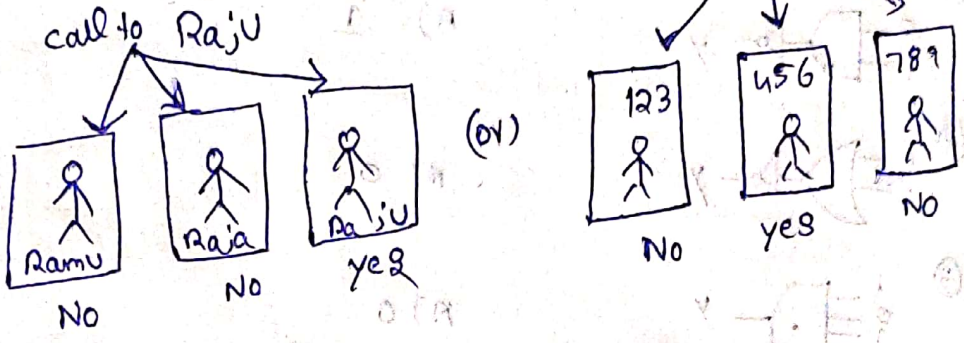
⑩  A) 0



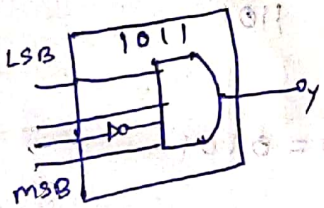


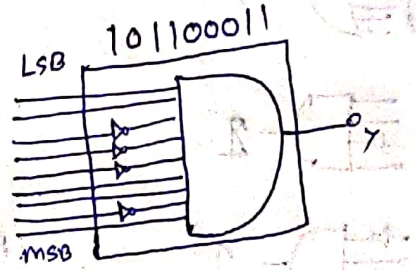


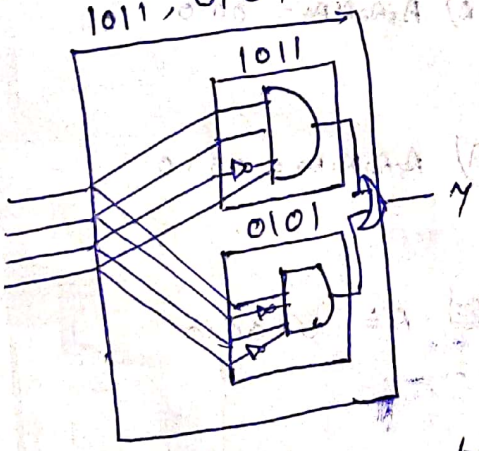
Combinational logic



combinational logic nothing but Binary name



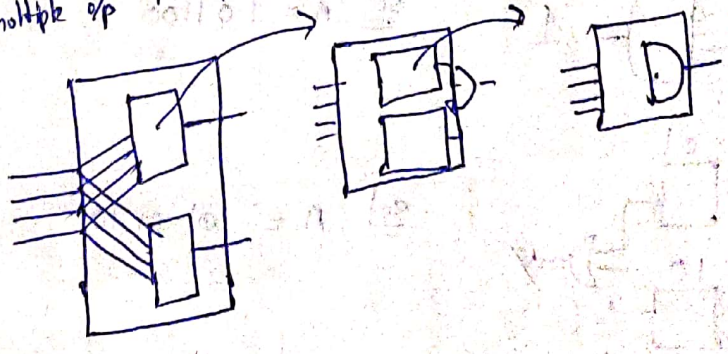


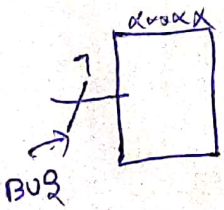


multiple i/p one output

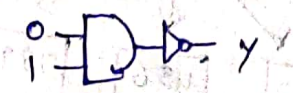
multiple ~~one~~ combination.

multiple i/p multiple o/p multiple combinations

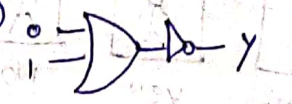




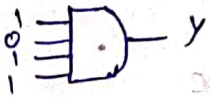
Combinational logic assessments

① 

A) 1

② 

A) 0

③ 

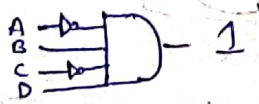
A) 0

④ 

A) 1

⑤ 

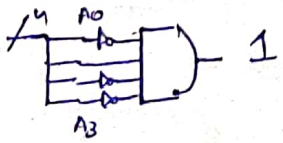
A) x = 1101

⑥ 

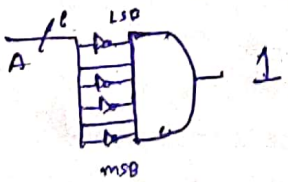
A) ABCD = 0101

⑦ 

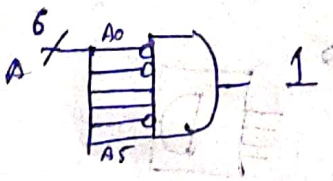
A) $A_3A_2A_1A_0$ = 0010

⑧ 

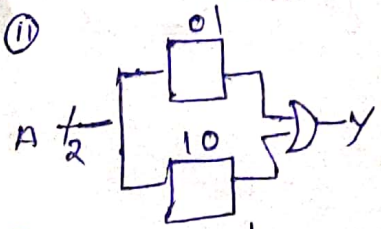
A) $A_3A_2A_1A_0$ = 0010

⑨ 

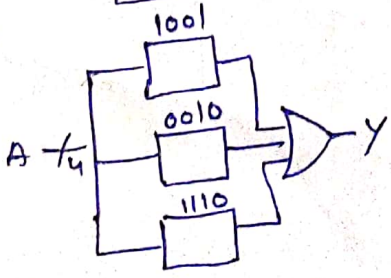
Sol A = 010010

⑩ 

Sol A = 101100

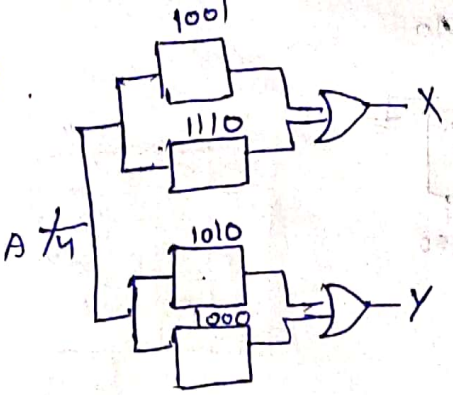
⑪ 

Sol A = 01 or 10

⑫ 

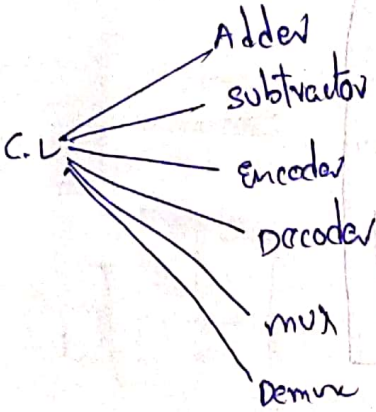
Sol 1001 or 0010 or 1110

(13)

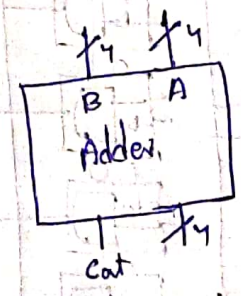


Sol (1001 or 1110), (1010 or 1000)

Application of logic



Adder



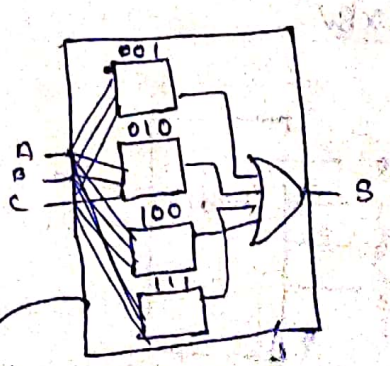
C_{in}	B	A	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

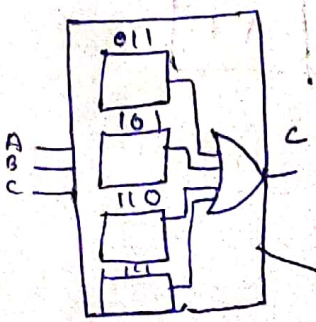
Sum truth table

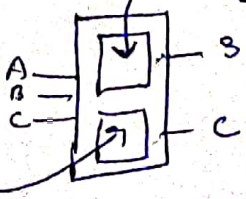
C_{in}	B	A	S
0	0	1	1
0	1	0	1
1	0	0	1
1	1	1	1

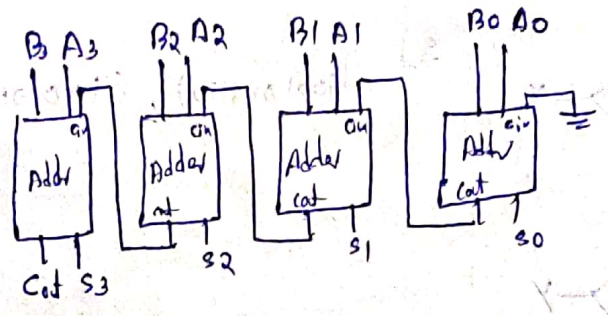
Cout table

C_{in}	B	A	Cout
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	0

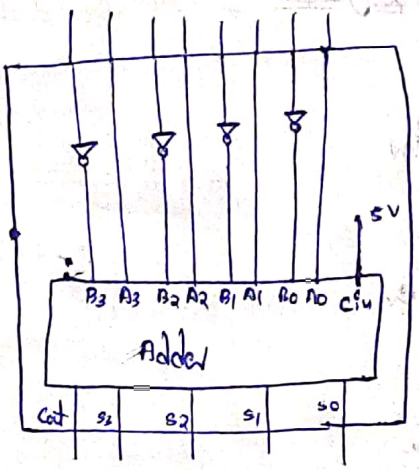




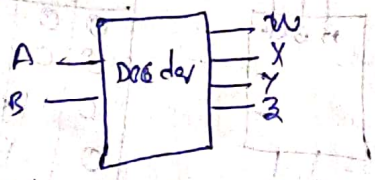




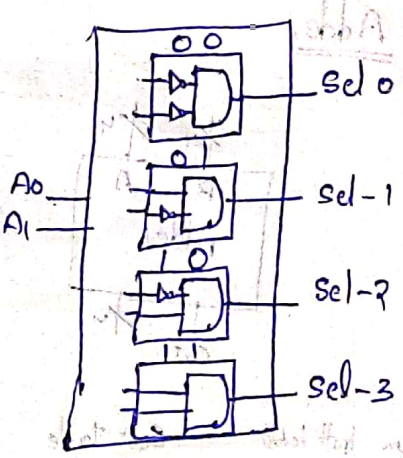
Subtration



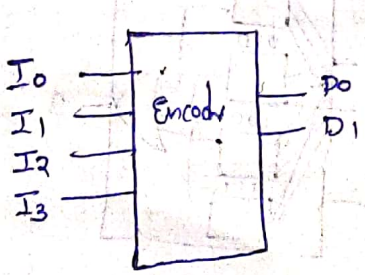
Decoder



0 0	sel 0 = 1
0 1	sel 1 = 1
1 0	sel 2 = 1
1 1	sel 3 = 1

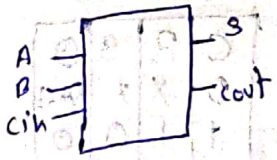


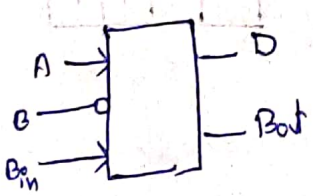
Encoder

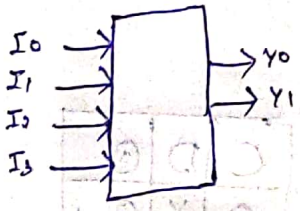


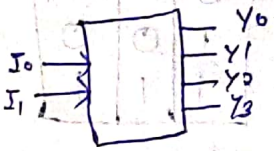
$I_3 I_2 I_1 I_0$	$D_1 D_0$
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1

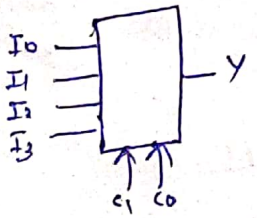
Combinational logic assessement

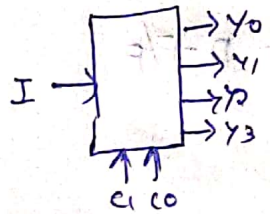
① 

② 

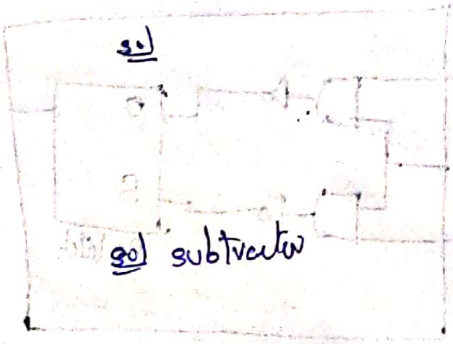
③ 

④ 

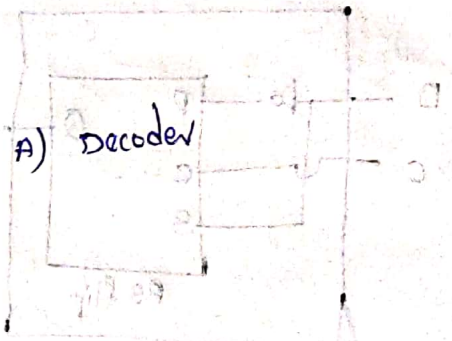
⑤ 

⑥ 

sol

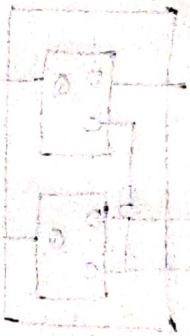


A) Encoder

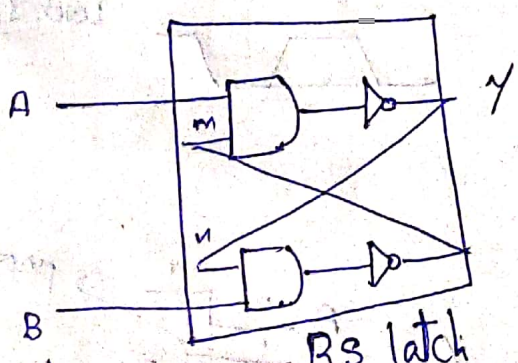


A) Decoder

A) mux



Sequential logic



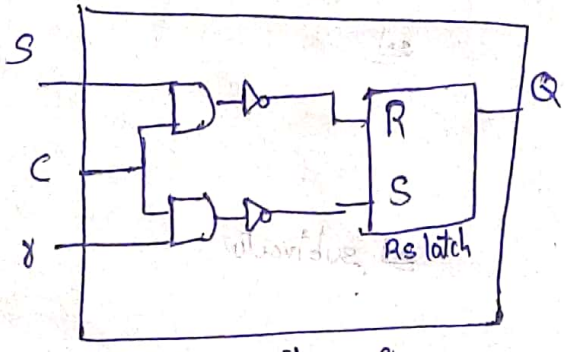
R S Qn

A	B	Y
1	0	0
1	1	0
0	1	1
1	1	1

stat with zero

1) 11 {after} 10 then y=0

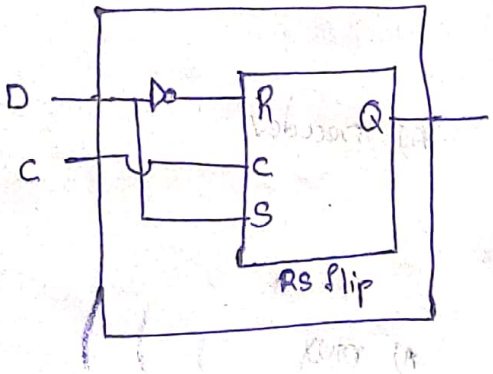
2) 11 {after} 01 then y=1



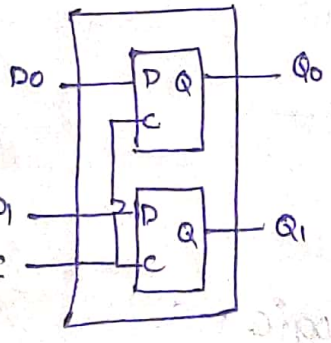
C	R	S	Q
0	X	X	Q_{n-1}
1	1	0	0
1	0	1	1

Rs flip-flop

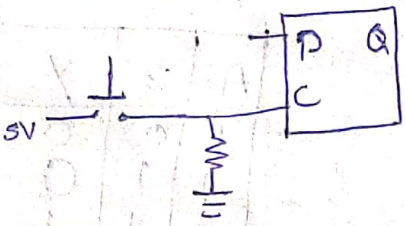
D-Flip flop



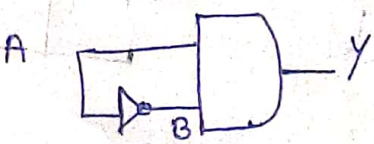
C	D	Q
0	X	Q_{n-1}
1	0	0
1	1	1

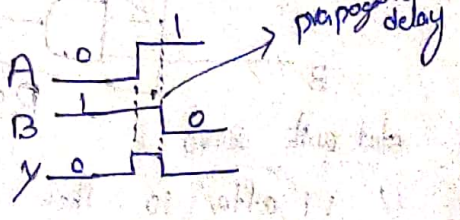


2 bit D-F/F

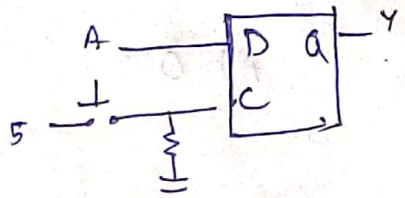


Level flip flop

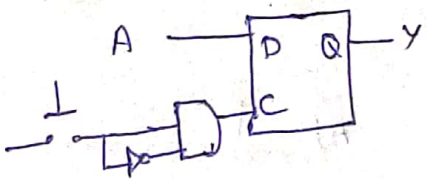




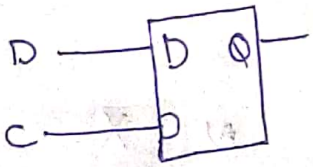
Edge Trigg F/F



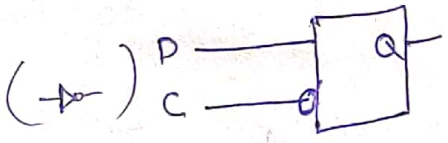
level Trigger F/F



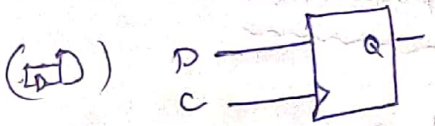
edge Trigger F/F



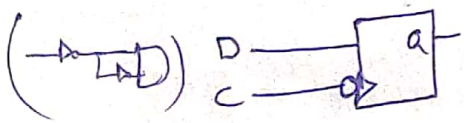
⇒ +ve level Trigger



⇒ -ve level Trigger

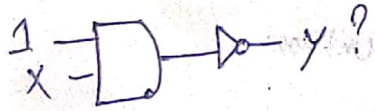


= +ve Trigger

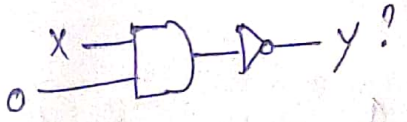


= -ve Trigger

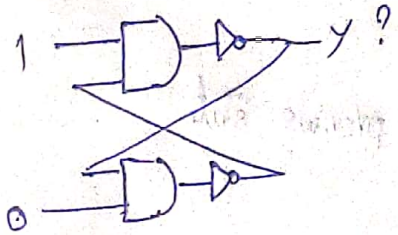
Sequential logic - assessement - 1

① 

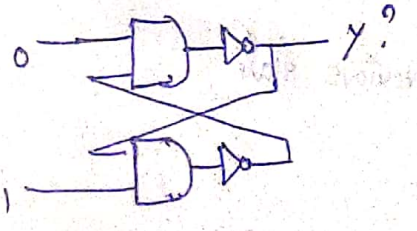
A) X

② 

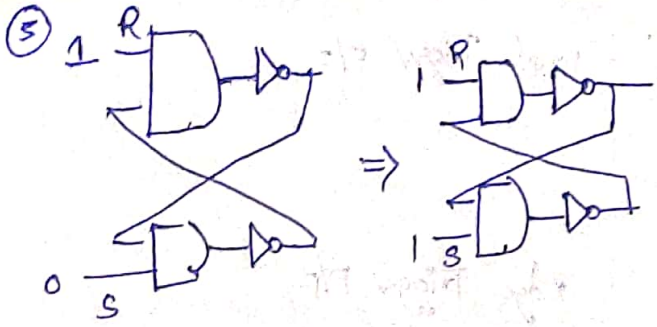
A) 1

③ 

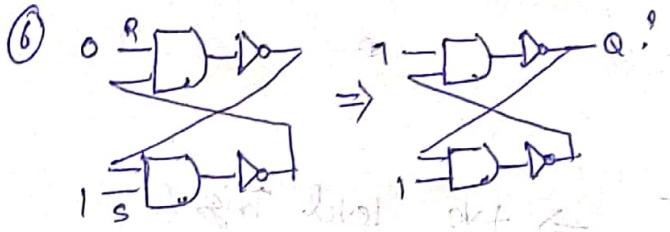
A) 0

④ 

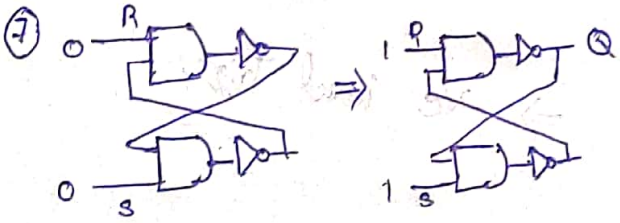
A) 1

(5) 

A) 0

(6) 

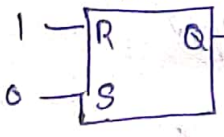
A) 1

(7) 

A) X

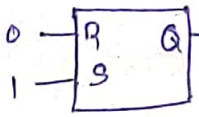
Sequential logic 2 - Assessement

(01) Rs latch



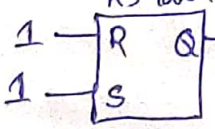
A) 0

(02) Rs latch



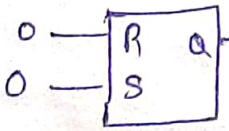
A) 1

(03) Rs latch



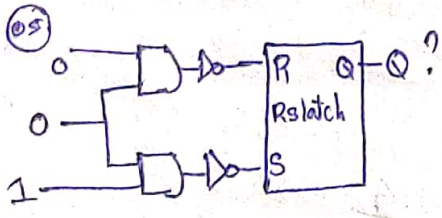
A) Unknown

(04)



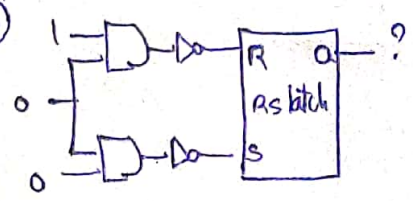
A) 1

(05)

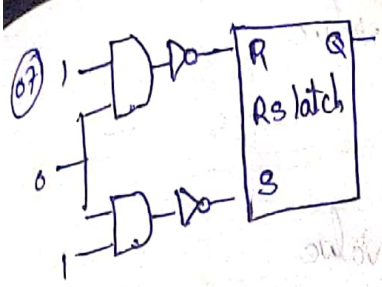


A) previous state

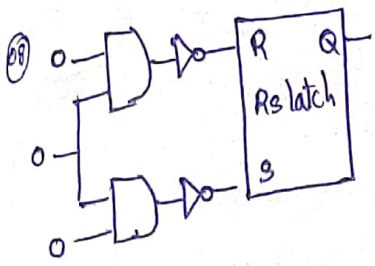
(06)



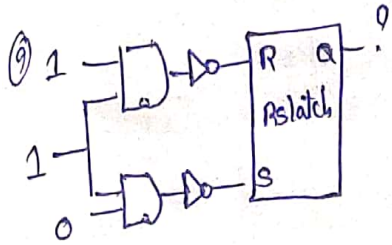
A) previous state

(07) 

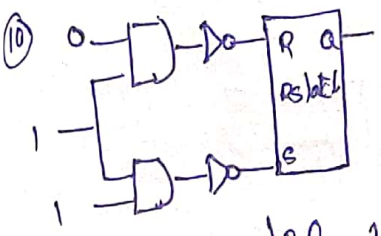
A) previous state

(08) 

A) previous state

(09) 

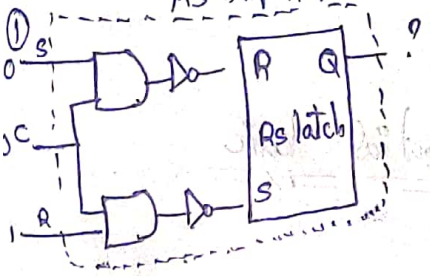
A) 1

(10) 

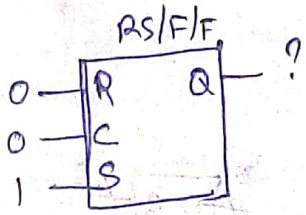
A) 0

Sequential logic problem part-3

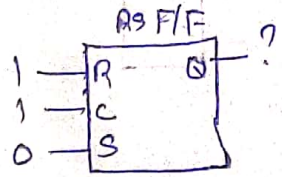
Rs flip flop

(1) 

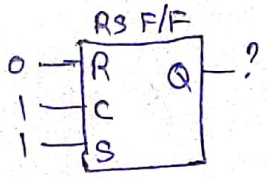
A) previous value

(2) 

A) previous value

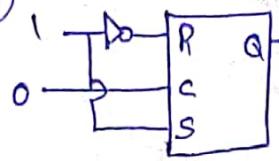
(3) 

A) 0

(4) 

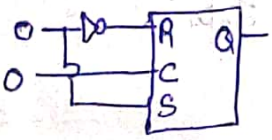
(4) 1

(5) RS F/F



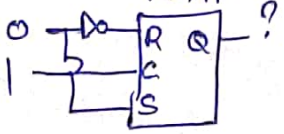
A) previous value

(6) RS F/F



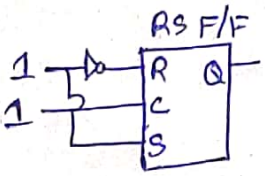
A) previous value

(07) RS F/F



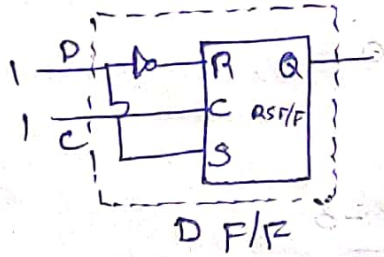
A) zero

(08) RS F/F



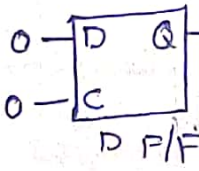
A) one

(9)



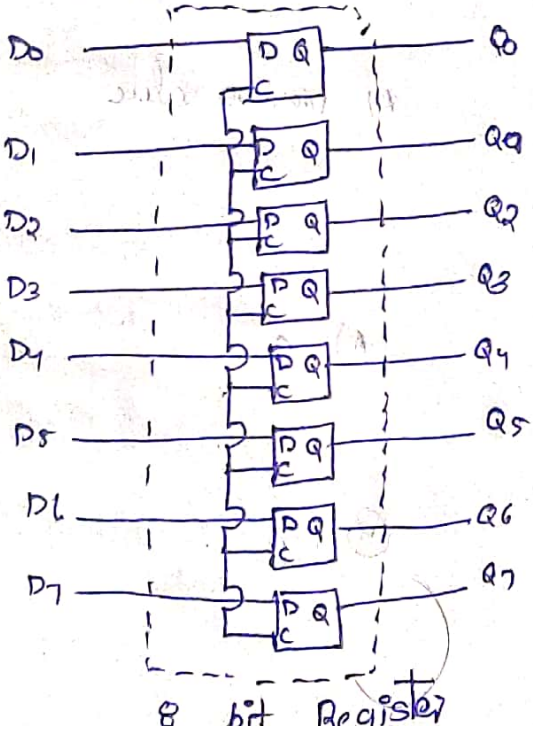
A) one

(10)

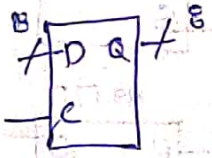


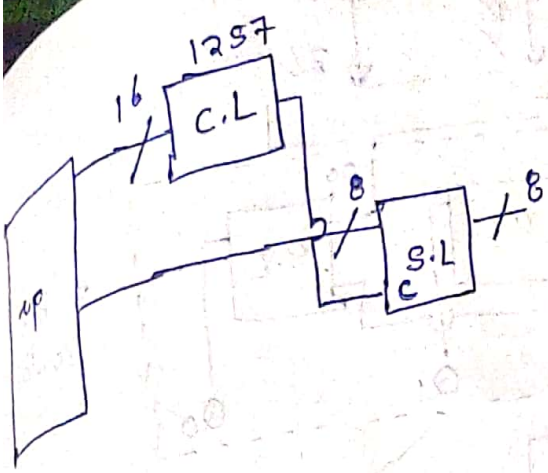
A) previous value

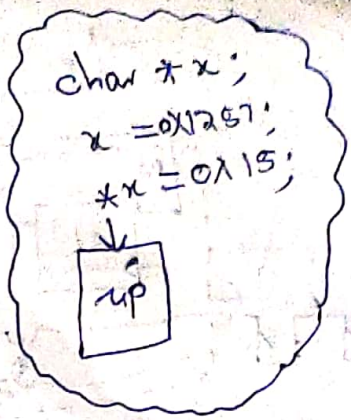
Applications of sequential logic

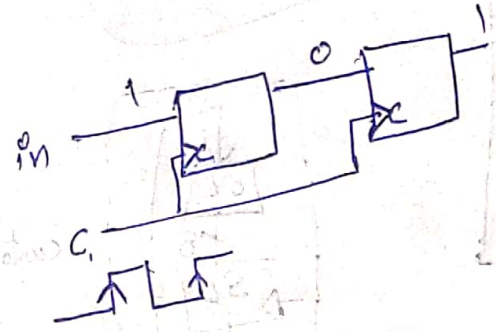


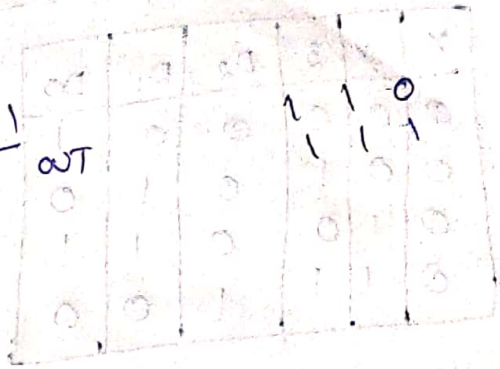
=

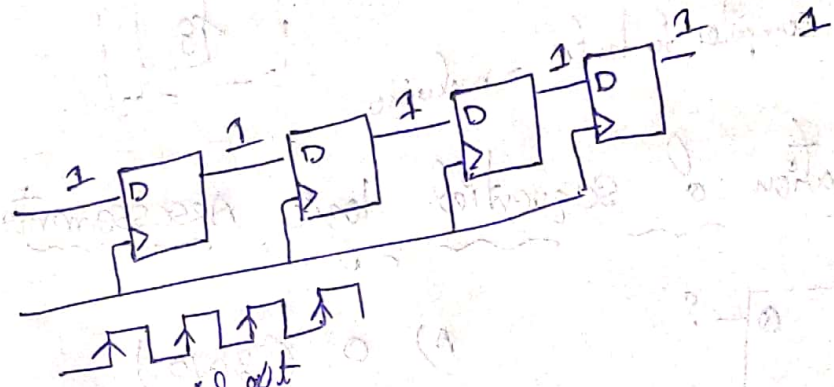






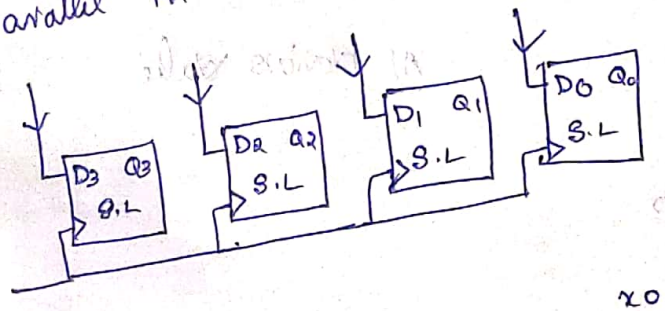


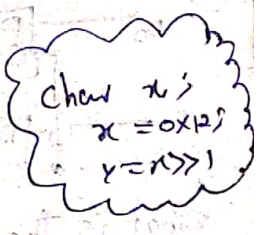


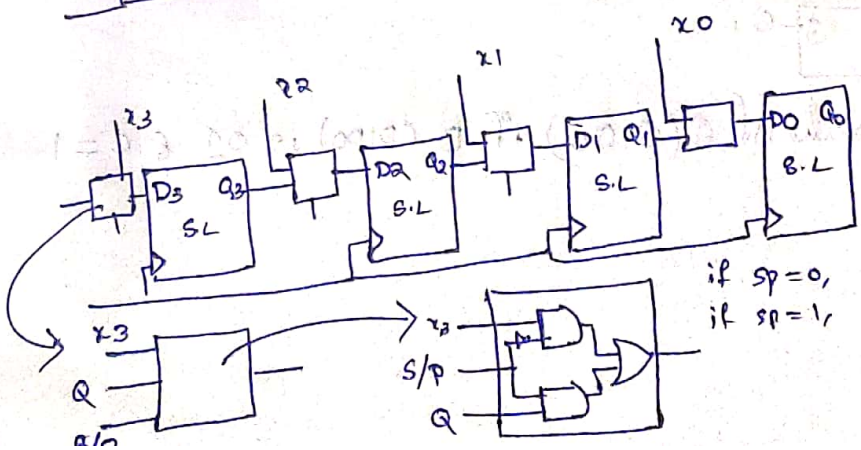


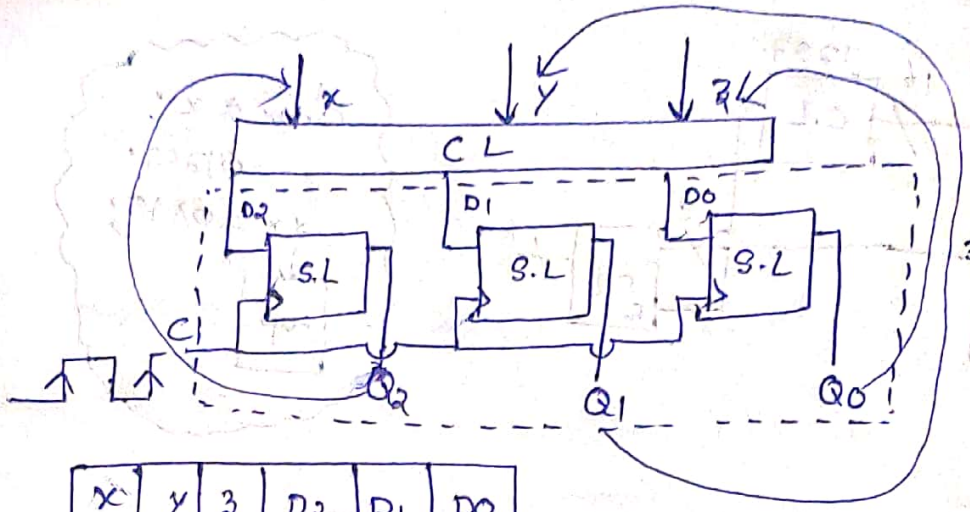
serial in serial out

parallel in

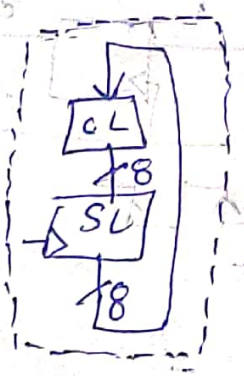








x	y	z	D_2	D_1	D_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0

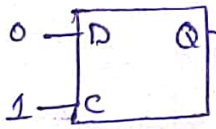


Text book

Digital computer fundamentals - malvino

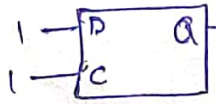
Application of sequential logic Assessments

(01)



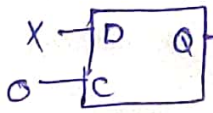
A) 0 (zero)

(2)



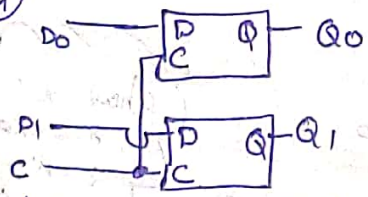
A) One

(3)



A) previous value

(4)



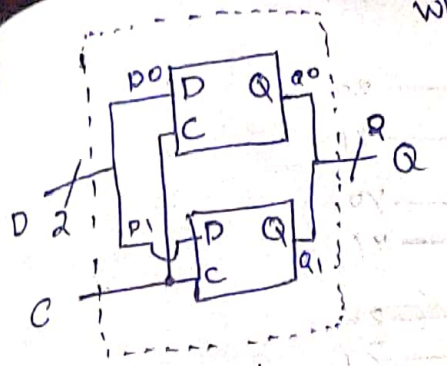
what is the value of Q(Q1Q0), if D (D1D0) is 01 & C = 1

A) 01

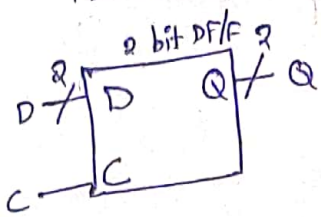
what is the value of Q if D=10 C=1

A) 10

⑤



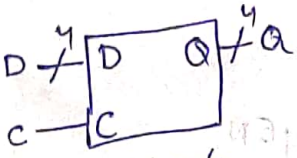
⑥



what is the value of Q if D=10 C=1

A) 10

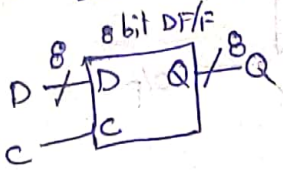
⑦



what is the value of Q if D= 1010 C=1

A) 1010

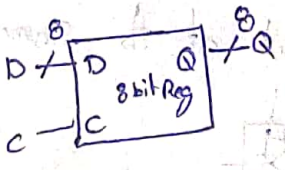
⑧



what is the value of Q if D= 10101010 C=1

A) 10101010

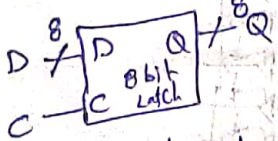
⑨



what is the value of Q if D=10101010 C=0

A) previous state

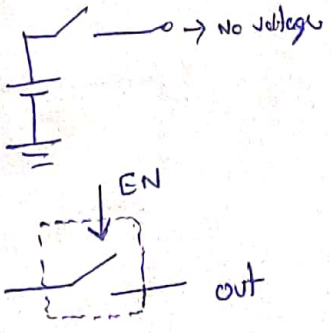
⑩



what is the value of Q if D=01010101 C=1

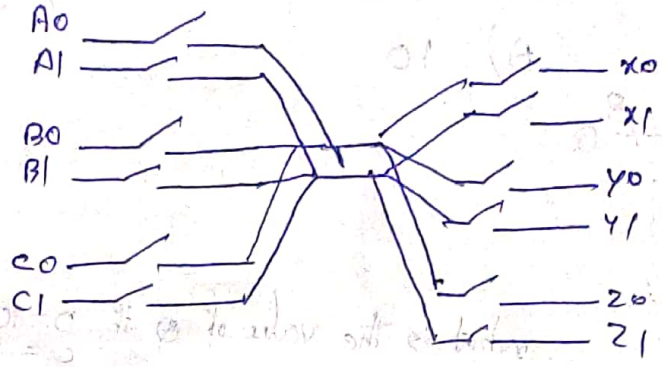
A) 01010101

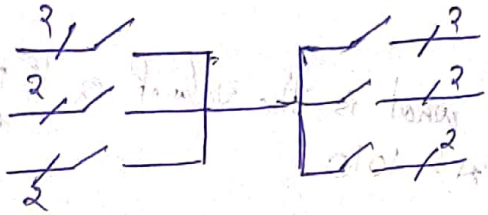
Tristate logic & it's applications

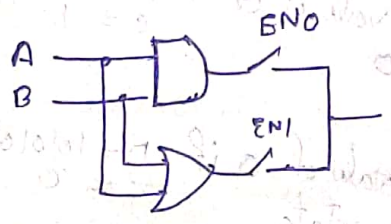


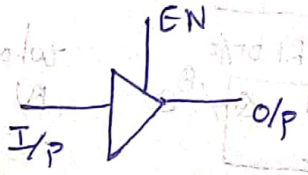
Tristate switch

EN	IN	out
5V	5V	5V
5V	0V	0V
0V	X	No Voltage

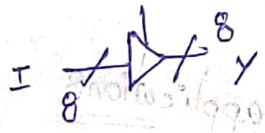


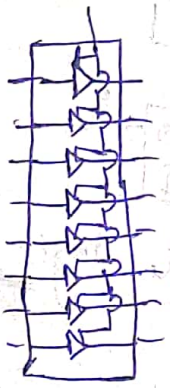


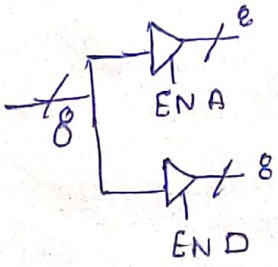


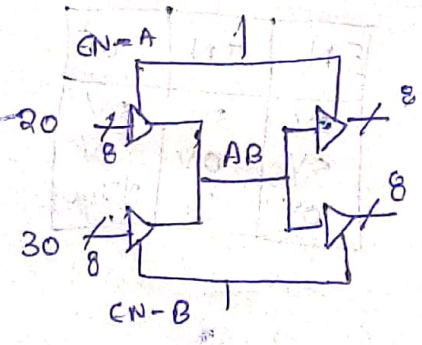


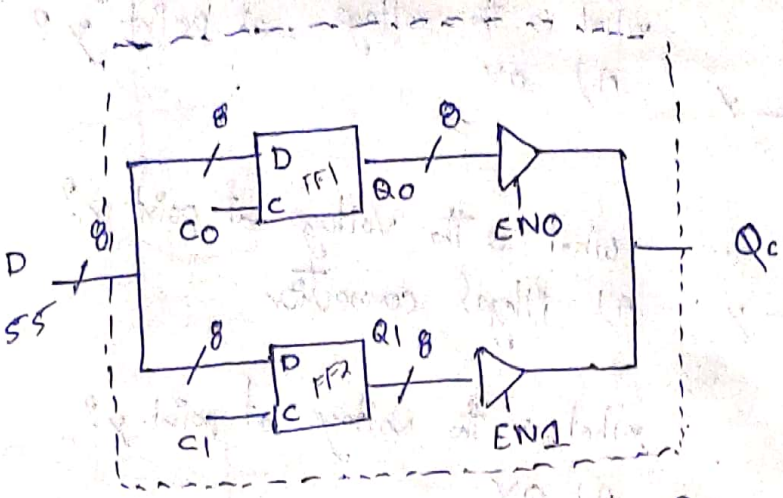
Note Never connect two ~~input~~ output at the same pla without Tristate







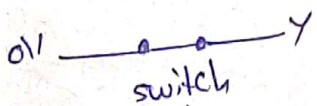




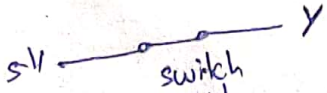
Read write memory (RAM)

D	Co	C1	ENO	EN1	Qo	Q1	Q
55	1	0	0	0			55
65	0	1	0		65	55	
65	0	0	1	0	65	55	65
11	11	11	0	1	65	55	55

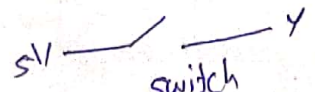
Tristate logic Assessement - 1

1) 

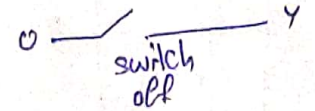
What is the voltage at point y?
A) 0V

2) 

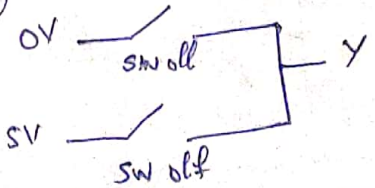
What is the voltage at point y?
A) 5V

3) 

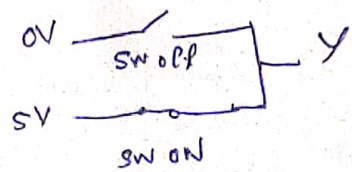
what is the voltage at point y?
A) Floating voltage

4) 

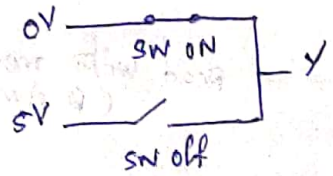
what is the voltage at point y?
A) Floating voltage

5) 

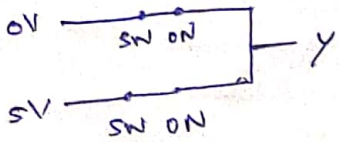
what is the voltage at point y?
A) Floating voltage

6) 

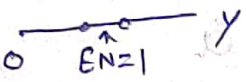
what is the voltage at point y?
A) 5V

⑦ 

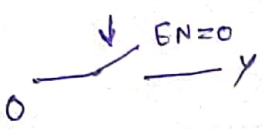
what is the voltage at point y?
A) 0V

⑧ 

what is the voltage at point y?
A) illegal connection

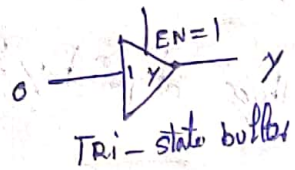
⑨ 

what is the voltage at point y?
A) 0V

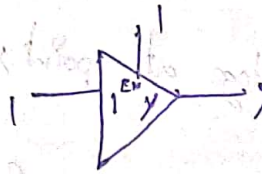
⑩ 

what is the voltage at point y?
A) floating voltage

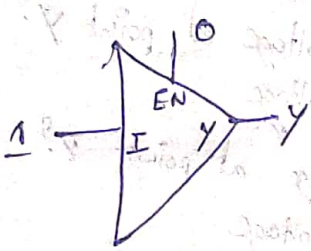
Tristate logic assessment - 2

① 

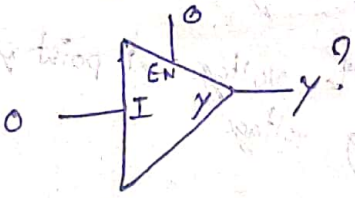
what is the logic value at point y?
A) zero

② 

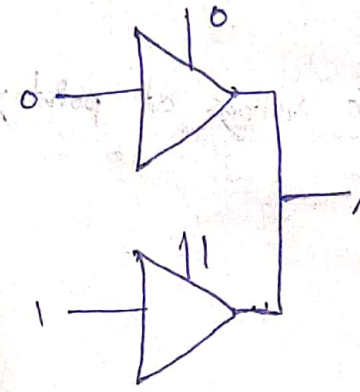
A) one

③ 

A) Floating

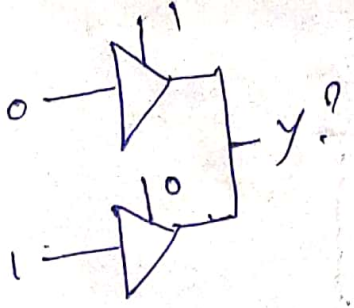
④ 

A) Floating

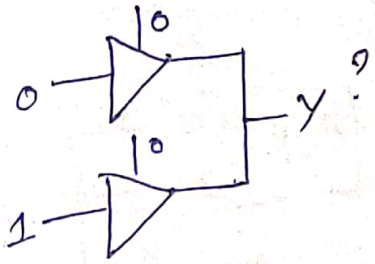
⑤ 

A) One

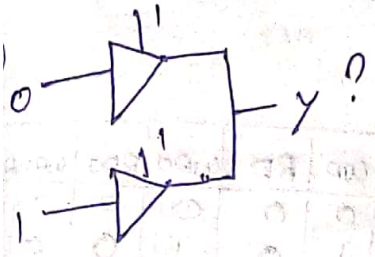
5)



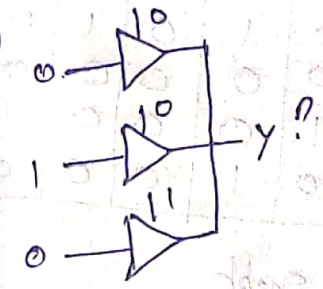
A) zero



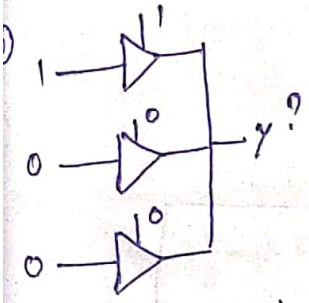
A) Floating



A) illegal conn

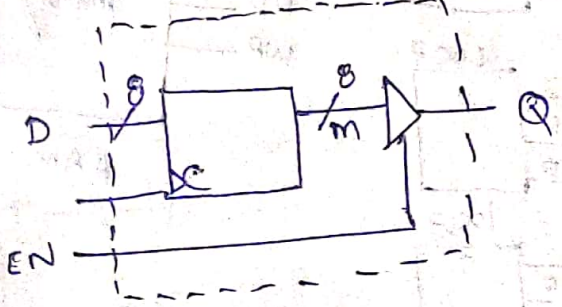


A) zero



A) one

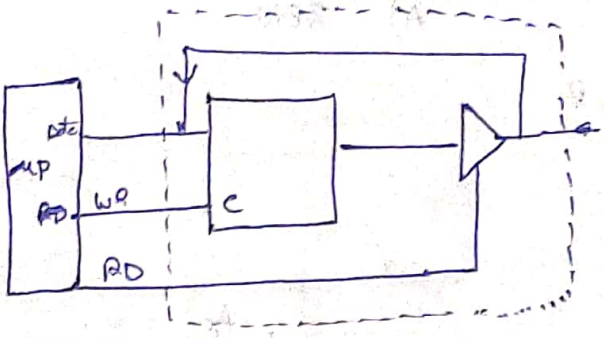
1 Byte Read write memory (RAM)

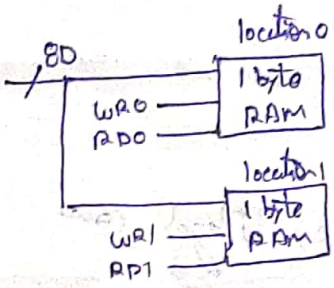


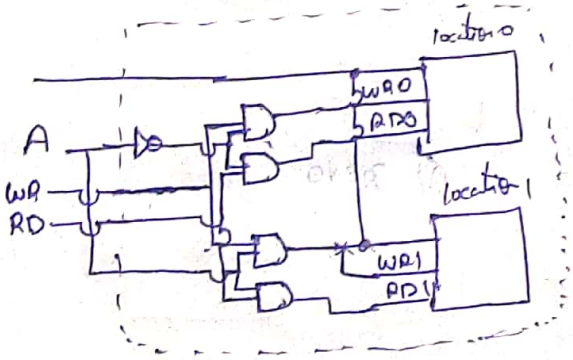
NV = No Voltage

D	C	EN	m	Q
12	1	0	12	NV
X	0	1	12	12
X	0	0	12	NV

when C is 1 = write
EN = 1 = Read
C = EN = 0 store

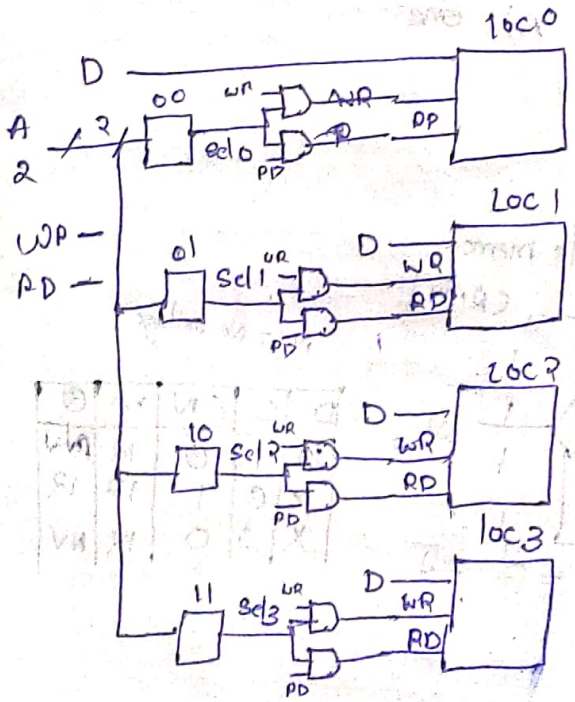


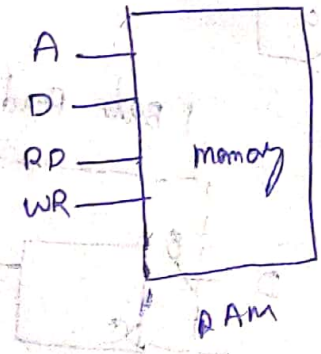




A	WR	RD	WR0	RD0	WR1	RD1
0	0	0	0	0	0	0
0	1	0	1	0	0	0
0	0	1	0	1	0	0
1	0	0	0	0	0	0
1	1	0	0	0	1	0
1	0	1	0	0	0	0

Note WR or RD one only need to Enable.





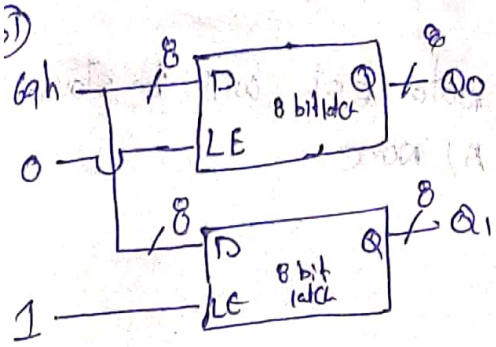
memory

volatile memory (RAM)

Non volatile memory (ROM)

RAM Assessment - 1

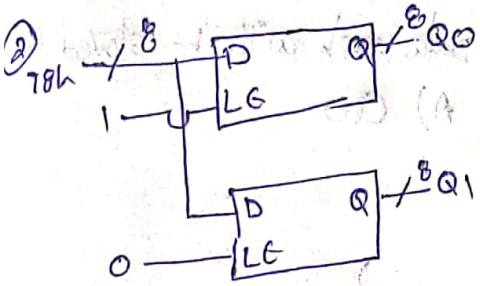
1)



Data 64h will be stored in?

A) Q1

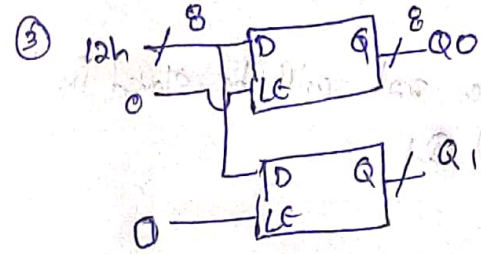
2)



Data 78h will be stored in?

A) Q0

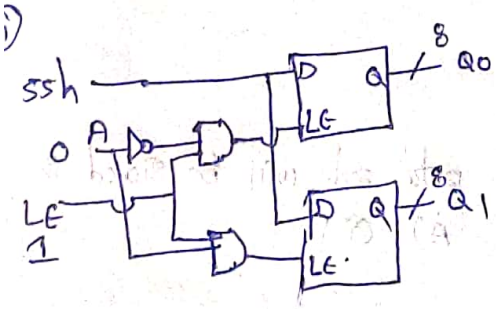
3)



Data 12h will be stored in

A) None

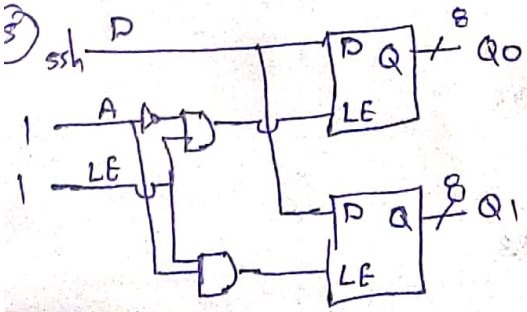
4)



Data 55h will be stored in?

A) Q0

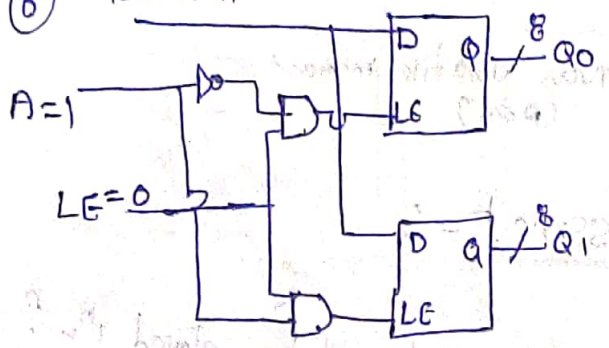
5)



Data 55h will be stored in?

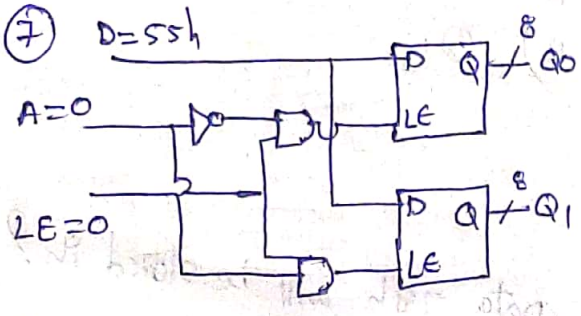
A) Q1

(6) D=55h



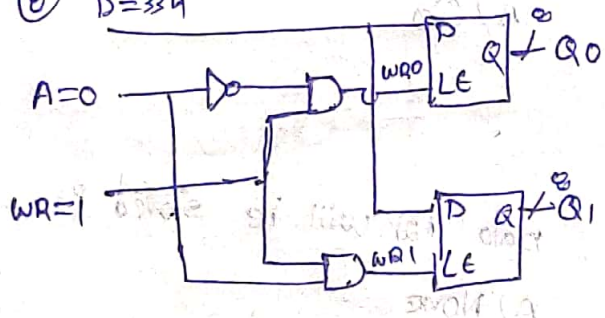
Data 55h will be stored in
A) None.

(7) D=55h



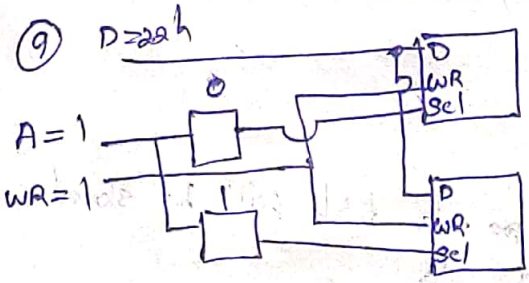
Data 55h will be stored in
A) None

(8) D=33h



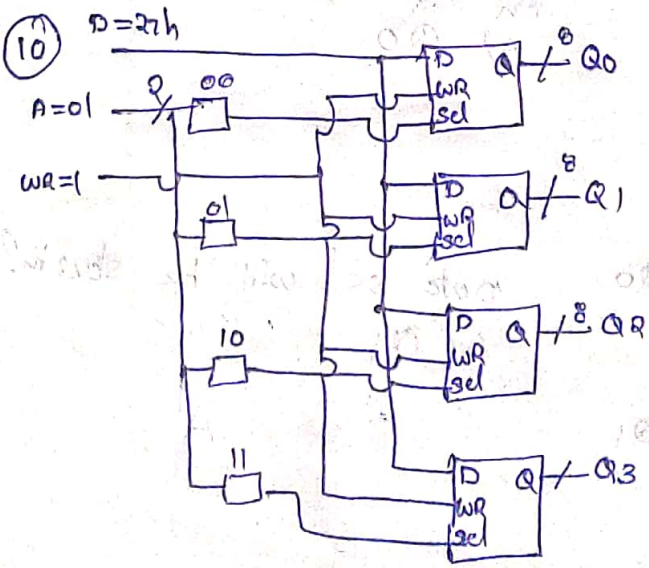
Data 33h will be stored in?
A) Q0

(9) D=22h



Data 22h will be stored in?
A) Q1

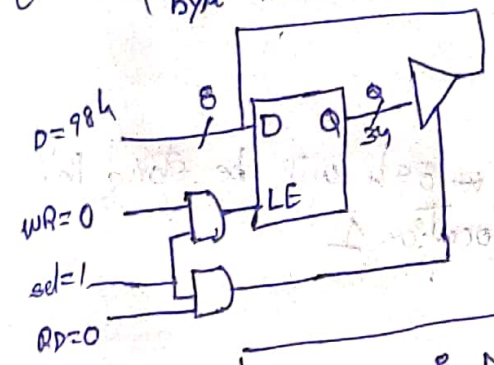
(10) D=27h



Data 27h will be stored in
A) Q1

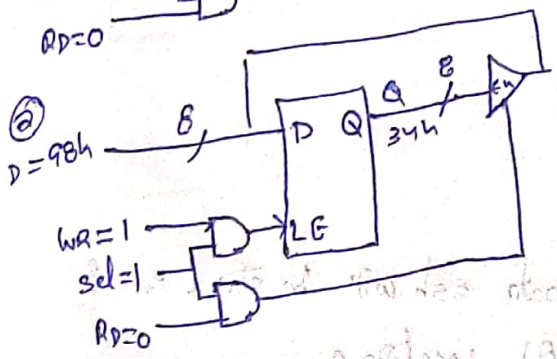
RAM 2 Assessment

① 1 byte Read write memory (RAM)



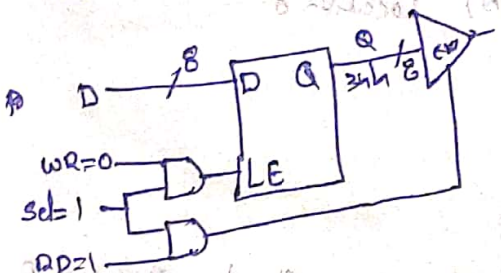
what is the value of Q?
A) 34h

②



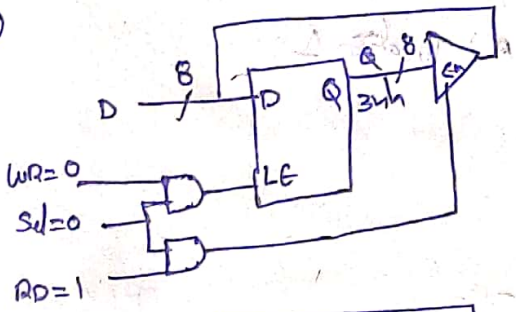
what is the value of Q?
A) 98h

③



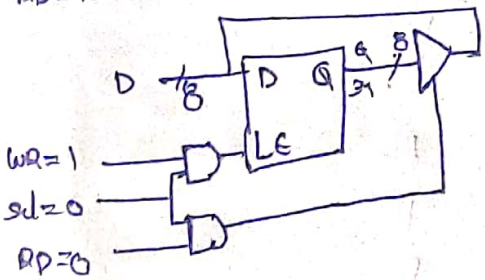
what is the value of D?
34

④



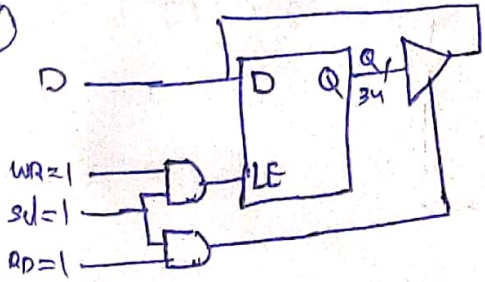
A) Floating

⑤



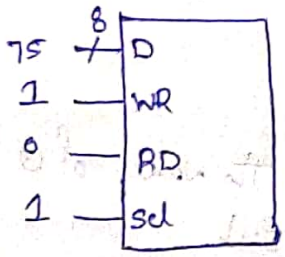
what is the value of Q?
A) 34h

⑥



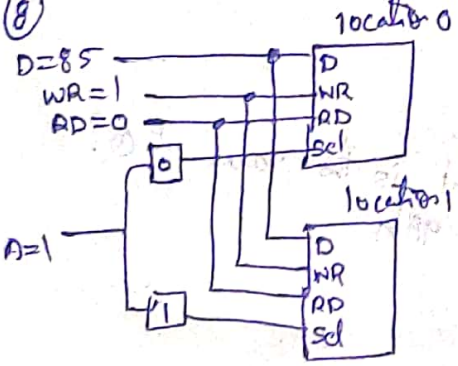
what is the value of Q?
A) illegal

1 byte RAM



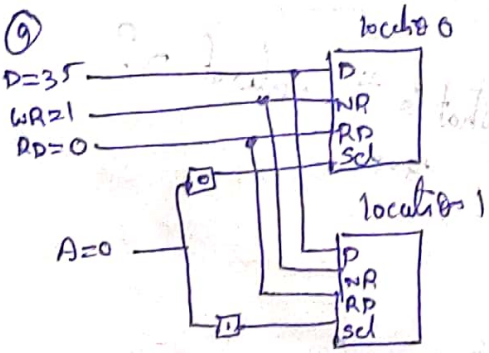
what is the value of Q?
A) 75h

(8)



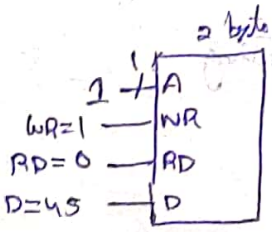
Data 85h will be stored in?
A) Location 1

(9)



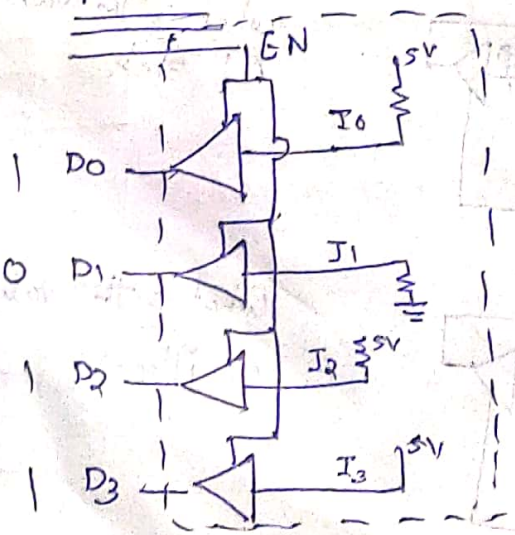
Data 35h will be stored in?
A) Location 0

(10)

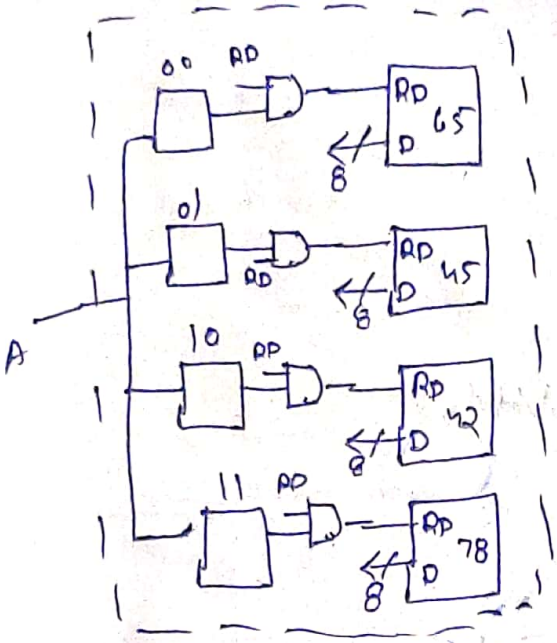


Data 45 will be stored in?
A) location 1

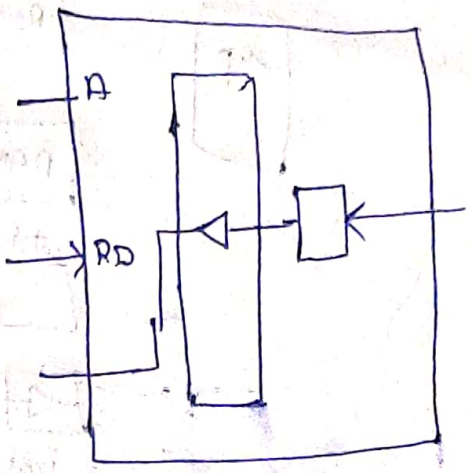
ROM

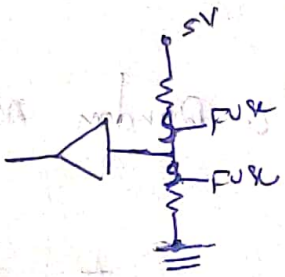


Read only memory
(Rom)



4 byte Rom





mask Rom – No change

PRom – one time change

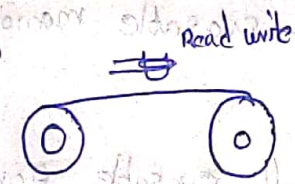
EPRom – Erasable Programmable

EEPRom – Electrically Erasable

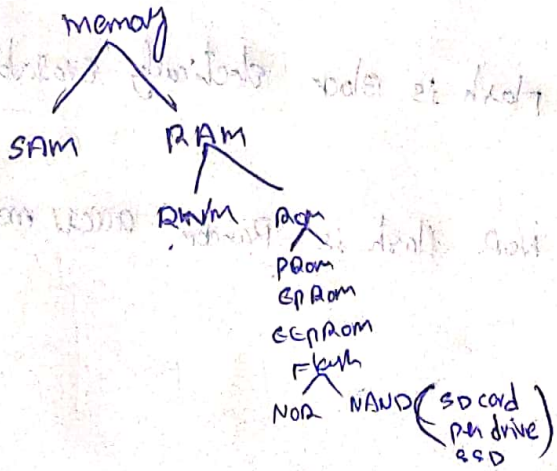
Flash – Block EEPRom

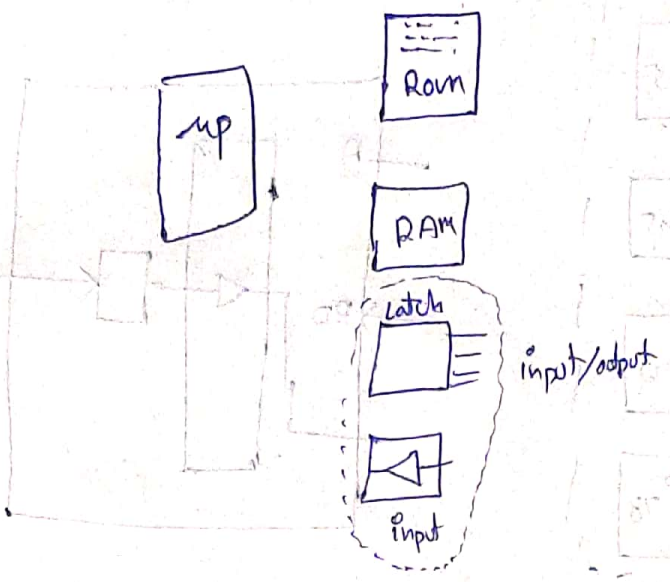
NOR NAND

magnetic Tape

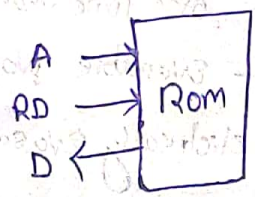


Sequential Access memory (SAM)





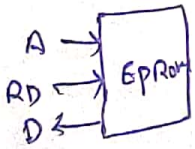
Rom Assessement

(01) 

Rom is a Random Acces memory

(2) 

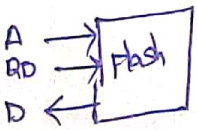
pRom is an one time programmble memory

(3) 

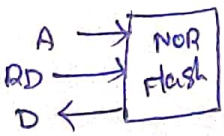
EpRom is uv evasable memory

(4) 

EEPRom is electically evasable Rom

(5) 

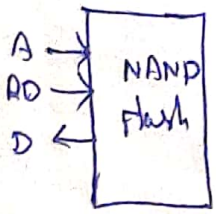
Flash is Block electically evasable Rom

(6) 

NOR flash is Random accesu memory

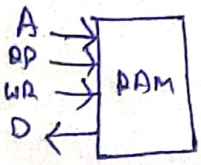
(7)

(7)



NAND Flash is sequential Access memory

(8)

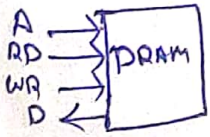


RAm is a Read write memory

(9)

Read write memory

(16)



Read write memory