Date: 17/10/2025

9. PROGRAMS ON DAC INTERFACING

AIM: Develop necessary interfacing circuit to interface DAC with 8051 and program to generate different stair case pattern.

TOOLS REQUIRED: PC, Keil uvision5

PROCEDURE:

- 1. Turn on the computer, create a folder on D drive saved with Register Number.
- 2. Open Keil uVision5 in desktop, or windows start menu → all programs → open Keil uVision5.

Creating Project:

- 3. Go to project → click on new uVision project → create a new folder saved with experiment number within the already existed register number folder in D drive mentioned in step 1, → enter the project name → click on save.
- 4. Select the device for target → In devices → Enter P89C51RD2XX in Search toolbar → click on ok → select **No** for dialog box message "Copy STARTUP.A51 to project folder and add files to project".

(or)

Choose NXP \rightarrow to select the device P89C51RD2xx \rightarrow click on ok \rightarrow select No for Copy STARTUP.A51 to the project folder.

Creating Coding File:

5. Go to file \rightarrow click on new \rightarrow go to save (choose the path to save the file, It is saved within the name of experiment number folder mentioned in step 3) \rightarrow enter a filename with extension $.asm \rightarrow$ save the file.

Linking the Coding File to Project:

- 6. Right-click on Source group1 in project bar → Add existing files to source group1→ choose the experiment number folder path and select all files in the folder → select .asm code file → click on add → click on close.
- 7. Write the assembly language program in .asm code file and save it.

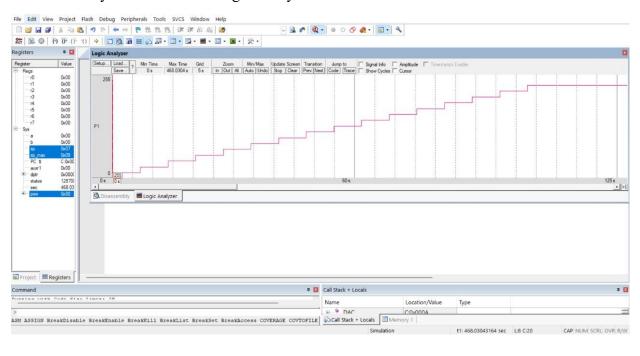
Executing the Code File:

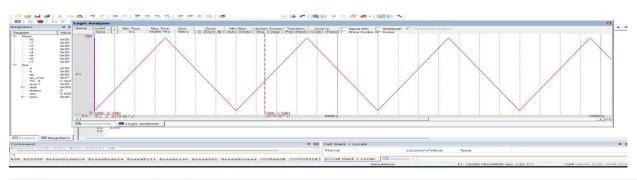
- 8. Right-click on .asm code file → Click on Build target to check the errors (i.e 0-Errors,0-Warning)
- 9. Go to debug → Click on Start/Stop Debug Session → click on ok for dialog box message "running code size limit 2K" → and Click on RUN in debug label
- 10. Observe the output in Register windows, Memory windows, Serial window.

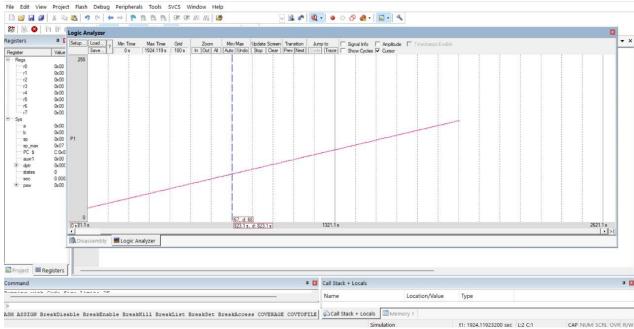
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OUTPUT:

View → Analysis Windows → Logic Analyzer







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PROGRAM:

ADDRESS	OPCODES	LABELS	MNEMONICS	OPERANDS
0000	7400		MOV	A, #00H
0002	F590	BACK:	MOV	P1, A
0004	2410		ADD	A, #10H
0006	110C		ACALL	DELAY
0008	70F8		JNZ	BACK
000A	80FE	HERE:	SJMP	HERE
000C	7890	DELAY:	MOV	R0, #90H
000E	79FF	WAIT1:	MOV	R1, #0FFH
0010	7AFF	WAIT2:	MOV	R2, #0FFH
0012	DAFE	WAIT3:	DJNZ	R2, WAIT3
0014	D9FA		DJNZ	R1, WAIT2
0016	D8F6		DJNZ	R0, WAIT1
0018	22		RET	
			END	

RESULT: The stair case is generated successfully in P1 port.

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