Si4684-A10

SINGLE-CHIP, FM/DAB/DAB+ RADIO RECEIVER

Features

- Worldwide FM band support (76–108 MHz)
- Advanced RDS/RBDS decoder
- DAB, DAB+ Band III support (168–240 MHz)
- Supports WorldDMB Receiver Profiles 1 and 2
- OFDM channel demodulator
  - Simultaneous decoding of up to 4 service components
  - Seamless dynamic multiplex reconfiguration
- Integrated SRAM supporting time and frequency de-interleaving
- Advanced seek functionality
- Advanced audio DSP processing
- Complete on-chip source decode
- I^2S digital audio out with ASRC
- Integrated 97 dB stereo audio DAC
- Concurrent I^2S / L-R stereo audio out
- Full range of analog and digital signal quality metrics
- Fully-integrated VCO / PLL / synthesizer
- Fully-integrated advanced AGC and alignment
- SPI, I^2C control interfaces
- FM sensitivity = 0.7 µV
- DAB sensitivity = –101 dBm
- WLCSP and QFN packages

Ordering Information:

See page 35.

Patents pending

Applications

- Mobile phones and tablets
- Clock and tabletop radios
- Personal navigation devices
- Stereo boomboxes
- Mini/micro systems
- Docking stations

Description

The Si4684 single-chip digital receiver is one member of a family of 100% CMOS digital radio broadcast receiver ICs from Silicon Labs. The Si46xx family provides revolutionary advances in size, power consumption, and performance to enable high-volume, cost-sensitive multimedia products to incorporate digital broadcast features. The family offers all-in-one, ultra-low power, multi-band digital broadcast receivers to support global analog and digital radio standards including AM, SW, LW, FM, FM RDS, HD, DAB, DAB+, DMB, and DRM(30).

Functional Block Diagram

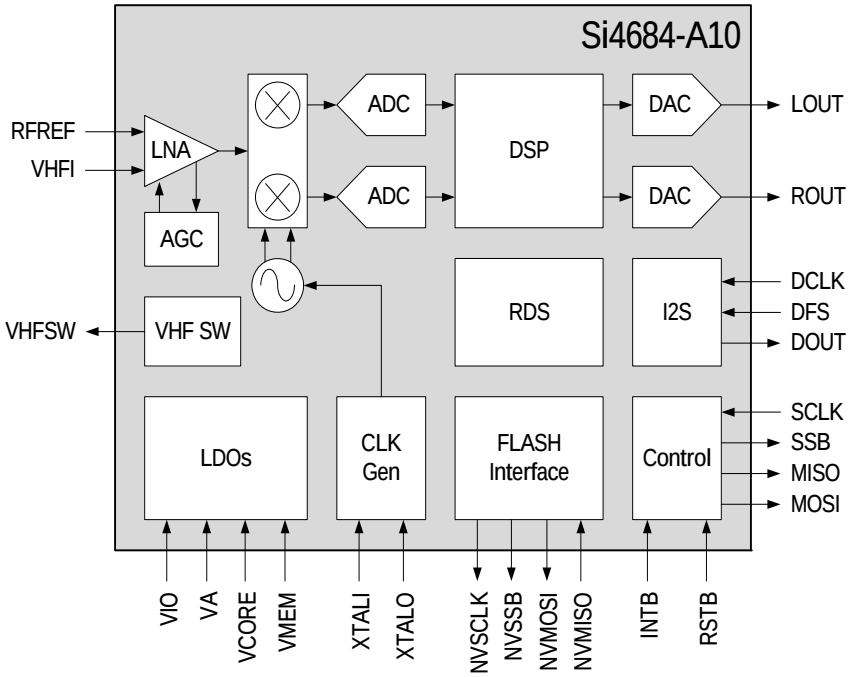


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Voltage	V_A		1.71	1.8	2.0	V
Interface Supply Voltage	V_{IO}		1.62	1.8	3.6	V
Core Digital Supply Voltage	V_{CORE}		1.62	1.8	2.0	V
Memory Supply Voltage	V_{MEM}		1.62	1.8	2.0	V

***Note:** All minimum (Min) and maximum (Max) specifications are guaranteed and apply across the recommended operating conditions. Typical (Typ) values apply at VA = VIO = VCORE = VMEM = 1.8 V, and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. DC Characteristics[1,2]

(T_{AMB} = 25 °C, VA = VIO = VMEM = VCORE = 1.8 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RESET						
VA		RSTB pin = low	—	0.5	5	µA
VCORE			—	1	8	µA
VMEM			—	1	8	µA
VIO			—	0.5	3	µA
STARTUP						
VA		RSTB pin = high	—	1	—	µA
VCORE			—	8.5	—	mA
VMEM			—	1	—	mA
VIO			—	160	—	µA
OPERATIONAL—Analog FM Mode						
VA		Analog FM reception	—	19.1	22.7	mA
VCORE			—	7.4	9.1	mA
VMEM			—	4.8	6.2	mA
VIO			—	0.1	0.1	mA
OPERATIONAL—DAB/DAB+ Mode[3]						
VA		DAB/DAB+ reception	—	23.9	25.0	mA
VCORE			—	14.0	17.0	mA
VMEM			—	9.0	13.3	mA
VIO			—	0.3	0.6	mA

Notes:

1. Power states are described in Section “6.5. Reset Timing and Power States” .
2. Characteristics apply to firmware FM 2.0.10 and firmware DAB 1.0.6. For later firmware versions see “Si468x Data Sheet Addendum”. Parameters are tested in production unless otherwise stated.
3. Guaranteed by characterization.
4. For input pins RSTB, SMODE, SCLK, SSB, MOSI, NVMISO, DCLK and DFS.
5. For output pins INTB, MISO, NVSBB, NVSCLK, NVMOSI and DOUT.

Table 2. DC Characteristics[1,2] (Continued)

(T_{AMB} = 25 °C, VA = VIO = VMEM = VCORE = 1.8 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I/O Voltages and Currents						
High Level Input Voltage[4]	V_{IH}		0.7 x V_{IO}	—	—	V
Low Level Input Voltage[4]	V_{IL}		—	—		V
High Level Input Current[4]	I_{IH}	V_{IO} = 3.6 V		—		µA
Low Level Input Current[4]	I_{IL}	V_{IO} = 3.6 V		—		µA
High Level Output Voltage[5]	V_{OH}	I_{OUT} = 500 µA		—	—	V
Low Level Output Voltage[5]	V_{OL}	I_{OUT} = –500 µA	—	—		V

Notes:

1. Power states are described in Section “6.5. Reset Timing and Power States” .
2. Characteristics apply to firmware FM 2.0.10 and firmware DAB 1.0.6. For later firmware versions see “Si468x Data Sheet Addendum”. Parameters are tested in production unless otherwise stated.
3. Guaranteed by characterization.
4. For input pins RSTB, SMODE, SCLK, SSB, MOSI, NVMISO, DCLK and DFS.
5. For output pins INTB, MISO, NVSBB, NVSCLK, NVMOSI and DOUT.

Table 3. SPI Control Interface Characteristics[1,2,3]

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}		—	—	10	MHz
SCLK High Time[3]	t_{HI}		20	—	—	ns
SCLK Low Time[3]	t_{LO}		20	—	—	ns
Input Rise Time[3]	t_F		—	—	20	ns
Input Fall Time[3]	t_R		—	—	20	ns
SSB Setup to SCLK Rise[3]	$t_{SU:SSB}$		10	—	—	ns
SSB Hold from SCLK Fall[3]	$t_{H:SSB}$		0	—	—	ns
MOSI Setup to SCLK Rise[3]	$t_{SU:MOSI}$		10	—	—	ns
MOSI Hold from SCLK Fall[3]	$t_{H:MOSI}$		0	—	—	ns
MISO Output Delay from SCLK Fall[3]	t_{PD}		0	—	20	ns
MISO Drive Delay from SSB Fall[3]	t_D		—	—	20	ns
MISO Tristate Delay from SSB Rise[3]	t_Z		—	—	20	ns
Capacitive Loading[3]	C_B		—	—	50	pF

Notes:

1. The SPI interface transparently supports Mode 0,0 and Mode 1,1, both of which use the rising edge of the clock to capture data. The user must not pulse SSB high between each byte, because SSB is used to frame commands and replies. SSB must be held low for the duration of the SPI transaction, and raised at the end to signal the completion of a command write or a reply read.
2. See SPI Control Interface Protocol in Figure 9, “Si4684 SPI Control Interface Bus Protocol – SPI Mode 0,0” and Figure 10, “Si4684 SPI Control Interface Bus Protocol – SPI Mode 1,1”.
3. Guaranteed by characterization.

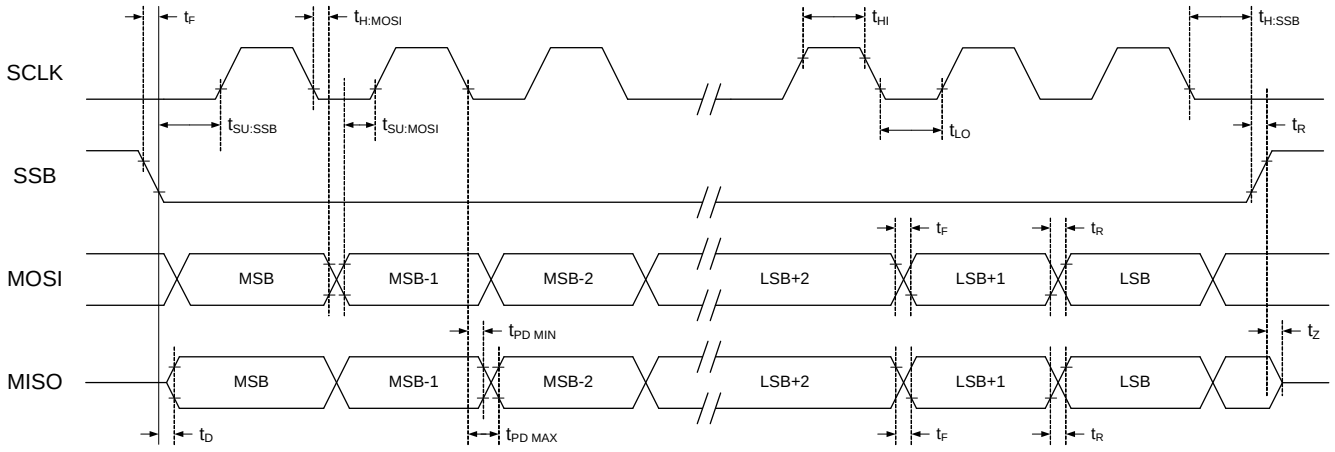


Figure 1. SPI Control Interface Timing Parameters

Table 4. I²C Control Interface Characteristics*

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL Frequency	f_{SCL}		0	—	400	kHz
SCL High Time	t_{HI}		0.6	—	—	µs
SCL Low Time	t_{LO}		1.3	—	—	µs
SCL Input to SDA ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCL Input from SDA ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDA Input to SCL ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDA Input from SCL ↓ Hold	$t_{HD:DAT}$		0	—	—	ns
SDA Output Delay	$t_{PD:DAT}$		50	—	900	ns
SCL Input to SDA ↓ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDA Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_B}{1pF}$	—	150	ns
SDA Input, SCL Rise/Fall Time	$t_{f:IN}$, $t_{r:IN}$		0	—	300	ns
Capacitive Loading	C_B		—	—	50	pF
Pulse Width Rejected by Input Filter	t_{SP}		—	—	50	ns

***Note:** Guaranteed by characterization.

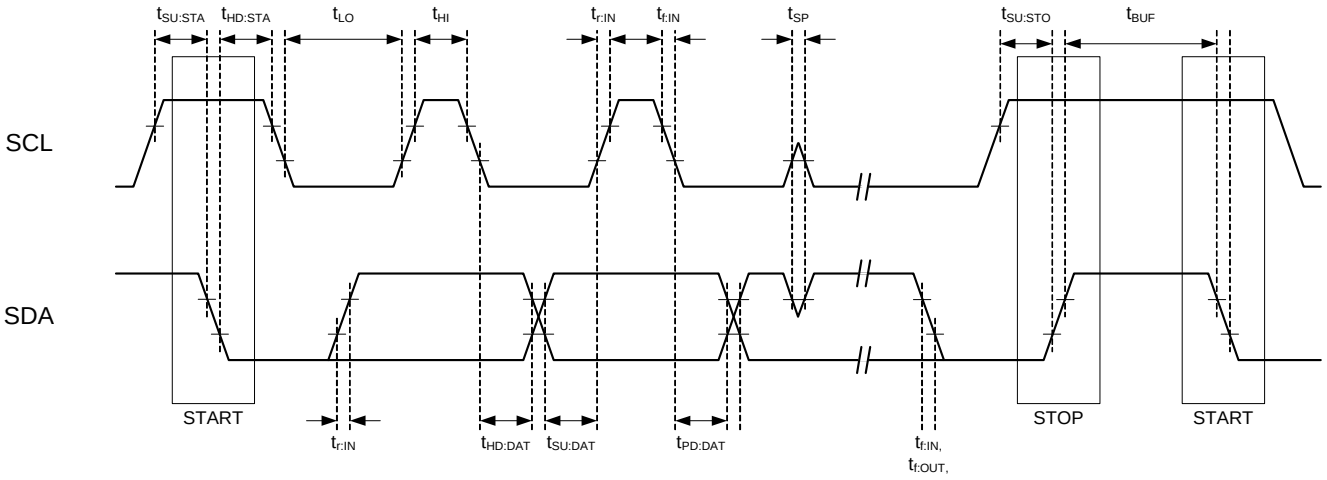


Figure 2. I²C Control Interface Timing Parameters

Table 5. I²S Digital Audio Interface Characteristics*

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Frequency	f_{DCLK}		—	—	15	MHz
DCLK Input Cycle Time	$t_{CYC:DCLK}$		66.7	—	—	ns
DCLK Input Pulse Width High	$t_{HI:DCLK}$		20	—	—	ns
DCLK Input Pulse Width Low	$t_{LO:DCLK}$		20	—	—	ns
DFS Setup Time	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time	$t_{HD:DFS}$		5	—	—	ns
DOUT Output Delay	$t_{PD:DOUT}$		0	—	10	ns
Capacitive Loading	C_B		—	—	50	pF

***Note:** Guaranteed by characterization.

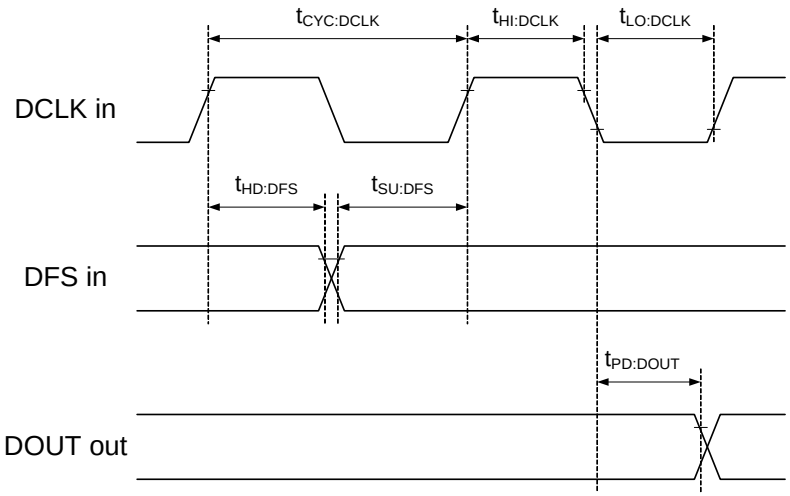


Figure 3. Digital Audio Interface Timing Parameters

Table 6. Serial Flash Interface Characteristics[1,2]

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
NVSCLK Frequency	f_{NVSCLK}		—	—	40	MHz
NVSCLK High Time	t_{HI}		10	—	—	ns
NVSCLK Low Time	t_{LO}		10	—	—	ns
Input/Output Rise Time	t_R		—	—	20	ns
Input/Output Fall Time	t_F		—	—	20	ns
NVSSB Setup to NVSCLK Rise	$t_{SU:NVSSB}$		10	—	—	ns
NVSSB Hold from NVSCLK Fall	$t_{H:NVSSB}$		0	—	—	ns
NVMOSI Setup to NVSCLK Rise	$t_{SU:NVMOSI}$		10	—	—	ns
NVMOSI Hold from NVSCLK Fall	$t_{H:NVMOSI}$		0	—	—	ns
NVMISO Setup to NVSCLK Rise	$t_{SU:NVMISO}$		10	—	—	ns
NVMISO Hold from NVSCLK Rise	$t_{H:NVMISO}$		10	—	—	ns

Notes:
1. The Serial Flash interface supports SPI Mode 1,1, which uses the rising edge of the clock to capture data.
2. Guaranteed by characterization.

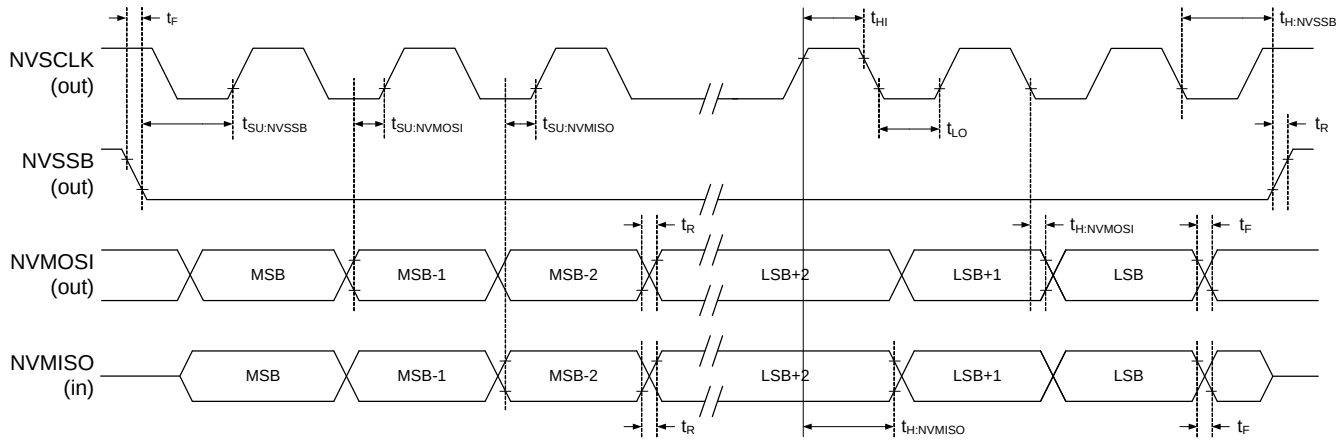


Figure 4. Serial Flash Interface Timing Parameters

Table 7. Analog FM Receiver Characteristics[1,2,3]

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Audio Sensitivity[4]		SINAD = 26 dB	—	0.7	1.0	µV
RDS Sensitivity[4,5]		F_{DEV} = 2 kHz, RDS BLER < 5%, Analog audio output mode	—	4	—	µV
Input IP3[5]		$\|f_2 - f_1\|$ > 2 MHz, $f_0 = 2 \times f_1 - f_2$, AGC is disabled	90	96	—	dBµV
Image Rejection[5]			35	45	—	dB
AM Suppression[5]		F_{DEV} = 22.5 kHz	53	58	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	35	43	—	dB
Audio Output Voltage		F_{DEV} = 22.5 kHz	48	52	55	mVrms
Audio Output L/R Imbalance		F_{DEV} = 75 kHz	–1	—	1	dB
Audio Frequency Response Low[5]		±3 dB	—	—	30	Hz
Audio Frequency Response High[5]		±3 dB	15	—	—	kHz
Audio Stereo Separation		F_{DEV} = 75 kHz	35	45	—	dB
Audio Mono SNR		F_{DEV} = 22.5 kHz	62	68	—	dB
Audio Stereo SNR[5]		F_{DEV} = 22.5 kHz	—	60	—	dB
Audio Mono THD		F_{DEV} = 75 kHz	—	0.1	0.5	%
Audio Mono SINAD		F_{DEV} = 75 kHz	60	—	—	dB
De-emphasis Time Constant[5]		FM_DEEMPHASIS = 75 µs	70	75	80	µs
		FM_DEEMPHASIS = 50 µs	45	50	54	µs
Seek/Tune Time[5]		Tune Mode = 0 (FM Analog mode)	—	—	60	ms/ch
RSSI Offset		RF Input levels of 0 and 60 dBµV	–3	—	3	dB

Notes:

1. Characteristics apply to firmware FM 2.0.10. For later firmware versions see “Si468x Data Sheet Addendum”. Parameters are tested in production unless otherwise stated.
2. Test Setup and Test Conditions are available in “AN651: Si46xx Evaluation Board Test Procedure”. Tested at RF = 98.0 MHz.
3. To ensure proper operation and receiver performance, follow the guidelines in “AN650: Si46xx Schematic and Layout Guide”. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. Signal generator reading. Voltage at VHF pin typically 6 dB higher.
5. Guaranteed by characterization.

Table 8. DAB Receiver Characteristics[1,2,3]

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency[4]	F_{rf}		168	—	240	MHz
Input IP3[4]		LNA gain = 5 dB	—	103	—	dBµV
Sensitivity[4]		BER = 10^{-4} LNA gain = 15 dB	—	2.0	—	µV
			—	–101	—	dBm
First Adjacent Selectivity[4,5]		BER = 10^{-4}, ±1.712 MHz	—	46	—	dB
Second Adjacent Selectivity[4,5]		BER = 10^{-4}, ±3.424 MHz	—	48	—	dB
Third Adjacent Selectivity[4,5]		BER = 10^{-4}, ±5.136 MHz	—	48	—	dB
Ensemble Acquisition Time[4,6]		For a valid channel, after powerup RF Level = –47 dBm	—	940	—	ms

Notes:

1. Characteristics apply to firmware DAB 1.0.6. For later firmware versions see “Si468x Data Sheet Addendum”. Parameters are tested in production unless otherwise stated.
2. Test Setup and Test Conditions are available in “AN651: Si46xx Evaluation Board Test Procedure”. Tested at RF = 195.936 MHz.
3. To ensure proper operation and receiver performance, follow the guidelines in “AN650: Si46xx Schematic and Layout Guide”. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. Guaranteed by characterization.
5. In selectivity measurements, RF blocker used is concord with the mask defined in section 7.3.3.1.1 in EN50248 (2001).
6. Time measured from the completion of the DAB tuning command to the setting of the ACQ bit indicating ensemble acquisition. For ETI filed used in BER test see AN651.

Table 9. Reference Clock and Crystal Characteristics[1]

(T_{AMB} = –40 to 85 °C, VA = 1.71 to 2.0 V, VIO = 1.62 to 3.6 V, VMEM = VCORE = 1.62 to 2.0 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
Reference Clock Frequency	RCLK		n x 5.4 (see Note 2)	n x 6.0 (see Note 2)	n x 6.6 (see Note 2)	MHz
Reference Clock Accuracy			–50	—	50	ppm
Reference Clock Duty Cycle			45	—	55	%
Reference Clock Phase Noise		See Mask in Figure 5	—	—	—	—
Crystal Oscillator						
Crystal Frequency			n x 5.4 (see Note 2)	n x 6.0 (see Note 2)	n x 6.6 (see Note 2)	MHz
Crystal Accuracy			–50	—	50	ppm
Crystal Load Capacitance[3,4]		6 MHz (500 Ω Startup ESR)	5	—	30	pF
		36.864 MHz (400 Ω Startup ESR)	5	—	7.5	pF
Crystal Startup ESR[3]		6 MHz (30 pF load capacitance)	—	—	500	Ω
		36.864 MHz (7.5 pF load capacitance)	—	—	400	Ω

Notes:

1. Guaranteed by design.
2. n = 1,2,3,4,5,6.
3. Refer to “AN649: Si46xx Programming Guide”, Section 8 for further details on how to choose crystal for Si46xx application.
4. If load capacitance > 14 pF, it requires two external capacitances due to limits in the internal tuning range.

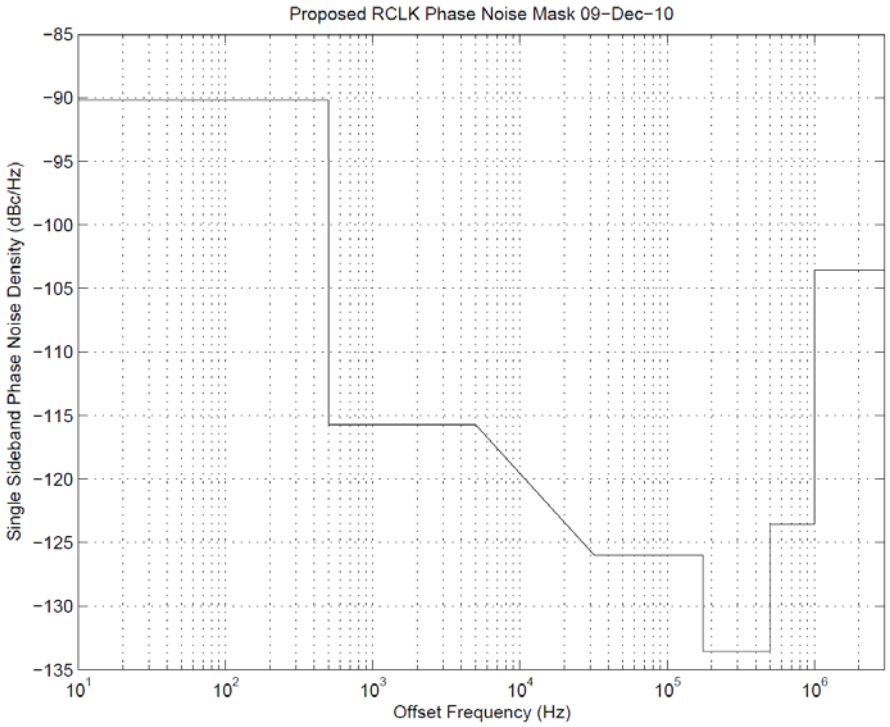


Figure 5. Reference Clock Phase Noise Mask (referred to 6 MHz)

Table 10. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A	—	–40	25	85	°C
Junction Temperature*	T_J	$\theta_{JA\ (QFN)}$ ~ 25 °C/W	—	—	90	°C
		$\theta_{JA\ (WLCSP)}$ ~ 33.5 °C/W	—	—	90	°C
***Note:** The θ_{JA} performance is layout and package dependent. Application recommendations to follow.						

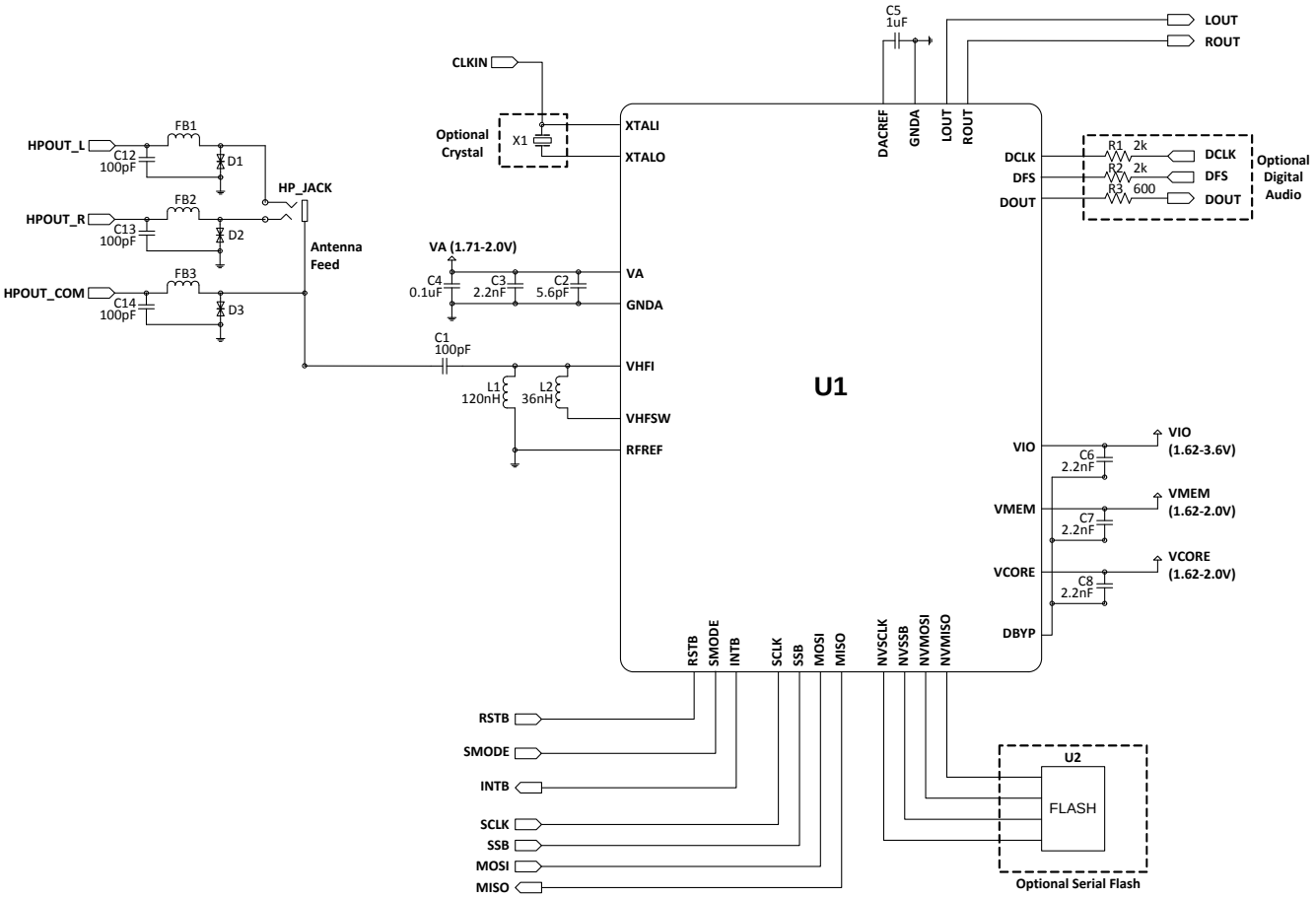
Table 11. Absolute Maximum Limits

Parameter	Symbol	Test Condition	Min	Max	Units
Analog Supply Voltage[1,2]	V_A		–0.3	2.2	V
Interface Supply Voltage[1,2]	V_{IO}		–0.3	3.9	V
Core Digital Supply Voltage[1,2]	V_{CORE}		–0.3	2.2	V
Memory Supply Voltage[1,2]	V_{MEM}		–0.3	2.2	V
Input Voltage[1,2,3]	V_{IN}		–0.3	V_{IO}+0.3	V
Input Current[1,2,3]	I_{IN}		—	10	mA
Operating Temperature[1,2]	T_{OP}		–45	95	C
Storage Temperature[1,2]	T_{STG}		–55	150	C
RF Input Level[1,2,4]	RF_{IN}		–0.3	1.7	V_{PK}
RF Input Level[1,2,5]	RF_{IN}		—	13	dBm
HBM ESD	V_{HBM}	QFN	—	4000	V
		WLCSP	—	4000	V
CDM ESD	V_{CDM}	QFN	—	1000	V
		WLCSP	—	900	V
MM ESD	V_{MM}	QFN	—	300	V
		WLCSP	—	300	V

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. Guaranteed by design.
3. For input pins RSTB, SMODE, SCLK, SSB, MOSI, NVMISO, DCLK and DFS.
4. At Analog pins XTALI, XTALO.
5. At RF pin VHFI and VHFSW.

2. Typical Application Schematic



***Note:** The application schematic assumes that the headphone amplifier uses true ground as HPOUT_COM.

3. Bill of Materials

Table 12. Bill of Materials

Required Component(s)	Value/Description
U1	Si4684 Digital Radio Receiver
L1	Tuning inductor, 120 nH, 0603 wire wound
L2	Tuning inductor, 36 nH, 0603 wire wound
C1	Band tuning cap, 100 pF
C2	VA Supply bypass capacitor, 5.6 pF
C3, C6, C7, C8	Supply bypass capacitor, 2.2 nF, Z5U/X7R
C4	Supply bypass capacitor, 0.1 µF, Z5U/X7R
C5	Supply bypass capacitor, 1 µF
C12, C13, C14	Filter capacitor, 100 pF
FB1, FB2, FB3	Ferrite bead filter, 1 kΩ
D1, D2, D3	ESD protection diode
Optional Component(s)	**Value/Description**
X1	Crystal
U2	Serial Flash, 16 Mb, Microchip SST25
R1, R2	Resistor, 2 kΩ
R3	Resistor, 600 kΩ

4. Functional Description

4.1. Overview

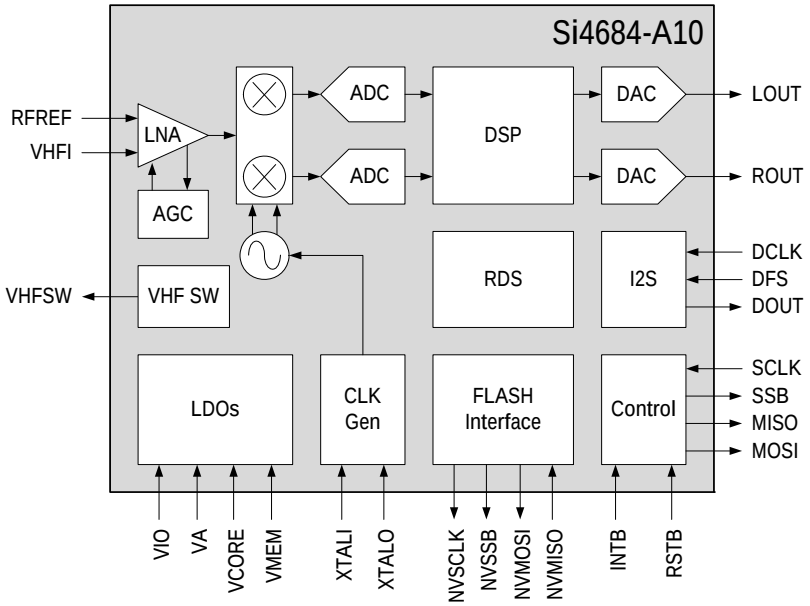


Figure 6. Si4684 Block Diagram

The Si4684 offers a complete and cost-effective platform to support global analog VHF Band II and digital VHF Band III radio standards by integrating multiband RF tuner, demodulator, channel decoder, and audio processing on a single die. The high level of integration and complete system production test simplifies design-in, increases system quality, and improves reliability and manufacturability.

The Si4684 supports worldwide analog FM radio reception and incorporates a fully integrated decoder for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RDBS), including all required symbol decoding, block synchronization, error detection, and error correction functions.

The Si4684 additionally supports digital DAB and DAB+ reception, incorporating digital channel demodulation and decoding functions, along with audio decoding.

Leveraging Silicon Laboratories' proven and patented digital low intermediate frequency (Low-IF) receiver architecture, the Si4684 delivers superior RF performance and interference rejection. The solution offers auto-calibrated digital tuning, and proven FM seek functionality based on multiple signal quality and band parameters. The Si4684 offers highly flexible and advanced audio processing including noise blanking, programmable soft mute, FM stereo-mono blend, and FM hi-cut filters. In addition, the Si4684 provides an integrated clock oscillator or accepts a reference clock and supports a selectable control interface (SPI or I^2C).

The Si4684 receiver system requires a minimal bill of materials and offers extremely low power consumption, making the solution ideal for handheld and portable consumer electronic devices.

4.2. Clocking

The Si4684 generates all internal clocking from an external crystal using an on-chip oscillator or an external programmable reference clock. The reference clock of Si4684 is a sinusoidal or rectangular clock provided by an external source on pin XTALI. The POWER_UP command enables the selection of an external crystal or reference clock. The Si4684 features programmable loading capacitors for the on-chip crystal oscillator, eliminating external loading capacitors.

4.3. Tuning

The Si4684 includes a complete, fully integrated PLL-VCO frequency synthesizer to generate the quadrature local oscillator (LO) input to the VHF mixer. No external loop filter capacitors or VCO inductors are required. The FM and DAB tuning commands automatically configure the frequency synthesizer to generate the appropriate LO frequency to receive the desired channel.

4.4. FM Receiver

The Si4684 FM receiver is based on Silicon Laboratories' proven FM radio family. The part leverages Silicon Laboratories' proven and patented Low-IF digital architecture, delivering excellent RF performance and interference rejection. The proven digital techniques provide excellent sensitivity in weak signal environments while providing superb selectivity and inter-modulation immunity in strong signal environments.

The Si4684 supports the worldwide FM broadcast band (76–108 MHz) with channel spacings of 50, 100, and 200 kHz. The Low-IF architecture utilizes a single converter stage and digitizes the audio signal using a high-resolution analog-to-digital converter. The stereo audio output can be directed either to an external headphone amplifier via the LOUT and ROUT pins or to other system ICs through a digital audio interface (I^2S).

4.4.1. FM Received Signal Qualifiers

A tuned signal's quality can vary with the environmental conditions, time of day, and geographical location among many other factors. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si4684 monitors and provides indicators of signal quality, allowing the on-chip DSP and host processor (if required) to perform signal processing. The Si4684 monitors and reports a set of industry-standard signal quality metrics including on-channel RSSI, SNR, multipath interference on FM signal and FM pilot detection.

4.4.2. FM De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4684 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs.

4.4.3. FM Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in compromised signal conditions. The Si4684 triggers soft mute by monitoring signal metrics such as audio SNR. The thresholds for activating soft mute are programmable, as are soft mute attenuation levels and attack and decay rates. The Si4684 provides the soft mute feature in the FM band.

4.4.4. FM Hi-Cut Control

Hi-cut control is employed on the Si4684 audio outputs with degradation of signal quality. Signal quality metrics such as audio SNR, on-channel RSSI, and multipath SNR are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for all metrics. Attack and release rates for hi-cut are programmable for all metrics. Hi-cut can be disabled by setting the hi-cut filter setting to the default audio bandwidth for FM.

4.5. DAB Radio Receiver

The Si4684 DAB radio receiver offers VHF Band III (168–240 MHz) reception capability and is fully compliant with ETSI EN 300 401 (DAB) and ETSI TS 102 563 (DAB+). The Si4684 DAB receiver supports DAB and DAB+ via an integrated source decoder that supports both MPEG Audio Layer 2 (DAB) and HE-AAC V2 (DAB+). The stereo audio output can be directed either to an external headphone amplifier via analog and/or to other system ICs through an I^2S digital audio interface.

The Si4684 DAB receiver additionally supports data services such as Dynamic Labels, Intellitext, Electronic Program Guide (EPG), Slideshow and Journaline® with the appropriate external decoders.

4.6. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 7, “MPX Signal Spectrum”.

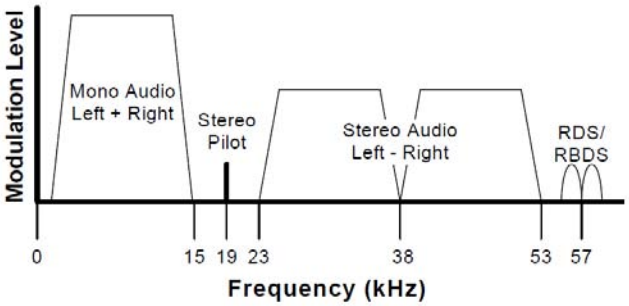


Figure 7. MPX Signal Spectrum

4.6.1. Stereo Decoder

The Si4684 integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0–15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

4.6.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Signal quality metrics such as on-channel RSSI and multipath SNR are monitored simultaneously in forcing a blend from stereo to mono. The metric, reflecting the poorest signal quality, takes priority and the stereo signal is blended appropriately. The thresholds for activating stereo-mono blend are programmable, as are the levels for a fully blended state. The attack and decay rates for each metric are programmable. The pilot detection metric is additionally available for read-out.

4.7. FM Seek and Valid Station Qualification

The FM seek function will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds including RSSI and SNR. The seek function can be programmed to stop at the band edge or wrap at the band and continue seeking until arriving at the original departure frequency. The device can be programmed to interrupt the host processor whenever the seek function is complete. Seek is complete when one of the following conditions are met:

1. A valid station is found.
2. No valid station is found and the stop frequency is found. The stop frequency can be programmed to either the band edge (no wrap) or the starting frequency (wrap).

The Si4684 seek functionality is performed completely on-chip. To facilitate this, the Si4684 can provide real time updates for the signal quality metrics to host processor for station qualification. The Si4684 uses RSSI, SNR, and frequency offset to qualify stations. These variables have programmable thresholds to tailor the seek function to the subjective tastes of customers. RSSI is employed first to screen all possible candidate stations. SNR and frequency offset are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations; however, the more challenging levels the thresholds are set to, the longer the overall seek time as more stations and more qualifiers will be assessed. It is recommended that RSSI be set to a mid-level threshold in conjunction with an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations whilst keeping the seek time to acceptable levels. In addition to the programmable thresholds, both RSSI and SNR have programmable qualification times. These times can be made shorter to decrease the seek time or made longer to increase the robustness of the seek function. Generally, the time to auto-scan and store valid channels for an entire FM band with all thresholds engaged is very short depending on the band content. Seek is initiated using the FM_SEEK_START command. The RSSI, SNR and frequency offset thresholds and qualification time settings are adjustable using properties.

4.8. RDS/RBDS Decoder

The Si4684 implements an advanced, patented, high-performance RDS/RBDS* processor for demodulation, symbol decoding, block synchronization, error detection, and error correction. The RDS decoder provides several significant benefits over traditional implementations, including very fast and robust RDS synchronization in noisy signal levels with very high block error rates (BLER), industry-leading sensitivity, and improved data reliability in all signal environments.

The Si4684 strong synchronization performance in very noisy/low SNR environments minimizes the number of instances of lost synchronization. Other less robust tuners must attempt to resynchronize in low SNR environments, resulting in lost data and lengthy delays in re-establishing data reception. The Si4684 maintains synchronization to the RDS transmission, despite high BLER. This results in fewer dropped connections, minimal resynchronization time, and greater data reliability in low SNR environments.

The Si4684 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block. The range of reportable block errors is 0, 1-2, 3-5, or 6+. More than six errors indicate that the corresponding block information word contains six or more non-correctable errors or that the block check word contains errors.

The Si4684 also provides highly configurable interrupts based on RDS-driven events and conditions. The default settings provide an interrupt when RDS is synchronized and when RDS group data has been received. The configurable interrupts can be set to provide frequent interrupts down to a single received block with BLER. The configurable interrupts also can be set to provide very infrequent interrupts, buffering up to 25 complete RDS groups (100 blocks) with BLER information by block in the on-chip FIFO. The Si4684 also provides configurable interrupts on changes or receipt of the key RDS blocks A and B. This flexibility allows adopters to either conduct extensive RDS data processing on the host or reserve the host processor in power-saving modes with minimal RDS interrupts, allowing the Si4684 to perform RDS processing on-chip.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

5. Audio Interface

5.1. Analog Audio

High-fidelity digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally.

5.2. Digital Audio Interface

The digital audio 3-pin interface consists of data serial lines containing audio data, a bit clock, and a word frame for left and right channel data. The digital audio interface operates in slave mode and supports the I^2S Audio format.

In the I^2S Audio format, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

5.2.1. Audio Sample Rates

The Si4684 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz.

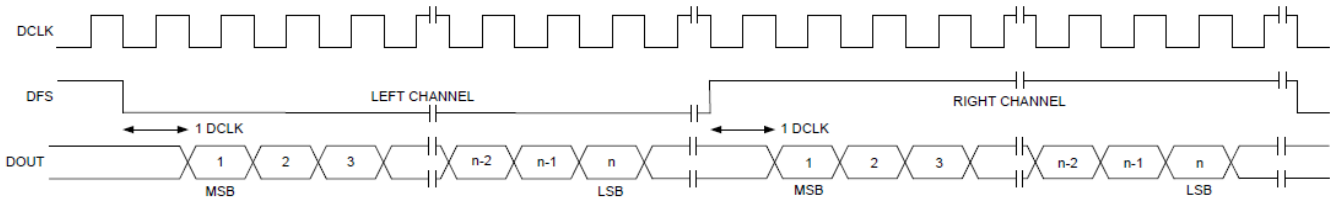


Figure 8. I^2S Audio Format

6. Control Interface

Two serial port slave protocols are supported, a Serial Peripheral (SPI) Control Interface Protocol and an I^2C Control Bus Interface Protocol, which allow an external controller to send commands and receive responses from the Si4684.

6.1. SPI Control Interface

The Si4684 control interface operates in SPI Mode when the SMODE pin is tied to GND.

The Si4684 SPI control interface supports the synchronous transfer of data between the part and an external controller via a 4-wire bus consisting of:

- a serial clock (SCLK), provided by the external controller
- a slave select (SSB), allows the master to select a slave device
- a slave data input pin (MOSI)
- a slave data output pin (MISO)

Because all data transfers across the SPI control interface are synchronized to the serial clock (SCLK), there are four possible modes that can be used in an SPI protocol, based on the serial clock's phase (CPHA) and polarity (CPOL).

The Si4684 SPI control interface supports SPI Mode 0 (CPHA=0, CPOL=0), and SPI Mode 3 (CPHA=1, CPOL=1). Figure 9, "Si4684 SPI Control Interface Bus Protocol – SPI Mode 0,0" and Figure 10, "Si4684 SPI Control Interface Bus Protocol – SPI Mode 1,1" show the SPI Control Interface bus protocols for SPI Modes 0 and 3, respectively.

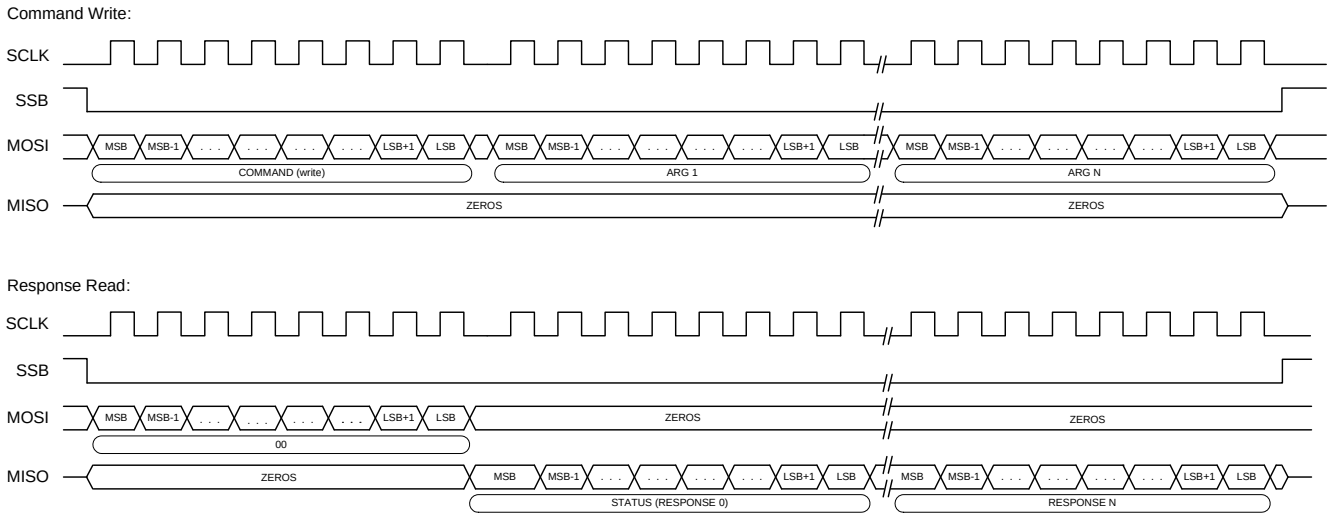


Figure 9. Si4684 SPI Control Interface Bus Protocol – SPI Mode 0,0

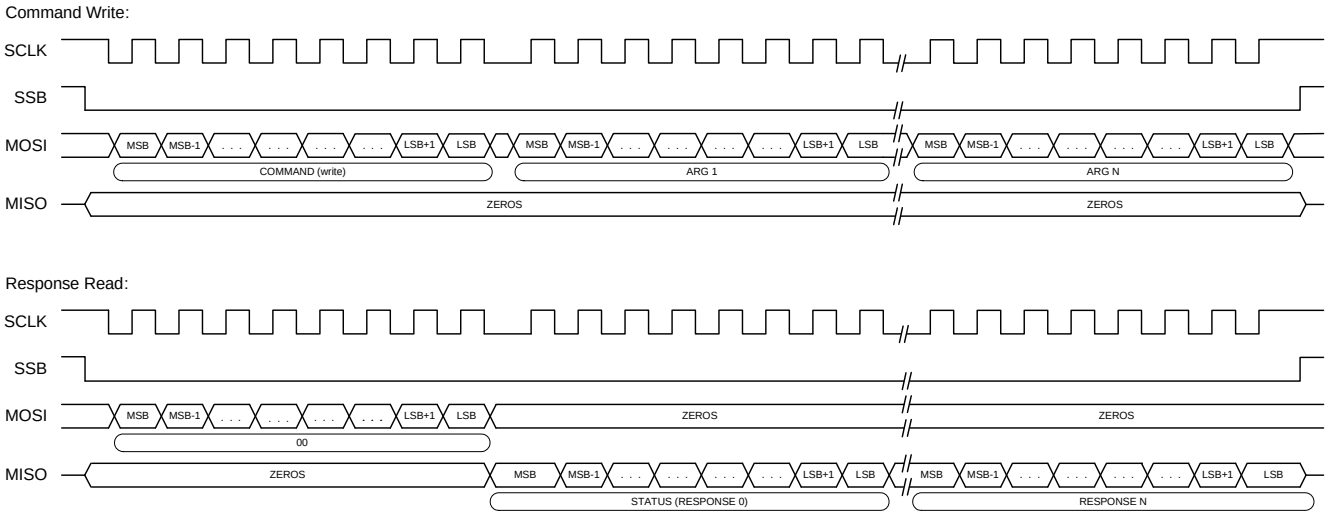


Figure 10. Si4684 SPI Control Interface Bus Protocol – SPI Mode 1,1

6.2. I²C Control Bus

The Si4684 Control interface operates in I²C Mode when the SMODE pin is tied to VIO.

The Si4684's I²C bus interface supports a 7-bit device addressing procedure and is capable of operating at clock rates up to 400 kHz. Individual data transfers to and from the device are eight bits. The I²C bus consists of two wires: a serial clock line (SCL) and a serial data line (SDA). SCL and SDA are mapped to the SCLK and MOSI pins, respectively.

6.2.1. I²C Device Address Selection

Four device I²C addresses are available, allowing up to four Si4684 receivers to share the same I²C bus. The 7-bit device address consists of a 5-bit fixed part (A6:A2), followed by a programmable 2-bit part (A1:A0). The bit which follows the device address indicates whether a read or write I²C operation occurs.

The voltage on the A0 and A1 lines are used to set the programmable 2-bit part of the device address. The A0 and A1 lines are mapped to the MISO and SSB pins, respectively. A0 and A1 are tied to either GND or VIO for address selection. The various I²C device addresses can be selected as summarized in Table 13.

Table 13. I²C Device Address Selection

A6:A2	A1:A0	A1 Voltage (Pin Connection)	A0 Voltage (Pin Connection)
11001	11	VIO	VIO
11001	10	VIO	GND
11001	01	GND	VIO
11001	00	GND	GND

6.2.2. I²C Standard Operation

An I²C bus transaction begins with the START condition, which occurs when SDA falls while SCL is high. Next, the user drives an 8-bit control byte serially on SDA, which is captured by the external device on rising edges of SCL. The control byte consists of a 7-bit device address followed by a read/write bit (read = 1, write = 0). The Si4684 acknowledges the control word by driving SDA low on the next falling edge of SCL.

Read and write operations are performed in accordance with the I²C bus specification. For write operations, the external device sends an 8-bit data byte on SDA, which is captured by the Si4684 on rising edges of SCL. The Si4684 acknowledges each data byte by driving SDA low for one cycle, after the next falling edge of SCL. The external device may write any number of data bytes in a single 2-wire transaction. The first byte is a command, and the next bytes are arguments.

For read operations, after the Si4684 has acknowledged the control byte, it drives an 8-bit data byte on SDA, changing the state of SDA after the falling edge of SCL. The external device acknowledges each data byte by driving SDA low for one cycle, after the next falling edge of SCL. If a data byte is not acknowledged, the transaction ends. The external device may read any number of data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4684. A 2-wire transaction ends with the STOP condition, which occurs when SDA rises while SCL is high.

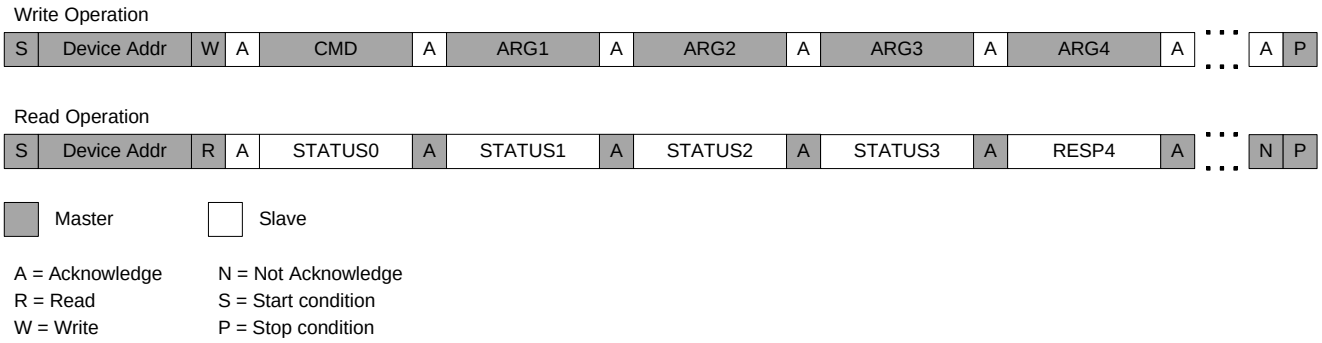


Figure 11. I²C Command/Response Protocol

6.3. Programming

To ease development time and offer maximum customization, the Si4684 provides a simple and powerful software command protocol in addition to the SPI and I^2C control interfaces to communicate with an external controller. The device is programmed using commands, arguments, properties, and responses. To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control actions such as start-up and shut-down, and tune to a station. Arguments are specific to a given command and are used to modify the command. Properties are a special command + argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold. After a command and arguments have been sent to the chip and processed, the user may read a response. The first 32 bits of the response contain the status field, which begins with the clear-to-send (CTS) bit. CTS = “1” indicates that the remaining bytes of response contain valid information and that the chip is ready to receive a new command.

6.4. Serial Flash Interface

The Si4684 Serial Flash interface supports the synchronous transfer of data between the part and an external serial flash memory via a 4-wire SPI bus consisting of the following:

- Serial clock (NVSCLK)
- Slave select (NVSSB), allows the Si4684 to select a slave device
- Master data input pin (NVMISO)
- Master data output pin (NVMOSI)

The Si4684 Serial Flash interface supports SPI Mode 3 (CPHA = 1, CPOL = 1).

6.5. Reset Timing and Power States

The Si4684 supports three power states:

- RESET
- STARTUP
- OPERATIONAL

6.5.1. RESET

The Si4684 is in its lowest-power state when the RSTB pin is asserted (held low). This is the RESET state. All analog and digital circuitry is disabled, and the VA, VCORE and VMEM power supplies are internally disconnected to reduce leakage.

6.5.2. STARTUP

Deasserting (holding high) the RSTB pin places the chip into the STARTUP state, which is a temporary state that enables the Si4684 to respond to the POWER_UP command, and other commands to load software and boot the Si4684.

6.5.3. OPERATIONAL

After software has been loaded, the BOOT command causes the Si4684 to enter the OPERATIONAL state, which is the highest-power state. The Si4684 can be returned to the RESET state by asserting (holding low) the RSTB pin.

Figure 12 shows required reset, startup, and shutdown timings for the Si4684. RSTB must be held low (asserted) during any power supply transitions and remain asserted for 10 µs after all power supplies are stable as specified in Figure 12. Failure to assert RSTB as indicated here may cause the device to malfunction and may result in permanent device damage.

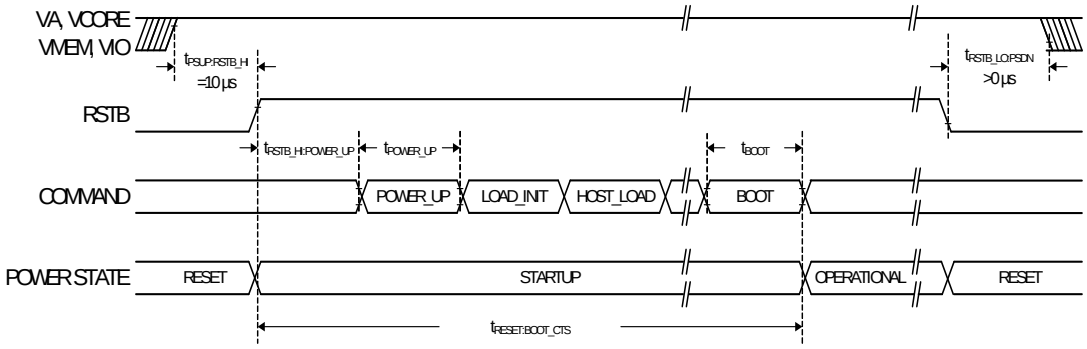


Figure 12. Reset, Startup, and Shutdown Timing

Table 14 shows typical STARTUP power state, POWER_UP command, and BOOT command timings.

Table 14. STARTUP Power State, POWER_UP Command, and BOOT Command Timings

Parameter	Symbol	Analog FM	DAB	Unit
Power supplies ramped up and stable to RSTB rise	$t_{PSUP:RSTB\_HI}$	10		µs
RSTB fall to start of power supplies ramp down	$t_{RSTB\_LO:PSDN}$	0		µs
RSTB rise to start of POWER_UP Command[1]	$t_{RSTB\_HI:POWER\_UP}$	5	5	ms
Start of POWER_UP Command to end of POWER_UP Command[1]	t_{POWER_UP}	3	3.2	ms
Start of BOOT Command to end of BOOT Command[1]	t_{BOOT}	63	269	ms
RSTB rise to end of BOOT Command Clear-to-Send (CTS)[1,2,3,4,5,6]	$t_{RESET:BOOT\_CTS}$	745	965	ms

Notes:

1. Characteristics apply to firmware FM 2.0.10 and firmware DAB 1.0.6. For later firmware versions see "Si468x Data Sheet Addendum".
2. Firmware downloaded with SPI bus @ 10 MHZ clock rate.
3. SPI bus transactions clocked as one continuous block of data.
4. CTS polled between each command.
5. Additional delay between CTS polls @ 1 ms.
6. HOST_LOAD commands sent with 4092-byte payloads.

7. Pin Descriptions

7.1. Si4684-A10-GM Pin Description

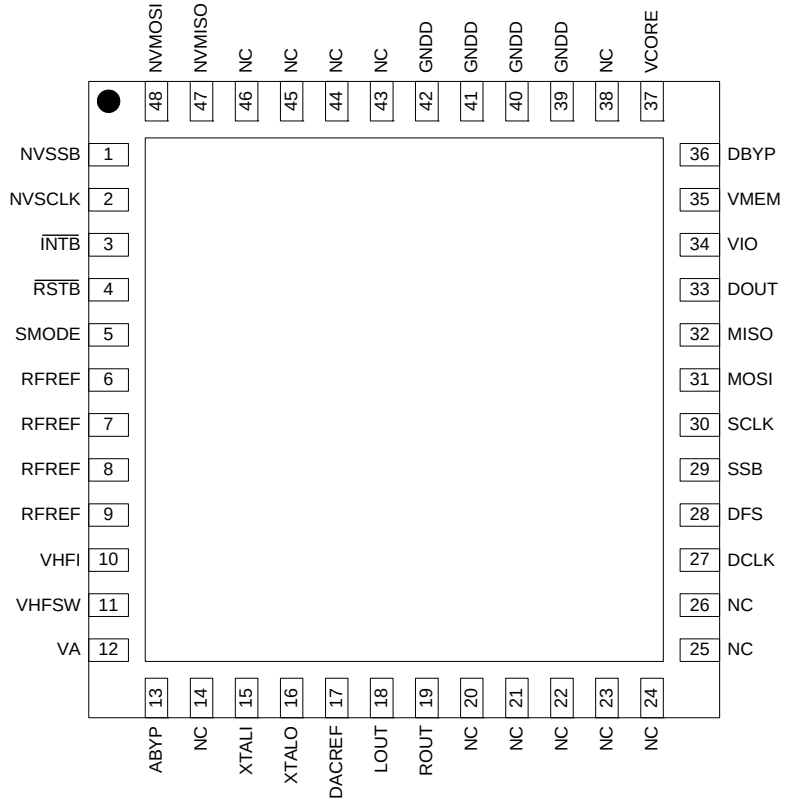


Figure 13. Si4684-A10-GM Pinout

Table 15. Pin Descriptions for Si4684-A10-GM

Pin Number	Pin Name	I/O	Description
1	NVSSB	O	SPI slave select for serial flash
2	NVSCLK	O	SPI clock for serial flash
3	INTB	O	Host IRQ
4	RSTB	I	Active low reset signal
5	SMODE	I	SMODE = 0 ⟶ SPI, SMODE = 1 ⟶ I^2C to control Si4684
6	RFREF	PWR	RF ground reference
7	RFREF	PWR	RF ground reference
8	RFREF	PWR	RF ground reference
9	RFREF	PWR	RF ground reference
10	VHFI	I	VHF LNA input
11	VHFSW	O	VHF front-end switch; 0 ⟶ switch open; 1 ⟶ switch closed
12	VA	PWR	Analog supply voltage
13	ABYP	PWR	Analog bypass

Table 15. Pin Descriptions for Si4684-A10-GM (Continued)

Pin Number	Pin Name	I/O	Description
14	NC	NC	No connect; leave floating
15	XTALI	I	Crystal amp input
16	XTALO	O	Crystal amp output
17	DACREF	PWR	DAC reference supply voltage
18	LOUT	O	Left channel audio DAC output (powered from VA)
19	ROUT	O	Right channel audio DAC output (powered from VA)
20	NC	NC	No connect; leave floating
21	NC	NC	No connect; leave floating
22	NC	NC	No connect; leave floating
23	NC	NC	No connect; leave floating
24	NC	NC	No connect; leave floating
25	NC	NC	No connect; leave floating
26	NC	NC	No connect; leave floating
27	DCLK	I/O	I^2S clock for digital audio
28	DFS	I/O	I^2S frame sync for digital audio
29	SSB	I	SPI slave select or I^2C address A1
30	SCLK	I	SPI or I^2C clock input
31	MOSI	I/O	SPI data input or I^2C data I/O
32	MISO	I/O	SPI data output or I^2C address A0
33	DOUT	O	I^2S audio output
34	VIO	PWR	Interface supply voltage
35	VMEM	PWR	Memory supply voltage
36	DBYP	PWR	Digital bypass
37	VCORE	PWR	Digital core supply voltage
38	NC	NC	No connect; leave floating
39	GNDD	PWR	Digital ground
40	GNDD	PWR	Digital ground
41	GNDD	PWR	Digital ground
42	GNDD	PWR	Digital ground
43	NC	NC	No connect; leave floating
44	NC	NC	No connect; leave floating
45	NC	NC	No connect; leave floating
46	NC	NC	No connect; leave floating
47	NVMISO	I	SPI master data input for serial flash
48	NVMOSI	O	SPI master data output for serial flash

7.2. Si4684-A10-GD Pin Description

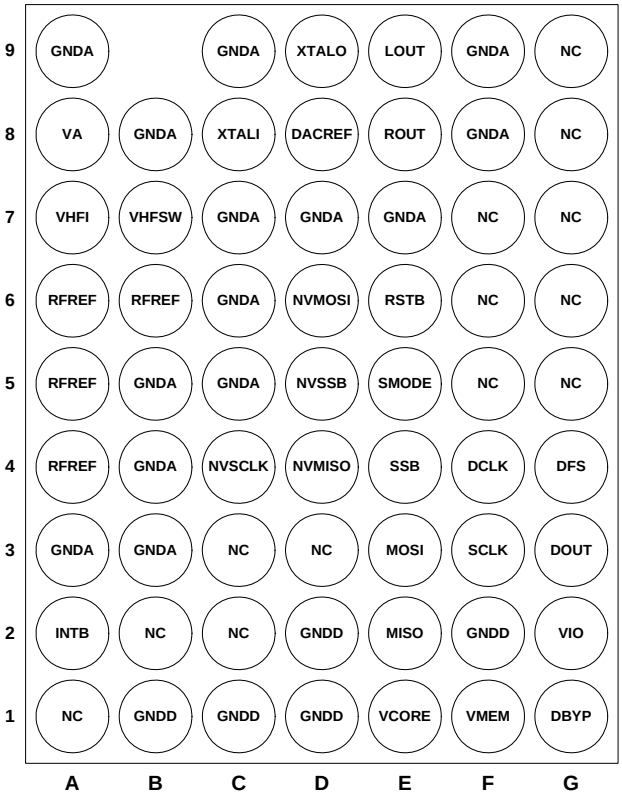


Figure 14. Si4684-A10-GD Pinout

Table 16. Pin Descriptions for Si4684-A10-GD

Pin Number	Pin Name	I/O	Description
A1	NC	NC	No connect; leave floating
A2	INTB	O	Host IRQ
A3	GNDA	PWR	Analog ground
A4	RFREF	PWR	RF ground reference
A5	RFREF	PWR	RF ground reference
A6	RFREF	PWR	RF ground reference
A7	VHFI	I	VHF LNA input
A8	VA	PWR	Analog supply voltage
A9	GNDA	PWR	Analog ground
B1	GNDD	PWR	Digital ground
B2	NC	NC	No connect; leave floating
B3	GNDA	PWR	Analog ground
B4	GNDA	PWR	Analog ground

Table 16. Pin Descriptions for Si4684-A10-GD (Continued)

Pin Number	Pin Name	I/O	Description
B5	GNDA	PWR	Analog ground
B6	RFREF	PWR	RF ground reference
B7	VHFSW	O	VHF front-end switch; 0 ⟶ switch open; 1 ⟶ switch closed
B8	GNDA	PWR	Analog ground
B9	NC	NC	No connect; leave floating
C1	GNDD	PWR	Digital ground
C2	NC	NC	No connect; leave floating
C3	NC	NC	No connect; leave floating
C4	NVSCLK	O	SPI clock for serial flash
C5	GNDA	PWR	Analog ground
C6	GNDA	PWR	Analog ground
C7	GNDA	PWR	Analog ground
C8	XTALI	I	Crystal amp input
C9	GNDA	PWR	Analog ground
D1	GNDD	PWR	Digital ground
D2	GNDD	PWR	Digital ground
D3	NC	NC	No connect; leave floating
D4	NVMISO	I	SPI master data input for serial flash
D5	NVSSB	O	SPI slave select for serial flash
D6	NVMOSI	O	SPI master data output for serial flash
D7	GNDA	PWR	Analog ground
D8	DACREF	PWR	DAC reference supply voltage
D9	XTALO	O	Crystal amp output
E1	VCORE	PWR	Digital core supply voltage
E2	MISO	I/O	SPI data output or I^2C address A0
E3	MOSI	I/O	SPI data input or I^2C data I/O
E4	SSB	I	SPI slave select or I^2C address A1
E5	SMODE	I	SMODE = 0 ⟶ SPI, SMODE = 1 ⟶ I^2C to control Si4684
E6	RSTB	I	Active low reset signal
E7	GNDA	PWR	Analog ground
E8	ROUT	O	Right channel audio DAC output (powered from VA)
E9	LOUT	O	Left channel audio DAC output (powered from VA)

Table 16. Pin Descriptions for Si4684-A10-GD (Continued)

Pin Number	Pin Name	I/O	Description
F1	VMEM	PWR	Memory supply voltage
F2	GNDD	PWR	Digital ground
F3	SCLK	I	SPI or I^2C clock input
F4	DCLK	I/O	I^2S clock for digital audio
F5	NC	NC	No connect; leave floating
F6	NC	NC	No connect; leave floating
F7	NC	NC	No connect; leave floating
F8	GNDA	PWR	Analog ground
F9	GNDA	PWR	Analog ground
G1	DBYP	PWR	Digital bypass
G2	VIO	PWR	Interface supply voltage
G3	DOUT	O	I^2S audio output
G4	DFS	I/O	I^2S frame sync for digital audio
G5	NC	NC	No connect; leave floating
G6	NC	NC	No connect; leave floating
G7	NC	NC	No connect; leave floating
G8	NC	NC	No connect; leave floating
G9	NC	NC	No connect; leave floating

8. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4684-A10-GM	FM/DAB/DAB+ Digital Radio Receiver with RDS/ RBDS	QFN Pb-free	–40 to 85 °C
Si4684-A10-GD	FM/DAB/DAB+ Digital Radio Receiver with RDS/ RBDS	WLCSP Pb-free	–40 to 85 °C
***Note:** Add an “R” at the end of the device part number to denote tape-and-reel option.			

9. Package Outlines

9.1. Si4684-A10-GM Package Outline

Figure 15 illustrates the package details for the Si4684. Table 18 lists the values for the dimensions shown in the illustration.

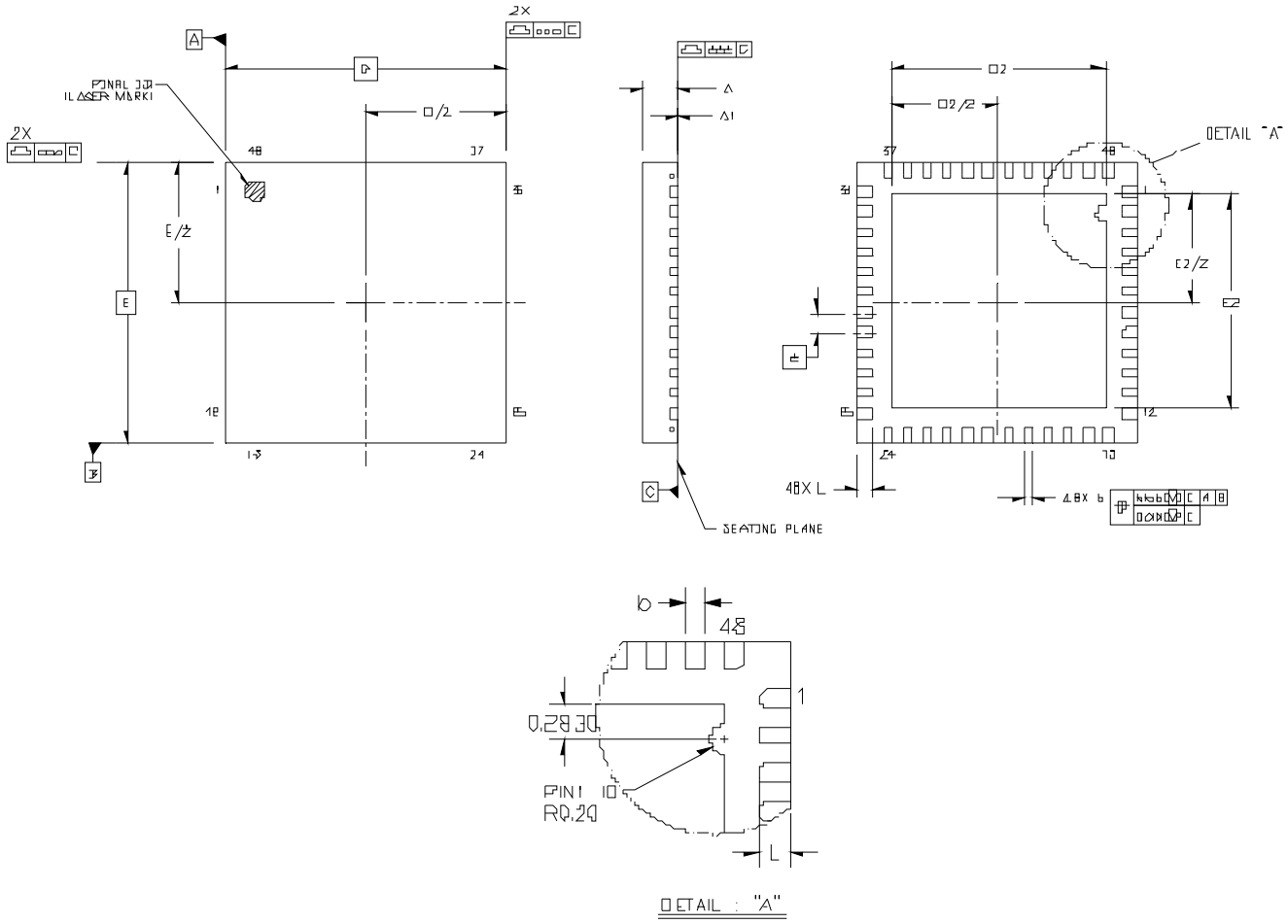


Figure 15. 7 x 7 mm 48-pin QFN

Table 17. Package Dimensions

Dimension	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	7.00 BSC		
D2	5.20	5.30	5.40
e	0.50 BSC		
E	7.00 BSC		
E2	5.20	5.30	5.40
L	0.30	0.40	0.50
aaa	0.15		
bbb	0.10		
ddd	0.05		
eee	0.08		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2. Si4684-A10-GD Package Outline

Figure 16 illustrates the package details for the Si4684. Table 18 lists the values for the dimensions shown in the illustration.

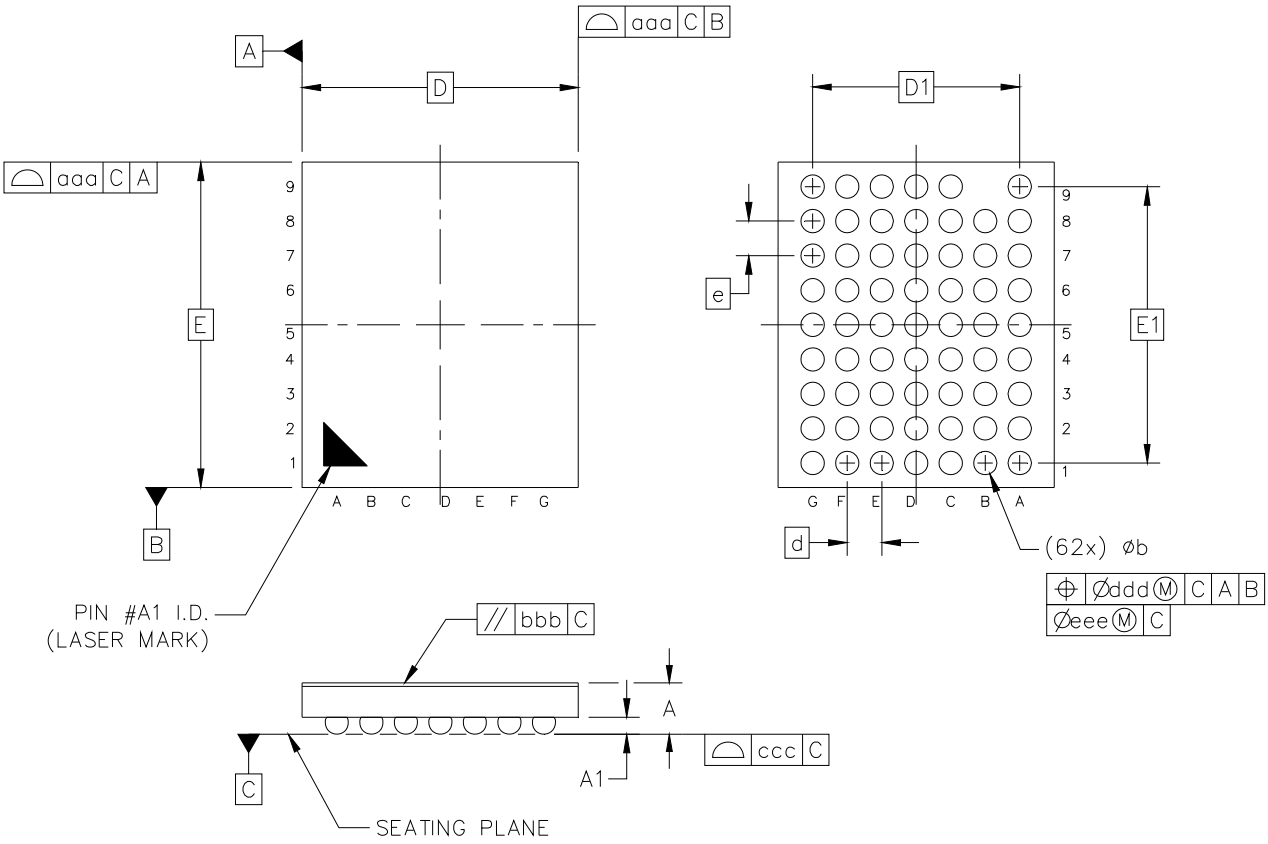


Figure 16. 3.2 x 3.7 mm 62-ball WLCSP

Table 18. Package Dimensions

Dimension	Millimeters		
	Min	Nom	Max
A	0.55	0.59	0.63
A1	0.18	0.20	0.22
b	0.22	0.27	0.32
D	3.20 BSC		
E	3.77 BSC		
d	0.40 BSC		
e	0.40 BSC		
D1	2.40 BSC		
E1	3.20 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.03		
ddd	0.15		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. PCB Land Patterns

10.1. Si4684-A10-GM PCB Land Pattern

Figure 17 illustrates the PCB land pattern details for the Si4684. Table 19 lists the values for the dimensions shown in the illustration.

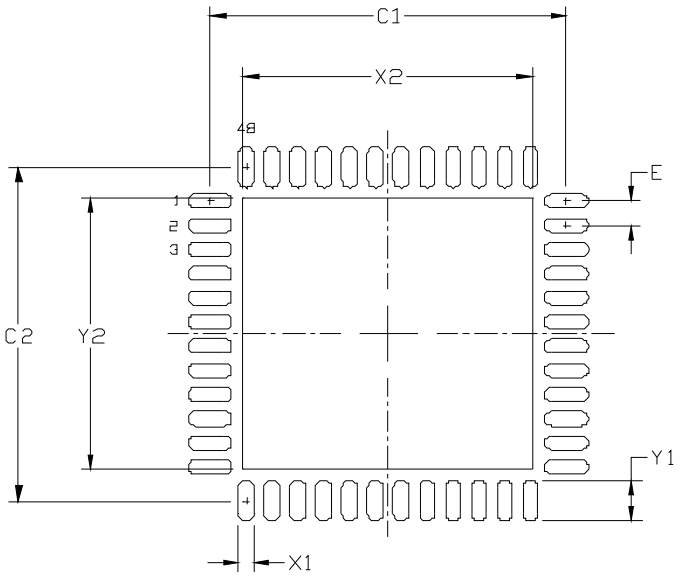


Figure 17. PCB Land Pattern

Table 19. PCB Land Pattern Dimensions

Dimension	Millimeters	
	Min	Max
C1	6.80	6.90
C2	6.80	6.90
E	0.50 BSC	
X1	0.20	0.30
X2	5.20	5.40
Y1	0.75	0.85
Y2	5.20	5.40

Notes:

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design:

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Solder Mask Design:

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 4x4 array of 1.1 mm square openings on 1.3 mm pitch should be used for the center ground pad.

Solder Mask Design:

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2. Si4684-A10-GD PCB Land Pattern

Figure 18 illustrates the PCB land pattern details for the Si4684. Table 20 lists the values for the dimensions shown in the illustration.

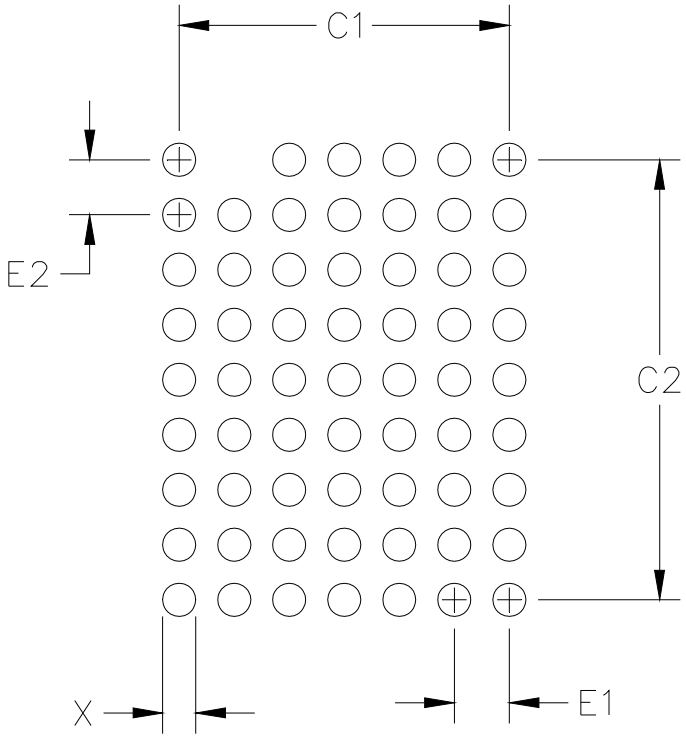


Figure 18. PCB Land Pattern

Table 20. PCB Land Pattern Dimensions

Dimension	Millimeters		
	Min	Nom	Max
X	0.23	0.24	0.25
C1		2.40	
C2		3.20	
E1		0.40	
E2		0.40	

Notes:

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensions and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design:

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

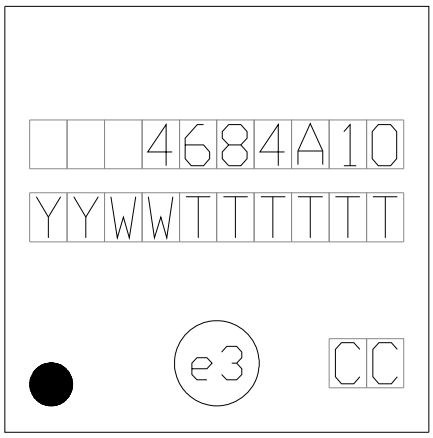
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly:

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Top Markings

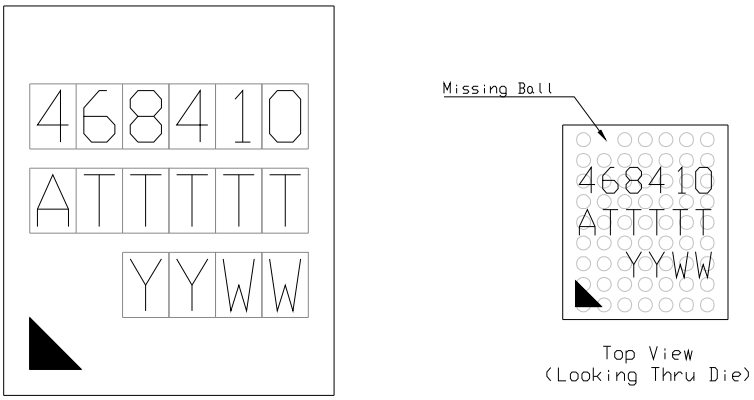
11.1. Si4684-A10-GM Top Marking



11.2. Si4684-A10-GM Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number (Right-justified)	4684 = Si4684 A = Part revision A 10 = Firmware revision 1.0
Line 2 Marking:	YY = Year WW = Work Week TTTTTT = Mfg Code	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date. Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Marking:	Circle = 1.3 mm diameter (Center Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	CC = Country Code (e.g., “TW” for Taiwan)
Pin 1 Mark:	Circle = 0.70 mm diameter (Bottom Left-justified)	

11.3. Si4684-A10-GD Top Marking



11.4. Si4684-A10-GD Top Marking Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number (Right-justified)	4684 = Si4684 10 = Firmware revision 1.0
Line 2 Marking:	A TTTTT = Mfg Code	A = Part revision A Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date.
Pin 1 Mark:	Right Triangle = 0.50 mm equal sides (Bottom Left-justified)	

DOCUMENT CHANGE LIST

Revision 0.6 to Revision 0.7

- Updated the typical application schematic to reflect the newly recommended front-end network
- Updated the audio interface section to remove all unsupported audio data formats
- Updated the part number for the QFN version
- Updated the top marking drawings

Revision 0.7 to Revision 0.8

- Added the junction temperature test condition and max limit spec for the WLCSP package to Table 10 on page 15.
- Updated the max current limits for the analog FM mode on page 5.
- Updated the applications list on the cover page.
- Updated the functional block diagram on page 2 and page 17.

Revision 0.8 to Revision 1.0

- Added voltage and current specs for the digital pins.
- Updated the Control Interface description on p.23 for improved accuracy.
- Changed the frequency cited in Note 2 of Table 8 on page 12 from 98.0 MHz to 195.936 MHz.
- Fixed the direction of the SSB and MISO signals in the functional block diagram in p.2 and p.18.
- Fixed the I^2S Digital Audio and Serial Flash interface timing diagrams on p.9 and p.10, respectively.
- Augmented the description, figure and table in Section "6.5. Reset Timing and Power States" on page 28 with additional Reset timing information.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.