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Replace each AND gate in Figure 5-6 with an AND gate with one additional input and connect this input to the following: $S_1 + S_0$ This will force the outputs of all the AND gates to zero, and, on the next clock edge, the register will be cleared if S_1 is 0 and S_0 is logic one. Also, replace each direct shift input with this equation: $S_1 S_0$ This will...

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