
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32H723VET_DUAL_merged1
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	01/07/2022

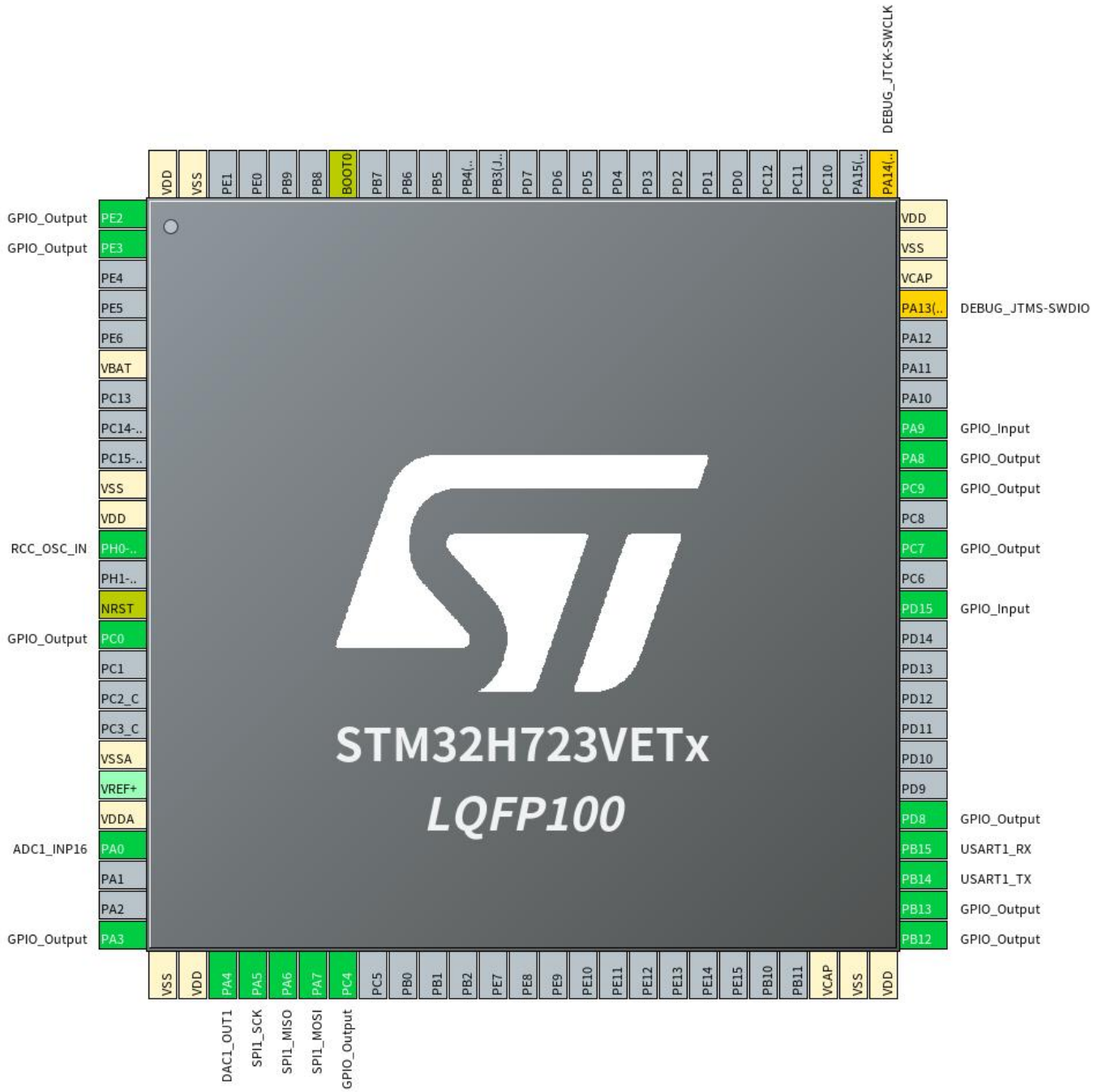
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



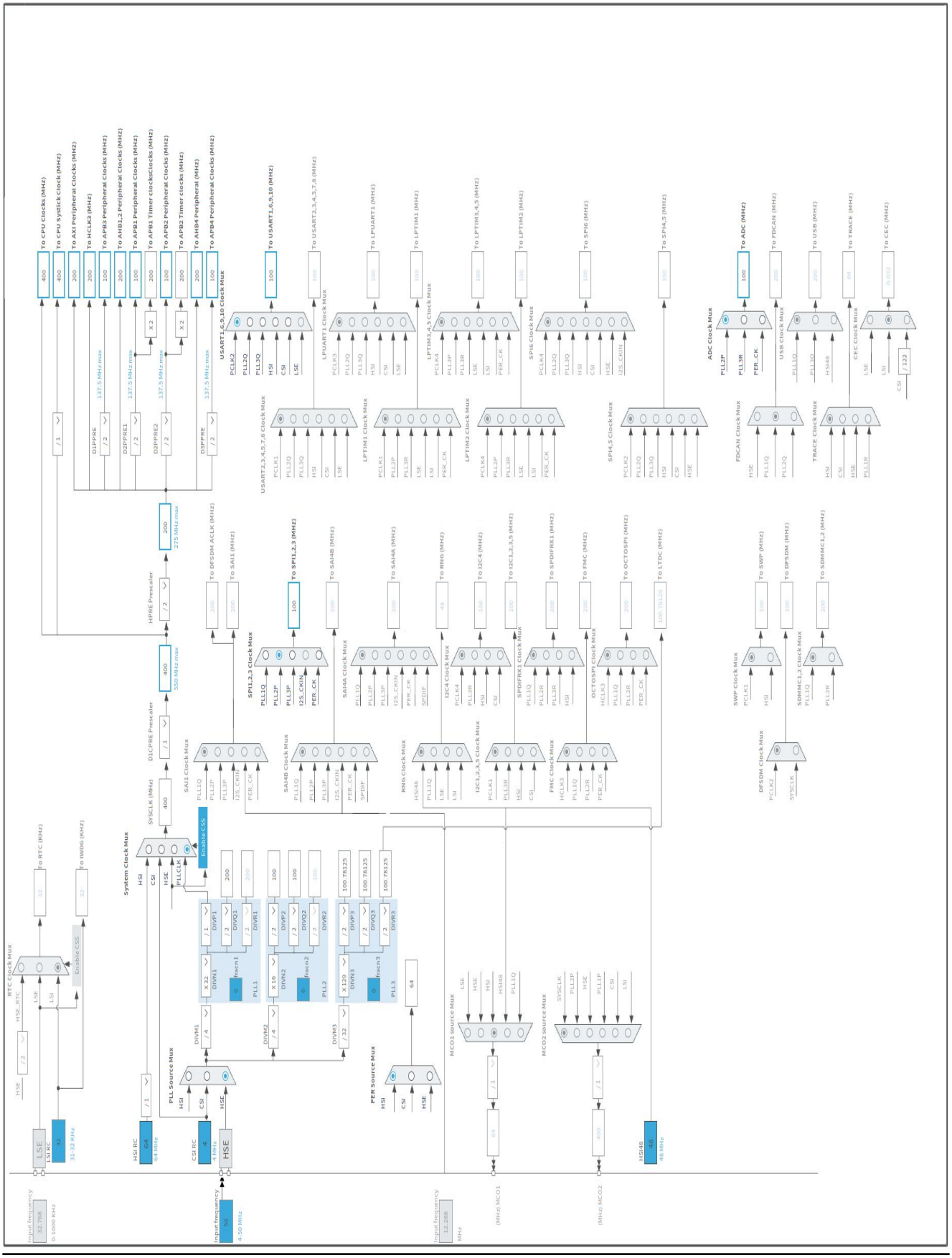
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	
2	PE3 *	I/O	GPIO_Output	
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	ADC1_INP16	
25	PA3 *	I/O	GPIO_Output	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DAC1_OUT1	
29	PA5	I/O	SPI1_SCK	
30	PA6	I/O	SPI1_MISO	
31	PA7	I/O	SPI1_MOSI	
32	PC4 *	I/O	GPIO_Output	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	
52	PB13 *	I/O	GPIO_Output	
53	PB14	I/O	USART1_TX	
54	PB15	I/O	USART1_RX	
55	PD8 *	I/O	GPIO_Output	
62	PD15 *	I/O	GPIO_Input	
64	PC7 *	I/O	GPIO_Output	
66	PC9 *	I/O	GPIO_Output	
67	PA8 *	I/O	GPIO_Output	
68	PA9 *	I/O	GPIO_Input	
72	PA13(JTMS/SWDIO) **	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
76	PA14(JTCK/SWCLK) **	I/O	DEBUG_JTCK-SWCLK	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function
** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32H723VET_DUAL_merged1
Project Folder	/mnt/development/engr/Programming/stm32/ITF/STM32H723VTE_DUAL_REV11
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_SPI1_Init	SPI1
4	MX_DMA_Init	DMA
5	MX_ADC1_Init	ADC1
6	MX_DAC1_Init	DAC1
7	MX_TIM6_Init	TIM6
8	MX_USART1_UART_Init	USART1
9	MX_TIM3_Init	TIM3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723VETx
Datasheet	DS13313_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

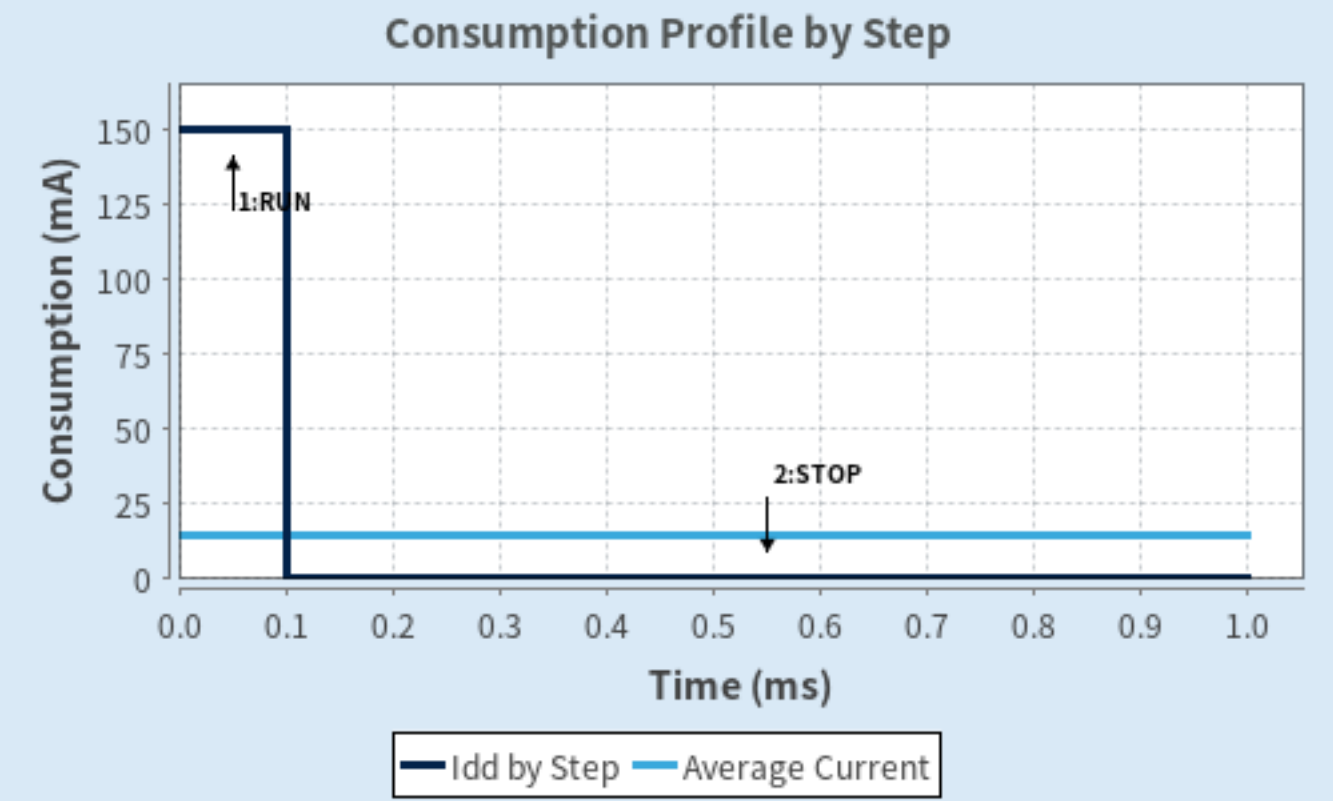
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-ON/Cache	NA
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL_CLOCKS_OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	94.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	1177.0	0.0
Ta Max	104.75	124.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN16: IN16 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 8 ***
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA One Shot Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 16
Sampling Time	**2.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. DAC1

OUT1 connected to: only external pin

7.2.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

7.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.3.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.5. SYS

Timebase Source: SysTick

7.6. TIM3

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1-1
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.7. TIM6

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**400 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. USART1

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable

TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	**Pull-down ***	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	**Pull-down ***	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	**Pull-down ***	**Very High ***	
USART1	PB14	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	Low

ADC1: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt	true	0	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	0	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI1 global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
TIM3 global interrupt	false	true	true

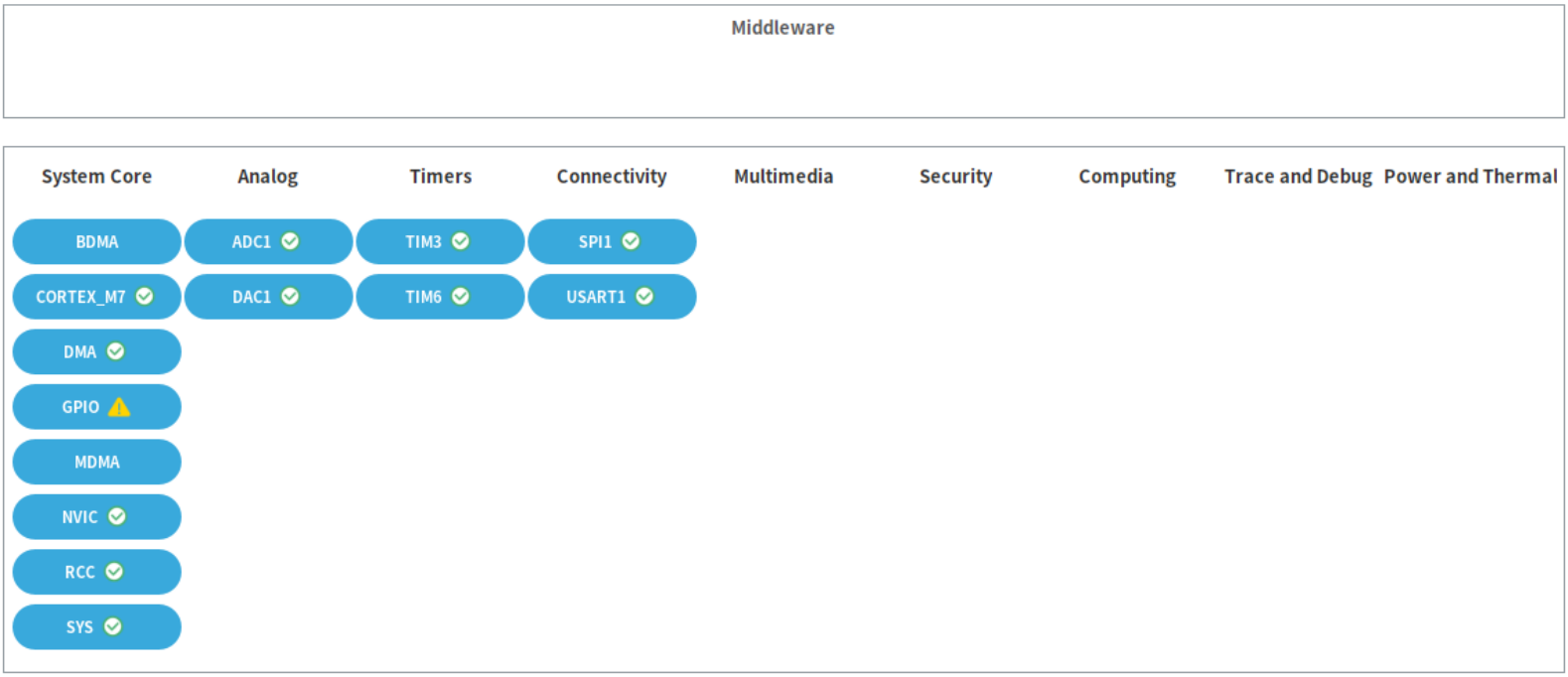
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
USART1 global interrupt	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00701028.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00603761.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00625312.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00663674.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf