BUG DOCUMENTATION FOR PROJECT 1

FETCH BUGS:

BUG 1) At reset, pc starts from x3001 instead of x3000.

BUG 2) When no branch is taken, i.e. br_taken==0, pc increments by 2 instead of 1.

BUG 4) When enable_fetch is low, instrmem_rd is "0" instead of "z"

BUG 3) npc_out is "pc+3" instead of "pc+1." An extra adder is present at the output of npc_out.

DECODE BUGS:

BUG 5) npc_out should be synchronously connected to npc_in. Instead, npc_out is synchronously connected to "npc_in + 1."

BUG 6) Opcodes for AND and ADD operations are swapped.

BUG 7) op2select should be "~Instr_dout [5]". Instead, op2select is set to Instr_dout[5]

BUG 8) For LEA instruction, pcselect1 is "2" instead of "1."

BUG 9) For LEA instruction, pcselect2 is "0" instead of "1."

BUG 10) For ALU operations, W_Control is "1" instead of "0"

BUG 11) For LEA operations, W_Control is "0" instead of "2"

BUG 29) NOT operation does not work. Internal case statement uses bits 3 and 0 of opcode instead of bits 1 and 0, to select between ALU, CONTROL and MEMORY instruction. For this part of the project, only ALU and LEA instructions are considered.

EXECUTE BUGS:

BUG 12) For ALU operations, src2 is derived from IR[3:1] instead of IR[2:0].

BUG 13) For Load instructions, src2 is fixed to 3'b1 instead of 3'b0.

BUG 14) For ALU operations, dr is derived from IR[10:8] instead of IR[11:9].

BUG 15) For Load instructions, dr is derived from IR[12:10] instead of IR[11:9].

BUG 16) After reset, W_Control_out, Mem_Control_out and M_data is synchronously connected to the corresponding inputs, without being sensitive to enable_execute. Instead the pipeline is always on.

BUG 17) pcselect2 and pcselect1 are swapped in their derivation from E_Control.

BUG 18) Inside the extension sub-block, the offset9 is generated by sign-extending the last 8 bits [7:0] of IR instead of 9 bits [8:0].

BUG 19) Inside the extension sub-block, the imm5 is generated by sign-extending the last 4 bits [3:0] of IR instead of 5 bits [4:0].

BUG 20) While doing AND operation, bits 5 and 6 of aluin2 are swapped.

WRITEBACK BUGS:

BUG 21) DR_in should be derived from aluout when W_Control is 0 and from pcout when W_Control is 2. Instead, DR_in is derived from aluout when W_Control is 2 and from pcout when W_Control is 0.

BUG 22) When DR_in is negative, psr should be 3'b100. Instead it is 3'b110.

BUG 23) While writing to the register file RF , the MSB and the LSB of the din are swapped.

BUG 24) While reading from the register file RF, the MSB of src1, is stuck to 1.

CONTROLLER BUGS:

BUG 25) The LC3 microcontroller pipeline does not wait for complete_instr to go high at the Fetch stage of the pipeline. Instead, the enable_decode always goes high next cycle after the enable_fetch.

BUG 26) One clock cycle after the enable_execute, the enable_decode goes high along with enable_writeback.

BUG 27) One clock cycle after the enable_decode, both enable_decode and enable_execute remain high, instead of only enable_execute.

BUG 28) One clock cycle after the enable_writeback, both enable_updatePC and enable_writeback remain high, instead of only enable_updatePC.