




# **C2000™ Software Diagnostic Library for TMS320F28004x**

## **API USER'S GUIDE**

---

# Copyright

Copyright © 2021 Texas Instruments Incorporated. All rights reserved. Other names and brands may be claimed as the property of others.

 Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this document.

Texas Instruments  
13905 University Boulevard  
Sugar Land, TX 77479  
<http://www.ti.com/c2000>



## Revision Information

This is version 2.01.00 of this document, last updated on Fri Feb 12 19:24:02 IST 2021.

# Table of Contents

<b>Copyright</b>	<b>1</b>
<b>Revision Information</b>	<b>1</b>
<b>1 Introduction</b>	<b>3</b>
1.1 Terms and Abbreviations	4
1.2 References	4
<b>2 Diagnostic Self-Test Library</b>	<b>5</b>
<b>3 Using the Diagnostic STL</b>	<b>6</b>
3.1 Overview of the Library	6
3.2 Using the Library	8
<b>4 Library Modules</b>	<b>9</b>
4.1 CAN Message RAM Test API Functions	9
4.2 CPU Register API Functions	13
4.3 CRC API Functions	16
4.4 March13N Test API Functions	20
4.5 Oscillator CPU Timer API Functions	26
4.6 Oscillator HRPWM API Functions	29
4.7 PIE RAM API Functions	31
4.8 Utilities API Functions	35
<b>5 Self-Test Application</b>	<b>39</b>
5.1 Getting Started	39
5.2 Example Behavior	40
5.3 STA_Tests API Functions	41
5.4 STA_Timer API Functions	43
5.5 STA_Comm API Functions	45
5.6 STA_Util API Functions	46
5.7 STA_User API Functions	48
<b>6 Integration Notes</b>	<b>50</b>
6.1 Cycle Time	50
6.2 Memory Usage	51
<b>7 Safety Feature and Diagnostic Examples</b>	<b>52</b>
7.1 Using DCSM for Freedom From Interference (FFI)	52
7.2 Test of ECC logic in Flash	53
7.3 Test of Flash Prefetch, Data Cache and Wait-States	53
7.4 Missing clock detection	54
7.5 RAM access protection violation detection	54
7.6 Test of parity/ECC logic in SRAM	55
7.7 Software test of watchdog operation	56
<b>IMPORTANT NOTICE</b>	<b>57</b>

# 1 Introduction

Terms and Abbreviations .....	4
References .....	4

This is a release of the C2000™ Software Diagnostic Library for F28004x devices. The Diagnostic Library is a collection of self-test libraries (STL) and examples. This document will provide an overview of the Software Diagnostic Library (SDL) and its functions.

Manufacturers of end equipments must take steps to ensure safe and reliable operation of their products in order to meet specific industry safety standards. Specific safety measures and diagnostic tests are recommended or required in order to meet each particular safety standard. The SDL is designed to enable customers to more efficiently and effectively work to meet such safety standards by their systems.

**Note that the SDL has not itself undergone any third-party assessment or certification to a particular standard.** It is intended to provide reference implementations of diagnostics and usage examples of hardware diagnostic features. The system integrator should consider which safety mechanisms are required by the standard they are targeting and whether the SDL will aid in achieving those safety mechanisms.

Considerations for integrating the SDL should include but are not limited to:

- the safety mechanism as such
- the targeted faults of the diagnostic test
- the API definitions (parameters, functionality, return values)
- the global error flags which could be set on a detected fault
- the error injection techniques available
- the memory requirements of the software components
- the time or cycle requirements for the diagnostic test
- the effect of the diagnostic test on the state of the peripheral and/or system
- the interrupt service routines used in the SDL

The source code of the SDL is provided to enable the system integrator to modify and test the software components as desired. For instance, a subset of SDL components utilize their own interrupt service routines. It may be desirable to integrate the functionality of the SDL ISRs into the system ISRs. In this case, the same ISR could be used to serve the purpose of the system as well as the diagnostic test.

For more information about diagnostic libraries for C2000 microcontrollers, visit the [C2000 Safety Software Libraries page on ti.com](http://ti.com).

## 1.1 Terms and Abbreviations

API	Application Programming Interface
C2000Ware	A cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation of your product.
C28x Driverlib	A set of header files describing the hardware and a set of drivers that use those header files to access the peripherals. The Driverlib and its examples are intended to be used with Code Composer Studio and TI's C2000 C Compiler. They will be delivered within C2000Ware.
CCS	Code Composer Studio
PEST	Periodic Self-Test
POST	Power-On Self-Test
SFO	Scale Factor Optimization
SM	Safety Mechanisms
STA	Self-Test Application
STL	Self-Test Library
SW	Software

## 1.2 References

<a href="#">SPRS945</a>	TMS320F28004x Piccolo™ Microcontrollers datasheet
<a href="#">SPRZ439</a>	TMS320F28004x MCUs silicon errata
<a href="#">SPRUI33</a>	TMS320F28004x Microcontrollers Technical Reference Manual
<a href="#">SPRUID8</a>	TMS320F28004x Safety Manual UG
<a href="#">SAFETI_CQKIT</a>	SafeTI™ Compiler Qualification Kit

## 2 Diagnostic Self-Test Library

Current and future C2000™ microcontrollers are designed with integrated features that can be used in safety-critical systems. Manufacturers of end equipment must take steps to ensure safe and reliable operation of their systems in order to meet the relevant standards.

Hardware features such as write-protected registers and supervisory circuits have all been integrated in C2000 MCUs. These features, leveraged to the diagnostic test and safety mechanism requirements of the targeted safety standard, make compliance in the electronic segment of the tests more easily achievable.

The C2000™ Software Diagnostic Library is a collection of optimized independent test functions for C2000 MCUs. The library includes C-callable optimized test functions that return the status of the test performed. In case of a failure returned signifying a detected fault, it is up to the user application to determine the appropriate action to take.

The SDL consists of individual functions that are called and managed by the user's application software. Each function is designed with a specific task to verify functionality of a device component using a specific safety mechanism consistent with safety standards with minimal impact on the real-time control performance of the target MCU. STL functions are provided to support POST, PEST, or both.

In addition to the library modules, the SDL also contains examples to demonstrate the use of the library and the configuration of hardware diagnostic features.

## 3 Using the Diagnostic STL

Overview of the Library .....	6
Using the Library .....	8

### 3.1 Overview of the Library

The following subsections briefly list and describe the error reporting mechanisms, contents, and coverage of the diagnostic library. The library is delivered with several example CCS projects. The `test_application` demonstrates the use of all the library modules. See the Self-Test Application section of this document for more details on the example.

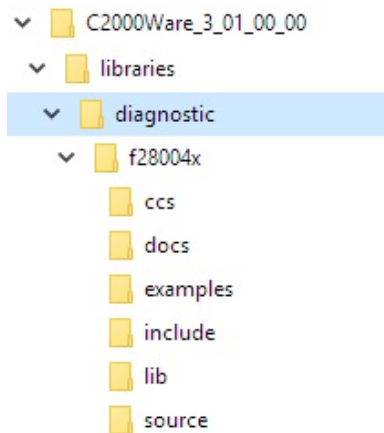


Figure 3.1: Directory Structure

### Error Reporting

All the API functions in the diagnostic library return the status of the test. If the test fails, the functions set a unique error code to a 32-bit global variable, **STL\_Util\_globalErrorFlags**. All codes are defined in `stl_util.h` and start with **STL\_UTIL\_** followed by a representation of the test. For example, **STL\_UTIL\_OSC\_TIMER2** represents the error code the oscillator frequency test.

### Library Files

The diagnostic library consists of the following files. All source files with a `.c` and `.asm` extension have an associated header file that contains function prototypes and data structures. For example for `stl_osc_ct.c` there is an associated `stl_osc_ct.h` file that declares the function prototypes, data types, and `#defines`.

File Name	Source Description
<code>stl_can_ram.c</code>	CAN Message RAM parity test

stl_cpu_reg.asm	C-callable assembly test of CPU, FPU, VCU registers
stl_crc.c	CRC code for E2E communications and memory tests
stl_crc_s.asm	C-callable assembly CRC code
stl_march.c	March test
stl_march_s.asm	C-callable assembly for March test
stl_osc_ct.c	Internal OSC Frequency test
stl_osc_hr.c	High Resolution OSC (HRPWM) Frequency test
stl_pie_ram.c	PIE RAM Redundancy test
stl_util.c	Utility functions, primarily for managing error flags



## 3.2 Using the Library

This section describes all the necessary steps that are required to rebuild and use the library in an application.

### Library Build Options

The current version of the library was built with CCSv9 using C28x Codegen Tools v18.12.3.LTS with the following options:

- -v28
- -ml
- -mt
- -vcu\_support=vcu0
- -float\_support=fpu32
- -tmu\_support=tmu0

### Rebuilding the Library

The diagnostic safety library ships with the original CCS projectspec file that was used to build the library. This project can be used as a template to modify and rebuild the library.

1. Create a new workspace.
2. Import the projectspec file found in `..\ccs\`
3. Make the required changes.
4. Right click project and select Build Configurations -> Clean All and when that completes Build Configurations -> Build All.
5. The new library will be placed in the `..\lib\` folder.

## 4 Library Modules

CAN Message RAM API Functions .....	9
CPU Registers Test API Functions .....	13
CRC API Functions .....	16
March13N Test API Functions .....	20
Oscillator CPU Timer API Functions .....	26
Oscillator HRPWM API Functions .....	29
PIE RAM API Functions .....	31
Utilities API Functions .....	35

### 4.1 CAN Message RAM Test API Functions

#### Macros

- #define **STL\_CAN\_RAM\_PASS**
- #define **STL\_CAN\_RAM\_ERROR**
- #define **STL\_CAN\_RAM\_ADDR\_OFFSET**
- #define **STL\_CAN\_RAM\_MAX\_ADDR\_OFFSET**
- #define **STL\_CAN\_RAM\_PARITY\_OFF**
- #define **STL\_CAN\_RAM\_NO\_COPY**

#### Functions

- void **STL\_CAN\_RAM\_testRAM** (const uint32\_t canBase, const **STL\_March\_Pattern** pattern, const uint32\_t startAddress, const uint32\_t endAddress, const uint32\_t copyAddress)
- void **STL\_CAN\_RAM\_injectError** (const uint32\_t canBase, const uint32\_t address, const uint32\_t xorMask)
- uint16\_t **STL\_CAN\_RAM\_checkErrorStatus** (const uint32\_t canBase)

#### 4.1.1 Detailed Description

The code for this module is contained in `source/stl_can_ram.c` and `source/stl_can_ram_s.asm`, with `include/stl_can_ram.h` containing the API declarations for use by applications.

#### Error Injection

Here are techniques to inject error:

**STL\_CAN\_RAM\_testRAM()**, **STL\_CAN\_RAM\_checkErrorStatus()**

- Call **STL\_CAN\_RAM\_injectError()** with an *xorMask* value that will cause errors.

## 4.1.2 Macro Definition Documentation

### 4.1.2.1 #define STL\_CAN\_RAM\_NO\_COPY

Value to indicate to [STL\\_CAN\\_RAM\\_testRAM\(\)](#) through the **copyAddress** parameter that the test should run a destructive test on the region of CAN message RAM without saving and restoring its contents.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 4.1.3 Function Documentation

### 4.1.3.1 void STL\_CAN\_RAM\_testRAM ( const uint32\_t *canBase*, const **STL\_March\_Pattern** *pattern*, const uint32\_t *startAddress*, const uint32\_t *endAddress*, const uint32\_t *copyAddress* )

Performs a March13N memory test on the specified range of CAN message RAM objects.

Parameters

<i>canBase</i>	is the base address of the CAN controller.
<i>pattern</i>	is the test pattern to use.
<i>startAddress</i>	is the starting address (inclusive) of the CAN message RAM range to test.
<i>endAddress</i>	is the end address (inclusive) of the CAN message RAM range to test.
<i>copyAddress</i>	is the address to copy the original contents of the memory under test. It will be used to restore the original memory at the end of the March13N memory test. If no save and restore is required, use a value of <b>STL_CAN_RAM_NO_COPY</b> .

This function performs a March13N memory test on the range of CAN message RAM objects specified by **canBase**, **startAddress** and **endAddress**. The test can save and restore the original contents of the message RAM by passing an address to a back up buffer through the **copyAddress** parameter. The test will copy the original contents of the memory to **copyAddress**, perform the memory test, and then copy the original contents back to the memory under test. To skip the save and restore, use a value of **STL\_CAN\_RAM\_NO\_COPY** for the **copyAddress** and a destructive test will be performed instead.

The test patterns and the March13N memory test algorithm provided test the memory for stuck-at-faults. The parity bits will show if any were detected. Use [STL\\_CAN\\_RAM\\_checkErrorStatus\(\)](#) to read the parity status.

#### Note

Note to take care calculating the size of memory needed for **copyAddress**. The March13N function is not specific to the CAN message RAM and does not take the byte addressability of the memory into account. Use a buffer twice the size of the actual message RAM region you are testing.

The STL\_March functions called by this test disable global CPU interrupts (DINT) and then re-enable them after the test has completed.

#### Returns

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

4.1.3.2 void STL\_CAN\_RAM\_injectError ( const uint32\_t *canBase*, const uint32\_t *address*, const uint32\_t *xorMask* )

Injects an error into a CAN message RAM address.

**Parameters**

<i>canBase</i>	is the base address of the CAN controller.
<i>address</i>	is the address of the word in the message RAM where the error will be injected.
<i>xorMask</i>	mask of the bit to flip in <b>address</b> .

This function injects an error at a specific memory **address**. **xorMask** specifies which bit to flip in order to corrupt the data or parity bits.

**Returns**

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

#### 4.1.3.3 uint16\_t STL\_CAN\_RAM\_checkErrorStatus ( const uint32\_t *canBase* )

Returns the status of the CAN message RAM parity error detected bit.

**Parameters**

<i>canBase</i>	is the base address of the CAN controller.
----------------	--

This function checks if any parity errors have been detected by the CAN message RAM parity logic.

**Returns**

If the CAN error status register indicates a parity error the function returns **STL\_CAN\_RAM\_ERROR**. Otherwise, the function returns **STL\_CAN\_RAM\_PASS**.

**Note**

Several bits in the CAN error status register (CAN\_ES) are cleared on a CPU read of the register which this function performs. If the potential clearing of these bits (see device Technical Reference Manual for details) is undesired behavior for your application, use different means of reading the status.

Referenced by [STA\\_Tests\\_testDevice\(\)](#), and [STA\\_User\\_canParityErrorISR\(\)](#).

## 4.2 CPU Register API Functions

### Macros

- `#define STL_CPU_REG_PASS`
- `#define STL_CPU_REG_FAIL`

### Functions

- `uint16_t STL_CPU_REG_testCPURegisters (bool injectError)`
- `uint16_t STL_CPU_REG_testFPURegisters (bool injectError)`
- `uint16_t STL_CPU_REG_testVCURegisters (uint32_t *scratchRAM, bool injectError)`
- `static uint16_t STL_CPU_REG_checkCPURegisters (bool injectError)`
- `static uint16_t STL_CPU_REG_checkFPURegisters (bool injectError)`
- `static uint16_t STL_CPU_REG_checkVCURegisters (bool injectError)`

### 4.2.1 Detailed Description

The code for this module is contained in `source/stl_cpu_reg.c` and `source/stl_cpu_reg.s.asm`, with `include/stl_cpu_reg.h` containing the API declarations for use by applications.

### Error Injection

The functions in this module all have an *injectError* parameter that when set to true, will overwrite an incorrect test pattern to a register instead of the expected pattern in order to generate a failure.

### 4.2.2 Function Documentation

4.2.2.1 `static uint16_t STL_CPU_REG_checkCPURegisters ( bool injectError )`  
`[inline], [static]`

Tests CPU registers.

#### Parameters

<i>injectError</i>	when <i>false</i> the test writes the test pattern to the registers as expected. When <i>true</i> , the test will write an unexpected error pattern to ACC to simulate a stuck bit, causing the test to fail.
--------------------	---

This function tests CPU core registers for stuck bits. The following registers are tested:

- ACC
- P
- XAR0 to XAR7
- XT

- SP
- IFR, IER and DBGIER
- ST0
- ST1 (excluding IDLESTAT and LOOP bits)
- DP

The values of ST0, ST1, DP, IER, IFR, and DBGIER and the save-on-entry XAR registers, as defined by the compiler calling convention, are saved and restored in this test.

Note that the IDLESTAT and LOOP bits of ST1 are not tested by this function as they are read-only. IDLESTAT is set when the IDLE instruction is used to enter a low-power mode. Performing a functional test of the low-power mode will indirectly serve as a test of IDLESTAT.

The LOOP bit is set by the LOOPZ and LOOPNZ instructions. The C2000 compiler will not generate code that uses these instructions. If an application contains hand-coded assembly that uses them, the LOOP bit may also be tested by performing a functional test of the applicable LOOP instruction.

#### Note

You should disable interrupts before calling this test.

#### Returns

If the test passes, the routine returns **STL\_CPU\_REG\_PASS**. Otherwise, it returns **STL\_CPU\_REG\_FAIL**.

References [STL\\_UTIL\\_CPU\\_REG](#), and [STL\\_Util\\_setErrorFlag\(\)](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

4.2.2.2 `static uint16_t STL_CPU_REG_checkFPURegisters ( bool injectError )`  
`[inline], [static]`

Tests FPU registers.

#### Parameters

<i>injectError</i>	when <i>false</i> the test writes the test pattern to the registers as expected. When <i>true</i> , the test will write an unexpected error pattern to R5H to simulate a stuck bit, causing the test to fail.
--------------------	---

This function tests FPU registers for stuck bits. The following registers are tested:

- R0H to R7H
- RND32, TF, ZI, NI, ZF, NF bits of STF register.
- Shadow registers for R0H to R7H and STF

The values of STF and the save-on-entry RnH registers, as defined by the compiler calling convention, are saved and restored in this test.

#### Note

You should disable interrupts before calling this test.

**Returns**

If the test passes, the routine returns **STL\_CPU\_REG\_PASS**. Otherwise, it returns **STL\_CPU\_REG\_FAIL**.

References [STL\\_UTIL\\_FPU\\_REG](#), and [STL\\_Util\\_setErrorFlag\(\)](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

4.2.2.3 `static uint16_t STL_CPU_REG_checkVCURegisters ( bool injectError )`  
`[inline], [static]`

Tests VCU registers.

**Parameters**

<i>injectError</i>	when <i>false</i> the test writes the test pattern to the registers as expected. When <i>true</i> , the test will write an unexpected error pattern to VR4 to simulate a stuck bit, causing the test to fail.
--------------------	---

This function tests VCU (Viterbi, Complex Math and CRC Unit) registers for stuck bits. The following registers are tested:

- VR0 to VR8
- VT0 and VT1
- VCRC
- VSTATUS

The value of VSTATUS saved and restored in this test.

**Note**

You should disable interrupts before calling this test.

**Returns**

If the test passes, the routine returns **STL\_CPU\_REG\_PASS**. Otherwise, it returns **STL\_CPU\_REG\_FAIL**.

References [STL\\_Util\\_setErrorFlag\(\)](#), and [STL\\_UTIL\\_VCU\\_REG](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).



## 4.3 CRC API Functions

### Data Structures

- struct [STL\\_CRC\\_Obj](#)

### Macros

- #define [STL\\_CRC\\_INIT\\_CRC](#)
- #define [STL\\_CRC\\_PASS](#)
- #define [STL\\_CRC\\_FAIL](#)

### Typedefs

- typedef [STL\\_CRC\\_Obj](#) \* [STL\\_CRC\\_Handle](#)

### Enumerations

- enum [STL\\_CRC\\_Parity](#) { [STL\\_CRC\\_PARITY\\_EVEN](#), [STL\\_CRC\\_PARITY\\_ODD](#) }

### Functions

- void [STL\\_CRC\\_reset](#) (void)
- void [STL\\_CRC\\_calculate](#) (const [STL\\_CRC\\_Handle](#) crcHandle)
- void [STL\\_CRC\\_calculateLowBytes](#) (const [STL\\_CRC\\_Handle](#) crcHandle)
- uint16\_t [STL\\_CRC\\_checkCRC](#) (const uint32\_t startAddress, const uint32\_t endAddress, const uint32\_t goldenCRC)

### 4.3.1 Detailed Description

The code for this module is contained in `source/stl_crc.c` and `source/stl_crc_s.asm` (F2837x only), with `include/stl_crc.h` containing the API declarations for use by applications.

### 4.3.2 Data Structure Documentation

#### 4.3.2.1 struct STL\_CRC\_Obj

CRC structure.

**Data Fields**

---

uint32_t	seedValue	Initial value of the CRC calculation.
uint16_t	numBytes	Number of bytes in the message buffer.
<a href="#">STL_CRC_Parity</a>	parity	Start the CRC from the low byte or high byte
uint32_t	crcResult	The calculated CRC.
void *	msgBuffer	Pointer to the message buffer.

### 4.3.3 Enumeration Type Documentation

#### 4.3.3.1 enum **STL\_CRC\_Parity**

Parity enumeration.

The parity is used by the CRC algorithm to determine whether to begin calculations from the low byte (EVEN) or from the high byte (ODD) of the first word (16-bit) in the message.

For example, if your message had 10 bytes and started at the address 0x8000 but the first byte was at the high byte position of the first 16-bit word, the user would call the CRC function with odd parity i.e. **STL\_CRC\_PARITY\_ODD**

Address: HI LO

0x8000 : B0 XX

0x8001 : B2 B1

0x8002 : B4 B3

0x8003 : B6 B5

0x8004 : B8 B7

0x8005 : XX B9

However, if the first byte was at the low byte position of the first 16-bit word, the user would call the CRC function with even parity i.e. **STL\_CRC\_PARITY\_EVEN**

Address: HI LO

0x8000 : B1 B0

0x8001 : B3 B2

0x8002 : B5 B4

0x8003 : B7 B6

0x8004 : B9 B8

#### Enumerator

**STL\_CRC\_PARITY\_EVEN** Even parity, CRC starts at the low byte of the first word (16-bit)

**STL\_CRC\_PARITY\_ODD** Odd parity, CRC starts at the high byte of the first word (16-bit)

### 4.3.4 Function Documentation

#### 4.3.4.1 void **STL\_CRC\_reset** ( void )

Workaround to the silicon issue of first VCU calculation on power up being erroneous.

Due to the internal power-up state of the VCU module, it is possible that the first CRC result will be incorrect. This condition applies to the first result from each of the eight CRC instructions. This rare condition can only occur after a power-on reset, but will not necessarily occur on every power on. A warm reset will not cause this condition to reappear.

Workaround(s): The application can reset the internal VCU CRC logic by performing a CRC calculation of a single byte in the initialization routine. This routine only needs to perform one CRC calculation and can use any of the CRC instructions.

#### Returns

None.

#### 4.3.4.2 void STL\_CRC\_calculate ( const **STL\_CRC\_Handle** *crcHandle* )

Runs the 32-bit CRC routine using polynomial 0x04c11db7.

##### Parameters

<i>crcHandle</i>	handle to the CRC object
------------------	--------------------------

Calculates the 32-bit CRC using polynomial 0x04c11db7 on the VCU or VCRC. Depending on the parity chosen the CRC begins at either the low byte (STL\_CRC\_PARITY\_EVEN) or the high byte (STL\_CRC\_PARITY\_ODD) of the first word (16-bit).

#### Note

The size of the message (bytes) is limited to 65535 bytes.

#### Returns

None.

#### 4.3.4.3 void STL\_CRC\_calculateLowBytes ( const **STL\_CRC\_Handle** *crcHandle* )

Runs the 32-bit CRC routine using polynomial 0x04c11db7.

##### Parameters

<i>crcHandle</i>	handle to the CRC object
------------------	--------------------------

Calculates the 32-bit CRC using polynomial 0x04c11db7 on the VCU or VCRC. This algorithm performs a CRC32 only on the low bytes (LSB) of each 16-bit word. The input **parity** has no effect. This function works on unpacked data.

#### Note

The size of the message (bytes) is limited to 65535 bytes.

#### Returns

None.

#### 4.3.4.4 uint16\_t STL\_CRC\_checkCRC ( const uint32\_t *startAddress*, const uint32\_t *endAddress*, const uint32\_t *goldenCRC* )

Calculates a CRC-32 value for specific memory range and compares it with the goldenCRC value.

**Parameters**

<i>startAddress</i>	- start address of CRC calculation.
<i>endAddress</i>	- end address of CRC calculation, inclusive.
<i>goldenCRC</i>	- golden CRC value.

This function performs a test of the memory range by calculating the CRC-32 value for the input memory range and comparing it with the golden CRC value.

**Note**

This function could be used with many memory types including Flash and Boot ROM.

**Returns**

If the calculated CRC matches the golden CRC, then the function returns **STL\_CRC\_PASS**.  
Otherwise, it returns **STL\_CRC\_FAIL**.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 4.4 March13N Test API Functions

### Data Structures

- struct [STL\\_March\\_InjectErrorObj](#)

### Macros

- #define [STL\\_MARCH\\_PASS](#)
- #define [STL\\_MARCH\\_CORR\\_ERROR](#)
- #define [STL\\_MARCH\\_UNC\\_ERROR](#)
- #define [STL\\_MARCH\\_BOTH\\_ERROR](#)

### Typedefs

- typedef [STL\\_March\\_InjectErrorObj](#) \* [STL\\_March\\_InjectErrorHandle](#)

### Enumerations

- enum [STL\\_March\\_Pattern](#) { [STL\\_MARCH\\_PATTERN\\_ONE](#), [STL\\_MARCH\\_PATTERN\\_TWO](#), [STL\\_MARCH\\_PATTERN\\_THREE](#), [STL\\_MARCH\\_PATTERN\\_FOUR](#) }

### Functions

- void [STL\\_March\\_testRAMCopy](#) (const [STL\\_March\\_Pattern](#) pattern, const uint32\_t startAddress, const uint32\_t length, const uint32\_t copyAddress)
- void [STL\\_March\\_testRAM](#) (const [STL\\_March\\_Pattern](#) pattern, const uint32\_t startAddress, const uint32\_t length)
- void [STL\\_March\\_injectError](#) (const [STL\\_March\\_InjectErrorHandle](#) errorHandle)
- uint16\_t [STL\\_March\\_checkErrorStatus](#) (void)

#### 4.4.1 Detailed Description

The code for this module is contained in `source/stl_march.c` and `source/stl_march_s.asm`, with `include/stl_march.h` containing the API declarations for use by applications.

### Error Injection

Here are techniques to inject error:

[STL\\_March\\_testRAM\(\)](#), [STL\\_March\\_testRAMCopy\(\)](#)

- Call [STL\\_March\\_injectError\(\)](#) with testMode and xorMask values that cause errors.

## 4.4.2 Data Structure Documentation

### 4.4.2.1 struct STL\_March\_InjectErrorObj

Defines the March memory test inject error object.

## Data Fields

uint32_t	address	Address (32-bit aligned)
uint32_t	ramSection	RAM section identifier.
uint32_t	xorMask	Mask to flip bits in test mode.
MemCfg_TestMode	testMode	Mode in which to inject error.

### 4.4.3 Typedef Documentation

#### 4.4.3.1 typedef **STL\_March\_InjectErrorObj\*** **STL\_March\_InjectErrorHandle**

Defines the RAM error logic test handle

### 4.4.4 Enumeration Type Documentation

#### 4.4.4.1 enum **STL\_March\_Pattern**

Values that must be used to pass to determine the test pattern for [STL\\_March\\_testRAMCopy\(\)](#) and [STL\\_March\\_testRAM\(\)](#)

##### Enumerator

**STL\_MARCH\_PATTERN\_ONE** Test Pattern One.

**STL\_MARCH\_PATTERN\_TWO** Test Pattern Two.

**STL\_MARCH\_PATTERN\_THREE** Test Pattern Three.

**STL\_MARCH\_PATTERN\_FOUR** Test Pattern Four.

### 4.4.5 Function Documentation

#### 4.4.5.1 void STL\_March\_testRAMCopy ( const **STL\_March\_Pattern** *pattern*, const uint32\_t *startAddress*, const uint32\_t *length*, const uint32\_t *copyAddress* )

Performs a March13N non-destructive memory test on the specified RAM memory.

##### Parameters

<i>pattern</i>	is the test pattern to use.
<i>startAddress</i>	is the address to start the memory test.
<i>length</i>	is the number of 32-bit words of the memory test minus 1.
<i>copyAddress</i>	is the address to copy the original contents of the memory under test. It will be used to restore the original memory at the end of the March13N memory test.

This function performs a March13N memory test on RAM specified by **startAddress** and **length**. This function performs a non-destructive memory test. This means that it will begin by copying the original contents of the memory to **copyAddress**, perform the memory test, and then copy the original contents back to the memory under test. The test patterns along with the March13N memory test algorithm provided, test memory for stuck-at-faults as well as boundary cases including worst case timings tailored for the C2000 RAM bank architecture.

This test is implemented to be able to perform a memory test on any section of RAM including the stack.

#### Note

If this code is running from RAM, be careful not to perform this memory test on itself, meaning do not perform the March13N memory test on the March13N program code in RAM. This will likely lead to an ITRAP. In order to test the program code for this March13N algorithm, the user can create a copy of this function in RAM or flash and run the memory test code from the copy.

This function disables global CPU interrupts (DINT) and then re-enables them after the test has completed.

**length** is the number of 32-bits words to test minus 1. For example, in order to test 8 32-bit words, length is 7.

#### Returns

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

4.4.5.2 void STL\_March\_testRAM ( const **STL\_March\_Pattern** *pattern*, const uint32\_t *startAddress*, const uint32\_t *length* )

Performs a March13N destructive memory test on the specified RAM memory.

#### Parameters

<i>pattern</i>	is the test pattern to use.
<i>startAddress</i>	is the address to start the memory test.
<i>length</i>	is the number of 32-bit words of the memory test minus 1.

This function performs a March13N memory test on RAM specified by **startAddress** and **length**. This test performs a destructive memory test, meaning the original contents will be lost by this test. The test patterns along with the March13N memory test algorithm provided, test memory for stuck-at-faults as well as boundary cases including worst case timings tailored for the C2000 RAM bank architecture.

#### Note

If this code is running from RAM, be careful not to perform this memory test on itself, meaning do not perform the March13N memory test on the March13N program code in RAM. This will likely lead to an ITRAP. In order to test the program code for this March13N algorithm, the user can create a copy of this function in RAM or flash and run the memory test code from the copy.

This function disables global CPU interrupts (DINT) and then re-enables them after the test has completed.

**length** is the number of 32-bits words to test minus 1. For example, in order to test 8 32-bit words, length is 7.

#### Returns

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).



```
4.4.5.3 void STL_March_injectError ( const STL_March_InjectErrorHandle errorHandle
)
```

Injects an error into a RAM memory address.

**Parameters**

<i>errorHandle</i>	the inject error handle specifying where and what type of error to inject into RAM.
--------------------	---

This function injects an error at a specific memory **address** in a specific **ramSection**. **testMode** specifies whether the error will be injected in the data or ECC/parity bits. **xorMask** specifies which bit or bits to flip in order to corrupt either the data or ECC/parity bits.

**Returns**

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

#### 4.4.5.4 uint16\_t STL\_March\_checkErrorStatus ( void )

Returns the status of the Memory Error Registers for RAM.

This function checks if there are any correctable or uncorrectable errors indicated by the Memory Error Registers and returns the status.

**Returns**

If the Memory Error Registers indicate a correctable error and/or an uncorrectable error in RAM, then the function returns **STL\_MARCH\_CORR\_ERROR**, **STL\_MARCH\_UNC\_ERROR**, or **STL\_MARCH\_BOTH\_ERROR**. Otherwise, the function returns **STL\_MARCH\_PASS**.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 4.5 Oscillator CPU Timer API Functions

### Data Structures

- struct [STL\\_OSC\\_CT\\_Obj](#)

### Macros

- #define **STL\_OSC\_CT\_FAIL**
- #define **STL\_OSC\_CT\_PASS**
- #define **STL\_OSC\_CT\_PERIOD**

### Typedefs

- typedef [STL\\_OSC\\_CT\\_Obj](#) \* [STL\\_OSC\\_CT\\_Handle](#)

### Functions

- void [STL\\_OSC\\_CT\\_startTest](#) (const [STL\\_OSC\\_CT\\_Handle](#) oscTimer2Handle)
- uint16\_t [STL\\_OSC\\_CT\\_stopTest](#) (const [STL\\_OSC\\_CT\\_Handle](#) oscTimer2Handle)

### 4.5.1 Detailed Description

The code for this module is contained in `source/stl_osc_ct.c`, with `include/stl_osc_ct.h` containing the API declarations for use by applications.

### Error Injection

Here are techniques to inject error:

**STL\_OSC\_CT\_startTest** and [STL\\_OSC\\_CT\\_stopTest\(\)](#)

- Set maxCount and minCount to values so that the Timer 2 counter will be out of range.
- Set the prescaler so that the Timer 2 counter will not be in the minCount/maxCount range.

### 4.5.2 Data Structure Documentation

#### 4.5.2.1 struct STL\_OSC\_CT\_Obj

Defines the OSC Timer 2 test object.

## Data Fields

uint32_t	minCount	Lower bound count.
uint32_t	maxCount	Upper bound count.
CPUTimer_ClockSource	clockSource	Clock source for Timer2.
CPUTimer_Prescaler	prescaler	Prescaler for selected clock source.

## 4.5.3 Function Documentation

### 4.5.3.1 void STL\_OSC\_CT\_startTest ( const **STL\_OSC\_CT\_Handle** *oscTimer2Handle* )

Starts CPU Timer 2 to test the oscillator source.

#### Parameters

<i>oscTimer2Handle</i>	is a pointer to the Oscillator Timer 2 object.
------------------------	--

This function disables CPU Timer 2 interrupts, configures the CPU Timer 2 to use the specified clock source and prescaler, starts the timer, and then returns.

The user should configure the PLL and CPU Timer with independent clock sources.

The user must preserve and restore the registers modified by this function. The following CPU Timer 2 and System Control registers are modified by the function.

- TCR
- PRD
- TPRH
- TPR
- TMR2CLKCTL

#### Note

When **CPUTIMER\_CLOCK\_SOURCE\_SYS** is selected as the **clockSource**, the **prescaler** is bypassed.

#### Returns

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

### 4.5.3.2 uint16\_t STL\_OSC\_CT\_stopTest ( const **STL\_OSC\_CT\_Handle** *oscTimer2Handle* )

Stops CPU Timer 2 and checks the elapsed time.

#### Parameters

<code>oscTimer2Handle</code>	is a pointer to the Oscillator Timer 2 object.
------------------------------	--

This function stops CPU Timer 2 and then compares the number of ticks that have elapsed with the min and max boundaries. This function is intended to be used in combination with [STL\\_OSC\\_CT\\_startTest\(\)](#) to perform a periodic test of the oscillator source.

**Returns**

If the elapsed number of ticks is not within the min and max boundaries, the function returns **STL\_OSC\_CT\_FAIL**. Otherwise, it returns **STL\_OSC\_CT\_PASS**.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 4.6 Oscillator HRPWM API Functions

### Data Structures

- struct [STL\\_OSC\\_HR\\_Obj](#)

### Macros

- #define **STL\_OSC\_HR\_PASS**
- #define **STL\_OSC\_HR\_FAIL**
- #define **STL\_OSC\_HR\_SFO\_INCOMPLETE**
- #define **STL\_OSC\_HR\_SFO\_COMPLETE**
- #define **STL\_OSC\_HR\_SFO\_ERROR**

### Typedefs

- typedef [STL\\_OSC\\_HR\\_Obj](#) \* [STL\\_OSC\\_HR\\_Handle](#)

### Functions

- uint16\_t [STL\\_OSC\\_HR\\_testSFO](#) (const [STL\\_OSC\\_HR\\_Handle](#) oscHRHandle)

### 4.6.1 Detailed Description

The code for this module is contained in `source/stl_osc_hr.c`, with `include/stl_osc_hr.h` containing the API declarations for use by applications.

### Error Injection

Here are techniques to inject error:

#### [STL\\_OSC\\_HR\\_testSFO\(\)](#)

- Set mepMax and mepMin the same value so that the MEP scale factor calculated by SFO calibration will be out of range.
- Disable HRPWM clock by clearing HRPWM bit in the PCLKCR0 register.
- Set sfoDelay to 0 to cause timeout.

### 4.6.2 Data Structure Documentation

#### 4.6.2.1 struct STL\_OSC\_HR\_Obj

Defines the OSC HR test object.

## Data Fields

uint32_t	ePWMBase	EPWM Base.
HRPWM_Channel	channel	HRPWM channel.
HRPWM_MEPEdgeMode	mepEdgeMode	Edge(s) controlled by MEP.
int16_t	mepMin	MEP lower bound.
int16_t	mepMax	MEP upper bound.
uint32_t	sfoDelay	SFO function delay.

### 4.6.3 Function Documentation

#### 4.6.3.1 uint16\_t STL\_OSC\_HR\_testSFO ( const **STL\_OSC\_HR\_Handle** *oscHRHandle* )

Tests the HRPWM SFO library's calibration process to ensure execution completion and verify value of MEP scale factor.

## Parameters

<i>oscHRHandle</i>	is a pointer to the OSC HR object.
--------------------	------------------------------------

This function runs calibration using the SFO Library Software to calculate an appropriate Micro Edge Positioner (MEP) scale factor for HRPWM-supported ePWM modules to verify this value.

The ePWM module used for the test is selected by *ePWMBase* member of the OSC HR test object. The valid range of inputs is from EPWM1\_BASE to EPWMx\_BASE where x is the value specified by PWM\_CH - 1. PWM\_CH is defined in the SFO library header file SFO\_V8.h. The channel member can be configured to select between channels A and B. The *mepEdgeMode* value is configured for the PWM edges to be controlled by MEP. The values *mepMin* and *mepMax* define the minimum and maximum bounds of the expected MEP scale factor range. The expected MEP scale factor for EPWMCLK of 100 MHz, given a step size of 150 ps, is about 66 MEP steps.  $(1/EPWMCLK)/\text{Step size} = (1/100 \text{ MHz})/150 \text{ ps}$  is about 66.

The *sfoDelay* value is the delay count required for the SFO() to finish calibration. The typical EPWM cycles required for SFO() to complete calibration if called repeatedly without interrupts is 130, 000 EPWMCLK cycles. Please refer to **Appendix A: SFO Library Software** of the Technical Reference Manual HRPWM chapter and the device datasheet for more details. The repetition rate at which SFO() needs to be executed depends on the application. If there is not a sufficiently large interval between SFO() calls, the SFO() will return and not advance to the next stage. The execution will only advance to the next stage if the previous call's execution has completed and SFO() is called again. This interval can be experimentally calculated for a particular application.

## Note

The SFO library binary is provided in the C2000Ware calibration libraries. The source code however is not publicly released. It may be made available in some cases upon request through an FAE.

## Returns

If the MEP scale factor calculated by the calibration falls within the MEP min and max values, the function returns **STL\_OSC\_HR\_PASS**. If the calibration fails to complete in the specified delay, if SFO() returns an error status, or if the calculated MEP scale factor is outside the range, this function returns **STL\_OSC\_HR\_FAIL**.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 4.7 PIE RAM API Functions

### Macros

- #define **STL\_PIE\_RAM\_PASS**
- #define **STL\_PIE\_RAM\_FAIL\_HANDLER**
- #define **STL\_PIE\_RAM\_MIN\_INDEX**
- #define **STL\_PIE\_RAM\_MAX\_INDEX**
- #define **STL\_PIE\_RAM\_REDUNDANT\_PIE\_ADDRESS**
- #define **STL\_PIE\_RAM\_TABLE\_ROW\_M**
- #define **STL\_PIE\_RAM\_TABLE\_COL\_M**
- #define **STL\_PIE\_RAM\_TABLE\_COL\_S**
- #define **STL\_PIE\_RAM\_VECT\_ID\_M**
- #define **STL\_PIE\_RAM\_VECT\_ID\_S**

### Functions

- void [STL\\_PIE\\_RAM\\_handler](#) (void)
- void [STL\\_PIE\\_RAM\\_configHandler](#) (const void \*handlerPtr)
- void [STL\\_PIE\\_RAM\\_injectFault](#) (uint16\_t entry)
- void [STL\\_PIE\\_RAM\\_restoreVector](#) (uint16\_t entry)
- void [STL\\_PIE\\_RAM\\_restoreTable](#) (const uint32\_t \*pieTableSourcePtr)
- uint16\_t [STL\\_PIE\\_RAM\\_testRAM](#) (void)
- uint16\_t [STL\\_PIE\\_RAM\\_testHandler](#) (uint32\_t interruptNumber)

### 4.7.1 Detailed Description

The code for this module is contained in `source/stl_pie_ram.c`, with `include/stl_pie_ram.h` containing the API declarations for use by applications.

### Error Injection

Here are techniques to inject error:

#### [STL\\_PIE\\_RAM\\_testRAM\(\)](#)

- Call [STL\\_PIE\\_RAM\\_injectFault\(\)](#) to bit-flip an entry of the redundant PIE RAM vector table.
- [STL\\_PIE\\_RAM\\_testHandler\(\)](#)
- Disable global interrupts with DINT macro.

### 4.7.2 Function Documentation

#### 4.7.2.1 void [STL\\_PIE\\_RAM\\_handler](#) ( void )

PIE RAM mismatch error handler used by [STL\\_PIE\\_RAM\\_testHandler\(\)](#).

This function sets a static global flag for [STL\\_PIE\\_RAM\\_testHandler\(\)](#) and also sets the global error flag for the STL library.



**Returns**

None.

4.7.2.2 void STL\_PIE\_RAM\_configHandler ( const void \* *handlerPtr* )

Configures a vector mismatch handler.

**Parameters**

<i>handlerPtr</i>	is a pointer or address of the PIE RAM vector mismatch error exception handler.
-------------------	---

This function configures a PIE RAM mismatch error handler for the users application. On a vector fetch mismatch, an exception will be taken and the error handler will be executed.

**Returns**

None.

4.7.2.3 void STL\_PIE\_RAM\_injectFault ( uint16\_t *entry* )

Injects a fault by bit-flipping an entry in the redundant PIE RAM vector table.

**Parameters**

<i>entry</i>	is an index of the PIE RAM and should be a multiple of 2 for 32-bit alignment.
--------------	--

This function bit-flips an entry of the redundant PIE RAM vector table in order to inject a fault. The **entry** parameter must be within the boundaries **STL\_PIE\_RAM\_MIN\_INDEX** and **STL\_PIE\_RAM\_MAX\_INDEX**.

Data writes to the redundant PIE vector table write only to the redundant table. This is how a fault may be injected. For more details see the device's Technical Reference Manual chapter on "Vector Address Validity Check."

**Returns**

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).4.7.2.4 void STL\_PIE\_RAM\_restoreVector ( uint16\_t *entry* )

Restores a PIE RAM redundant vector entry from the PIE RAM vector table.

**Parameters**

<i>entry</i>	is an index of the PIE RAM and should be a multiple of 2 for 32-bit alignment.
--------------	--

This function restores the PIE RAM vector entry and consequently the redundant PIE RAM vector table.

**Note**

This function can be used to restore the fault injected by [STL\\_PIE\\_RAM\\_injectFault\(\)](#).

**Returns**

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).**4.7.2.5 void STL\_PIE\_RAM\_restoreTable ( const uint32\_t \* *pieTableSourcePtr* )**

Restores the PIE RAM from the initialization source.

**Parameters**

<i>pieTableSourcePtr</i>	is a pointer to the source of the PIE vector table in the user's application.
--------------------------	---

This function restores the PIE RAM vector table and consequently the redundant PIE RAM vector table.

**Note**

This function restores the entire PIE RAM table and not just a single vector entry.

**Returns**

None.

**4.7.2.6 uint16\_t STL\_PIE\_RAM\_testRAM ( void )**

Tests PIE RAM integrity.

This function checks the integrity of PIE RAM vector by comparing the entries in the main PIE vector with the redundant PIE vector located at a higher memory address location. There is a redundant PIE RAM vector table starting at 0X1000D00 which is used for data integrity of the PIE. Data writes to the PIE vector table also write to the redundant PIE vector table. For more details see the device's Technical Reference Manual chapter on "PIE Vector Address Validity Check."

**Note**

The user may call [STL\\_PIE\\_RAM\\_configHandler\(\)](#) in order to register an error handler for PIE RAM mismatch.

A failure of this test will not trigger the PIE RAM mismatch handler. Only when a vector is fetched in the PIE and there is a mismatch will the handler be serviced.

**Returns**

If the test passes, it returns **STL\_PIE\_RAM\_TEST\_PASS**. If the test fails, it returns the address in the PIE vector table of the last failure.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).**4.7.2.7 uint16\_t STL\_PIE\_RAM\_testHandler ( uint32\_t *interruptNumber* )**

Tests PIE RAM integrity.

**Parameters**

<i>interruptNumber</i>	is the 32-bit interrupt value used in the interrupt driver found in hw_ints.h.
------------------------	--

This function checks the functionality of the PIE RAM mismatch error handler. It will inject an error for the input interrupt, enable the interrupt, and force the interrupt. It will then check to see that the error handler was serviced properly. Afterward, it will restore the PIE RAM and and restore the original error handler. It will also acknowledge the PIE so that further interrupts from that group can be serviced.

**Note**

This test only covers PIE interrupts. This test does not cover CPU interrupts.

**Returns**

If the test passes, it returns **STL\_PIE\_RAM\_PASS**. If the test fails, and the error handler was not serviced, then it returns **STL\_PIE\_RAM\_FAIL\_HANDLER**.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 4.8 Utilities API Functions

### Macros

- #define **STL\_UTIL\_CPU\_RATE**

### Enumerations

- enum **STL\_Util\_ErrorFlag** {  
[STL\\_UTIL\\_CRC](#), [STL\\_UTIL\\_CPU\\_REG](#), [STL\\_UTIL\\_FPU\\_REG](#), [STL\\_UTIL\\_VCU\\_REG](#),  
[STL\\_UTIL\\_PIE\\_RAM\\_MISMATCH](#), [STL\\_UTIL\\_PIE\\_RAM\\_INT](#), [STL\\_UTIL\\_OSC\\_TIMER2](#),  
[STL\\_UTIL\\_OSC\\_HR\\_MEP\\_RANGE](#),  
[STL\\_UTIL\\_OSC\\_HR\\_SFO](#), [STL\\_UTIL\\_OSC\\_HR\\_DELAY](#), [STL\\_UTIL\\_MARCH](#),  
[STL\\_UTIL\\_CAN\\_RAM\\_PARITY](#) }

### Functions

- static void [STL\\_Util\\_delayUS](#) (uint32\_t microseconds)
- void [STL\\_Util\\_setErrorFlag](#) (const [STL\\_Util\\_ErrorFlag](#) errorFlag)
- uint32\_t [STL\\_Util\\_getErrorFlag](#) (void)
- void [STL\\_Util\\_clearErrorFlag](#) (const [STL\\_Util\\_ErrorFlag](#) errorFlag)

### 4.8.1 Detailed Description

The code for this module is contained in `source/stl_util.c` and `source/stl_util_s.asm`, with `include/stl_util.h` containing the API declarations for use by applications.

### 4.8.2 Enumeration Type Documentation

#### 4.8.2.1 enum **STL\_Util\_ErrorFlag**

Values to be passed to [STL\\_Util\\_setErrorFlag\(\)](#) and [STL\\_Util\\_clearErrorFlag\(\)](#). These correspond to different errors in the STL.

##### Enumerator

- STL\_UTIL\_CRC** CRC check.
- STL\_UTIL\_CPU\_REG** CPU register test.
- STL\_UTIL\_FPU\_REG** FPU register test.
- STL\_UTIL\_VCU\_REG** VCU register test.
- STL\_UTIL\_PIE\_RAM\_MISMATCH** PIE RAM.
- STL\_UTIL\_PIE\_RAM\_INT** PIE RAM handler failed to execute.
- STL\_UTIL\_OSC\_TIMER2** OSC timer 2.
- STL\_UTIL\_OSC\_HR\_MEP\_RANGE** MEP out of range.
- STL\_UTIL\_OSC\_HR\_SFO** SFO calibration error.
- STL\_UTIL\_OSC\_HR\_DELAY** SFO delay error.

**STL\_UTIL\_MARCH** March RAM test.

**STL\_UTIL\_CAN\_RAM\_PARITY** March test for CAN message RAM.

## 4.8.3 Function Documentation

### 4.8.3.1 static void STL\_Util\_delayUS ( uint32\_t *microseconds* ) [inline], [static]

Delay for a specified number of microseconds

#### Parameters

<i>microseconds</i>	is the number of microseconds to delay.
---------------------	---

This function calls SysCtl\_delay() to achieve a delay in microseconds. The function will convert the desired delay in microseconds to the count value expected by the function. *microseconds* is the number of microseconds to delay.

#### Note

If this function does not get inlined (for instance, if the optimizer is turned off) the delay will be made less accurate by the overhead of the additional function call.

#### Returns

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

### 4.8.3.2 void STL\_Util\_setErrorFlag ( const **STL\_Util\_ErrorFlag** *errorFlag* )

Sets a global error flag.

#### Parameters

<i>errorFlag</i>	is a STL_Util_ErrorFlag that will be set in globalErrorFlags.
------------------	---

This function sets an error flag in the global globalErrorFlags.

#### Returns

None.

Referenced by [STL\\_CPU\\_REG\\_checkCPURegisters\(\)](#), [STL\\_CPU\\_REG\\_checkFPURegisters\(\)](#), and [STL\\_CPU\\_REG\\_checkVCURegisters\(\)](#).

### 4.8.3.3 uint32\_t STL\_Util\_getErrorFlag ( void )

Gets the error flag status of globalErrorFlags.

This function returns the global globalErrorFlags.

#### Returns

Returns the global globalErrorFlags.

4.8.3.4    `void STL_Util_clearErrorFlag ( const STL_Util_ErrorFlag errorFlag )`

Clears a flag of globalErrorFlags.

**Parameters**

<i>errorFlag</i>	is a STL_Util_ErrorFlag that will be cleared in globalErrorFlags.
------------------	---

This function clears a flag of globalErrorFlags.

**Returns**

None.

## 5 Self-Test Application

This section will describe the Self-Test Application (or STA) example project delivered with the diagnostic library. The STA is an example which provides a demonstration of the SDL modules and diagnostic functions.

The STA is designed to act as an example application which configures the system and calls the SDL APIs to perform the safety diagnostic tests made available in the diagnostic library. The STA is not intended to limit the customer to any implementation of safety diagnostic functions. Instead, it is intended to aid integration of the SDL into the user's end application or system by providing a demonstration of how to use the library. It is the responsibility of the system integrator to meet any and all safety compliance standards in their end application.

The STA has been tested on the controlCARD and docking station.

Getting Started .....	39
Example Behavior .....	40
STA_Tests API Functions .....	41
STA_Timer API Functions .....	43
STA_Comm API Functions .....	45
STA_Util API Functions .....	46
STA_User API Functions .....	48

### 5.1 Getting Started

The Code Composer Studio project containing the STA can be imported into CCS by going to **Project -> Import CCS Projects...** and browsing to the search directory below.

```
"diagnostic\<device>\examples\test_application"
```

Right click on the newly imported project in the Project Explorer pane and select **Build Project**. This will build the default RAM configuration of the project. The project provides several other build configurations for different levels of optimization and running the application from Flash, but the RAM configuration is a good starting point for getting familiar with the STA.

Connect and power your controlCARD according to the controlCARD info sheet in directory

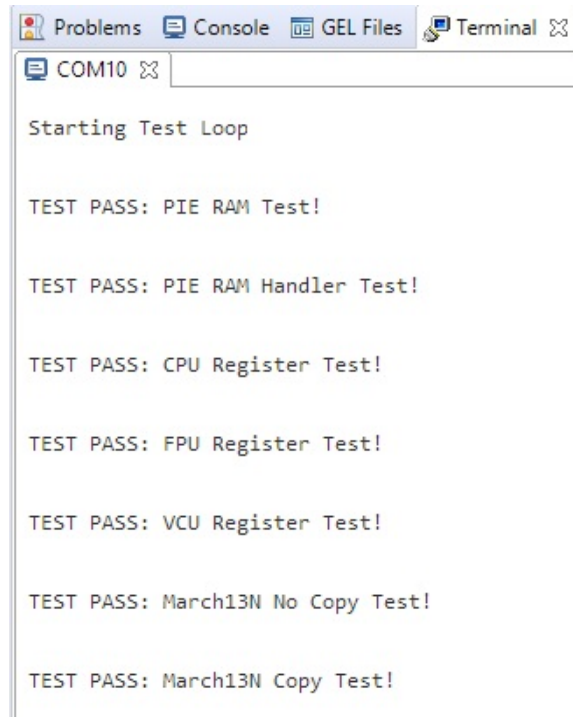
```
"<C2000Ware_install>\boards\controlCARDs\"
```

The STA uses the SCIA module to communicate test progress and results through the controlCARD's USB-to-UART adapter. Before running the application, set up a terminal session with 9600 baud rate, 8-N-1. Note that CCS contains a terminal window that can be accessed by going to **View -> Terminal**.

With the test application project selected in the Project Explorer, go to **Run -> Debug**. This will launch a debug session using the .ccxml to which the project is linked. By default, the XDS100v2 is used as this is the on-board debug probe for the controlCARD.

Run the application. In the terminal, you should see a looping message indicating test cases passing.



A screenshot of a terminal window within a development environment. The window has tabs for 'Problems', 'Console', 'GEL Files', and 'Terminal'. The 'Terminal' tab is active, showing output from a serial port named 'COM10'. The output text is as follows:

```
Starting Test Loop

TEST PASS: PIE RAM Test!

TEST PASS: PIE RAM Handler Test!

TEST PASS: CPU Register Test!

TEST PASS: FPU Register Test!

TEST PASS: VCU Register Test!

TEST PASS: March13N No Copy Test!

TEST PASS: March13N Copy Test!
```

Figure 5.1: Passing Terminal Output

## 5.2 Example Behavior

Most tests will display a PASS message in the terminal when they execute successfully with error injection disabled and display a FAIL message when they execute successfully when error injection is enabled. To toggle error injection, add the *enableErrorInject* variable to the CCS Expressions view. Setting its value to 1 will enable error injection. Setting it back to 0 will disable it.

The STA has built in profiling code for measuring cycle counts of the library functions as they are used by the STA. This functionality is turned on by default and uses CPU Timer 1 to capture time elapsed and records the result to an array called *STA\_Tests\_cycleCounts* which can be viewed in the CCS Expressions view.

The profiling can be turned off by changing the value of macro **STA\_UTIL\_PROFILE** to 0 and recompiling. More details about the functions used for profiling can be found in the following sections.

Note that it is not possible to inject an error for the all tests. In particular, the **STA\_MARCH** and **STA\_MARCH\_CAN** tests are expected to return PASS even when *enableErrorInject* is set. The core API used by these tests is [STL\\_March\\_testRAM\(\)](#). This function performs the March13n algorithm on the RAM memory addresses specified without a copy and restore of their original contents unlike **STA\_MARCH\_COPY** and **STA\_MARCH\_CAN\_COPY**. Since the first operation performed on the memory as part of the algorithm is a write which triggers a recalculation of the parity or ECC, any error injected prior to running the test will be overwritten before it can be detected.

## 5.3 STA\_Tests API Functions

### Macros

- #define **STA\_TESTS\_PASS**
- #define **STA\_TESTS\_FAIL**

### Enumerations

- enum **STA\_TestsTypes** {  
**STA\_TEST\_START**, **STA\_TEST\_PIE\_RAM**, **STA\_TEST\_PIE\_HANDLER**, **STA\_CPU\_REG**,  
**STA\_FPU\_REG**, **STA\_VCU\_REG**, **STA\_MARCH**, **STA\_MARCH\_COPY**,  
**STA\_MARCH\_CAN**, **STA\_MARCH\_CAN\_COPY**, **STA\_CAN\_RAM\_PARITY**,  
**STA\_FLASH\_CRC**,  
**STA\_OSC\_CT**, **STA\_OSC\_HR**, **STA\_TEST\_END**, **STA\_TESTS\_NUMBERS** }

### Functions

- unsigned char \* **STA\_Tests\_testDevice** (STA\_TestsTypes testItem)
- void **STA\_Tests\_injectErrorEnable** (void)
- void **STA\_Tests\_injectErrorDisable** (void)

### Variables

- const STA\_TestsTypes **STA\_Tests\_testArray** [STA\_TESTS\_NUMBERS]
- uint32\_t **STA\_Tests\_cycleCounts** [STA\_TESTS\_NUMBERS]

### 5.3.1 Detailed Description

This module contains the core test execution function for this application. It defines the list of test cases to be executed and their implementations.

The code for this module is contained in `sta_tests.c`, with `sta_tests.h` containing the API declarations.

### 5.3.2 Function Documentation

#### 5.3.2.1 unsigned char\* STA\_Tests\_testDevice ( STA\_TestsTypes testItem )

Executes the safety library tests as an example.

**Parameters**

<i>testItem</i>	is the enumerated type <code>STA_test_types</code> test to perform.
-----------------	---

This function configures the device for each specific test. If injected errors are enabled, then this function will inject an error for the test being performed. It will then execute each STL test and return a message of characters to be printed to the terminal via SCI.

**Returns**

Returns a pointer to a message string indicating a pass or fail status and the test name. This string will be printed out of SCIA to the user.

References `STL_March_InjectErrorObj::address`, `STL_OSC_CT_Obj::maxCount`, `STL_OSC_HR_Obj::mepMin`, `STL_OSC_CT_Obj::minCount`, `STA_User_canParityErrorISR()`, `STA_User_initMarch()`, `STA_User_initOSCHRTTest()`, `STA_User_initOSCTimer2Test()`, `STA_Util_startProfiler()`, `STA_Util_stopProfiler()`, `STL_CAN_RAM_checkErrorStatus()`, `STL_CAN_RAM_injectError()`, `STL_CAN_RAM_NO_COPY`, `STL_CAN_RAM_testRAM()`, `STL_CPU_REG_checkCPURegisters()`, `STL_CPU_REG_checkFPURegisters()`, `STL_CPU_REG_checkVCURegisters()`, `STL_CRC_checkCRC()`, `STL_March_checkErrorStatus()`, `STL_March_injectError()`, `STL_MARCH_PATTERN_FOUR`, `STL_MARCH_PATTERN_ONE`, `STL_MARCH_PATTERN_THREE`, `STL_MARCH_PATTERN_TWO`, `STL_March_testRAM()`, `STL_March_testRAMCopy()`, `STL_OSC_CT_startTest()`, `STL_OSC_CT_stopTest()`, `STL_OSC_HR_testSFO()`, `STL_PIE_RAM_injectFault()`, `STL_PIE_RAM_restoreVector()`, `STL_PIE_RAM_testHandler()`, `STL_PIE_RAM_testRAM()`, `STL_Util_delayUS()`, `STL_March_InjectErrorObj::testMode`, and `STL_March_InjectErrorObj::xorMask`.

### 5.3.2.2 void STA\_Tests\_injectErrorEnable ( void )

Enables errors to be injected into the tests.

This function sets the global variable **STA\_Tests\_injectError** to true.

**Returns**

None.

### 5.3.2.3 void STA\_Tests\_injectErrorDisable ( void )

Disables errors to be injected into the tests.

This function sets the global variable **STA\_Tests\_injectError** to false.

**Returns**

None.

## 5.4 STA\_Timer API Functions

### Functions

- \_\_interrupt void [STA\\_Timer\\_timer0Isr](#) (void)
- void [STA\\_Timer\\_config](#) (uint16\_t msTimeOut)
- bool [STA\\_Timer\\_isTimedOut](#) (void)
- void [STA\\_Timer\\_clearTimeOut](#) (void)
- void [STA\\_Timer\\_restart](#) (void)

### 5.4.1 Detailed Description

This module handles the initialization and handling of the CPU timer system used to time the execution of the tests run by this application.

The code for this module is contained in `sta_timer.c`, with `sta_timer.h` containing the API declarations.

### 5.4.2 Function Documentation

#### 5.4.2.1 \_\_interrupt void STA\_Timer\_timer0Isr ( void )

Timer 0 ISR.

Referenced by [STA\\_Timer\\_config\(\)](#).

#### 5.4.2.2 void STA\_Timer\_config ( uint16\_t *msTimeOut* )

Configures Timer 0 to tick so that the STA will continue to make progress.

##### Parameters

<i>msTimeOut</i>	is the number of milliseconds between each execution of a test found in <code>sta_tests.c</code> . Another test will execute every time this STA timer runs out.
------------------	--

##### Returns

None.

References [STA\\_Timer\\_timer0Isr\(\)](#).

#### 5.4.2.3 bool STA\_Timer\_isTimedOut ( void )

Checks if Timer 0 has timed-out.

##### Returns

Returns true if the timer has timed-out and false if it has not.

#### 5.4.2.4 void STA\_Timer\_clearTimeOut ( void )

Clears Timer 0 time-out flag.

**Returns**

None.

#### 5.4.2.5 void STA\_Timer\_restart ( void )

Restarts Timer 0.

**Returns**

None.

## 5.5 STA\_Comm API Functions

### Macros

- #define **STA\_COMM\_BAUD\_RATE**

### Functions

- void [STA\\_Comm\\_configSCIA](#) (void)
- void [STA\\_Comm\\_transmitData](#) (unsigned char \*msg)

### 5.5.1 Detailed Description

This module handles the configuration of the SCIA module for communication over the board USB-to-UART adapter. This path will allow the application to send test pass/fail status to a terminal program.

The code for this module is contained in `sta_comm.c`, with `sta_comm.h` containing the API declarations.

### 5.5.2 Function Documentation

#### 5.5.2.1 void STA\_Comm\_configSCIA ( void )

Configures SCIA for serial communication.

This function configures SCIA for communication to a serial communication terminal for 9600 baud rate, 8-N-1.

#### Returns

None.

#### 5.5.2.2 void STA\_Comm\_transmitData ( unsigned char \* msg )

Transmits data via SCIA.

#### Parameters

<i>msg</i>	is a \0 terminated array of characters
------------	--

This function transmits the **msg** via SCIA to a serial communication terminal.

#### Returns

None.

## 5.6 STA\_Util API Functions

### Macros

- #define [STA\\_UTIL\\_PROFILE](#)

### Functions

- void [STA\\_Util\\_configProfiler](#) (uint32\_t base)
- static void [STA\\_Util\\_startProfiler](#) (uint32\_t base)
- static uint32\_t [STA\\_Util\\_stopProfiler](#) (uint32\_t base)

### 5.6.1 Detailed Description

This module contains utility functions for this test application. This primarily includes the functions used to profile the cycle counts of the SDL functions.

The code for this module is contained in `sta_util.c`, with `sta_util.h` containing the API declarations.

### 5.6.2 Macro Definition Documentation

#### 5.6.2.1 #define STA\_UTIL\_PROFILE

Used to enable or disable CPUTimer cycle profiling of STA tests. A value of 0 will disable cycle profiling. A value of not 0 will enable cycle profiling.

### 5.6.3 Function Documentation

#### 5.6.3.1 void STA\_Util\_configProfiler ( uint32\_t *base* )

Configures the CPUTimer specified by the parameter **base** for profiling cycle counts.

##### Parameters

<i>base</i>	is the base address of a valid CPUTimer.
-------------	--

##### Returns

None.

#### 5.6.3.2 static void STA\_Util\_startProfiler ( uint32\_t *base* ) [inline], [static]

Starts the CPUTimer used for profiling cycles.

**Parameters**

<i>base</i>	is the base address of a valid CPUTimer.
-------------	--

**Returns**

None.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

5.6.3.3 `static uint32_t STA_Util_stopProfiler ( uint32_t base ) [inline], [static]`

Stops the CPUTimer used for profiling cycles.

**Parameters**

<i>base</i>	is the base address of a valid CPUTimer.
-------------	--

**Returns**

Returns the number of cycles elapsed since [STA\\_Util\\_startProfiler\(\)](#) was called.

Referenced by [STA\\_Tests\\_testDevice\(\)](#).



## 5.7 STA\_User API Functions

### Macros

- #define **STA\_USER\_MARCH\_DATA\_SIZE**
- #define **STA\_USER\_MARCH\_CAN\_COPY\_SIZE**
- #define **STA\_USER\_MARCH\_CANA\_OBJ32\_START\_ADDR**
- #define **STA\_USER\_MARCH\_CANA\_OBJ4\_END\_ADDR**
- #define **STA\_USER\_MARCH\_CANA\_OBJ6\_START\_ADDR**
- #define **STA\_USER\_MARCH\_CANA\_OBJ15\_END\_ADDR**
- #define **STA\_USER\_PIE\_RAM\_ENTRY**
- #define **STA\_USER\_PIE\_TEST\_INT**
- #define **STA\_USER\_PIE\_TEST\_INT\_GROUP\_M**
- #define **STA\_USER\_DCSM\_OTP\_GOLDEN\_CRC**
- #define **STA\_USER\_CAN\_RAM\_GOLDEN\_CRC**
- #define **STA\_USER\_OSC\_DELAY\_US**
- #define **STA\_USER\_OSC\_MIN\_COUNT**
- #define **STA\_USER\_OSC\_MAX\_COUNT**
- #define **STA\_USER\_OSC\_HR\_MEP**
- #define **STA\_USER\_OSC\_HR\_MEP\_MIN**
- #define **STA\_USER\_OSC\_HR\_MEP\_MAX**

### Functions

- void [STA\\_User\\_initMarch](#) (void)
- void [STA\\_User\\_initOSCTimer2Test](#) (void)
- void [STA\\_User\\_initOSCHRTTest](#) (void)
- \_\_interrupt void [STA\\_User\\_canParityErrorISR](#) (void)

### Variables

- [STL\\_March\\_InjectErrorObj](#) **STA\_User\_marchErrorObj**
- [STL\\_March\\_InjectErrorHandle](#) **STA\_User\_marchErrorHandle**
- uint16\_t **STA\_User\_marchTestData** [STA\_USER\_MARCH\_DATA\_SIZE]
- uint16\_t **STA\_User\_marchTestDataCopy** [STA\_USER\_MARCH\_DATA\_SIZE]
- uint16\_t **STA\_User\_marchTestDataCANCopy** [STA\_USER\_MARCH\_CAN\_COPY\_SIZE]
- bool **STA\_User\_canInterruptFlag**
- uint16\_t **STA\_User\_parityErrorCode**
- uint16\_t **STA\_User\_canErrorReturnVal**
- [STL\\_OSC\\_CT\\_Obj](#) **STA\_User\_oscTimer2Obj**
- [STL\\_OSC\\_CT\\_Handle](#) **STA\_User\_oscTimer2Handle**
- [STL\\_OSC\\_HR\\_Obj](#) **STA\_User\_oscHRObj**
- [STL\\_OSC\\_HR\\_Handle](#) **STA\_User\_oscHRHandle**

### 5.7.1 Detailed Description

This module contains the declaration and initialization of the various objects and handles required by SDL modules tested in this application.

The code for this module is contained in `sta_user.c`, with `sta_user.h` containing the API declarations.

## 5.7.2 Function Documentation

### 5.7.2.1 void STA\_User\_initMarch ( void )

This function initializes the inject error object for March13N test.

**Returns**

None

References [STL\\_March\\_InjectErrorObj::address](#), [STL\\_March\\_InjectErrorObj::ramSection](#), [STL\\_March\\_InjectErrorObj::testMode](#), and [STL\\_March\\_InjectErrorObj::xorMask](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

### 5.7.2.2 void STA\_User\_initOSCTimer2Test ( void )

This function initializes the Oscillator Timer2 test objects.

**Returns**

None

References [STL\\_OSC\\_CT\\_Obj::clockSource](#), [STL\\_OSC\\_CT\\_Obj::maxCount](#), [STL\\_OSC\\_CT\\_Obj::minCount](#), and [STL\\_OSC\\_CT\\_Obj::prescaler](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

### 5.7.2.3 void STA\_User\_initOSCHRTTest ( void )

This function initializes the object for the Oscillator HRPWM test.

**Returns**

None

References [STL\\_OSC\\_HR\\_Obj::channel](#), [STL\\_OSC\\_HR\\_Obj::ePWMBase](#), [STL\\_OSC\\_HR\\_Obj::mepEdgeMode](#), [STL\\_OSC\\_HR\\_Obj::mepMax](#), [STL\\_OSC\\_HR\\_Obj::mepMin](#), and [STL\\_OSC\\_HR\\_Obj::sfoDelay](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

### 5.7.2.4 \_\_interrupt void STA\_User\_canParityErrorISR ( void )

CAN ISR to execute upon parity error detection in CAN message RAM.

**Returns**

None

References [STL\\_CAN\\_RAM\\_checkErrorStatus\(\)](#).

Referenced by [STA\\_Tests\\_testDevice\(\)](#).

## 6 Integration Notes

Profiling data is provided below for evaluation. These numbers were taken using the compiler settings and version for the RELEASE build configuration of the library project and the RAM\_RELEASE and FLASH\_RELEASE configurations of the STA.

Cycle Time .....	50
Memory Usage .....	51

### 6.1 Cycle Time

The cycle counts shown are based on the configuration of the modules used in the STA. The counts are not necessarily the worst-case cycle count and may vary depending on the module parameters. For example, some of the memory tests have configurable memory ranges over which the test should be performed, meaning the larger the memory section, the longer the test runs.

API	PASS Cycles (RAM)	FAIL Cycles (RAM)	PASS Cycles (Flash)	FAIL Cycles (Flash)
STL_PIE_RAM_testRAM	5324	5329	8199	8199
STL_PIE_RAM_testHandler	262	171	289	192
STL_CPU_REG_checkCPURegisters	655	55	710	84
STL_CPU_REG_checkFPURegisters	287	124	356	166
STL_CPU_REG_checkVCURegisters	358	120	399	151
STL_March_testRAM	405	405	671	671
STL_March_testRAMCopy	503	503	892	892
STL_CAN_RAM_testRAM	6661	6661	8228	8228
STL_CAN_RAM_testRAM (with copy)	16233	16330	21605	21725
STL_CRC_checkCRC	8268	8275	299	304
STL_OSC_CT_startTest + STL_OSC_CT_stopTest	147	143	173	176
STL_OSC_HR_testSFO	131878	131879	132120	132129

## 6.2 Memory Usage

The following shows the size in 16-bit words of the STL APIs. These values were obtained from the STA .map file.

API	Memory (16-bit words)
STL_CAN_RAM_checkErrorStatus	14
STL_CAN_RAM_injectError	39
STL_CAN_RAM_testRAM	62
STL_CPU_REG_testCPURegisters	205
STL_CPU_REG_testFPURegisters	106
STL_CPU_REG_testVCURegisters	110
STL_CRC_checkCRC	40
STL_CRC_calculate	56
STL_CRC_calculateLowBytes	46
STL_CRC_reset	5
STL_March_checkErrorStatus	38
STL_March_injectError	16
STL_March_testRAM	35
STL_March_testRAMCopy	47
STL_OSC_CT_startTest	61
STL_OSC_CT_stopTest	29
STL_OSC_HR_testSFO	120
STL_PIE_RAM_handler	5
STL_PIE_RAM_injectFault	18
STL_PIE_RAM_restoreVector	10
STL_PIE_RAM_testHandler	101
STL_PIE_RAM_testRAM	32
STL_Util_setErrorFlag	6

There is also a contribution of 134 words from the driverlib functions used by the library. Use of the STL\_OSC\_HR module results in an additional 497 words from the SFO library.

## 7 Safety Feature and Diagnostic Examples

Many of the safety features and diagnostics documented in the device safety manual are very system-specific and not well suited to being implemented as SDL APIs. However many still require special procedures or hardware test modes that may require some demonstration beyond their documented descriptions. For these particular cases, a series of examples have been created as part of the SDL to provide such a demonstration.

Using DCSM for Freedom From Interference (FFI) .....	52
Test of ECC logic in Flash .....	53
Test of Flash Prefetch, Data Cache and Wait-States .....	53
Missing clock detection .....	54
RAM access protection violation detection .....	54
Test of parity/ECC logic in SRAM .....	55
Software test of watchdog operation .....	56

### 7.1 Using DCSM for Freedom From Interference (FFI)

#### sdl\_ex\_dcsm\_ffl

This example demonstrates how to configure and use DCSM and how the DCSM blocks writes from one secured zone to another, simulating the its use to create firewalls between code of different safety requirement criticality.

It uses the default passwords to allocate one LSRAM block and one flash sector to zone 1 and another to zone 2. In this example, zoning of memories is done by programming the DCSM OTP. The values that are programmed can be found in in dcsm.asm. Secured RAM blocks are partitioned to contain data arrays used in the example, and secured Flash sectors contain the program code. Once secure, both zone1LockedArray and zone2LockedArray are immutable outside of the safety functions residing in the same zone.

!!!IMPORTANT!! By default, assignments in dcsm.asm are commented out and the sections mapped to OTP in dcsm.cmd are given the "type = DSECT" attribute to prevent programming of the OTP. In this state, this example is expected to fail (result = FAIL) because the memories won't actually be secured. If you are sure you want to permanently update the zones' link pointers and zone select blocks, uncomment the code in dcsm.asm and remove "type = DSECT" from dcsm.cmd.

Parts of this example were generated with assistance from the DCSM Tool. We strongly recommend using this tool to generate the code for your DCSM configuration. Refer to the following guide for more information: <http://www.ti.com/lit/pdf/spracp8>

#### Note

This example assumes you have not written to the DCSM OTP before and that the first zone select block is available for use. If this is not the case, you will need to update the link pointer, zone select block address, and passwords to use the next available zone select block.

#### External Connections

- None.

**Watch Variables**

- **result** - Status indicating success of blocking writes to secured zones.
- **errorZone1NotChanged**, **errorZone2NotChanged**, **errorZone1Changed**, **errorZone2Changed** - Count of errors found during execution.
- **zone1LockedArray** - Array located in zone 1 secured memory.
- **zone2LockedArray** - Array located in zone 2 secured memory.

## 7.2 Test of ECC logic in Flash

### sdl\_ex\_flash\_ecc\_test

This example demonstrates how to test the Flash ECC logic functionality.

A software test of the Flash ECC logic can be performed with the help of ECC test registers. Using the test registers, you can generate both single bit errors and uncorrectable errors. For additional details on the implementation of this diagnostic, see the "SECEDED Logic Correctness Check" section in the device technical reference manual.

**External Connections**

- None.

**Watch Variables**

- **nmiISRFlag** - Indicates that the NMI was triggered and called the ISR.
- **nmiStatus** - NMI status flags read in the ISR.
- **errorISRFlag** - Indicates that the correctable ECC error interrupt was triggered and called the ISR.
- **errorStatus** - Error status flags read in the ISR, indicating whether an error was single-bit or uncorrectable.
- **errorCount** - Number of correctable errors detected read in the ISR.
- **errorType** - For a single-bit error, indicates whether it was in the data or ECC bits.
- **dataOut** - For a single-bit error, displays the corrected data.
- **result** - Status of a successful detection and handling of ECC errors.

## 7.3 Test of Flash Prefetch, Data Cache and Wait-States

### sdl\_ex\_flash\_prefetch\_test

This example demonstrates how to test the behavior of the flash prefetch, data cache, and wait-states. Each of these configurations are altered one by one and the impact they have on a test function's execution time is measured. It is expected that an increase in the execution time will be observed in each case.

Note that as mentioned in the safety manual description of this diagnostic, a golden value may be used to check the execution time. This wasn't used for this example because of possible compiler differences between users' environments, but can be used in your actual application.

#### External Connections

- None.

#### Watch Variables

- **baseCycles** - Execution time of runPrefetchTestCode();
- **failCount** - Number of tests that returned failures.
- **result** - Status of flash configuration logic test.

## 7.4 Missing clock detection

### sdl\_ex\_mcd\_test

This example demonstrates how to check the missing clock detection functionality.

Once the MCD is simulated by disconnecting the clock to the MCD module an NMI is generated. This NMI determines that an MCD error was generated due to a clock failure which is handled in the ISR.

Before the MCD the clock frequency will be as per device initialization. Post MCD error, the clock will be running at the speed of INTOSC1 with the PLL disabled (10 MHz).

The example also shows how to lock the PLL after missing clock detection, by first explicitly switching the clock source to INTOSC1, resetting the missing clock detect circuit and then re-locking the PLL. After that the clock frequency will be restored to the original configuration.

#### External Connections

- None.

#### Watch Variables

- **fail** - Indicates that a missing clock was either not detected or was not handled correctly.
- **nmISRFlag** - Indicates that the missing clock failure caused an NMI to be triggered and called the ISR to handle it.
- **mcdDetect** - Indicates that a missing clock was detected.
- **result** - Status of a successful handling of missing clock detection.

## 7.5 RAM access protection violation detection

### sdl\_ex\_ram\_access\_protect

This example demonstrates a functional test of the RAM access protection violation detection and handling for several different types accesses. The example generates a number of master or

non-master fetch, write, or read violations from the CPU, CLA, and DMA as applicable to the device.

#### External Connections

- None.

#### Watch Variables

- **violationISRFlag** - Indicates that the access violation interrupt was triggered and called the ISR.
- **illegalISRFlag** - Indicates that a CPU fetch violation interrupt was generated and the ITRAP ISR ran.
- **violationStatus** - Access protection violation status flags read in the ISR.
- **violationAddr** - Address at which the access violation occurred.
- **result** - Status of a successful detection and handling of RAM access protection violations.

## 7.6 Test of parity/ECC logic in SRAM

### sdl\_ex\_ram\_ecc\_parity\_test

This example demonstrates how to check the SRAM ECC or parity logic functionality.

Three types of SRAM errors are generated to demonstrate the use of the SRAM test modes and the checking of the related flag and information registers. These types are parity errors (LSx, GSx, and CLAMSG RAMs) and correctable and uncorrectable ECC errors (M0 and M1 RAMs).

#### External Connections

- None.

#### Watch Variables

- **nmiISRFlag** - Indicates that the NMI was triggered and called the ISR.
- **nmiStatus** - NMI status flags read in the ISR.
- **errorISRFlag** - Indicates that the correctable RAM error interrupt was triggered and called the ISR.
- **errorStatus** - Correctable RAM error status flags read in the ISR.
- **errorCount** - Number of correctable errors detected read in the ISR.
- **errorAddr** - Address at which the error was detected.
- **result** - Status of a successful detection and handling of RAM errors.



## 7.7 Software test of watchdog operation

### sdl\_ex\_watchdog

This example shows how to use the wakeup interrupt to test the operation of the watchdog. The example generates two watchdog interrupts. The first is caused by delaying the reset of the watchdog too long, causing it to overflow. The second uses the windowing functionality to reset the counter before the minimum threshold can be reached.

#### External Connections

- None.

#### Watch Variables

- **wakeISRFlag** - Indicates the watchdog ISR was executed.
- **result** - Status of successful generation of expected watchdog pulse.

---

# IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

## Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

## Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated