

# **F28002x Firmware Development Package**

## **USER'S GUIDE**



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# 1 Introduction

The Texas Instruments® F28002x Firmware development package includes a device-specific driver library, a group of example applications that demonstrate key device functionality, and other development files such as linker command files that assist in getting started with a F28002x device.

**The following chapter provides a step by step guide for creating a new project from scratch as well as debugging. It is highly recommended that users new to the F28002x family of devices start by reading this section first.**

The F28002x devices have a set of example applications that users can load and run on their device.

- The driver library example applications can be found in the `~/driverlib/f28002x/examples` directory.
- The bit-field example applications can be found in the `~/device_support/f28002x/examples` directory.

## **F28002x Example Projects**

- Driverlib Example projects tested with: C2000 Compiler v20.2.1.LTS

As users move past evaluation, and get started developing their own application, TI recommends they maintain a similar project directory structure to that used in the example projects. Example projects have a hierarchy as follows:

- Main project directory
  - Project folder
    - \* Project sources (\*.c, \*.h)
    - \* CCS folder (ccs)
      - CCS projectspec file

## 1.1 Detailed Revision History

### V3.04.00.00

- Updated Driver Library to v3.04.00.00
- Added LAUNCHXL-F280025C DriverLib Demo Example
- Adding LAUNCHXL-F280025C bit-field Demo Example
- Added ERAD examples ported from F28004x
- Added CLB Type 3 examples
- Updated driverlib examples to support LAUNCHXL-F280025C
- Added new examples for I2C, ADC
- Added Flash linker command file with CRC

### V3.03.00.00

- Updated Driver Library to v3.03.00.00

- Added projectspec for driverlib.
- Updated compiler version to 20.2.1.LTS for all driverlib examples
- Updated the examples to use the new pinmap macro names.
- Added Sysconfig pinmux support to all examples
- Added CLB Type2 examples - clb\_ex18 to clb\_ex23
- Added LIN examples
- Added eCAP example to demonstrate generation of phase-shifted APWM outputs-ecap\_ex3\_apwm\_phase\_shift
- Added Example for Baud Tune via SCI - baud\_tune\_via\_uart
- Added ADC Examples - adc\_ex4 to adc\_ex9
- Added FSI Examples - fsi\_ex5 to fsi\_ex8
- Added EPWM Examples - epwm\_ex5, epwm\_ex6
- Added Interrupt Example- interrupt\_ex3\_with\_i2c\_sci\_spi\_loopback
- Added DCSM Tool example- dcsm\_security\_tool
- Updated examples to disable watchdog by default

#### **V3.02.00.00**

- Updated driverlib examples for GPIO, SPI, I2C, SCI to use sysconfig
- Added Temperature sensor example in bitfield format.
- Added DCSM example which will load the OTP Values.

#### **V3.01.00.00**

- Updated Driver Library to v3.01.00.00
- CLB tool enhancements to support for 2 tiles on F28002x
- New driverlib examples: Added CLB examples, pinumx examples with sysconfig support, daisy-chain examples , interrupt-nesting example

#### **v3.00.00.00**

- First Release of C2000Ware 3.00.00 with support only for F28002x



## 2 Getting Started and Troubleshooting

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### 2.1 Introduction

This guide aims to give you, the user, a step by step guide for how to create and debug projects from scratch. This guide will focus on the user of a F28002x controlCARD, but these same ideas should apply to other boards with minimal translation.

### 2.2 Project Creation

A typical F28002x application consists of setting up a CCS project, which involves configuring the build settings, file linking, and adding in any source code.

## CCS Project Creation

1. From the main CCS window select File -> New -> CCS Project. Select your Target as "TMS320F280025C". Name your project and choose a location for it to reside. Click Finish and your project will be created.

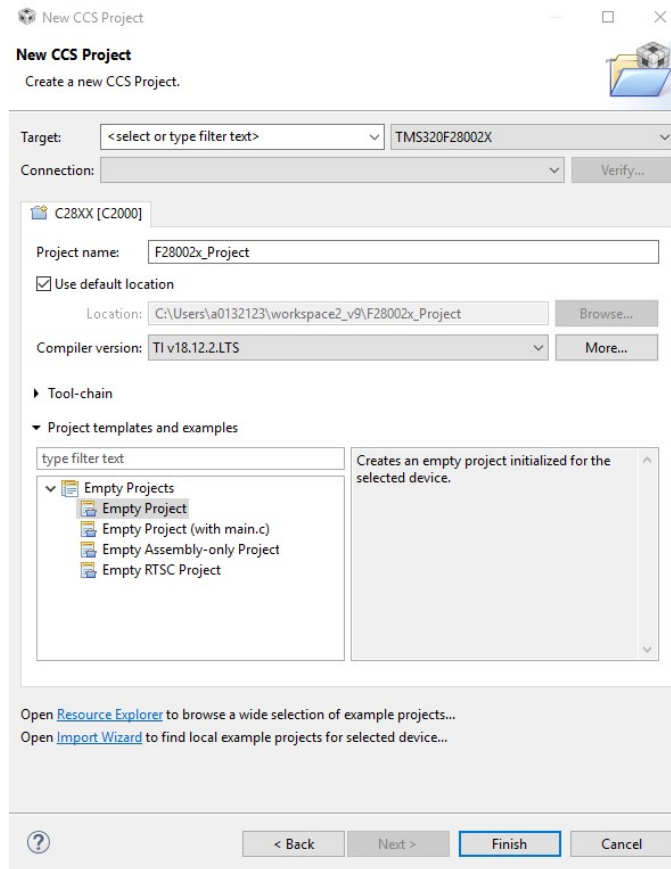


Figure 2.1: Creating a new C28 project

2. Before we can successfully build a project we need to setup some build specific settings. Right click on your project and select Properties. Look at the Processor Options and ensure they match the below image:

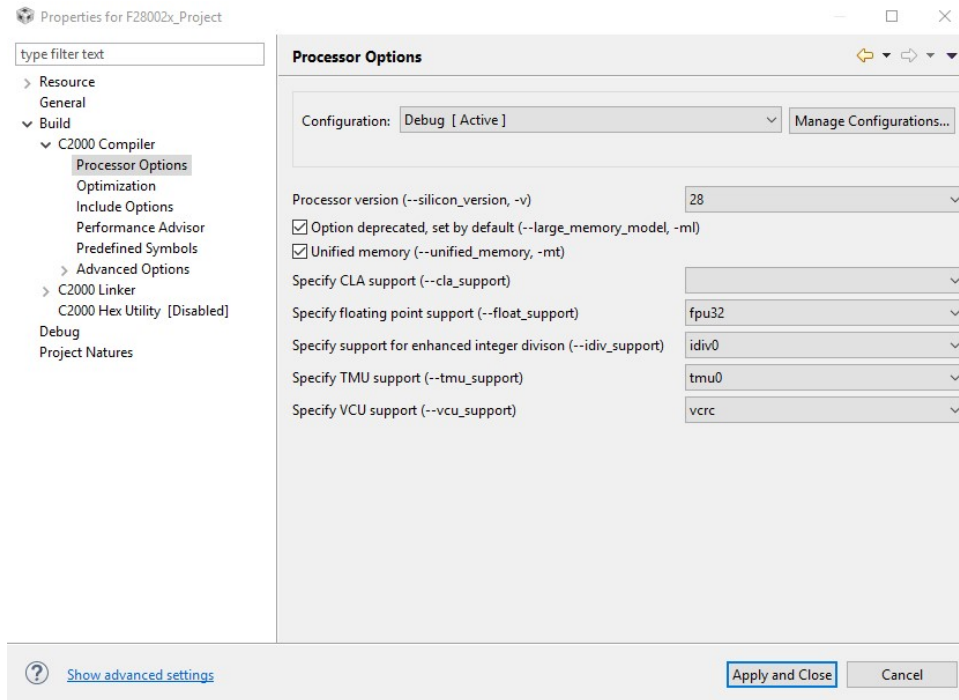


Figure 2.2: Project configuration dialog box

3. In the C2000 Compiler entry look for and select the Include Options. Click on the add directory icon to add a directory to the search path. Click the File System button to browse to the `driverlib\f28002x\driverlib` folder of your C2000Ware installation (typically `C:\ti\c2000\C2000Ware_<version>\driverlib\f28002x\driverlib`). Click ok to add this path, and repeat this same process to add the `device_support\f28002x\common\include` directory.

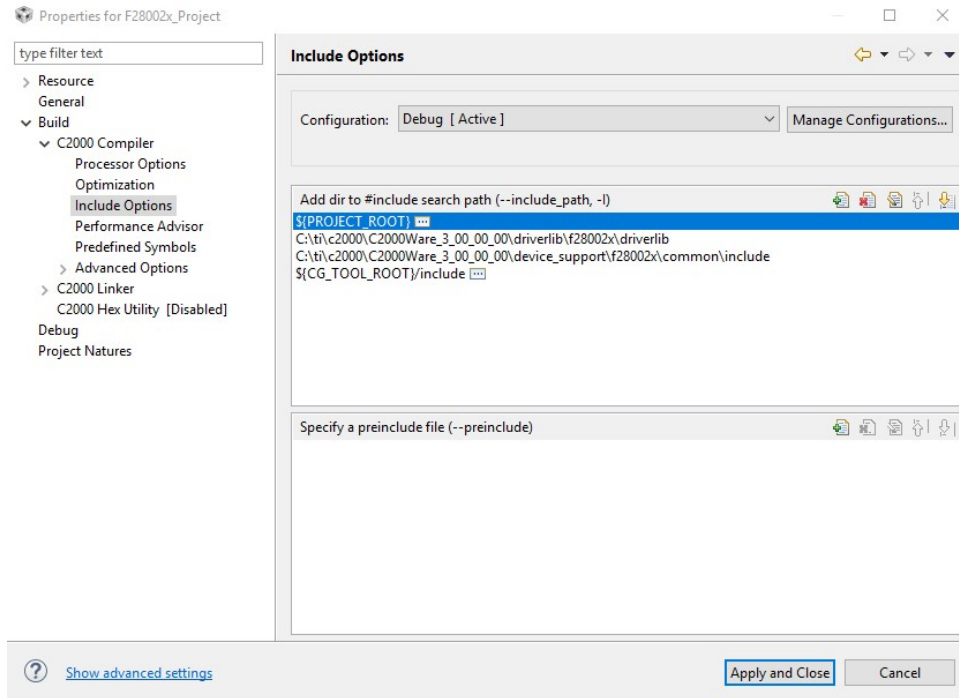


Figure 2.3: Project configuration dialog box

- Click on the Linker File Search Path. Add the following directory to the search path: `device_support\f28002x\common\cmd`. Then you'll also want to add the following files: `rts2800_fpu32_eabi.lib` and `28002x_generic_ram_lnk.cmd`. Finally, delete `libc.a`, we will use `rts2800_fpu32_eabi.lib` as our run time support library instead. Select ok to close out of the Build Properties.

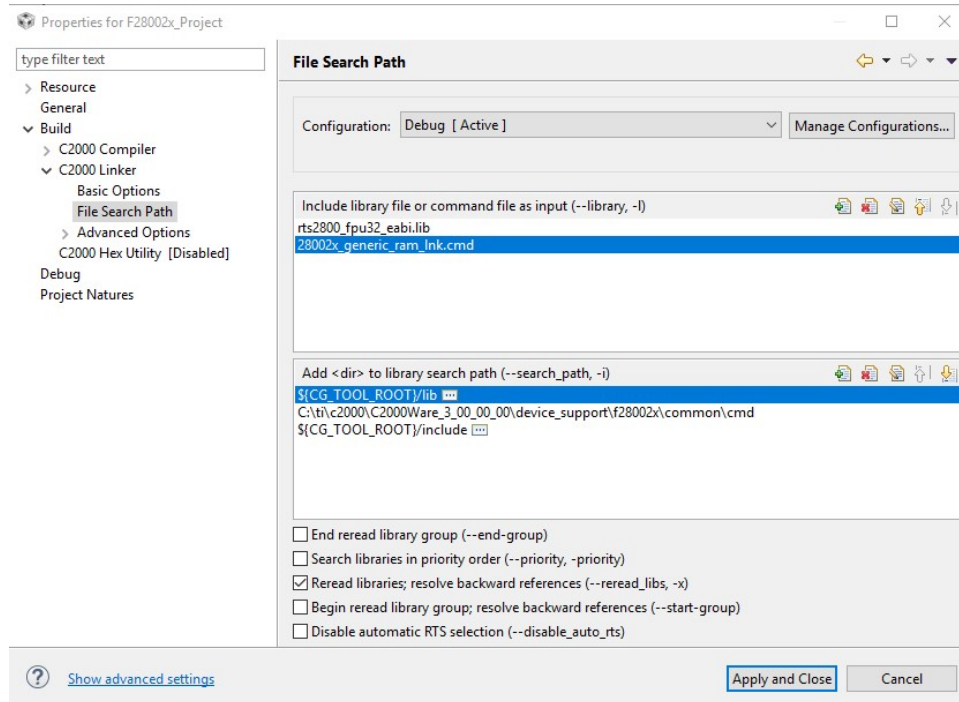


Figure 2.4: Project configuration dialog box

5. In the project explorer, check that no linker command file got added during project setup. If so, remove the linker command file that got added.
6. Next we need to link in a few files which are used by the header files. To do this right click on your project in the workspace and select Add Files. Navigate to the `device_support\f28002x\common\source` directory, and select `device.c`. After you select the file, you'll have the option to copy the file into the project or link it. We recommend you link files like this to the project as you will probably not modify these files. Link in the following file as well:

- `driverlib\f28002x\driverlib\ccs\Debug\driverlib.lib`

At this point your project workspace should look like the following:

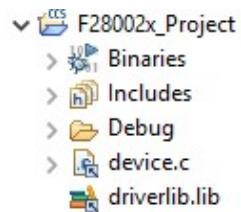


Figure 2.5: Linking files to project

7. Create a new file by right clicking on the project and selecting New -> File. Name this file main.c and copy the following code into it:

```
#include "driverlib.h"
#include "device.h"

void main(void)
{
    // Initialize device clock and peripherals
    Device_init();

    // Initialize GPIO and configure the GPIO pin as a push-pull output
    Device_initGPIO();
    GPIO_setPadConfig(DEVICE_GPIO_PIN_LED1, GPIO_PIN_TYPE_STD);
    GPIO_setDirectionMode(DEVICE_GPIO_PIN_LED1, GPIO_DIR_MODE_OUT);

    // Initialize PIE and clear PIE registers. Disables CPU interrupts.
    Interrupt_initModule();

    // Initialize the PIE vector table with pointers to the shell Interrupt
    // Service Routines (ISR).
    Interrupt_initVectorTable();

    // Enable Global Interrupt (INTM) and realtime interrupt (DBGM)
    EINT;
    ERTM;

    // Loop Forever
    for(;;)
    {
        // Turn on LED
        GPIO_writePin(DEVICE_GPIO_PIN_LED1, 0);

        // Delay for a bit.
        DEVICE_DELAY_US(500000);

        // Turn off LED
        GPIO_writePin(DEVICE_GPIO_PIN_LED1, 1);

        // Delay for a bit.
        DEVICE_DELAY_US(500000);
    }
}
```

8. Save main.c and then attempt to build the project by right clicking on it and selecting Build Project. Assuming the project builds, setup a target configuration file for your device (View -> Target Configurations), and try debugging this project on a F28002x device. When the code runs, you should see the LED blink.

## 2.3 Project: Adding Bitfield or Driverlib Support

F28002x devices support two types of development software, driver library APIs and bitfield structures. Each have their advantages and are implemented to be compatible together within the same user application. This section details how to add driverlib support to a bitfield project as well as how to add bitfield support to a driverlib project.

### Adding Driverlib Support

1. Add the following include directory path to the project: `driverlib\f28002x\driverlib`
2. Include the following header file in the project main source file: `device_support\f28002x\common\include\driverlib.h`
3. Add or link the `driverlib.lib` library to the project. Location of file: `driverlib\f28002x\driverlib\ccs\Debug`

### Adding Bitfield Support

1. Add the following include directory path to the project: `device_support\f28002x\headers\include`
2. Include the following header file in the project main source file: `device_support\f28002x\headers\include\f28002x_device.h`
3. Add or link the `f28002x_globalvariabledefs.c` file to the project. Location of file: `device_support\f28002x\headers\source`
4. Add or link the `f28002x_headers_nonbios.cmd` file to the project. Location of file: `device_support\f28002x\headers\cmd`

## 2.4 Troubleshooting

There are a number of things that can cause the user trouble while bringing up a debug session the first time. This section will try to provide solutions to the most common problems encountered with the Piccolo devices.

### "I get an error when I try to import the example projects"

This occurs when one imports a project for which he or she doesn't have the code generation tools for or the latest CCS device support update supporting your device. Please ensure that you have at least version 16.9.1.LTS of the C2000 Code Generation Tools and have updated your CCS device support through the CCS "Install New Software" menu under "Help".

### "My F28002x device isn't in the target configuration selection list"

The list of available device for debug is determined based on a number of factors, including drivers and tools chains available on the host system. If your system has previously been used only for development on previous C2000 devices, you may not have the required CCS device files. In CCS click on "Help, Check for updates" and follow the dialog boxes to update your CCS installation.

### "I cannot connect to the target"

This is most often times caused by either a bad target configuration, or simply the emulator being physically disconnected. If you are unable to connect to a target check the following things:

1. Ensure the target configuration is correct for the device you have.



2. Ensure the emulator is plugged in to both the computer and the device to be debugged.
3. Ensure that the target device is powered.

**"I cannot load code"**

This is typically caused by an error in the GEL script or improperly linked code. Advanced users may potentially alter GEL files depending on their overall system configuration. If you are having trouble loading code, check the linker command files and maps to ensure that they match the device memory map. If these appear correct, there is a chance there is something wrong in one of your GEL scripts.

**"When a core gets an interrupt, it faults"**

Ensure that the interrupt vector table is where the interrupt controller thinks it is. On the core, the interrupt vector table may be mapped to either RAM or flash. Please ensure that your vector table is where the interrupt controller thinks it is.

**"When the CPU comes up, it is not fresh out of reset"**

F28002x devices support several boot modes, several of which allow program code to be loaded into and executed out of RAM via one of the device many serial peripherals. If the boot mode pins are in the wrong state at power up, one of these peripheral boot modes may be entered accidentally before the debugger is connected. This leaves the chip in an unclear state with potentially several of the peripherals configured as well as the interrupt vector table setup. If you are seeing strange behavior check to ensure that the "Boot to Flash" or "Boot to RAM" boot mode is selected.



## 3 Interrupt Service Routine Priorities

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### 3.1 Interrupt Hardware Priority Overview

With the PIE block enabled, the interrupts are prioritized in hardware by default as follows:

**Global Priority (CPU Interrupt level):**

CPU Interrupt	Hardware Priority
Reset	1(Highest)
INT1	5
INT2	6
INT3	7
INT4	8
INT5	9
INT6	10
INT7	11
...	...
INT12	16
INT13	17
INT14	18
DLOGINT	19(Lowest)
RTOSINT	20
reserved	2
NMI	3
ILLEGAL	-
USER1	-(Software Interrupts)
USER2	-
...	...

CPU Interrupts INT1 - INT14, DLOGINT and RTOSINT are maskable interrupts. These interrupts can be enabled or disabled by the CPU Interrupt enable register (IER).

**Group Priority (PIE Level):**

If the Peripheral Interrupt Expansion (PIE) block is enabled, then CPU interrupts INT1 to INT12 are connected to the PIE. This peripheral expands each of these 12 CPU interrupt into 16 interrupts. Thus the total possible number of available interrupts in the PIE is 192.

Each of the PIE groups has its own interrupt enable register (PIEIERx) to control which of the 16 interrupts (INTx.1 - INTx.16) are enabled and permitted to issue an interrupt.

CPU Interrupt	PIE Group	PIE Interrupts							
		Highest ————— Hardware Priority Within the Group ————— Lowest							
INT1	1	INT1.1	INT1.2	INT1.3	INT1.4	INT1.5	INT1.6	INT1.7	INT1.8
INT2	2	INT2.1	INT2.2	INT2.3	INT2.4	INT2.5	INT2.6	INT2.7	INT2.8
INT3	3	INT3.1	INT3.2	INT3.3	INT3.4	INT3.5	INT3.6	INT3.7	INT3.8
... etc ...									
... etc ...									
INT12	12	INT12.1	INT12.2	INT12.3	INT12.4	INT12.5	INT12.6	INT12.7	INT4.8

Table 3.1: PIE Group Hardware Priority

## 3.2 PIE Interrupt Priorities

The PIE block is organized such that the interrupts are in a logical order. Interrupts that typically require higher priority, are organized higher up in the table and will thus be serviced with a higher priority by default.

The interrupts in a control subsystem can be categorized as follows (ordered highest to lowest priority):

### 1. Non-Periodic, Fast Response

These are interrupts that can happen at any time and when they occur, they must be serviced as quickly as possible. Typically these interrupts monitor an external event.

On the F28002x devices, such interrupts are allocated to the first few interrupts within PIE Group 1 and PIE Group 2. This position gives them the highest priority within the PIE group. In addition, Group 1 is multiplexed into the CPU interrupt INT1. CPU INT1 has the highest hardware priority. PIE Group 2 is multiplexed into the CPU INT2 which is the 2nd highest hardware priority.

### 2. Periodic, Fast Response

These interrupts occur at a known period, and when they do occur, they must be serviced as quickly as possible to minimize latency. The A/D converter is one good example of this. The A/D sample must be processed with minimum latency.

On the F28002x devices, such interrupts are allocated to the group 1 in the PIE table. Group 1 is multiplexed into the CPU INT1. CPU INT1 has the highest hardware priority.

### 3. Periodic

These interrupts occur at a known period and must be serviced before the next interrupt. Some of the PWM interrupts are an example of this. Many of the registers are shadowed, so the user has the full period to update the register values.

In the F28002x device's PIE modules, such interrupts are mapped to group 2 - group 5. These groups are multiplexed into CPU INT3 to INT5 (the ePWM and eCAP), which are the next lowest hardware priority.

### 4. Periodic, Buffered

These interrupts occur at periodic events, but are buffered and hence the processor need

only service such interrupts when the buffers are ready to filled/emptied. All of the serial ports (SCI / SPI / I2C / CAN) either have FIFOs or multiple mailboxes such that the CPU has plenty of time to respond to the events without fear of losing data.

In the F28002x device, such interrupts are mapped to INT6, INT8, and INT9, which are the next lowest hardware priority.

### 3.3 Software Prioritization of Interrupts

The user will probably find that the PIE interrupts are organized where they should be for most applications. However, some software prioritization may still be required for some applications.

Recall that the basic software priority scheme on the C28x works as follows:

- **Global Priority**

This priority can be managed by manipulating the CPU IER register. This register controls the 16 maskable CPU interrupts (INT1 - INT16).

- **Group Priority**

This can be managed by manipulating the PIE block interrupt enable registers (PIEIERx). There is one PIEIERx per group and each control the 16-interrupts multiplexed within that group.

The F28 software prioritization of interrupt example demonstrates how to configure the Global priority (via IER) and group priority (via PIEIERx) within an ISR in order to change the interrupt service priority based on user assigned levels. The steps required to do this are:

1. **Set the global priority**

Modify the IER register to allow CPU interrupts with a higher user priority to be serviced.

2. **Set the Group priority**

Modify the appropriate PIEIERx register to allow group interrupts with a higher user set priority to be serviced.

3. **Enable interrupts**

The software prioritized interrupts example provides a method using mask values that are configured during compile time to allow you to manage this easily.

To setup software prioritization for the example, the user must first assign the desired global priority levels and group priority levels.

This is done as follows:

1. *User assigns global priority levels*

INT1PL - INT16PL

These values are used to assign a priority level to each of the 16 interrupts controlled by the CPU IER register. A value of 1 is the highest priority while a value of 16 is the lowest. More than one interrupt can be assigned the same priority level. In this case the default hardware priority would determine which would be serviced first. A priority of 0 is used to indicate that

the interrupt is not used.

2. *User assigns PIE group priority levels*

GxyPL (where x = PIE group number 1 - 12 and y = interrupt number 1 - 16)

These values are used to assign a priority level to each of the 16 interrupts within a PIE group. A value of 1 is the highest priority while a value of 16 is the lowest. More than one interrupt can be assigned the same priority level. In this case the default hardware priority would determine which would be serviced first. A priority of 0 is used to indicate that the interrupt is not used.

Once the user has defined the global and group priority levels, the compiler will generate mask values that can be used to change the IER and PIEIERx registers within each ISR. In this manner the interrupt software prioritization will be changed. The masks that are generated at compile time are:

■ **IER mask values**

MINT1 - MINT16

The user assigned INT1PL - INT16PL values are used at compile time to calculate an IER mask for each CPU interrupt. This mask value will be used within an ISR to allow CPU interrupts with a higher priority to interrupt the current ISR and thus be serviced at a higher priority level.

■ **PIEIERxy mask values**

MGxy (where x = PIE group number 1 - 12 and y = interrupt number 1 - 16)

The assigned group priority levels (GxyPL) are used at compile time to calculate PIEIERx masks for each PIE group. This mask value will be used within an ISR to allow interrupts within the same group that have a higher assigned priority to interrupt the current ISR and thus be serviced at a higher priority level.

### 3.3.1 Using the IER/PIEIER Mask Values

Within an interrupt service routine, the global and group priority can be changed by software to allow other interrupts to be serviced. The procedure for setting an interrupt priority using the mask values created is the following:

1. **Set the global priority**

- Modify IER to allow CPU interrupts from the same PIE group as the current ISR.
- Modify IER to allow CPU interrupts with a higher user defined priority to be serviced.

2. **Set the group priority**

- Save the current PIEIERx value to a temporary register.
- The PIEIER register is then set to allow interrupts with a higher priority within a PIE group to be serviced.

3. **Enable interrupts**

- Enable all PIE interrupt groups by writing all 1's to the PIEACK register
- Enable global interrupts by clearing INTM

4. **Execute ISR.** Interrupts that were enabled in steps 1-3 (those with a higher software priority) will be allowed to interrupt the current ISR and thus be serviced first.

5. Restore the PIEIERx register

6. Exit

### 3.3.2 Example Code

The sample C code below shows an example of an Interrupt service routine for a SPI transmit FIFO. This interrupt is connected to PIE group 6.

```
//  
// SPI A Transmit FIFO ISR  
//  
__interrupt void spiTxFIFOISR(void)  
{  
    uint16_t i;  
  
    //  
    // Send data  
    //  
    for(i = 0; i < 2; i++)  
    {  
        SPI_writeDataNonBlocking(SPIA_BASE, sData[i]);  
    }  
  
    //  
    // Increment data for next cycle  
    //  
    for(i = 0; i < 2; i++)  
    {  
        sData[i] = sData[i] + 1;  
    }  
  
    //  
    // Clear interrupt flag and issue ACK  
    //  
    SPI_clearInterruptStatus(SPIA_BASE, SPI_INT_TXFF);  
    Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP6);  
}  
  
/*!
```





## 4 Driver Library Example Applications

These example applications show how to make use of various peripherals of a F28002x device. These applications are intended for demonstration and as a starting point for new applications.

All these examples are setup using the Code Composer Studio (CCS) "projectspec" format. Upon importing the "projectspec", the example project will be generated in the CCS workspace with copies of the source and header files included.

All of these examples reside in the `driverlib/f28002x/examples` subdirectory of the C2000Ware package.

**Example Projects require CCS v9.1.0 or newer**

### 4.1 ADC PPB PWM trip (adc\_ppb\_pwm\_trip)

This example demonstrates EPWM tripping through ADC limit detection PPB block. ADCAINT1 is configured to periodically trigger the ADCA channel 2 post initial software forced trigger. The limit detection post-processing block(PPB) is configured and if the ADC results are outside of the defined range, the post-processing block will generate an ADCxEVTy event. This event is configured as EPWM trip source through configuring EPWM XBAR and corresponding EPWM's trip zone and digital compare sub-modules. The example showcases

- one-shot
- cycle-by-cycle
- and direct tripping of PWMs through ADCAEVT1 source via Digital compare submodule.

The default limits are 0LSBs and 3600LSBs. With VREFHI set to 3.3V, the PPB will generate a trip event if the input voltage goes above about 2.9V.

#### External Connections

- A2 should be connected to a signal to convert
- Observe the following signals on an oscilloscope
  - ePWM1(GPIO0 - GPIO1)
  - ePWM2(GPIO2 - GPIO3)
  - ePWM3(GPIO4 - GPIO5)
- 

#### Watch Variables

- adcA2Results - digital representation of the voltage on pin A2

### 4.2 ADC ePWM Triggering Multiple SOC

This example sets up ePWM1 to periodically trigger a set of conversions on ADCA and ADCC. This example demonstrates multiple ADCs working together to process a batch of conversions using the available parallelism accross multiple ADCs.

ADCA Interrupt ISRs are used to read results of both ADCA and ADCC.

#### External Connections

- A0, A1, A2 and C2, C3, C4 pins should be connected to signals to be converted.

#### Watch Variables

- **adcAResult0** - Digital representation of the voltage on pin A0
- **adcAResult1** - Digital representation of the voltage on pin A1
- **adcAResult2** - Digital representation of the voltage on pin A2
- **adcCResult0** - Digital representation of the voltage on pin C2
- **adcCResult1** - Digital representation of the voltage on pin C3
- **adcCResult2** - Digital representation of the voltage on pin C4

## 4.3 ADC Burst Mode

This example sets up ePWM1 to periodically trigger ADCA using burst mode. This allows for different channels to be sampled with each burst.

Each burst triggers 3 conversions. A0 and A1 are part of every burst while the third conversion rotates between A2, A3, and A4. This allows high importance signals to be sampled at high speed while lower priority signals can be sampled at a lower rate.

ADCA Interrupt ISRs are used to read results for ADCA.

#### External Connections

- A0, A1, A2, A3, A4

#### Watch Variables

- **adcAResult0** - Digital representation of the voltage on pin A0
- **adcAResult1** - Digital representation of the voltage on pin A1
- **adcAResult2** - Digital representation of the voltage on pin A2
- **adcAResult3** - Digital representation of the voltage on pin A3
- **adcAResult4** - Digital representation of the voltage on pin A4

## 4.4 ADC Burst Mode Oversampling

This example sets up ePWM1 to periodically trigger SOC0 and SOC1 on ADCA (to sample A0 and A1). Additionally, the ADC burst mode is also triggered using ePWM1. The burst SOC's are used to accumulate multiple conversions to oversample A2 over multiple ePWM periods.

#### External Connections

- A0, A1, A2

**Watch Variables**

- **adcAResult0** - Digital representation of the voltage on pin A0
- **adcAResult1** - Digital representation of the voltage on pin A1
- **adcAResult2** - Digital representation of the voltage on pin A2

## 4.5 ADC SOC Oversampling

This example sets up ePWM1 to periodically trigger a set of conversions on ADCA including multiple SOC's that all convert A2 to achieve oversampling on A2.

ADCA Interrupt ISRs are used to read results of ADCA.

**External Connections**

- A0, A1, A2 should be connected to signals to be converted.

**Watch Variables**

- **adcAResult0** - Digital representation of the voltage on pin A0
- **adcAResult1** - Digital representation of the voltage on pin A1
- **adcAResult2** - Digital representation of the voltage on pin A2

## 4.6 ADC Software Triggering

This example converts some voltages on ADCA and ADCC based on a software trigger.

The ADCC will not convert until ADCA is complete, so the ADCs will not run asynchronously. However, this is much less efficient than allowing the ADCs to convert synchronously in parallel (for example, by using an ePWM trigger).

**External Connections**

- A0, A1, C2, and C3 should be connected to signals to convert

**Watch Variables**

- **adcAResult0** - Digital representation of the voltage on pin A0
- **adcAResult1** - Digital representation of the voltage on pin A1
- **adcCResult0** - Digital representation of the voltage on pin C2
- **adcCResult1** - Digital representation of the voltage on pin C3

## 4.7 ADC ePWM Triggering

This example sets up ePWM1 to periodically trigger a conversion on ADCA.

**External Connections**

- A0 should be connected to a signal to convert

#### Watch Variables

- **adcAResults** - A sequence of analog-to-digital conversion samples from pin A0. The time between samples is determined based on the period of the ePWM timer.

## 4.8 ADC Temperature Sensor Conversion

This example sets up the ePWM to periodically trigger the ADC. The ADC converts the internal connection to the temperature sensor, which is then interpreted as a temperature by calling the `ADC_getTemperatureC()` function.

#### Watch Variables

- **sensorSample** - The raw reading from the temperature sensor
- **sensorTemp** - The interpretation of the sensor sample as a temperature in degrees Celsius.

## 4.9 ADC Synchronous SOC Software Force (adc\_soc\_software\_sync)

This example converts some voltages on ADCA and ADCC using input 5 of the input X-BAR as a software force. Input 5 is triggered by toggling GPIO0, but any spare GPIO could be used. This method will ensure that both ADCs start converting at exactly the same time.

#### External Connections

- A2, A3, C2, C3 pins should be connected to signals to convert

#### Watch Variables

- **adcAResult0** : a digital representation of the voltage on pin A2
- **adcAResult1** : a digital representation of the voltage on pin A3
- **adcCResult0** : a digital representation of the voltage on pin C2
- **adcCResult1** : a digital representation of the voltage on pin C3

## 4.10 ADC Continuous Triggering (adc\_soc\_continuous)

This example sets up the ADC to convert continuously, achieving maximum sampling rate.

#### External Connections

- A0 pin should be connected to signal to convert

#### Watch Variables

- **adcAResults** - A sequence of analog-to-digital conversion samples from pin A0. The time between samples is the minimum possible based on the ADC speed.

## 4.11 ADC Continuous Conversions Read by DMA (adc\_soc\_continuous\_dma)

This example sets up two ADC channels to convert simultaneously. The results will be transferred by the DMA into a buffer in RAM.

### External Connections

- A3 & C3 pins should be connected to signals to convert

### Watch Variables

- **adcADataBuffer** : a digital representation of the voltage on pin A3
- **adcCDataBuffer** : a digital representation of the voltage on pin C3

## 4.12 ADC PPB Offset (adc\_ppb\_offset)

This example software triggers the ADC. Some SOC's have automatic offset adjustment applied by the post-processing block. After the program runs, the memory will contain ADC & post-processing block(PPB) results.

### External Connections

- A2, C2 pins should be connected to signals to convert

### Watch Variables

- **adcAResult** : a digital representation of the voltage on pin A2
- **adcAPPBResult** : a digital representation of the voltage on pin A2, minus 100 LSBs of automatically added offset
- **adcCResult** : a digital representation of the voltage on pin C2
- **adcCPPBResult** : a digital representation of the voltage on pin C2 plus 100 LSBs of automatically added offset

## 4.13 ADC PPB Limits (adc\_ppb\_limits)

This example sets up the ePWM to periodically trigger the ADC. If the results are outside of the defined range, the post-processing block will generate an interrupt.

The default limits are 1000LSBs and 3000LSBs. With VREFHI set to 3.3V, the PPB will generate an interrupt if the input voltage goes above about 2.4V or below about 0.8V.

### External Connections

- A0 should be connected to a signal to convert

#### Watch Variables

- None

## 4.14 ADC PPB Delay Capture (adc\_ppb\_delay)

This example demonstrates delay capture using the post-processing block.

Two asynchronous ADC triggers are setup:

- ePWM1, with period 2048, triggering SOC0 to convert on pin A0
- ePWM2, with period 9999, triggering SOC1 to convert on pin A2

Each conversion generates an ISR at the end of the conversion. In the ISR for SOC0, a conversion counter is incremented and the PPB is checked to determine if the sample was delayed.

After the program runs, the memory will contain:

- **conversion** : the sequence of conversions using SOC0 that were delayed
- **delay** : the corresponding delay of each of the delayed conversions

## 4.15 BGCRC CPU Interrupt Example

This example demonstrates how to configure and trigger BGCRC from the CPU. BGCRC module is configured for 1 KB of GS0 RAM which is programmed with a known data. The pre-computed CRC value is used as the golden CRC value. Interrupt is generated once the computation is done and checks if no error flags are raised. Calculation uses the 32-bit polynomial 0x04C11DB7 and seed value 0x00000000.

#### External Connections

- None.

#### Watch Variables

- pass - This should be 1.
- runStatus - BGCRC running status. This will be BGCRC\_ACTIVE if the module is running, BGCRC\_IDLE if the module is idle

## 4.16 CAN External Loopback

This example shows the basic setup of CAN in order to transmit and receive messages on the CAN bus. The CAN peripheral is configured to transmit messages with a specific CAN ID. A message is

then transmitted once per second, using a simple delay loop for timing. The message that is sent is a 2 byte message that contains an incrementing pattern.

This example sets up the CAN controller in External Loopback test mode. Data transmitted is visible on the CANTXA pin and is received internally back to the CAN Core. Please refer to details of the External Loopback Test Mode in the CAN Chapter in the Technical Reference Manual.

#### **External Connections**

- None.

#### **Watch Variables**

- msgCount - A counter for the number of successful messages received
- txMsgData - An array with the data being sent
- rxMsgData - An array with the data that was received

## **4.17 CAN External Loopback with Interrupts**

This example shows the basic setup of CAN in order to transmit and receive messages on the CAN bus. The CAN peripheral is configured to transmit messages with a specific CAN ID. A message is then transmitted once per second, using a simple delay loop for timing. The message that is sent is a 4 byte message that contains an incrementing pattern. A CAN interrupt handler is used to confirm message transmission and count the number of messages that have been sent.

This example sets up the CAN controller in External Loopback test mode. Data transmitted is visible on the CANTXA pin and is received internally back to the CAN Core. Please refer to details of the External Loopback Test Mode in the CAN Chapter in the Technical Reference Manual.

#### **External Connections**

- None.

#### **Watch Variables**

- txMsgCount - A counter for the number of messages sent
- rxMsgCount - A counter for the number of messages received
- txMsgData - An array with the data being sent
- rxMsgData - An array with the data that was received
- errorFlag - A flag that indicates an error has occurred

## **4.18 CAN External Loopback with DMA**

This example sets up the CAN module to transmit and receive messages on the CAN bus. The CAN module is set to transmit a 4 byte message internally. An interrupt is used to assert the DMA request line which then triggers the DMA to transfer the received data from the CAN interface register to the receive buffer array. A data check is performed once the transfer is complete.

This example sets up the CAN controller in External Loopback test mode. Data transmitted is visible on the CANTXA pin and is received internally back to the CAN Core. Please refer to details of the External Loopback Test Mode in the CAN Chapter in the Technical Reference Manual.

#### External Connections

- None.

#### Watch Variables

- txMsgCount - A counter for the number of messages sent
- rxMsgCount - A counter for the number of messages received
- txMsgData - An array with the data being sent
- rxMsgData - An array with the data that was received

## 4.19 CAN Error Generation Example

This example demonstrates the ways of handling CAN Error conditions. It generates the CAN Packets and sends them over GPIO. It is looped back externally to be received in CAN module. The CAN Interrupt service routine reads the Error status and demonstrates how different Error conditions can be detected.

Change `ERR_CFG` define to the different Error Scenarios and run the example. The corresponding Error Flag will be set in status variable of `canalSR()` routine. Uses a CPU Timer (Timer 0) for periodic timer interrupt of `CANBITRATE`  $\mu$ Sec. On the Timer interrupt, it sends the required CAN Frame type with the specified error conditions.

#### Note:

CAN modules on the device need to be connected to via CAN transceivers.

Please refer to the application note titled "Configurable Error Generator for Controller Area Network" at [www.ti.com/lit/pdf/spracq3](http://www.ti.com/lit/pdf/spracq3) for further details on this example.

#### External Connections

- ControlCARD GPIOTX\_PIN(GPIO4) should be connected to GPIO5(CANRXA)

#### Watch Variables Transmit

- status - variable in `canalSR` for checking error Status

## 4.20 CLB Timer Two States

For the detailed description of this example, please refer to: `C2000Ware_PATH Tool Users Guide.pdf`



## **4.21 CLB Interrupt Tag**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.22 CLB Output Intersect**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.23 CLB PUSH PULL**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.24 CLB Multi Tile**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.25 CLB Glue Logic**

For the detailed description of this example, please refer to : C2000Ware\_PATH Tool Users Guide.pdf

## **4.26 CLB AOC Control**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.27 CLB AOC Release Control**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.28 CLB Combinational Logic**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.29 CLB XBARs**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.30 CLB AOC Control**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.31 CLB Serializer**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.32 CLB LFSR**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.33 CLB Lock Output Mask**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.34 CLB INPUT Pipeline Mode**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.35 CLB Clocking and PIPELINE Mode**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.36 CLB SPI Data Export**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.37 CLB SPI Data Export DMA**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.38 CLB GPIO Input Filter**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.39 CLB Auxiliary PWM**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.40 CLB PWM Protection**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## **4.41 CLB Signal Generator**

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## 4.42 CLB State Machine

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## 4.43 CLB External Signal AND Gate

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## 4.44 CLB Timer

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## 4.45 CLB Empty Project

For the detailed description of this example, please refer to: C2000Ware\_PATH Tool Users Guide.pdf

## 4.46 CMPSS Asynchronous Trip

This example enables the CMPSS1 COMPH comparator and feeds the asynchronous CTRIPOUTH signal to the GPIO14/OUTPUTXBAR3 pin and CTRIPH to GPIO13/EPWM7B.

CMPSS is configured to generate trip signals to trip the EPWM signals. CMPIN1P is used to give positive input and internal DAC is configured to provide the negative input. Internal DAC is configured to provide a signal at VDD/2. An EPWM signal is generated at GPIO13 and is configured to be tripped by CTRIPOUTH.

When a low input(VSS) is provided to CMPIN1P,

- Trip signal(GPIO14) output is low
- PWM7B(GPIO13) gives a PWM signal

When a high input(higher than VDD/2) is provided to CMPIN1P,

- Trip signal(GPIO14) output turns high
- PWM7B(GPIO13) gets tripped and outputs as high

### External Connections

- Give input on CMPIN1P (The pin is shared with ADCINA2)

- Outputs can be observed on GPIO14 and GPIO13 using an oscilloscope

**Watch Variables**

- None

## 4.47 CMPSS Digital Filter Configuration

This example enables the CMPSS1 COMPH comparator and feeds the output through the digital filter to the GPIO14/OUTPUTXBAR3 pin.

CMPIN1P is used to give positive input and internal DAC is configured to provide the negative input. Internal DAC is configured to provide a signal at VDD/2.

When a low input(VSS) is provided to CMPIN1P,

- GPIO14 output is low

When a high input(higher than VDD/2) is provided to CMPIN1P,

- GPIO14 output turns high

**External Connections**

- Give input on CMPIN1P (The pin is shared with ADCINA2)
- Output can be observed on GPIO14 using an oscilloscope

**Watch Variables**

- None

## 4.48 DCC Single shot Clock verification

This program uses the XTAL clock as a reference clock to verify the frequency of the PLLRAW clock.

The Dual-Clock Comparator Module 0 is used for the clock verification. The clocksource0 is the reference clock (Fclk0 = 20Mhz) and the clocksource1 is the clock that needs to be verified (Fclk1 = 100Mhz). Seed is the value that gets loaded into the Counter.

Please refer to the TRM for details on counter seed values to be set.

**External Connections**

- None

**Watch Variables**

- **status/result** - Status of the PLLRAW clock verification

## 4.49 DCC Single shot Clock measurement

This program demonstrates Single Shot measurement of the INTOSC2 clock post trim using XTAL as the reference clock.

The Dual-Clock Comparator Module 0 is used for the clock measurement. The clocksource0 is the reference clock (Fclk0 = 20Mhz) and the clocksource1 is the clock that needs to be measured (Fclk1 = 10Mhz). Since the frequency of the clock1 needs to be measured an initial seed is set to the max value of the counter.

Please refer to the TRM for details on counter seed values to be set.

### External Connections

- None

### Watch Variables

- **result** - Status if the INTOSC2 clock measurement completed successfully.
- **meas\_freq1** - measured clock frequency, in this case for INTOSC2.

## 4.50 DCC Continuous clock monitoring

This program demonstrates continuous monitoring of PLL Clock in the system using INTOSC2 as the reference clock. This would trigger an interrupt on any error, causing the decrement/ reload of counters to stop. Further, dump the counters into the RAM to measure the error over a 200us window. The error would be based on the non-zero counter value.

The Dual-Clock Comparator Module 0 is used for the clock monitoring. The clocksource0 is the reference clock (Fclk0 = 10Mhz) and the clocksource1 is the clock that needs to be monitored (Fclk1 = 100Mhz). Seed is the value that gets loaded into the Counter. The clock0 and clock1 seed are set to achieve a window of 300us. For the sake of demo a slight variance is given to clock1 seed value to generate an error on continuous monitoring.

Please refer to the TRM for details on counter seed values to be set.

### External Connections

- None

### Watch Variables

- **status/result** - Status of the PLLRAW clock monitoring
- **cnt0** - Counter0 Value measure when error is generated
- **cnt1** - Counter1 Value measure when error is generated
- **valid** - Valid0 Value measure when error is generated

## 4.51 DMA GSRAM Transfer (dma\_ex1\_gsram\_transfer)

This example uses one DMA channel to transfer data from a buffer in RAMGS0 to a buffer in RAMGS1. The example sets the DMA channel PERINTFRC bit repeatedly until the transfer of 16 bursts (where each burst is 8 16-bit words) has been completed. When the whole transfer is complete, it will trigger the DMA interrupt.

### Watch Variables

- **sData** - Data to send
- **rData** - Received data

## 4.52 eCAP APWM Example

This program sets up the eCAP module in APWM mode. The PWM waveform will come out on GPIO5. The frequency of PWM is configured to vary between 5Hz and 10Hz using the shadow registers to load the next period/compare values.

## 4.53 eCAP Capture PWM Example

This example configures ePWM3A for:

- Up count mode
- Period starts at 500 and goes up to 8000
- Toggle output on PRD

eCAP1 is configured to capture the time between rising and falling edge of the ePWM3A output.

### External Connections

- eCAP1 is on GPIO16
- ePWM3A is on GPIO4
- Connect GPIO4 to GPIO16.

### Watch Variables

- **ecap1PassCount** - Successful captures.
- **ecap1IntCount** - Interrupt counts.

## 4.54 eCAP APWM Phase-shift Example

This program sets up the eCAP1 and eCAP2 modules in APWM mode to generate the two phase-shifted PWM outputs of same duty and frequency value. The frequency, duty and phase values can be programmed of choice by updating the defined macros. By default 10 Khz frequency, 50% duty

and 30% phase shift values are used. eCAP2 output leads the eCAP1 output by 30% GPIO14 and GPIO15 are used as eCAP1/2 outputs and can be probed using analyzer/CRO to observe the waveforms

## 4.55 ePWM Chopper

This example configures ePWM1, ePWM2, ePWM3 and ePWM4 as follows

- ePWM1 with Chopper disabled (Reference)
- ePWM2 with chopper enabled at 1/8 duty cycle
- ePWM3 with chopper enabled at 6/8 duty cycle
- ePWM4 with chopper enabled at 1/2 duty cycle with One-Shot Pulse enabled

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO2 EPWM2A
- GPIO3 EPWM2B
- GPIO4 EPWM3A
- GPIO5 EPWM3B
- GPIO6 EPWM4A
- GPIO7 EPWM4B

### Watch Variables

- None.

## 4.56 EPWM Configure Signal

This example configures ePWM1, ePWM2, ePWM3 to produce signal of desired frequency and duty. It also configures phase between the configured modules.

Signal of 10kHz with duty of 0.5 is configured on ePWMxA & ePWMxB with ePWMxB inverted. Also, phase of 120 degree is configured between ePWM1 to ePWM3 signals.

During the test, monitor ePWM1, ePWM2, and/or ePWM3 outputs on an oscilloscope.

- ePWM1A is on GPIO0
- ePWM1B is on GPIO1
- ePWM2A is on GPIO2
- ePWM2B is on GPIO3
- ePWM3A is on GPIO4
- ePWM3B is on GPIO5



## 4.57 Realization of Monoshot mode

This example showcases how to generate monoshot PWM output based on external trigger i.e. generating just a single pulse output on receipt of an external trigger. And the next pulse will be generated only when the next trigger comes. The example utilizes external synchronization and T1 action qualifier event features to achieve the desired output.

ePWM1 is used to generate the monoshot output and ePWM2 is used as an external trigger for that. No external connections are required as ePWM2A is fed as the trigger using Input X-BAR automatically.

ePWM1 is configured to generate a single pulse of 0.5us when received an external trigger. This is achieved by enabling the phase synchronization feature and configuring EPWMxSYNCl as EXTSYNCIN1. And this EPWMxSYNCl is also configured as T1 event of action qualifier to set output HIGH while "CTR = PRD" action is used to set output LOW.

ePWM2 is configured to generate a 100 KHz signal with a duty of 1% (to simulate a rising edge trigger) which is routed to EXTSYNCIN1 using Input XBAR.

Observe GPIO0 (EPWM1A : Monoshot Output) and GPIO2 (EPWM2 : External Trigger) on oscilloscope.

**NOTE :** In the following example, the ePWM timer is still running in a continuous mode rather than a one-shot mode thus for more reliable implementation, refer to CLB based one shot PWM implementation demonstrated in "clb\_ex17\_one\_shot\_pwm" example

## 4.58 EPWM Action Qualifier (epwm\_up\_aq)

This example configures ePWM1, ePWM2, ePWM3 to produce an waveform with independent modulation on EPWMxA and EPWMxB.

The compare values CMPA and CMPB are modified within the ePWM's ISR.

The TB counter is in up count mode for this example.

View the EPWM1A/B(GPIO0 & GPIO1), EPWM2A/B(GPIO2 & GPIO3) and EPWM3A/B(GPIO4 & GPIO5) waveforms via an oscilloscope.

## 4.59 ePWM Trip Zone

This example configures ePWM1 and ePWM2 as follows

- ePWM1 has TZ1 as one shot trip source
- ePWM2 has TZ1 as cycle by cycle trip source

Initially tie TZ1 high. During the test, monitor ePWM1 or ePWM2 outputs on a scope. Pull TZ1 low to see the effect.

### External Connections

- ePWM1A is on GPIO0
- ePWM2A is on GPIO2

- TZ1 is on GPIO12

This example also makes use of the Input X-BAR. GPIO12 (the external trigger) is routed to the input X-BAR, from which it is routed to TZ1.

The TZ-Event is defined such that ePWM1A will undergo a One-Shot Trip and ePWM2A will undergo a Cycle-By-Cycle Trip.

## 4.60 ePWM Up Down Count Action Qualifier

This example configures ePWM1, ePWM2, ePWM3 to produce a waveform with independent modulation on ePWMxA and ePWMxB.

The compare values CMPA and CMPB are modified within the ePWM's ISR.

The TB counter is in up/down count mode for this example.

View the ePWM1A/B(GPIO0 & GPIO1), ePWM2A/B(GPIO2 & GPIO3) and ePWM3A/B(GPIO4 & GPIO5) waveforms on oscilloscope.

## 4.61 ePWM Synchronization

This example configures ePWM1, ePWM2, ePWM3 and ePWM4 as follows

- ePWM1 without phase shift as master
- ePWM2 with phase shift of 300 TBCLKs
- ePWM3 with phase shift of 600 TBCLKs
- ePWM4 with phase shift of 900 TBCLKs

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO2 EPWM2A
- GPIO3 EPWM2B
- GPIO4 EPWM3A
- GPIO5 EPWM3B
- GPIO6 EPWM4A
- GPIO7 EPWM4B

### Watch Variables

- None.

## 4.62 ePWM Digital Compare

This example configures ePWM1 as follows

- ePWM1 with DCAEVT1 forcing the ePWM output LOW
- GPIO25 is used as the input to the INPUT XBAR INPUT1
- INPUT1 (from INPUT XBAR) is used as the source for DCAEVT1
- GPIO25's PULL-UP resistor is enabled, in order to test the trip, PULL this pin to GND

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO25 TZ1, pull this pin low to trip the ePWM

### Watch Variables

- None.

## 4.63 ePWM Digital Compare Event Filter Blanking Window

This example configures ePWM1 as follows

- ePWM1 with DCAEVT1 forcing the ePWM output LOW
- GPIO25 is used as the input to the INPUT XBAR INPUT1
- INPUT1 (from INPUT XBAR) is used as the source for DCAEVT1
- GPIO25's PULL-UP resistor is enabled, in order to test the trip, PULL this pin to GND
- ePWM1 with DCBEVT1 forcing the ePWM output LOW
- GPIO25 is used as the input to the INPUT XBAR INPUT1
- INPUT1 (from INPUT XBAR) is used as the source for DCAEVT1
- GPIO25's PULL-UP resistor is enabled, in order to test the trip, PULL this pin to GND
- DCBEVT1 uses the filtered version of DCBEVT1
- The DCFILT signal uses the blanking window to ignore the DCBEVT1 for the duration of DC Blanking window

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO25 TRIPIN1, pull this pin low to trip the ePWM

### Watch Variables

- None.

## 4.64 ePWM Valley Switching

This example configures ePWM1 as follows

- ePWM1 with DCAEVT1 forcing the ePWM output LOW
- GPIO25 is used as the input to the INPUT XBAR INPUT1
- INPUT1 (from INPUT XBAR) is used as the source for DCAEVT1
- GPIO25 is set to output and toggled in the main loop to trip the PWM
  
- ePWM1 with DCBEVT1 forcing the ePWM output LOW
- GPIO25 is used as the input to the INPUT XBAR INPUT1
- INPUT1 (from INPUT XBAR) is used as the source for DCAEVT1
- GPIO25 is set to output and toggled in the main loop to trip the PWM
- DCBEVT1 uses the filtered version of DCBEVT1
- The DCFILT signal uses the valley switching module to delay the
- DCFILT signal by a software defined DELAY value.

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO25 TRIPIN1 (Output Pin, toggled through software)

### Watch Variables

- None.

## 4.65 ePWM Digital Compare Edge Filter

This example configures ePWM1 as follows

- ePWM1 with DCBEVT2 forcing the ePWM output LOW as a CBC source
- GPIO25 is used as the input to the INPUT XBAR INPUT1
- INPUT1 (from INPUT XBAR) is used as the source for DCBEVT2
- GPIO25 is set to output and toggled in the main loop to trip the PWM
- The DCBEVT2 is the source for DCFILT
- The DCFILT will count edges of the DCBEVT2 and generate a signal to to trip the ePWM on the 4th edge of DCBEVT2

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO25 TRIPIN1 (Output Pin, toggled through software)

### Watch Variables

- None.

## 4.66 ePWM Deadband

This example configures ePWM1 through ePWM6 as follows

- ePWM1 with Deadband disabled (Reference)
- ePWM2 with Deadband Active High
- ePWM3 with Deadband Active Low
- ePWM4 with Deadband Active High Complimentary
- ePWM5 with Deadband Active Low Complimentary
- ePWM6 with Deadband Output Swap (switch A and B outputs)

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B
- GPIO2 EPWM2A
- GPIO3 EPWM2B
- GPIO4 EPWM3A
- GPIO5 EPWM3B
- GPIO6 EPWM4A
- GPIO7 EPWM4B
- GPIO8 EPWM5A
- GPIO9 EPWM5B
- GPIO10 EPWM6A
- GPIO11 EPWM6B

### Watch Variables

- None.

## 4.67 ePWM DMA

This example configures ePWM1 and DMA as follows:

- ePWM1 is set up to generate PWM waveforms
- DMA5 is set up to update the CMPAHR, CMPA, CMPBHR and CMPB every period with the next value in the configuration array. This allows the user to create a DMA enabled fifo for all the CMPx and CMPxHR registers to generate unconventional PWM waveforms.
- DMA6 is set up to update the TBPHSHR, TBPHS, TBPRDHR and TBPRD every period with the next value in the configuration array.
- Other registers such as AQCTL can be controlled through the DMA as well by following the same procedure. (Not used in this example)

### External Connections

- GPIO0 EPWM1A
- GPIO1 EPWM1B

**Watch Variables**

- None.

## 4.68 Frequency Measurement Using eQEP

This example will calculate the frequency of an input signal using the eQEP module. ePWM1A is configured to generate this input signal with a frequency of 5 kHz. It will interrupt once every period and call the frequency calculation function. This example uses the IQMath library to simplify high-precision calculations.

In addition to the main example file, the following files must be included in this project:

- **eqep\_ex1\_calculation.c** - contains frequency calculation function
- **eqep\_ex1\_calculation.h** - includes initialization values for frequency structure

The configuration for this example is as follows

- Maximum frequency is configured to 10KHz (baseFreq)
- Minimum frequency is assumed at 50Hz for capture pre-scalar selection

**SPEED\_FR:** High Frequency Measurement is obtained by counting the external input pulses for 10ms (unit timer set to 100Hz).

$$SPEED\_FR = \frac{Count\ Delta}{10ms}$$

**SPEED\_PR:** Low Frequency Measurement is obtained by measuring time period of input edges. Time measurement is averaged over 64 edges for better results and the capture unit performs the time measurement using pre-scaled SYSCLK.

Note that the pre-scalar for capture unit clock is selected such that the capture timer does not overflow at the required minimum frequency. This example runs indefinitely until the user stops it.

For more information about the frequency calculation see the comments at the beginning of eqep\_ex1\_calculation.c and the XLS file provided with the project, eqep\_ex1\_calculation.xls.

**External Connections**

- Connect GPIO25/eQEP1A to GPIO0/ePWM1A

**Watch Variables**

- **freq.freqHzFR** - Frequency measurement using position counter/unit time out
- **freq.freqHzPR** - Frequency measurement using capture unit

## 4.69 Position and Speed Measurement Using eQEP

This example provides position and speed measurement using the capture unit and speed measurement using unit time out of the eQEP module. ePWM1 and a GPIO are configured to generate simulated eQEP signals. The ePWM module will interrupt once every period and call the position/speed calculation function. This example uses the IQMath library to simplify high-precision calculations.

In addition to the main example file, the following files must be included in this project:

- **eqep\_ex2\_calculation.c** - contains position/speed calculation function
- **eqep\_ex2\_calculation.h** - includes initialization values for position/speed structure

The configuration for this example is as follows

- Maximum speed is configured to 6000rpm (baseRPM)
- Minimum speed is assumed at 10rpm for capture pre-scalar selection
- Pole pair is configured to 2 (polePairs)
- Encoder resolution is configured to 4000 counts/revolution (mechScaler)
- Which means:  $4000 / 4 = 1000$  line/revolution quadrature encoder (simulated by ePWM1)
- ePWM1 (simulating QEP encoder signals) is configured for a 5kHz frequency or 300 rpm ( $= 4 * 5000 \text{ cnts/sec} * 60 \text{ sec/min} / 4000 \text{ cnts/rev}$ )

**SPEEDRPM\_FR:** High Speed Measurement is obtained by counting the QEP input pulses for 10ms (unit timer set to 100Hz).

**SPEEDRPM\_FR** = (Position Delta / 10ms) \* 60 rpm

**SPEEDRPM\_PR:** Low Speed Measurement is obtained by measuring time period of QEP edges. Time measurement is averaged over 64 edges for better results and the capture unit performs the time measurement using pre-scaled SYSCCLK.

Note that the pre-scaler for capture unit clock is selected such that the capture timer does not overflow at the required minimum frequency. This example runs indefinitely until the user stops it.

For more information about the position/speed calculation see the comments at the beginning of eqep\_ex2\_calculation.c and the XLS file provided with the project, eqep\_ex2\_calculation.xls.

### External Connections

- Connect GPIO25/eQEP1A to GPIO0/ePWM1A (simulates eQEP Phase A signal)
- Connect GPIO29/eQEP1B to GPIO1/ePWM1B (simulates eQEP Phase B signal)
- Connect GPIO23/eQEP1I to GPIO2 (simulates eQEP Index Signal)

### Watch Variables

- **posSpeed.speedRPMFR** - Speed meas. in rpm using QEP position counter
- **posSpeed.speedRPMPR** - Speed meas. in rpm using capture unit
- **posSpeed.thetaMech** - Motor mechanical angle (Q15)
- **posSpeed.thetaElec** - Motor electrical angle (Q15)

## 4.70 ePWM frequency Measurement Using eQEP via xbar connection

This example will calculate the frequency of an PWM signal using the eQEP module. ePWM1A is configured to generate this input signal with a frequency of 5 kHz. This ePWM signal is connected to input of eQEP using Input CrossBar and EPWM XBAR. ePWM module will interrupt once every period and call the frequency calculation function. This example uses the IQMath library to simplify high-precision calculations.

In addition to the main example file, the following files must be included in this project:

- **eqep\_ex1\_calculation.c** - contains frequency calculation function
- **eqep\_ex1\_calculation.h** - includes initialization values for frequency structure

The configuration for this example is as follows

- Maximum frequency is configured to 10KHz (baseFreq)
- Minimum frequency is assumed at 50Hz for capture pre-scalar selection
- GPIO0 is connected to output of INPUT\_XBAR1
- INPUT\_XBAR1 is connected to output of PWMXBAR at TRIP4
- eQEPA source is configured as PWMXBAR.1 output (TRIP4)

**SPEED\_FR:** High Frequency Measurement is obtained by counting the external input pulses for 10ms (unit timer set to 100Hz).

$$SPEED\_FR = \frac{Count\ Delta}{10ms}$$

**SPEED\_PR:** Low Frequency Measurement is obtained by measuring time period of input edges. Time measurement is averaged over 64 edges for better results and the capture unit performs the time measurement using pre-scaled SYSCLK.

Note that the pre-scalar for capture unit clock is selected such that the capture timer does not overflow at the required minimum frequency. This example runs indefinitely until the user stops it.

For more information about the frequency calculation see the comments at the beginning of eqep\_ex1\_calculation.c and the XLS file provided with the project, eqep\_ex1\_calculation.xls.

### Watch Variables

- **freq.freqHzFR** - Frequency measurement using position counter/unit time out
- **freq.freqHzPR** - Frequency measurement using capture unit

## 4.71 Frequency Measurement Using eQEP via unit timeout interrupt

This example will calculate the frequency of an input signal using the eQEP module. ePWM1A is configured to generate this input signal with a frequency of 5 kHz. EQEP unit timeout is set which



will generate an interrupt every **UNIT\_PERIOD** microseconds and frequency calculation occurs continuously

The configuration for this example is as follows

- PWM frequency is specified as 5000Hz
- UNIT\_PERIOD is specified as 10000 us
- Min frequency is  $(1/(2*10\text{ms}))$  i.e 50Hz
- Highest frequency can be  $(2^{32})/(2*10\text{ms})$
- Resolution of frequency measurement is 50hz

**freq** : Frequency Measurement is obtained by counting the external input pulses for UNIT\_PERIOD (unit timer set to 10 ms).

#### External Connections

- Connect GPIO25/eQEP1A to GPIO0/ePWM1A

#### Watch Variables

- **freq** - Frequency measurement using position counter/unit time out
- **pass** - If measured frequency matches with PWM frequency then pass = 1 else 0

## 4.72 Motor speed and direction measurement using eQEP via unit timeout interrupt

This example can be used to sense the speed and direction of motor using eQEP in quadrature encoder mode. ePWM1A is configured to simulate motor encoder signals with frequency of 5 kHz on both A and B pins with 90 degree phase shift (so as to run this example without motor). EQEP unit timeout is set which will generate an interrupt every **UNIT\_PERIOD** microseconds and speed calculation occurs continuously based on the direction of motor

The configuration for this example is as follows

- PWM frequency is specified as 5000Hz
- UNIT\_PERIOD is specified as 10000 us
- Simulated quadrature signal frequency is 20000Hz ( $4 * 5000$ )
- Encoder holes assumed as 1000
- Thus Simulated motor speed is 300rpm ( $5000 * (60 / 1000)$ )

**freq** : Simulated quadrature signal frequency measured by counting the external input pulses for UNIT\_PERIOD (unit timer set to 10 ms). **speed** : Measure motor speed in rpm **dir** : Indicates clockwise (1) or anticlockwise (-1)

#### External Connections (if motor encoder signals are simulated by ePWM)

- Connect GPIO20/eQEP1A to GPIO0/ePWM1A
- Connect GPIO21/eQEP1B to GPIO1/ePWM1B With motor
- Comment in "MOTOR" in includes

- Connect GPIO25/eQEP1A to encoder A output
- Connect GPIO29/eQEP1B to encoder B output

#### Watch Variables

- **freq** : Simulated motor frequency measurement is obtained by counting the external input pulses for UNIT\_PERIOD (unit timer set to 10 ms).
- **speed** : Measure motor speed in rpm
- **dir** : Indicates clockwise (1) or anticlockwise (-1)
- **pass** - If measured quadrature frequency matches with i.e. input quadrature frequency (4 \* PWM frequency) then pass = 1 else fail = 1 (\*\* only when "MOTOR" is commented out)

## 4.73 ERAD CTM Max Load Profile Function

This example uses HWBP1, HWBP2 and COUNTER1 of the ERAD module to profile a function. Two dummy variable are written to inside the function (delayFunction), startCounts and endCounts. The writes to these variables trigger HWBP1 and HWBP2 respectively. The COUNTER1 module is setup to operate in START-STOP mode and count the number of CPU cycles elapsed between the the two HWBPs. Additionally the same routine is called numerous times with a parameter sent to the routine, which creates the function to run for longer/shorter(A simple delay) Finally the maximum time consumed by that routine across iterations can be simply known by reading the MAX COUNT register which keeps track of the maximum time consumed between any of the START and STOP events

#### Watch Variables

- numberOfCPUCycles1 - the number of cpu cycles after Test-1 is complete
- numberOfCPUCycles2 - the number of cpu cycles after Test-2 is complete
- numberOfCPUCycles3 - the number of cpu cycles after Test-3 is complete

#### External Connections

None

## 4.74 ERAD HWBP Stack Threshold Detection

This example uses HWBP1 to monitor the STACK. The HWBP is set to monitor the data write access bus and interrupt the CPU when an access is detected to a set threshold on the Stack, so user can take a decision of further actions

#### Watch Variables

- functionCallCount - the number of times the recursive function attempting to overflow the STACK is called.
- StackThresholdReached - Variable indicating the Set Threshold on stack has reached

#### External Connections

None

## 4.75 ERAD Profile Function

This example contains a basic FIR calculation and sorting algorithm to help demonstrate the function profiling capability of the ERAD peripheral. A number of FIR sums are calculated within a loop and are then sorted using the insertion sort algorithm. Cycle counts of both the FIR calculations and the sorting algorithm are output to the screen through the scripting console. In this example, it can be seen that sorting the data takes up a majority of the CPU cycles executed in this program.

To properly use the provided ERAD script, the following variables must be set in the scripting environment prior to launching the ERAD script:

- `var PROJ_NAME = "erad_ex2_profilefunction"`
- `var PROJ_WKSPC_LOC = "<proj_workspace_path>"`
- `var PROJ_CONFIG = "<name of active configuration [CPU1_FLASH|CPU1_RAM]>"`

To run the ERAD script, use the following command in the scripting console:

- `loadJSFile("<proj_workspace_path>\\erad_ex2_profilefunction\\profile_function.js", 0);`

Note that the script must be run after loading and running the .out on the C28x core.

The included JavaScript file, `profile_function.js`, uses Debug Server Scripting (DSS) features. For information on using the DSS, please visit: [http://software-dl.ti.com/ccs/esd/documents/users\\_guide/sdto\\_dss\\_handbook.html](http://software-dl.ti.com/ccs/esd/documents/users_guide/sdto_dss_handbook.html)

This example uses 4 HW breakpoints and 2 counters:

- `HWBP_1` : PC = start address of `performFIR`
- `HWBP_2` : PC = end address of `performFIR`
- `HWBP_3` : PC = start address of `sortMax`
- `HWBP_4` : PC = end address of `sortMax`
- `CTM_1` : Used to count the `performFIR` execution cycles. Configured in start-stop mode with start event as `HWBP_1` and stop event as `HWBP_2`
- `CTM_2` : Used to count the `sortMax` execution cycles. Configured in start-stop mode with start event as `HWBP_3` and stop event as `HWBP_4`

### External Connections

- None.

### Watch Variables

- `FIR_iterationCounter` - A counter for the number of times FIR calculation and sorting was performed

### Profiling Script Output

- Current FIR cycle count (`CTM_1`)
- Max FIR cycle count (maximum value of `CTM_1`)
- Current sorting function cycle count (`CTM_2`)
- Max sorting function cycle count (maximum value of `CTM_2`)

Note that the the counters are reset after the stop event. The counter value remains 0 till the next start event occurs. The javascript continuously reads the counter value in a while(1) and hence the current counter may return 0.

## 4.76 ERAD Profiling Interrupts

This example configures CPU Timer0, 1, and 2 to be profiled using the ERAD module. Included is a JavaScript file, `profile_interrupts.js`, which is used with the scripting console to program ERAD registers and view profiling data.

To properly use the provided ERAD script, the following variables must be set in the scripting environment prior to launching the ERAD script:

- `var PROJ_NAME = "erad_ex1_profileinterrupts"`
- `var PROJ_WKSPC_LOC = "<proj_workspace_path>"`
- `var PROJ_CONFIG = "<name of active configuration [CPU1_FLASH|CPU1_RAM]>"`

To run the ERAD script, use the following command in the scripting console:

- `loadJSFile("<proj_workspace_path>\\erad_ex1_profileinterrupts\\profile_interrupts.js", 0);`

The included JavaScript file, `profile_interrupts.js`, uses Debug Server Scripting (DSS) features. For information on using the DSS, please visit: [http://software-dl.ti.com/ccs/esd/documents/users\\_guide/sdto\\_dss\\_handbook.html](http://software-dl.ti.com/ccs/esd/documents/users_guide/sdto_dss_handbook.html)

Note that the script must be run after loading and running the .out on the C28x core. Only CPU timer 2 ISR is profiled in this example.

This example uses 2 HW breakpoints and 4 counters:

- `HWBP_1` : PC = start address of `cpuTimer2ISR`
- `HWBP_2` : PC = end address of `cpuTimer2ISR`
- `CTM_1` : Used to count the `cpuTimer2ISR` execution cycles. Configured in start-stop mode with start event as `HWBP_1` and stop event as `HWBP_2`
- `CTM_2` : Used to count the number of times the system event `TIMER2_TINT2` has occurred. Configured in rising-edge count mode with counting input as system event `TIMER2_TINT2` (`INP_SEL[25]`)
- `CTM_3` : Used to count the number of times `cpuTimer2ISR` executes. Configured in rising-edge count mode with counting input as `HWBP_1` (`INP_SEL[0]`)
- `CTM_4` : Used to count the latency from the system event `TIMER2_TINT2` to `cpuTimer2ISR` entry. Configured in start-stop mode with start event as `TIMER2_TINT2` and stop event as `HWBP_1`

### External Connections

- None

### Watch Variables

- `cpuTimer0IntCount`

- cpuTimer1IntCount
- cpuTimer2IntCount

#### Profiling Script Output

- Current ISR cycle count (CTM\_1)
- Max ISR cycle count (maximum value of CTM\_1)
- Interrupt occurrence count (CTM\_2)
- ISR execution count (CTM\_3)
- ISR entry delay cycle count (maximum value of CTM\_4)

Note that the large difference between Interrupt occurrence count (CTM\_2) and ISR execution count (CTM\_3) is because the ISR takes more number of cycles than the actual interrupt period. ISR entry delay cycle count will also be higher due to the same reason.

## 4.77 ERAD Stack Overflow

This example shows the basic setup of CAN in order to transmit and receive messages on the CAN bus. The CAN peripheral is configured to transmit messages with a specific CAN ID. A message is then transmitted once per second, using a simple delay loop for timing. The message that is sent is a 2 byte message that contains an incrementing pattern.

This example sets up the CAN controller in External Loopback test mode. Data transmitted is visible on the CANTXA pin and is received internally back to the CAN Core.

A buffer is created to store message history up to 50 messages for the duration of the program. A logic error is intentionally made to allow the buffer to overflow, eventually causing a stack overflow. The included JavaScript file, `stack_overflow.js`, programs ERAD registers in order to detect the stack overflow and halt the CPU once the illegal write is made. The illegal write is made after 507 messages are received.

To properly use the provided ERAD script, the following variables must be set in the scripting environment prior to launching the ERAD script:

- `var PROJ_NAME = "erad_ex3_stackoverflow"`
- `var PROJ_WKSPC_LOC = <proj_workspace_path>`

To run the ERAD script, use the following command in the scripting console:

- `loadJSFile("<proj_workspace_path>\\erad_ex3_stackoverflow\\stack_overflow.js", 0);`

Note that the script must be run after loading and running the .out on the C28x core.

The included JavaScript file, `stack_overflow.js`, uses Debug Server Scripting (DSS) features. For information on using the DSS, please visit: [http://software-dl.ti.com/ccs/esd/documents/users\\_guide/sdto\\_dss\\_handbook.html](http://software-dl.ti.com/ccs/esd/documents/users_guide/sdto_dss_handbook.html)

This example uses 1 HW watchpoint :

- `HWBP_1 : Data Write Address Bus = Stack end address + 1`

#### External Connections

- None.

#### Watch Variables

- msgCount - A counter for the number of successful messages received
- txMsgData - An array with the data being sent
- rxMsgData - An array with the data that was received
- msgHistoryBuff - An array meant to store the last 50 messages received

#### Profiling Script Output

- "STACK OVERFLOW detected. Halting CPU." will be printed in the scripting console when a stack overflow occurs (that is, when the watchpoint is hit)

## 4.78 ERAD Profile Function

This example uses BUSCOMP1, BUSCOMP2 and COUNTER1 of the ERAD module to profile a function (delayFunction). It calculates the CPU cycles taken between the the start address of the function to the end address of the function

Two dummy variable are written to inside the function - startCount and endCount. BUSCOMP3, BUSCOMP4 and COUNTER2 are used to profile the time taken between the access to startCount variable till the access to endCount variable.

Both the counters are setup to operate in START-STOP mode and count the number of CPU cycles spend between the respective bus comparator events.

#### Watch Variables

- cycles\_Functio - the maximum number of cycles between the start of function to the end of function
- cycles\_Data - the maximum number of cycles taken between accessing startCount variable to endCount variable

#### External Connections

None

## 4.79 ERAD HWBP Monitor Program Counter

In this example, the function delayFunction is called multiple times. The function does read and writes to the global variables startCount and endCount.

The BUSCOMP1 and COUNTER1 is used to count the number of times the function delayFunction was invoked. BUSCOMP2 is used to generate an interrupt when there is read access to the start-Count variable and BUSCOMP3 is used to generate an interrupt when there is a write access to the endCount variable

#### Watch Variables

- funcCount - number of times the function delayFunction was invoked
- isrCount - number of times the ISR was invoked

**External Connections**

- None

## 4.80 ERAD HWBP Stack Overflow Detection

This example uses BUSCOMP1 to monitor the stack. The Bus comparator is set to monitor the data write access bus and generate an RTOS interrupt CPU when a write is detected to end of the STACK within a threshold.

**Watch Variables**

- functionCallCount - the number of times the recursive function overflowing the STACK is called.
- x indicates that the ISR has been entered

**External Connections**

None

## 4.81 ERAD Profiling Interrupts

This example shows how an ISR can be profiled by ERAD. The CPU timer generates interrupts periodically. We set up the counters to count the CPU cycles elapsed while executing the ISR, to count the number of interrupts, the number of ISR executions and the CPU cycles elapsed between the interrupt and the execution of the ISR.

This example uses 2 bus comparators and 4 counters:

- BUSCOMP\_1 : PC = start address of cpuTimer1ISR
- BUSCOMP\_2 : PC = address of cpuTimer1IntCount variable access. This specifies the end address of the code of interest.
- COUNTER\_1 : Used to count the cpuTimer1ISR execution cycles. Configured in start-stop mode with start event as BUSCOMP\_1 and stop event as BUSCOMP\_2
- COUNTER\_2 : Used to count the number of times the system event TIMER1\_TINT1 has occurred. Configured in rising-edge count mode with counting input as system event TIMER1\_TINT1
- COUNTER\_3 : Used to count the number of times cputimer2ISR executes. Configured in rising-edge count mode with counting input as BUSCOMP\_1
- COUNTER\_4 : Used to count the latency from the system event TIMER1\_TINT1 to cpuTimer1ISR entry. Configured in start-stop mode with start event as TIMER1\_TINT1 and stop event as BUSCOMP\_1

We configure the COUNTER1 to generate an interrupt once it reaches a threshold value.

**External Connections**

- None

#### Profiling Output

- Current ISR cycle count (COUNTER\_1)
- Interrupt occurrence count (COUNTER\_2)
- ISR execution count (COUNTER\_3)
- ISR entry delay cycle count (maximum value of COUNTER\_4)
- x - To show that the ISR executed

FILE: erad\_ex5\_restricted\_write\_detect.c

TITLE: erad\_ex5\_restrictedwrite\_detect

## 4.82 ERAD MEMORY ACCESS RESTRICT

This example uses BUSCOMP1 to monitor the Data Write Address Bus. It monitors the bus and generates an RTOS interrupt if a certain region of memory is accessed by the PC. The user may disable the Bus Comparator to access that region.

Use the COM port (Baud=9600) to try to write to the restricted area.

#### Watch Variables

- x : stores the number of times the region of memory is accessed

#### External Connections

- None

#####

FILE: erad\_ex6\_interrupt\_order.c

TITLE: ERAD INTERRUPT ORDER

## 4.83 ERAD INTERRUPT ORDER

This example uses a COUNTER to monitor the sequence of ISRs executed. An interrupt is generated if the ISRs executed are not in the expected order. The expected order is CPUTimer0 ,then CPUTimer1 and then CPUTimer2

The counter is configured in Start-Stop Mode to count the number of times CPUTimer interrupt occurs between the CPUTimer1 interrupt and CPUTimer2 ISRs. Ideally, this count should be zero if the interrupts are occurring in the expected order. we configure a threshold value of 1 to generate an RTOS interrupt. This indicates that the CPUTimer2 interrupt has come out of order.

For demonstration purposes, this example disables CPUTimer1 to simulate this error.

#### Watch Variables



- cpuTimer0IntCount: Number of executions of ISR0
- cpuTimer1IntCount: Number of executions of ISR1
- cpuTimer2IntCount: Number of executions of ISR2

**External Connections**

- None

## 4.84 ERAD AND CLB

This example uses 4 BUS COMPARATORS of ERAD along with the CLB. One bus comparator monitors a write to x, another one monitors a write to y. The other two monitor a write of 0x1 and 0x0. By using the LUTs in the CLB1 tile, we can monitor a write of 0x1 to x or 0x0 to x. These are used to change the state of FSM2 in the CLB1 tile. If y is accessed before writing a 0x1 to x, an interrupt is generated and y is changed to 0x0 again. The LED2 indicates when access to y is allowed(it is off at this point) The LED1 indicates if an invalid access is attempted. A COUNTER in ERAD is used to count the number of access attempts to y.

**Watch Variables**

- y
- x
- a - counts the number of access attempts to y

**External Connections**

None

## 4.85 ERAD PWM PROTECTION

This example uses a BUS COMPARATOR and the CLB to detect the event when the delay between the interrupt and the ISR execution is longer than expected. The PWM output is also tripped in this case.

**Watch Variables**

- adcAResults stores the results of the conversions from the ADC

**External Connections**

- Monitor the PWM output (GPIO0)

## 4.86 Flash Programming with AutoECC, DataAndECC, DataOnly and EccOnly

This example demonstrates how to program Flash using API's following options 1. AutoEcc generation 2. DataOnly and EccOnly 3. DataAndECC

**External Connections**

- None.

**Watch Variables**

- None.

## 4.87 FSI Loopback:CPU Control

Example sets up infinite data frame transfers where trigger happens through **CPU**. Automatic(Hw triggered) Ping frame transmission is also setup along with data.

User can edit some of configuration parameters as per usecase. These are as below. Default values can be referred in code where these globals are defined

- **nWords** - Number of words per transfer may be from 1 -16
- **nLanes** - Choice to select single or double lane for frame transfers
- **fsiClock** - FSI Clock used for transfers
- **txUserData** - User data to be sent with Data frame
- **txDataFrameTag** - Frame tag used for Data transfers
- **txPingFrameTag** - Frame tag used for Ping transfers
- **txPingTimeRefCntr** - Tx Ping timer reference counter
- **rxWdTimeoutRefCntr** - Rx Watchdog timeout reference counter

For any errors during transfers i.e. **error** events such as Frame Overrun, Underrun, Watchdog timeout and CRC/EOF/TYPE errors, execution will stop immediately and status variables can be looked into for more details. Execution will also stop for any mismatch between received data and sent ones and also if transfers takes unusually long time(detected through software counters - txTimeOutCntr and rxTimeOutCntr)

**External Connections**

For FSI internal loopback (`EXTERNAL_FSI_ENABLE == 0`), no external connections needed

For FSI external loopback (`EXTERNAL_FSI_ENABLE == 1`), external connections are required. The FSI TX pins should be connected to the FSI RX pins of the same device. See below for external connections to include and GPIOs used:

External Connections Required between FSI TX and RX of the same device:

- FSIRX\_CLK to FSITX\_CLK
- FSIRX\_RX0 to FSITX\_TX0
- FSIRX\_RX1 to FSITX\_TX1

ControlCard FSI Header GPIOs:

- GPIO\_27 -> FSITX\_CLK
- GPIO\_26 -> FSITX\_TX0
- GPIO\_25 -> FSITX\_TX1

- GPIO\_13 -> FSIRX\_CLK
- GPIO\_12 -> FSIRX\_RX0
- GPIO\_11 -> FSIRX\_RX1

**Watch Variables**

- **dataFrameCnt** Number of Data frame transfered
- **error** Non zero for transmit/receive data mismatch

## 4.88 FSI DMA frame transfers:DMA Control

Example sets up infinite data frame transfers where DMA trigger happens once through CPU and then DMA takes control to transfer data iteratively. This example demonstrates the FSI feature about triggering DMA events which in turn can copy data and trigger next transfer.

Two DMA channels are setup for FSI Tx operation and two for Rx. Four areas in GS0 memories are also setup as source and sink for data and tag values of frame under transmission.

Automatic(Hw triggered) Ping frame transmission is also setup along with data.

If there are any comparison failures during transfers or any of error event occurs, execution will stop.

**External Connections**

For FSI internal loopback (EXTERNAL\_FSI\_ENABLE == 0), no external connections needed

For FSI external loopback (EXTERNAL\_FSI\_ENABLE == 1), external connections are required. The FSI TX pins should be connected to the FSI RX pins of the same device. See below for external connections to include and GPIOs used:

External Connections Required between FSI TX and RX of the same device:

- FSIRX\_CLK to FSITX\_CLK
- FSIRX\_RX0 to FSITX\_TX0
- FSIRX\_RX1 to FSITX\_TX1

ControlCard FSI Header GPIOs:

- GPIO\_27 -> FSITX\_CLK
- GPIO\_26 -> FSITX\_TX0
- GPIO\_25 -> FSITX\_TX1
- GPIO\_13 -> FSIRX\_CLK
- GPIO\_12 -> FSIRX\_RX0
- GPIO\_11 -> FSIRX\_RX1

**Watch Variables**

- **countDMAtransfers** Number of Data frame transfered
- **error** Non zero for transmit/receive data mismatch

## 4.89 FSI data transfer by external trigger

FSI frame transfer can be triggered by external sources. It can connect up to 32 trigger sources but as of now, only 16 ePWMx-SOCy(x-1:8, y-A:B) are supported. FSI supports external trigger for both PING and DATA frame transfers and in this example we demonstrate how to setup infinite DATA transfers using selectable ePWM-SOC as a trigger source. The TB counter for ePWM operation is in up/down count mode for this example.

Automatic(Hw triggered) Ping frame transmission is also setup along with data.

If there are any comparison failures during transfers or any of error event occurs, execution will stop.

### External Connections

For FSI internal loopback, no external connections needed

### Watch Variables

- **dataFrameCnt** Number of Data frame transfered
- **error** Non zero for transmit/receive data mismatch

## 4.90 FSI data transfers upon CPU Timer event

Example sets up infinite data frame transfers where trigger comes from ISR handling the periodic CPU Timer event. Automatic(Hw triggered) Ping frame transmission is also setup along with data.

CPU Timer0 is chosen for setting up periodic timer events. User can choose any other Timer-1/Timer-2 as well.

Automatic(Hw triggered) Ping frame transmission is also setup along with data.

If there are any comparison failures during transfers or any of error event occurs, execution will stop.

### External Connections

For FSI internal loopback (EXTERNAL\_FSI\_ENABLE == 0), no external connections needed

For FSI external loopback (EXTERNAL\_FSI\_ENABLE == 1), external connections are required. The FSI TX pins should be connected to the respective FSI RX pins of the same device. See below for external connections to include and GPIOs used:

External Connections Required between FSI TX and RX of the same device:

- FSIRX\_CLK to FSITX\_CLK
- FSIRX\_RX0 to FSITX\_TX0
- FSIRX\_RX1 to FSITX\_TX1

ControlCard FSI Header GPIOs:

- GPIO\_27 -> FSITX\_CLK
- GPIO\_26 -> FSITX\_TX0
- GPIO\_25 -> FSITX\_TX1

- GPIO\_13 -> FSIRX\_CLK
- GPIO\_12 -> FSIRX\_RX0
- GPIO\_11 -> FSIRX\_RX1

**Watch Variables**

- **dataFrameCntr** Number of Data frame transfered
- **error** Non zero for transmit/receive data mismatch

## 4.91 FSI and SPI communication(fsi\_ex6\_spi\_master\_tx)

FSI supports SPI compatibility mode to talk to the devices not having FSI but SPI module. Example sets up infinite data frame transfers where FSI acts like master Tx and SPI as slave Rx. API to decode FSI frame received at SPI end is implemented and checks are made to ensure received details(frame tag/type, userdata, data) match with transfered frame.

If there are any comparison failures during transfers or any of error event occurs, execution will stop.

**External Connections**

For FSI <-> SPI communication, make below connections in GPIO settings

- GPIO\_27 -> GPIO\_3 :: To connect FSITX\_CLK with SPICLK\_A
- GPIO\_26 -> GPIO\_2 :: To connect FSITX\_TX0 with SPISIMO\_A
- GPIO\_25 -> GPIO\_0 :: To connect FSITX\_TX1 with SPISTEA

**Watch Variables**

- **dataFrameCntr** Number of Data frame transfered
- **error** Non zero for transmit/receive data mismatch

## 4.92 FSI and SPI communication(fsi\_ex7\_spi\_slave\_rx)

FSI supports SPI compatibility mode to talk to the devices not having FSI but SPI module. Example sets up infinite data frame transfers where FSI acts like slave Rx and SPI as master Rx. API to build the FSI frame at SPI end before transfer is implemented in SW and checks are made to ensure received details(frame tag/type, userdata, data) on FSI Rx match with transferred data.

If there are any comparison failures during transfers or any of error event occurs, execution will stop.

**External Connections**

For FSI(Rx) <-> SPI(Tx) communication, make connections in GPIO settings

There is no requirement for a chip select signal to be used when connected to the FSIRX. This is because the FSIRX will respond to any incoming clock edge.

- GPIO\_13 -> GPIO\_3 :: To connect FSIRXCLK with SPICLK\_A

- **GPIO\_12** -> **GPIO\_2** :: To connect FSIRX0 with SPISIMOA

#### Watch Variables

- **dataFrameCntr** Number of Data frame transfered
- **error** Non zero for transmit/receive data mismatch

## 4.93 FSI P2Point Connection:Rx Side

Example sets up FSI receiving device in a point to point connection to the FSI transmitting device. Example code to set up FSI transmit device is implemented in a separate file.

In a real scenario two separate devices may power up in arbitrary order and there is a need to establish a clean communication link which ensures that receiver side is flushed to properly interpret the start of a new valid frame.

There is no true concept of a master or a slave node in the FSI protocol, but to simplify the data flow and connection we can consider transmitting device as master and receiving side as slave. Transmitting side will be driver of initialization sequence.

Handshake mechanism which must take place before actual data transmission can be usecase specific; points described below can be taken as an example on how to implement the handshake from receiving side -

- Setup the receiver interrupts to detect PING type frame reception
- Begin the first PING loop + Wait for receiver interrupt + If the FSI Rx has received a PING frame with **FSI\_FRAME\_TAG0**, come out of loop. Otherwise iterate the loop again.
- Begin the second PING loop + Send the Flush sequence + Send the PING frame with tag + Wait for receiver interrupt + If the FSI Rx has received a PING frame with **FSI\_FRAME\_TAG1**, come out of loop. Otherwise iterate the loop again.
  - Now, the receiver side has received the acknowledged PING frame(tag1), so it is ready for normal operation further.

After above synchronization steps, FSI Rx can be configured as per usecase i.e. nWords, lane width, enabling events etc and start the infinite transfers. More details on establishing the communication link can be found in device TRM.

User can edit some of configuration parameters as per usecase, similar to other examples.

**nWords** - Number of words per transfer may be from 1 -16 **nLanes** - Choice to select single or double lane for frame transfers **fsiClock** - FSI Clock used for transfers **txUserData** - User data to be sent with Data frame **txDataFrameTag** - Frame tag used for Data transfers **txPingFrameTag** - Frame tag used for Ping transfers **txPingTimeRefCntr** - Tx Ping timer reference counter **rxWdTimeoutRefCntr** - Rx Watchdog timeout reference counter

#### External Connections

For FSI external P2P connection, external connections are required to be made between two devices. Device 1's FSI TX and RX pins need to be connected to device 2's FSI RX and TX pins respectively. See below for external connections to make and GPIOs used:

External connections required between independent RX and TX devices:

- **FSIRX\_CLK** to **FSITX\_CLK**

- FSIRX\_RX0 to FSITX\_TX0
- FSIRX\_RX1 to FSITX\_TX1

ControlCard FSI Header GPIOs:

- GPIO\_27 -> FSITX\_CLK
- GPIO\_26 -> FSITX\_TX0
- GPIO\_25 -> FSITX\_TX1
- GPIO\_13 -> FSIRX\_CLK
- GPIO\_12 -> FSIRX\_RX0
- GPIO\_11 -> FSIRX\_RX1

#### Watch Variables

- **dataFrameCntr** Number of Data frame received
- **error** Non zero for transmit/receive data mismatch

## 4.94 FSI P2Point Connection:Tx Side

Example sets up FSI transmitting device in a point to point connection to the FSI receiving device. Example code to set up FSI receiving device is implemented in a separate file.

In a real scenario two separate devices may power up in arbitrary order and there is a need to establish a clean communication link which ensures that receiver side is flushed to properly interpret the start of a new valid frame.

There is no true concept of a master or a slave node in the FSI protocol, but to simplify the data flow and connection we can consider transmitting device as master and receiving side as slave. Transmitting side will be driver of initialization sequence.

Handshake mechanism which must take place before actual data transmission can be usecase specific; points described below can be taken as an example on how to implement the handshake from transmitting side -

- Setup the receiver interrupts to detect PING type frame reception
- Begin the PING loop + Send the Flush sequence + Send a PING frame with the frame tag **FSI\_FRAME\_TAG0** + Wait for some time(determined by application) + If the FSI Rx has received a PING frame with **FSI\_FRAME\_TAG1**, come out of loop. Otherwise iterate the loop again
  - Send a PING frame with the frame tag **FSI\_FRAME\_TAG1**

After above synchronization steps, FSI Tx can be configured as per usecase i.e. nWords, lane width, enabling events etc and start the infinite transfers. More details on establishing the communication link can be found in device TRM.

User can edit some of configuration parameters as per usecase, similar to other examples.

**nWords** - Number of words per transfer may be from 1 -16 **nLanes** - Choice to select single or double lane for frame transfers **fsiClock** - FSI Clock used for transfers **txUserData** - User data

to be sent with Data frame **txDataFrameTag** - Frame tag used for Data transfers **txPingFrameTag** - Frame tag used for Ping transfers **txPingTimeRefCntr** - Tx Ping timer reference counter **rxWdTimeoutRefCntr** - Rx Watchdog timeout reference counter

### External Connections

For FSI external P2P connection, external connections are required to be made between two devices. Device 1's FSI TX and RX pins need to be connected to device 2's FSI RX and TX pins respectively. See below for external connections to make and GPIOs used:

External connections required between independent RX and TX devices:

- FSIRX\_CLK to FSITX\_CLK
- FSIRX\_RX0 to FSITX\_TX0
- FSIRX\_RX1 to FSITX\_TX1

ControlCard FSI Header GPIOs:

- GPIO\_27 -> FSITX\_CLK
- GPIO\_26 -> FSITX\_TX0
- GPIO\_25 -> FSITX\_TX1
- GPIO\_13 -> FSIRX\_CLK
- GPIO\_12 -> FSIRX\_RX0
- GPIO\_11 -> FSIRX\_RX1

### Watch Variables

- **dataFrameCntr** Number of Data frame transmitted
- **error** Non zero for transmit/receive data mismatch

## 4.95 Device GPIO Setup

Configures the device GPIO into two different configurations This code is verbose to illustrate how the GPIO could be setup. In a real application, lines of code can be combined for improved code size and efficiency.

This example only sets-up the GPIO. Nothing is actually done with the pins after setup.

**In general:**

- All pullup resistors are enabled. For ePWMs this may not be desired.
- Input qual for communication ports (CAN, SPI, SCI, I2C) is asynchronous
- Input qual for Trip pins (TZ) is asynchronous
- Input qual for eCAP and eQEP signals is synch to SYSCLKOUT
- Input qual for some I/O's and \_\_interrupts may have a sampling window

## 4.96 Device GPIO Toggle

Configures the device GPIO through the sysconfig file. The GPIO pin is toggled in the infinit loop.



## 4.97 Device GPIO Interrupt

Configures the device GPIOs through the sysconfig file. One GPIO output pin, and one GPIO input pin is configured. The example then configures the GPIO input pin to be the source of an external interrupt which toggles the GPIO output pin.

## 4.98 External Interrupt (XINT)

In this example AIO pins are configured as digital inputs. Two other GPIO signals (connected externally to AIO pins) are toggled in software to trigger external interrupt through AIO224 and AIO225 (AIO224 assigned to XINT1 and AIO225 assigned to XINT2). The user is required to externally connect these signals for the program to work properly. Each interrupt is fired in sequence: XINT1 first and then XINT2.

GPIO34 will go high outside of the interrupts and low within the interrupts. This signal can be monitored on a scope.

### External Connections

- Connect GPIO30 to AIO224. AIO224 will be assigned to XINT1
- Connect GPIO31 to AIO225. AIO225 will be assigned to XINT2
- GPIO34 can be monitored on an oscilloscope

### Watch Variables

- xint1Count for the number of times through XINT1 interrupt
- xint2Count for the number of times through XINT2 interrupt
- loopCount for the number of times through the idle loop

## 4.99 HIC 16-bit Memory Access Example

Example sets up Host Interface Controller Module in 16-bit mode the data memory of device is accessed by the **External** Host.

This example is validated on an TI Internal Validation Platform will not run in F28002x Control Card The example initializes the GPIOs for 16 bit Memory access mode with separate Read and Write Control Pins, Extended Wait, and nRDY pin The example demonstrates the following sequences 1. Sending a message to the Host using Device to Host buffer, Passing a token which triggers an interrupt at the Host. 2. Waits for the Host to clear the interrupt. 3. Then waits for a message from Host which contains the code 0x1 in buffer index 0 and index 1 contains the Base address to be configured 4. Configures the base address for Page 0 5. Sends a message to Host after that is configured 6. After this step the external host can use the address 0-0xFF to access the Base address region in System memory

### External Connections

This is tested on TI Internal validation platform hence no connection needed on Control card. This has been tested with F2838x EMIF interface.

**Watch Variables**

None

## 4.100 HIC 8-bit Memory Access Example

Example sets up Host Interface Controller Module in 8-bit mode the data memory of device is accessed by the External Host.

- This follows example configuration for pin constrained applications described in the Application note titled Application guide for peripheral expansion using HIC(SPRACR2). -This example is validated on an TI Internal Validation Platform will not run in F28002x Control Card. This is to be run with a corresponding Host side code emif\_ex8\_8bit\_asram\_hic\_adc is run on F2838x based host first and then this example is run.
- The example initializes the HIC for 8 bit Memory access mode with Single Read and Write Control Pin
- DMA is configured to do transfer of the ADC result from ADCRESULT0-15 to HIC D2H buffer.
- The example configures CPUTIMER0 to generate an event every second on which the ADC SOC0-15 start conversion.
- The timer is enabled on receiving HIC\_START\_TOKEN on the H2D Token from the host.
- The end of ADC\_SOC15 will generate a DMA event
- The DMA ISR signals the host with HIC\_DATA\_TOKEN to signal data write.
- The Host is interrupted with HIC\_INT on ADC End of conversion event
- The DMA Channel is stopped after HIC\_TEST\_NUM\_SAMPLES samples are collected This example can be used as a reference to implement Communication between Host and HIC with minimal number of pins. Please refer to device TRM and application note titled 'Application guide for peripheral expansion using HIC'(SPRACR2) for further details about Host interface Controller applications.

**External Connections**

This is tested on TI Internal validation platform hence no connection needed on Control card. This has been tested with F2838x EMIF interface with emif\_ex8\_8bit\_asram\_hic\_adc example Analog channel A7 has been used as Analog Input to Sample

**Watch Variables**

numDMAInterrupts

## 4.101 HIC 16-bit Memory Access FSI Example

Example sets up Host Interface Controller Module in 16-bit mode the FSI Memory region of device is accessed by the External Host. This follows example configuration for performance critical applications described in the Application note titled "Application guide for peripheral expansion using HIC"(SPRACR2).

emif\_ex7\_16bit\_asram\_hic\_fsi is to be run on the host before running this example on F28002x side.

This example is validated on an TI Internal Validation Platform will not run in F28002x Control Card 1. The example initializes the GPIOs for 16 bit HIC Memory access mode with separate Read and Write Control Pins, Extended Wait, and nRDY pin 2. Configures the base address for Region 0 to access FSI Tx Memory region 3. Sets up the FSI module in Loopback mode 4. The EVTTRIG interface of HIC is enabled to route FSI Rx events to the Host through the HIC\_INT 5. Sending a message to the Host using Device to Host buffer, Passing a token 6. This sets up the FSI direct bridge over HIC. The host can then access the FSI registers over HIC

**External Connections**

This is tested on TI Internal validation platform hence no connection needed on Control card. This has been tested with F2838x EMIF interface.

**Watch Variables**

None - Use the Host to access FSI region

## 4.102 HRCAP Capture and Calibration Example

This example configures ECAP3 to use HRCAP functionality to capture time between edges on input GPIO2.

**External Connections**

The user must provide a signal to GPIO2. XCLKOUT has been configured to GPIO16 and can be externally jumped to serve this purpose.

**Watch Variables**

- onTime1, onTime2
- offTime1, offTime2
- period1, period2

## 4.103 HRPWM Duty Control with SFO

This example modifies the MEP control registers to show edge displacement for high-resolution period with ePWM in Up count mode due to the HRPWM control extension of the respective ePWM module.

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

- updates MEP\_ScaleFactor dynamically when HRPWM is in use
- updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value
- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

#### External Connections

- Monitor ePWM1/2/3/4 A/B pins on an oscilloscope.

## 4.104 HRPWM Slider

This example modifies the MEP control registers to show edge displacement due to HRPWM. Control blocks of the respective ePWM module channel A and B will have fine edge movement due to HRPWM logic.

Monitor ePWM1 A/B pins on an oscilloscope.

## 4.105 HRPWM Period Control

This example modifies the MEP control registers to show edge displacement for high-resolution period with ePWM in Up-Down count mode due to the HRPWM control extension of the respective ePWM module.

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

- updates MEP\_ScaleFactor dynamically when HRPWM is in use
- updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value
- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

#### External Connections

- Monitor ePWM1/2/3/4 A/B pins on an oscilloscope.

## 4.106 HRPWM Duty Control with UPDOWN Mode

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

- updates MEP\_ScaleFactor dynamically when HRPWM is in use
- updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value
- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

#### **External Connections**

- Monitor ePWM1/2/3/4 A/B pins on an oscilloscope.

## **4.107 HRPWM Slider Test**

This example modifies the MEP control registers to show edge displacement due to HRPWM. Control blocks of the respective ePWM module channel A and B will have fine edge movement due to HRPWM logic. Load the f2838x\_hrpwm\_slider.gel file. Select the HRPWM\_eval from the GEL menu. A FineDuty slider graphics will show up in CCS. Load the program and run. Use the Slider to and observe the EPWM edge displacement for each slider step change. This explains the MEP control on the EPwmxA channels.

Monitor ePWM1 & ePWM2 A/B pins on an oscilloscope.

## **4.108 HRPWM Duty Up Count**

This example modifies the MEP control registers to show edge displacement for high-resolution period with ePWM in Up count mode due to the HRPWM control extension of the respective ePWM module.

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

- updates MEP\_ScaleFactor dynamically when HRPWM is in use
- updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value
- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

To run this example:

1. Run this example at maximum SYSCLKOUT
2. Activate Real time mode
3. Run the code

#### External Connections

- Monitor ePWM1/2 A/B pins on an oscilloscope.

#### Watch Variables

- status - Example run status
- updateFine - Set to 1 use HRPWM capabilities and observe in fine MEP steps(default) Set to 0 to disable HRPWM capabilities and observe in coarse SYSCLKOUT cycle steps

## 4.109 HRPWM Period Up-Down Count

This example modifies the MEP control registers to show edge displacement for high-resolution period with ePWM in Up-Down count mode due to the HRPWM control extension of the respective ePWM module.

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

- updates MEP\_ScaleFactor dynamically when HRPWM is in use
- updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value
- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

To run this example:

1. Run this example at maximum SYSCLKOUT
2. Activate Real time mode
3. Run the code

#### External Connections

- Monitor ePWM1/2 A/B pins on an oscilloscope.

**Watch Variables**

- **updateFine** - Set to 1 use HRPWM capabilities and observe in fine MEP steps(default) Set to 0 to disable HRPWM capabilities and observe in coarse SYSCLKOUT cycle steps

## 4.110 I2C Digital Loopback with FIFO Interrupts

This program uses the internal loopback test mode of the I2C module. Both the TX and RX I2C FIFOs and their interrupts are used. The pinmux and I2C initialization is done through the sysconfig file.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

```
0000 0001
0001 0002
0002 0003
....
00FE 00FF
00FF 0000
etc..
```

This pattern is repeated forever.

**External Connections**

- None

**Watch Variables**

- **sData** - Data to send
- **rData** - Received data
- **rDataPoint** - Used to keep track of the last position in the receive stream for error checking

## 4.111 I2C EEPROM

This program will write 1-14 words to EEPROM and read them back. The data written and the EEPROM address written to are contained in the message structure, `i2cMsgOut`. The data read back will be contained in the message structure `i2cMsgIn`.

**External Connections**

- Connect external I2C EEPROM at address 0x50
- Connect `DEVICE_GPIO_PIN_SCIRXDA` on to external EEPROM SDA (serial data) pin
- Connect `DEVICE_GPIO_PIN_SCITXDA` on to external EEPROM SCL (serial clock) pin

**Watch Variables**

- **i2cMsgOut** - Message containing data to write to EEPROM
- **i2cMsgIn** - Message containing data read from EEPROM

## 4.112 I2C Digital External Loopback with FIFO Interrupts

This program uses the I2CA and I2CB modules for achieving external loopback. The I2CA TX FIFO and the I2CB RX FIFO are used along with their interrupts.

A stream of data is sent on I2CA and then compared to the received stream on I2CB. The sent data looks like this:

```
0000 0001
0001 0002
0002 0003
....
00FE 00FF
00FF 0000
etc..
```

This pattern is repeated forever.

**External Connections**

- Connect SCLA(GPIO43) to SCLB (GPIO3) and SDAA(GPIO42) to SDAB (GPIO2)
- Connect GPIO31 to an LED used to depict data transfers.

**Watch Variables**

- **sData** - Data to send
- **rData** - Received data
- **rDataPoint** - Used to keep track of the last position in the receive stream for error checking

## 4.113 I2C EEPROM

This program will shows how to perform different EEPROM write and read commands using I2C polling method EEPROM used for this example is AT24C256

**External Connections**

- Connect external I2C EEPROM at address 0x50 ————— Signal | I2CA | EEPROM ————— SCL | GPIO43 | SCL SDA | GPIO26 | SDA Make sure to connect GND pins if EEPROM and C2000 device are in different board. —————



## 4.114 I2C master slave communication using FIFO interrupts

This program shows how to use I2CA and I2CB modules in both master and slave configuration. This example uses I2C FIFO interrupts and doesn't use polling.

Example1: I2CA as Master Transmitter and I2CB working Slave Receiver  
 Example2: I2CA as Master Receiver and I2CB working Slave Transmitter  
 Example3: I2CB as Master Transmitter and I2CA working Slave Receiver  
 Example4: I2CB as Master Receiver and I2CA working Slave Transmitter

**External Connections** on launchpad should be made as shown below

Signal | I2CA | I2CB | SCL | GPIO43 | GPIO3 SDA  
 | GPIO26 | GPIO2

**Watch Variables** in memory window

- I2CA\_TXdata
- I2CA\_RXdata
- I2CB\_TXdata
- I2CB\_RXdata stream for error checking

#####

## 4.115 I2C EEPROM

This program will show how to perform different EEPROM write and read commands using I2C interrupts. The EEPROM used for this example is AT24C256.

**External Connections**

- Connect external I2C EEPROM at address 0x50 | Signal | I2CA | EEPROM | SCL | GPIO43 | SCL SDA | GPIO26 | SDA. Make sure to connect GND pins if EEPROM and C2000 device are in different board.
- Example 1: EEPROM Byte Write Example 2: EEPROM Byte Read Example 3: EEPROM word (16-bit) write Example 4: EEPROM word (16-bit) read Example 5: EEPROM Page write Example 6: EEPROM word Paged read

**Watch Variables**

- TX\_MsgBuffer - Message buffer which stores the data to be transmitted
- RX\_MsgBuffer - Message buffer which stores the data to be received

#####

## 4.116 External Interrupts (ExternalInterrupt)

This program sets up GPIO0 as XINT1 and GPIO1 as XINT2. Two other GPIO signals are used to trigger the interrupt (GPIO30 triggers XINT1 and GPIO31 triggers XINT2). The user is required to

externally connect these signals for the program to work properly.

XINT1 input is synced to SYSCLKOUT.

XINT2 has a long qualification - 6 samples at 510\*SYSCLKOUT each.

GPIO34 will go high outside of the interrupts and low within the interrupts. This signal can be monitored on a scope.

Each interrupt is fired in sequence - XINT1 first and then XINT2

#### External Connections

- Connect GPIO30 to GPIO0. GPIO0 will be assigned to XINT1
- Connect GPIO31 to GPIO1. GPIO1 will be assigned to XINT2

Monitor GPIO34 with an oscilloscope. GPIO34 will be high outside of the ISRs and low within each ISR.

#### Watch Variables

- XINT1Count for the number of times through XINT1 interrupt
- XINT2Count for the number of times through XINT2 interrupt
- loopCount for the number of times through the idle loop

## 4.117 CPU Timer Interrupt Software Prioritization

This examples demonstrates the software prioritization of interrupts through CPU Timer Interrupts. Software prioritization of interrupts is achieved by enabling interrupt nesting.

In this device, hardware priorities for CPU Timer 0, 1 and 2 are set as timer 0 being highest priority and timer 2 being lowest priority. This example configures CPU Timer0, 1, and 2 priority in software with timer 2 priority being highest and timer 0 being lowest in software and prints a trace for the order of execution.

For most applications, the hardware prioritizing of the interrupts is sufficient. For applications that need custom prioritizing, this example illustrates how this can be done through software. User specific priorities can be configured in `sw_prioritized_isr_level.h` header file.

To enable interrupt nesting, following sequence needs to followed in ISRs. **Step 1:** Set the global priority: Modify the IER register to allow CPU interrupts with a higher user priority to be serviced. Note: at this time IER has already been saved on the stack. **Step 2:** Set the group priority: (optional) Modify the appropriate PIEIERx register to allow group interrupts with a higher user set priority to be serviced. Do NOT clear PIEIER register bits from another group other than that being serviced by this ISR. Doing so can cause erroneous interrupts to occur. **Step 3:** Enable interrupts: There are three steps to do this: a. Clear the PIEACK bits b. Wait at least one cycle c. Clear the INTM bit. **Step 4:** Run the main part of the ISR **Step 5:** Set INTM to disable interrupts. **Step 6:** Restore PIEIERx (optional depending on step 2) **Step 7:** Return from ISR

Refer to below link on more details on Interrupt nesting in C28x devices: [C2000Ware>.html](http://www.ti.com/lit/zip/c2000ware)

#### External Connections

- None

**Watch Variables**

- `tracelSR` - shows the order in which ISRs are executed.

## 4.118 Multiple interrupt handling of I2C, SCI & SPI Digital Loopback

This program is used to demonstrate how to handle multiple interrupts when using multiple communication peripherals like I2C, SCI & SPI Digital Loopback all in a single example. The data transfers would be done with FIFO Interrupts.

It uses the internal loopback test mode of these modules. Both the TX and RX FIFOs and their interrupts are used. Other than boot mode pin configuration, no other hardware configuration is required.

A stream of data is sent and then compared to the received stream. The sent data looks like this for I2C and SCI:

```
0000 0001
0001 0002
0002 0003
....
00FE 00FF
00FF 0000
etc..
```

The sent data looks like this for SPI:

```
0000 0001
0001 0002
0002 0003
....
FFFE FFFF
FFFF 0000
etc..
```

This pattern is repeated forever.

**External Connections**

- None

**Watch Variables**

- `sDataI2cA` - Data to send through I2C
- `rDataI2cA` - Received I2C data
- `rDataPoint` - Used to keep track of the last position in the receive I2C stream for error checking

- **sDataSpiA** - Data to send through SPI
- **rDataSpiA** - Received SPI data
- **rDataPointSpiA** - Used to keep track of the last position in the receive SPI stream for error checking
- **sDataSciA** - SCI Data being sent
- **rDataSciA** - SCI Data received
- **rDataPointA** - Keep track of where we are in the SCI data stream. This is used to check the incoming data

## 4.119 F280025C LaunchPad Out of Box Demo Example

This program is the demo program that comes pre-loaded on the F280025C LaunchPad development kit. The program starts by flashing the two user LEDs. After a few seconds the LEDs stop flashing and the device starts sampling ADCINA6 once a second. If the sample is greater than midscale the red LED on the board is lit, while if it is lower the green LED is lit. Sample data is also displayed in a serial terminal via the board's back channel UART. You may view this data by configuring a serial terminal to the correct COM port at 115200 Baud 8-N-1.

### External Connections

- Connect to COM port at 115200 Baud 8-N-1 for serial data
- Connect signal to ADCINA6 to change LED based on value

### Watch Variables

- None.

## 4.120 LED Blinky Example

This example demonstrates how to blink a LED.

### External Connections

- None.

### Watch Variables

- None.

## 4.121 LED Blinky Example with DCSM

This example demonstrates how to blink a LED and program the DCSM OTP.

### External Connections

- None.

**Watch Variables**

- None.

## 4.122 LIN Internal Loopback with Interrupts

This example configures the LIN module in master mode for internal loopback with interrupts. The module is setup to perform 8 data transmissions with different transmit IDs and varying transmit data. Upon reception of an ID header, an interrupt is triggered on line 0 and an interrupt service routine (ISR) is called. The received data is then checked for accuracy.

**Note:**

The example can be adjusted to use interrupt line 1 instead of line 0 by un-commenting "LIN\_setInterruptLevel1()"

**External Connections**

- None.

**Watch Variables**

- txData - An array with the data being sent
- rxData - An array with the data that was received
- result - The example completion status (PASS = 0xABCD, FAIL = 0xFFFF)
- level0Count - The number of line 0 interrupts
- level1Count - The number of line 1 interrupts

## 4.123 LIN SCI Mode Internal Loopback with Interrupts

This example configures the LIN module in SCI mode for internal loopback with interrupts. The LIN module performs as a SCI with a set character and frame length in a non-multi-buffer mode. The module is setup to continuously transmit a character, wait to receive that character, and repeat.

**External Connections**

- None.

**Watch Variables**

- rxCount - The number of RX interrupts
- transmitChar - The character being transmitted
- receivedChar - The character received

## 4.124 LIN SCI MODE Internal Loopback with DMA

This example configures the LIN module in SCI mode for internal loopback with the use of the DMA. The LIN module performs as SCI with a set character and frame length in multi-buffer mode. When the transmit buffers in the LINTD0 and LINTD1 registers have enough space, the DMA will transfer data from global variable sData into those transmit registers. Once the received buffers in the LINRD0 and LINRD1 registers contain data, the DMA will transfer the data into the global variable rdata.

When all data has been placed into rData, a check of the validity of the data will be performed in one of the DMA channels' ISRs.

### External Connections

- None

### Watch Variables

- **sData** - Data to send
- **rData** - Received data

## 4.125 LIN Internal Loopback without interrupts(polled mode)

This example configures the LIN module in master mode for internal loopback with interrupts. The module is setup to perform 8 data transmissions with different transmit IDs and varying transmit data. Waits for reception of an ID header. The received data is then checked for accuracy.

### External Connections

- None.

### Watch Variables

- txData - An array with the data being sent
- rxData - An array with the data that was received
- result - The example completion status (PASS = 0xABCD, FAIL = 0xFFFF)

## 4.126 Low Power Modes: Device Idle Mode and Wakeup using GPIO

This example puts the device into IDLE mode and then wakes up the device from IDLE using XINT1 which triggers on a falling edge of GPIO0.

The GPIO0 pin must be pulled from high to low by an external agent for wakeup. GPIO0 is configured as an XINT1 pin to trigger an XINT1 interrupt upon detection of a falling edge.

Initially, pull GPIO0 high externally. To wake device from IDLE mode by triggering an XINT1 interrupt, pull GPIO0 low (falling edge). The wakeup process begins as soon as GPIO0 is held low for the time indicated in the device datasheet.

GPIO1 is pulled high before entering the IDLE mode and is pulled low when in the external interrupt ISR.

#### **External Connections**

- GPIO0 needs to be pulled low to wake up the device.
- On device wakeup, the GPIO1 will be low and LED1 will start blinking

## **4.127 Low Power Modes: Device Standby Mode and Wakeup using GPIO**

This example puts the device into STANDBY mode. If the lowest possible current consumption in STANDBY mode is desired, the JTAG connector must be removed from the device board while the device is in STANDBY mode.

This example puts the device into STANDBY mode and then wakes up the device from STANDBY using an LPM wakeup pin.

The pin GPIO0 is configured as the LPM wakeup pin to trigger a WAKEINT interrupt upon detection of a low pulse. Initially, pull GPIO0 high externally. To wake device from STANDBY mode, pull GPIO0 low for at least (2+QUALSTDBY), OSCLKS, then pull it high again.

The example then wakes up the device from STANDBY using GPIO0. GPIO0 wakes the device from STANDBY mode when a low pulse (signal goes high->low->high) is detected on the pin. This pin must be pulsed by an external agent for wakeup.

GPIO1 is pulled high before entering the STANDBY mode and is pulled low when in the wakeup ISR.

#### **External Connections**

- GPIO0 needs to be pulled low to wake up the device.
- On device wakeup, the GPIO1 will be low and LED1 will start blinking

## **4.128 Low Power Modes: Device Idle Mode and Wakeup using Watchdog**

This example puts the device into IDLE mode and then wakes up the device from IDLE using watchdog timer.

The device wakes up from the IDLE mode when the watchdog timer overflows, triggering an interrupt. A pre scalar is set for the watchdog timer to change the counter overflow time.

GPIO1 is pulled high before entering the IDLE mode and is pulled low when in the wakeup ISR.

#### **External Connections**

- On device wakeup, the GPIO1 will be low and LED1 will start blinking

## 4.129 Low Power Modes: Device Standby Mode and Wakeup using Watchdog

This example puts the device into STANDBY mode. If the lowest possible current consumption in STANDBY mode is desired, the JTAG connector must be removed from the device board while the device is in STANDBY mode.

This example puts the device into STANDBY mode then wakes up the device from STANDBY using watchdog timer.

The device wakes up from the STANDBY mode when the watchdog timer overflows triggering an interrupt. In the ISR, the GPIO1 is pulled low. the LED is toggled to indicate the device is out of STANDBY mode. A pre scalar is set for the watch dog timer to change the counter overflow time.

The example then wakes up the device from STANDBY using GPIO0. GPIO0 wakes the device from STANDBY mode when a low pulse (signal goes high->low->high)is detected on the pin. This pin must be pulsed by an external agent for wakeup.

As soon as GPIO0 goes high again after the pulse, the device should wake up, and GPIO1 can be observed to toggle low.

### External Connections

- On device wakeup, the GPIO1 will be low and LED1 will start blinking

## 4.130 Correctable & Uncorrectable Memory Error Handling

This example demonstrates error handling in case of various erroneous memory read/write operations. Error handling in case of CPU read/write violations, correctable & uncorrectable memory errors has been demonstrated.

Test functions used in this example

- generateMasterCPUWrViolation -
  - This test configures Memconfig to block CPU writes to GS0 RAM. A write attempt to this memory location by CPU causes RAM\_ACC\_VIOL Interrupt
- generateParityMemUncorrError
  - This test induces parity error in GS0 RAM. A read from the corrupted memory location causes NMI
- generateECCMemCorrError
  - This test induces single bit ECC error in GS0 RAM. A read from the corrupted memory location causes INT\_RAM\_CORR\_ERR Interrupt
- generateECCMemUncorrError
  - This test induces double bit ECC error in GS0 RAM. A read from the corrupted memory location causes NMI
- forceNonMasterDMARReadViolation



- This forces a DMA access violation using MemCfg\_forceViolationInterrupt API. This causes RAM\_ACC\_VIOL Interrupt

**External Connections**

- None

**Watch Variables**

- **testStatusGlobal** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **errCountGlobal** - Error counter

## 4.131 Tune Baud Rate via UART Example

This example demonstrates the process of tuning the UART/SCI baud rate of a C2000 device based on the UART input from another device. As UART does not have a clock signal, reliable communication requires baud rates to be reasonably matched. This example addresses cases where a clock mismatch between devices is greater than is acceptable for communications, requiring baud compensation between boards. As reliable communication only requires matching the EFFECTIVE baud rate, it does not matter which of the two boards executes the tuning (the board with the less-accurate clock source does not need to be the one to tune; as long as one of the two devices tunes to the other, then proper communication can be established).

To tune the baud rate of this device, SCI data (of the desired baud rate) must be sent to this device. The input SCI baud rate must be within the +/- MARGINPERCENT of the TARGETBAUD chosen below. These two variables are defined below, and should be chosen based on the application requirements. Higher MARGINPERCENT will allow more data to be considered "correct" in noisy conditions, and may decrease accuracy. The TARGETBAUD is what was expected to be the baud rate, but due to clock differences, needs to be tuned for better communication robustness with the other device.

NOTE: Lower baud rates have more granularity in register options, and therefore tuning is more affective at these speeds.

**External Connections** for Control Card

- SCIA\_RX/eCAP1 is on GPIO9, connect to incoming SCI communications
- SCIA\_TX is on GPIO8, for observation externally

**Watch Variables**

- **avgBaud** - Baud rate that was detected and set after tuning

## 4.132 SCI FIFO Digital Loop Back

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. The pinmux and SCI modules are configured through the sysconfig file.

This test uses the loopback test mode of the SCI module to send characters starting with 0x00 through 0xFF. The test will send a character and then check the receive buffer for a correct match.

**Watch Variables**

- **loopCount** - Number of characters sent
- **errorCount** - Number of errors detected
- **sendChar** - Character sent
- **receivedChar** - Character received

## 4.133 SCI Digital Loop Back with Interrupts

This test uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Both interrupts and the SCI FIFOs are used.

A stream of data is sent and then compared to the received stream. The SCI-A sent data looks like this:

```
00 01
01 02
02 03
....
FE FF
FF 00
etc..
```

The pattern is repeated forever.

**Watch Variables**

- **sDataA** - Data being sent
- **rDataA** - Data received
- **rDataPointA** - Keep track of where we are in the data stream. This is used to check the incoming data

## 4.134 SCI Echoback

This test receives and echo-backs data through the SCI-A port.

A terminal such as 'putty' can be used to view the data from the SCI and to send information to the SCI. Characters received by the SCI port are sent back to the host.

**Running the Application** Open a COM port with the following settings using a terminal:

- Find correct COM port
- Bits per second = 9600
- Data Bits = 8

- Parity = None
- Stop Bits = 1
- Hardware Control = None

The program will print out a greeting and then ask you to enter a character which it will echo back to the terminal.

**Watch Variables**

- loopCounter - the number of characters sent

**External Connections**

Connect the USB cable from Control card J1:A to PC

## 4.135 SPI Digital Loopback

This program uses the internal loopback test mode of the SPI module. This is a very basic loopback that does not use the FIFOs or interrupts. A stream of data is sent and then compared to the received stream. The pinmux and SPI modules are configured through the sysconfig file.

The sent data looks like this:

0000 0001 0002 0003 0004 0005 0006 0007 .... FFFE FFFF 0000

This pattern is repeated forever.

**External Connections**

- None

**Watch Variables**

- **sData** - Data to send
- **rData** - Received data

## 4.136 SPI Digital Loopback with FIFO Interrupts

This program uses the internal loopback test mode of the SPI module. Both the SPI FIFOs and their interrupts are used.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001

0001 0002

0002 0003

....

FFFE FFFF

FFFF 0000

etc..

This pattern is repeated forever.

#### External Connections

- None

#### Watch Variables

- **sData** - Data to send
- **rData** - Received data
- **rDataPoint** - Used to keep track of the last position in the receive stream for error checking

## 4.137 SPI Digital External Loopback with FIFO Interrupts

This program uses the external loopback between two SPI modules. Both the SPI FIFOs and their interrupts are used. SPIA is configured as a slave and receives data from SPI B which is configured as a master.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001

0001 0002

0002 0003

....

FFFE FFFF

FFFF 0000

etc..

This pattern is repeated forever.

#### External Connections

-GPIO40 and GPIO8 - SPISIMO -GPIO41 and GPIO10 - SPISOMI -GPIO22 and GPIO9 - SPICLK  
-GPIO23 and GPIO11 - SPISTE

#### Watch Variables

- **sData** - Data to send
- **rData** - Received data
- **rDataPoint** - Used to keep track of the last position in the receive stream for error checking

## 4.138 SPI Digital Loopback with DMA

This program uses the internal loopback test mode of the SPI module. Both DMA interrupts and the SPI FIFOs are used. When the SPI transmit FIFO has enough space (as indicated by its FIFO

level interrupt signal), the DMA will transfer data from global variable sData into the FIFO. This will be transmitted to the receive FIFO via the internal loopback.

When enough data has been placed in the receive FIFO (as indicated by its FIFO level interrupt signal), the DMA will transfer the data from the FIFO into global variable rData.

When all data has been placed into rData, a check of the validity of the data will be performed in one of the DMA channels' ISRs.

#### **External Connections**

- None

#### **Watch Variables**

- **sData** - Data to send
- **rData** - Received data

## **4.139 SPI Digital External Loopback without FIFO Interrupts**

This program uses the external loopback between two SPI modules. Both the SPI FIFOs and interrupts are not used in this example. SPIA is configured as a slave and SPI B is configured as master. This example demonstrates full duplex communication where both master and slave transmits and receives data simultaneously.

#### **External Connections**

-GPIO40 and GPIO8 - SPISIMO -GPIO41 and GPIO10 - SPISOMI -GPIO22 and GPIO9 - SPICLK  
-GPIO23 and GPIO11 - SPISTE

#### **Watch Variables**

- **TxDData\_SPIA** - Data send from SPIA (slave)
- **TxDData\_SPIB** - Data send from SPIB (master)
- **RxDData\_SPIA** - Data received by SPIA (slave)
- **RxDData\_SPIB** - Data received by SPIB (master)

## **4.140 SPI EEPROM**

This program will write 8 bytes to EEPROM and read them back. The device communicates with the EEPROM via SPI and specific opcodes. This example is written to work with the SPI Serial EEPROM AT25128/256.

#### **External Connections**

- Connect external SPI EEPROM
- Connect GPIO08 (SIMO) to external EEPROM SI pin
- Connect GPIO10 (SOMI) to external EEPROM SO pin
- Connect GPIO09 (CLK) to external EEPROM SCK pin

- Connect GPIO11 (CS) to external EEPROM CS pin
- Connect the external EEPROM VCC and GND pins

#### Watch Variables

- writeBuffer - Data that is written to external EEPROM
- readBuffer - Data that is read back from EEPROM
- error - Error count

## 4.141 Missing clock detection (MCD)

This example demonstrates the missing clock detection functionality and the way to handle it. Once the MCD is simulated by disconnecting the OSCCLK to the MCD module an NMI would be generated. This NMI determines that an MCD was generated due to a clock failure which is handled in the ISR.

Before an MCD the clock frequency would be as per device initialization (100Mhz). Post MCD the frequency would move to 10Mhz or INTOSC1.

The example also shows how we can lock the PLL after missing clock detection, by first explicitly switching the clock source to INTOSC1, resetting the missing clock detect circuit and then re-locking the PLL. Post a re-lock the clock frequency would be 100Mhz but using the INTOSC1 as clock source.

#### External Connections

- None.

#### Watch Variables

- **fail** - Indicates that a missing clock was either not detected or was not handled correctly.
- **mcd\_clkfail\_isr** - Indicates that the missing clock failure caused an NMI to be triggered and called an the ISR to handle it.
- **mcd\_detect** - Indicates that a missing clock was detected.
- **result** - Status of a successful handling of missing clock detection

## 4.142 CPU Timers

This example configures CPU Timer0, 1, and 2 and increments a counter each time the timer asserts an interrupt.

#### External Connections

- None

#### Watch Variables

- cpuTimer0IntCount
- cpuTimer1IntCount
- cpuTimer2IntCount

## 4.143 Watchdog

This example shows how to service the watchdog or generate a wakeup interrupt using the watchdog. By default the example will generate a Wake interrupt. To service the watchdog and not generate the interrupt, uncomment the `SysCtl_serviceWatchdog()` line in the main for loop.

### External Connections

- None.

### Watch Variables

- `wakeCount` - The number of times entered into the watchdog ISR
- `loopCount` - The number of loops performed while not in ISR





## 5 Bit-Field Example Applications

These example applications show how to make use of various peripherals of a F28002x device. These applications are intended for demonstration and as a starting point for new applications.

All these examples are setup using the Code Composer Studio (CCS) "projectspec" format. Upon importing the "projectspec", the example project will be generated in the CCS workspace with copies of the source and header files included.

All of these examples reside in the `device_support/f28002x/examples` subdirectory of the C2000Ware package.

**Example Projects require CCS v9.1.0 or newer**

### 5.1 ADC ePWM Triggering

This example sets up ePWM1 to periodically trigger a conversion on ADCA.

#### External Connections

- A1 should be connected to a signal to convert

#### Watch Variables

- **adcAResults** - A sequence of analog-to-digital conversion samples from pin A1. The time between samples is determined based on the period of the ePWM timer.

### 5.2 ADC temperature sensor conversion

This example sets up the ePWM to periodically trigger the ADC. The ADC converts the internal connection to the temperature sensor, which is then interpreted as a temperature by calling the `GetTemperatureC` function.

After the program runs, the memory will contain:

- **sensorSample** : The raw reading from the temperature sensor.
- **sensorTemp** : The interpretation of the sensor sample as a temperature in degrees Celsius.

### 5.3 eCAP APWM Example

This program sets up the eCAP module in APWM mode. The PWM waveform will come out on GPIO5. The frequency of PWM is configured to vary between 5Hz and 10Hz using the shadow registers to load the next period/compare values.

## 5.4 Device GPIO Setup

Configures the F28002X GPIO into two different configurations. This code is verbose to illustrate how the GPIO could be setup. In a real application, lines of code can be combined for improved code size and efficiency. This example only sets-up the GPIO. Nothing is actually done with the pins after setup.

## 5.5 F280025C LaunchPad Out of Box Demo Example

This program is the demo program that comes pre-loaded on the F280025C LaunchPad development kit. The program starts by flashing the two user LEDs. After a few seconds the LEDs stop flashing and the device starts sampling ADCINA6 once a second. If the sample is greater than midscale the red LED on the board is lit, while if it is lower a green LED is lit. Sample data is also displayed in a serial terminal via the board's back channel UART. You may view this data by configuring a serial terminal to the correct COM port at 115200 Baud 8-N-1.

### External Connections

- Connect to COM port at 115200 Baud 8-N-1 for serial data
- Connect to ADCINA6 to change LED based on value

### Watch Variables

- None.

## 5.6 LED Blinky Example

This example demonstrates how to blink a LED.

### External Connections

- None.

### Watch Variables

- None.

## 5.7 SCI Echoback

This test receives and echo-backs data through the SCI-A port.

A terminal such as 'putty' can be used to view the data from the SCI and to send information to the SCI. Characters received by the SCI port are sent back to the host.

**Running the Application** Open a COM port with the following settings using a terminal:

- Find correct COM port

- Bits per second = 9600
- Data Bits = 8
- Parity = None
- Stop Bits = 1
- Hardware Control = None

The program will print out a greeting and then ask you to enter a character which it will echo back to the terminal.

**Watch Variables**

- loopCounter - the number of characters sent

**External Connections**

Connect the USB Cable on Control Card J1A to a PC

## 5.8 SPI Digital Loop Back

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Interrupts are not used.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001 0002 0003 0004 0005 0006 0007 .... FFFE FFFF

This pattern is repeated forever.

**Watch Variables**

- **sdata** - sent data
- **rdata** - received data

## 5.9 SPI Digital Loop Back with DMA (spi\_loopback\_dma)

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Both DMA Interrupts and the SPI FIFOs are used.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001

0001 0002

0002 0003

....

007E 007F

**Watch Variables**

- **sData** - Data to send
- **rData** - Received data
- **rData\_point** - Used to keep track of the last position in the receive stream for error checking

## 5.10 CPU Timers

This example configures CPU Timer0, 1, and 2 and increments a counter each time the timer asserts an interrupt.

### External Connections

- None

### Watch Variables

- CpuTimer0.InterruptCount
- CpuTimer1.InterruptCount
- CpuTimer2.InterruptCount



---

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