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	NOTES:				TI-SBL R1.0 R1.0 TI-SBL R1.1 R1.1	Initial Release to PCB	14-May-2012	
	1) EDI — Entermal Desirabanal Interferent Lucra descent Mataliana					Edited Order of Boot Mode Switches Added ENET Address Resistors Fixed Ethernet PHY LED order R43: 100K to 0R0 ded XRSn connection through HSEC connect	16-July-2012	D
	(A) GPIO24, 25, 36, 37, 40, 41, 48-53, 68, 69, 70, 71 - SDRAM Memory Interface Data + Address							-
	(B) GPIO12, 13, 18, 19, 26, 27, 54, 55 - SRAM Memory Interface Address							-
	(C) GPIO56-62 - SDRAM&SRAM CS, DQM, etc (D) GPIO34, 35, 28, 29 - SRAM Extended Address							
	(C) GPIO47 - Clock							_
	(5) 33 2 3 3 3							
С	2) ENET Differer	ntial Pairs - 100 Ohm						
	(A) ENET_TD+ & ENET_TD- (B) ENET_RD+ & ENET_RD-							
	3) USB Differential Pairs - 90 Ohm							C
	o) cod differential rails to offin							
	(A) USB-DM & USB-DP (B) USB0_GPIO-42 & USB0_GPIO-45							
	(C) MCU_GPIO-4	(C) MCU_GPIO-42 & MCU_GPIO-45						
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			Texas Instruments Inc					
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					F28M36x control	CARD	1.1	
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