Piccolo F2806x controlCARD

Texas Instrument's **Piccolo F2806x controlCARD** can be used as a quick evaluation board with control, connectivity signals and ports to F2806x MCU.

1. The controlCARD features: Rev0.3:

- Small size – 90mm x 25mm (3.5" x 1.2")
- DIMM100 compatible cards for C2000 system application boards
- Built in Isolated XDS100 V2 JTAG port for easy interface to Code composer 4.2.x
- Supports USB host/device
- All GPIO, ADC and other key signals routed to gold connector fingers
- Single 5V input supply to the controlCARD and external supply pin decoupling with L+C connected close to the device
- Clamping diode protection at ADC input pins
- Anti-aliasing filter (noise filter) at ADC input pins
- Ground plane
- Isolated RS-232 communication

N ote:

1. **See cautionary notes /errata for rev 0.2 card BOM and isolation care in section 2.**
2. **Download ControlSUITE from www.ti.com for latest update on software, documentation and examples**

2. Exceptions on Docking station/cCARD set up:

- While using ISO JTAG port on the cCARD, the JTAG port on the docking station will not be active.

- CAUTION: J200 supports USB host/device connectivity. This USB port is not isolated USB port. Care should be taken while connecting external USB devices, while this card is plugged in high power application boards. External USB isolation buffer will be required, while debugging high power application boards/systems.

- **Apply caution while using these board in high voltage board testing. Use external isolator if necessary.**

2.1 Errata/Caution

2.1.1 Rev0.3 ISO Control cards have isolated JTAG stage. Earlier control cards have wrong cap (C276 - .10uf/ 10V) values between the isolation section.

The existing caps are not recommended for good isolation. Please remove these caps while emulating in high voltage environment (>10V).

All control cards shipping from Nov'11 (R0.3) will have 450V isolation capability.

Each controlCARD includes a "Hardware Developer's Package", a set of "soft collateral" files which makes deploying this technology very easy, these files include:

- Schematics
- Bill of materials (BOM)
- Gerber files

3. References

Isolated JTAG – ISO JTAG:

J1	USB_A connector is intended for XDS100V2 JTAG emulation and SCI communication through dedicated FTDI logic

Connectivity ports:

J200	USB micro AB connector supports USB 2.0 host/device

LEDs:

LD1	Turns on when controlCARD is powered on (Green)
LD2	Controlled by GPIO-31 (Red)
LD3	Controlled by GPIO-34 (Red)
LD4	Turns on when ISO JTAG logic is powered on (Green)
D2	Uart/SCI/ toggle indicator through Isolated buffer
D3	Uart/SCI/ toggle indicator through Isolated buffer

SW1: Controls the boot options of the F2806x device

Position 1 (GPIO-34)	Position 2 (TDO)	
0	0	Parallel I/O
0	1	Wait mode
1	0	SCI
1	1	(default) Get mode; the default get mode is boot from FLASH

SW2: ADC VREF control

By default, the ADC will convert from 0 to 3.3V. However, if the ADC in the ADC registers is configured to use external limits, the ADC will convert its full range of resolution from VREF-LO to VREF-HI.

Position1 - Controls VREF-HI, the value that the ratio-metric ADC will convert as the maximum 12-bit value, which is 0x0FFF. In the downward position, VREF-HI will be connected to 3.3V. In the upward position, VREF-HI will be connected to pin 66 of the DIMM100-socket. This would allow a

connecting board to control the ADC VREF-HI value. This extends VREF-HI connections to both the ADCs on the F2806x device.

Position 2 - Controls VREF-LO, the value that the ratio-metric ADC will convert as the minimum 12-bit value, which is 0x0000. In the downward position, VREF-LO will be connected to 0V. In the upward position, VREF-LO will be connected to pin 16 of the DIMM100-socket. This would allow a connecting board to control the ADC-VREFLO value. This extends VREF-LO connections to both the ADCs on the F2806x device.

SW3: TRST/ ISO SCI communication signal enables

Position 1:

ON - TRST signal from ISO JTAG circuit will be connected to F2806x. Needed during JTAG debug using ISO JTAG.

OFF - TRST signal from ISO JTAG circuit will NOT be connected to F2806x. Needed when the application is running from flash at power up without the JTAG connections.

Position 2:

ON - RS-232 transceiver will be enabled and allow communication through a serial cable via pins 2 and 42 of the DIMM-100 socket. Putting SW3 in the “ON” position will allow the F28069 controlCARD to be DIMM signal compatible with the F2808, F28044, F28335, F28035 and F28027 controlCARDs. GPIO-28 will be stuck as logic high in this position.

OFF - The default option. SW3 in the “OFF” position allows GPIO-28 to be used as a GPIO. Serial communication is still possible, through the FTDI – FT2232 chip.