Chapter 1

HSMC-to-VLDB PCB design

In order to interface the GBTx (see chapter **??**) electrically In order for communication and the ability to send and monitor test data, a form of electrical connection between the Field-Programmable Gate Array (FPGA) and the Versatile Link (VLDB) is required. The VLDB has twenty additional HDMI female connectors which connects to the Low-Voltage Differential Signaling (LVDS) transceivers for high-speed communication with the Common Readout Unit (CRU). The FPGA board that is used for this thesis has two High-Speed Mezzanine Card (HSMC) connectors with port A containing the LVDS transceivers. In addition to the LVDS signals, the connection also needs to contain the Radiation-hard optical link, i.e support for SFP fiber-optic cabling.

1.1 Specification

1.2 Design discussion

The design discussion and planning of the Printed Circuit Board (PCB) was done together with Ph. D. Arild Velure.

The initial plan was to design a PCB with a male Small Form-Factor Pluggable HSMC board (SFP)-contact in one end connected with two High-Definition Multimedia Interface (HDMI) connectors, one on each side of the PCB, making an adapter that can be plugged directly into the SFP-connectors on the SFP-board with HDMI cables to the VLDB. This design was quickly scratched as there was no loose male SFP connectors available on the marked, only female. The design plan was then changed to use only one PCB board with female SFPs-connectors on one side, wired to HDMI-connectors on the other side, acting as a middle joint

between the SFP-board and the VLDB with SFP- and HDMI-cables connecting the three boards together.

The end result was a design that could be directly mounted on the FPGA through the HSMC connector. By copying one of the SFP-to-HSMC connections from the original SFP-board design files (the one concerning the EKS SE VE ERR (XCVR)-protocol, see [**?**]), we found that we could remove the SFP-board completely from the connection chain and eliminate the resulting need for electrical SFP-cables. This would also remove the middle joint in the chain, reducing complexity and saving costs. The resulting design was a board connected to the FPGA via the HSMC-connector, with LVDS-signals running to ten HDMI connectors and XCVR-signals running to one SFP-connector for fiber-optic communication.

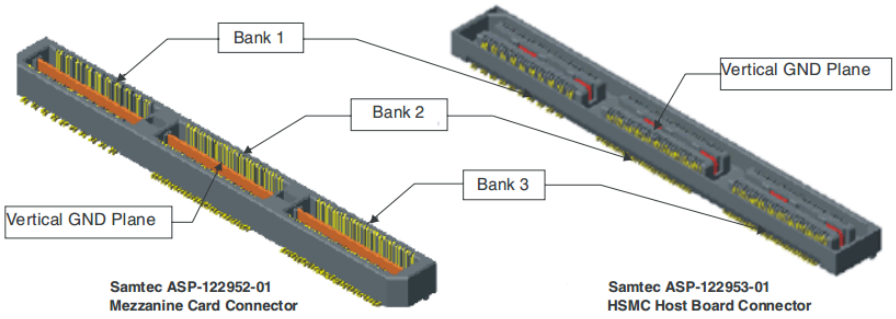

Figure 1.1: Male (ASP-122952) and female (ASP-122953) HSMC-connectors. The male type is to be connected at the bottom of the HSMC-to-VLDB PCB [**?** , Figure 2-1].

1.3 High Speed PCB Design

When transmitting signals through a conductor at high frequencies, the conductor no longer acts as an ideal wire. The signal voltage stops acting instantaneous across the conducting path, and factors like impedance mismatch and reflections becomes important for the quality of the signal to remain the same through the whole transmission. This section gives a brief explanation of high frequency signal behavior and the compensation methods that was practiced during the design of the HSMC-to-VLDB PCB.

1.3.1 Transmission lines

When signal rise/fall times becomes comparable with the propagation delay of the conductor, the signal no longer acts instantaneous. The conductor becomes what is known as a transmission line, with the signals voltage and current acting like waves propagation through the conductor. The general rule for determining if a signal is propagating along a transmission line is when the rise/fall time of the signal is less than 1/4 of the signal period, so that the high and low states are recognizable [**?**].
For an LVDS-protocol, with signal speeds reaching up to $3.125\ \mathrm{Gbit/s}$, the trace becomes a transmission line if the signal propagation time along the trace is less than 1/4 of the signal period, i.e $80\mathrm{ps}$.
The propagation velocity of a signal is given by:

$$v = \frac{c}{\sqrt{\epsilon_r}} \tag{1.1}$$

, where ϵ_r is the dielectric constant of the epoxy material FR4, often used as a material to separate the copper layers on the PCBs. ϵ_r has a value of around 4.05 @ $3\ \mathrm{GHz}$ [**?**]. A signal thus propagates through the conductor at a velocity of approximately $15\ \mathrm{mm/ns}$ [**?** , example 13.7].
Thus, by assuming a constant transmitting frequency of $3.125\ \mathrm{Gbit/s}$, a conductor becomes a transmission line if the length of the conductor stretches longer than $12\ \mathrm{mm}$ between transmitter and receiver. This short length is very difficult to avoid when designing a PCB with microstrip traces running from one connector out to eleven other connectors. The traces on the HSMC-to-VLDB PCB are therefore considered as transmission lines.

1.3.2 Reflections and characteristic impedance

Since the signals no longer acts instantaneous, the transmitter can not see what is connected at the receiving end at the time it sends a pulse down the conducting channel. All it sees is the channel impedance, called the characteristic impedance, Z_0, of the channel [**?**].
The type of trace that is used in the HSMC-to-VLDB PCB design is called a microstrip, which is when the signal traces run along traces on the outer layers of the PCB with the ground plane on the layer underneath.
A microstrip has a characteristic impedance that is given by:

$$Z_0 = \frac{60}{\sqrt{0.475\epsilon_r + 0.67}} \times \ln \frac{4h}{0.67(0.8w + t)} \tag{1.2}$$

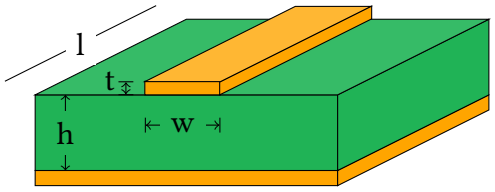

Figure 1.2: Cross-section of a single-ended microstrip with the copper trace on top, followed by a dielectric layer and a ground plane. h is the thickness of the dielectric, t is the copper thickness, l is the microstrip length, and w is the copper width.

, where ϵ_r is the dielectric constant, h is the height of the microstrip seen from the ground plane, i.e the thickness of the FR4 layer, w is the width of the microstrip, and t is the thickness of the copper [**?**].

It is important to match the impedance of the trace to that of the load impedance at the receiving end, or vice versa. With these being different, the energy of the signal cannot be fully absorbed at the receiving end, resulting in a partly reflection of the signal wave back to the transmitter. The ratio of the wave reflected back is given by:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1.3}$$

, where Z_L is the load impedance and Z_0 is the characteristic impedance.

Ideally the Z_L and Z_0 should be equal to avoid reflections. Impedance mismatch can cause waste of signal energy and interference with other signal pulses being transmitted through the channel [**?**].

When looking at the datasheet for cables with differential signals, such as HDMI-cables, it is often supplied a differential impedance between the cables instead of a characteristic impedance for each cable. Knowing the characteristic impedance, it is possible to calculate the corresponding differential impedance between two microstrip traces (or vice versa):

$$Z_{diff} = 2 \times Z_0[1 - 0.48e^{(-0.96 \times \frac{s}{h})}] \tag{1.4}$$

, where Z_0 is the characteristic impedance of the individual microstrips (assuming they are equal and have the same length), s is the spacing between the microstrips and h is the same as in the equation above [**?**].

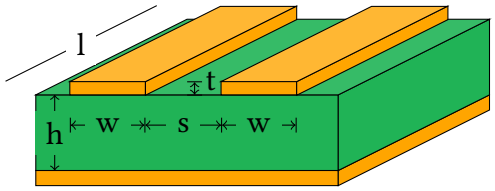

Figure 1.3: Cross-section of a corresponding differential microstrip. s is the spacing between the strips.

1.3.3 Routing

As mentioned in section **??**, differential signals have noise advantages over single ended signals. This is the case only if the pairs have *equal* path lengths and the individual wires in each pair are routed as close to one another as possible. In addition, to keep crosstalk to its minimum, individual pairs has to be routed a distance away from other wires (In reality, this only becomes a problem when dealing with wiring in the micro-scale domain). Twisting the individual wires in each pair to some extent will also contribute to common noise rejection [**?**]. This was taken into consideration when routing the PCB.
The individual wires in each pair was kept as close as possible, with a space constraint according to the required differential impedance Z_{diff} of approximately $100\ \Omega$ (See equation 1.6). When routing, twisting the wires (where possible) was achieved by purposely making the wires overlap at the viases). After routing the wires, attempts were made to separate the pairs a distance from one another, but this was not a critical stage.

1.4 PCB design parameters

To avoid signal reflections, the PCB needed a characteristic impedance matching that of the cables and termination, in this case a single wire impedance of $50\ \Omega$, and a differential impedance of $100\ \Omega$. This was derived from the fact that the HDMI-cables were specified to have a differential impedance of approximately $100\ \Omega$, which is also the case of the termination resistance at the receiving end (this must be manually set for the FPGA transceivers).
The PCB was chosen to be four layers, with signals running on the top and bottom copper layers, and the two middle planes for voltages and ground respectively.
For thicknesses of the different PCB copper layers and the FR4 in between, Elprint has a set of predefined *stack-ups* available in Macaos. It is possible to define custom stack-ups as well, but this will result in a more costly PCB. The 4036 pre-defined stack-up has a copper thickness of $18\ \mu\text{m}$ on the two outer layers following an FR4 thickness of $65\ \mu\text{m}$ between the outer layers and the power

planes, with the power planes having a thickness of 35 µm. Between the power planes is another FR4 layer with a thickness of 1.4mm making the total PCB thickness of a standard 1.6mm. With a mircostrip width of 100 µm, the formula for characteristic impedance yields:

$$Z_0 = \frac{60}{\sqrt{(0.475 \times 4.05) + 0.67}} \ln 3.96 \tag{1.5}$$

, which gives a characteristic impedance Z_0 of $51.3\ \Omega$ @ 3 GHz.
With a 300 µm spacing between the differential traces, the formula for differential impedance yields:

$$Z_{diff} = 2 \times 51.3\ \Omega[1 - 0.48e^{(-0.96 \times \frac{300}{65})}] \tag{1.6}$$

, which gives a differential impedance Z_{diff} of $102\ \Omega$ @ 3 GHz.

Orcad PCB Editor has a built-in impedance calculator which yields similar results as shown above:

	Layer	Type	t [µm]	ϵ_r	w [µm]	$Z_0[\Omega]$	Spacing [µm]	$Z_{diff}[\Omega]$
1	Surface	Air		1				
2	Top	Conductor	18		100	51.3	300	102
3		Dielectric	65	4.05				
4	Voltage	Plane	35					
5		Dielectric	1400	4.05				
6	Gnd	Plane	35					
7		Dielectric	65	4.05				
8	Bottom	Conductor	18		100	51.3	300	102
9	Surface	Air		1				

Table 1.1: The layers of the PCB and their traits, where t is the layer thickness and w is the width of the trace. The PCB has an overall thickness of 1.6 mm

1.5 Further specification and ordering

The PCB schematic was designed using *Orcad Capture CIS* and the layout using *Orcad PCB Editor*, with design parameters meeting *Elprint's* capabilities [**?**]. The PCB layout was then exported into *Gerber-files* and imported into *Macaos* for further manufacture specification and validation. The PCB was then ordered from Elprint.

1.6 Soldering process

All the components on the PCB was soldered by hand, with the exception of the ground pads underneath the HSMC, which had to be soldered using solder paste and a solder oven.

1.6.1 Martin Rework Station

The HSMC-connector has several ground pads underneath the connector itself, making it impossible to reach when soldering by hand. The solution to this was to apply solder paste on the pads with the help the Martin Rework Station dispenser module that was available in the lab. The dispenser module forces the solder paste out of the syringe using pressurized air. By pressing a foot pedal connected to the dispenser, you apply a controlled air pulse that pushes on the piston of the solder paste syringe. The force of the air pulse can be adjusted using the dispenser Guided User Interface (GUI). For the ground pads, a force of $2.50ccm$ was suitable.

1.6.2 Solder Oven

The oven was set to a warm-up temperature of 150 for 60 seconds, and then a climb temperature of max 220 with a climb-time of 120 seconds.

1.7 PCB faults and compensations

After receiving the PCBs, further inspection revealed that all viases had missing solder mask. This exposes the metal of the vias to the surface of the PCB and can possibly cause connection shorts between the viases and the pads and/or metallic casings when soldering. The reason for the viases not to have a solder mask is because it was missing in the pad file. A solution to fix this in a future PCB print would obviously be to include a solder mask in the pad file. With the current PCB print, however, a temporary solution would be to apply thin *kapton tape* where most critical.

The exposed viases was later shown not to be as critical as first thought, due to the following points:

- The viases that are exposed underneath the HDMI casings are in fact connected to ground, making the possible shorts between the viases and the

already ground connected casing not a critical problem.

- The exposed viases underneath the HSMC-connector could potentially connect to the ground pads when applying solder paste to the pads. This was avoided by carefully applying a thin line of solder paste in the middle of the ground pads. This prevented the solder paste to float over to the neighboring viases when melting it in the oven. A possible drawback to this would be bad connection between the ground pads and the HSMC-connector, but a quick check using a multimeter proved that the HSMC was indeed connected to all the ground pads.

In fact, when testing the PCB, the exposure of viases on the transmitter and receiver lines revealed to be quite useful probe points when using an oscilloscope to measure the signal integrity. Due to the lack of extra added probe points, measuring signals at the PCB viases became the most convenient way of directly measuring the signals on the transmitter and receiver lines (see subsection below). A lesson until next PCB-prototype is to include easily accessible probe points on lines that are relevant for oscilloscope measurement.

On the current version of the PCB, some of the receiver lines includes a $10\ \mathrm{k}\Omega$ pull-up resistor (R91, R92, R95, R96, R97, R99, R100 and R101 in the schematic). The reason why these are included could possibly be due to a misinterpretation of the SFP-schematic in which the design of the PCB was based on. This is concluded because two of the pull-up resistors (R100 and R101 in the schematic) are connected to receiver signals that are only used in the SFP-design, but not in this design. The pull-up resistors are therefore not included, and the lines are left open.

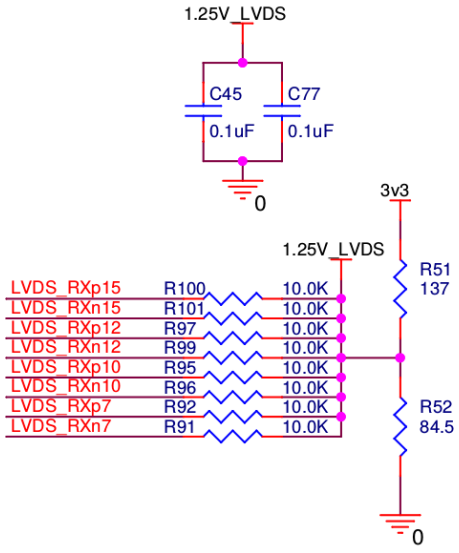

Figure 1.4: Pull-up resistors on some of the receiver lines.

Later discussions with Arild revealed that the transmitters on the GBT-VLDB did not have voltage pull-ups, which is necessary for the LVDS-signals. The current PCB will therefore not work properly with the GBT-VLDB card. Later versions of the PCB should therefore contain resistors pulling up to $1.25\mathrm{V}$ on the receiver lines in order for it to work.

Chapter 2

Testing and verification of the HDMI daughter card

To verify a working PCB, the HDMI daughter card underwent a series of tests. The sections below summarizes these tests.

2.1 Connectivity test

Since all the components on the PCB was hand soldered (with the exception of the ground pads underneath the HSMC contact), it was particularly important to check for accidental shorts between pins and/or pads.

2.1.1 Purpose of test

- Verify that there are no shorts between the pins and/or pads of the PCB.
- Check for current draw to confirm that there are no short on the power-lines.

2.1.2 Experimental setup

The setup involves the use of a multimeter to go through all pins and check for connection faults according to the schematic. After all shorts have been eliminated, the PCB is to be connected to an external power supply to verify current-draw.

2.1.3 Results

Using a multimeter, all connections were checked and verified that there were no shorts (Some pins on the HSMC were indeed shorted and had to be re-soldered). The PCB was then connected to an external power supply and it was verified that the current draw, with all HDMI-connections left open, were no more than the current drawn from the power-LED, i.e $18\ \mathrm{mA}$.

To confirm connectivity and that there were no further connecting shorts between the pads and/or pins, a simple test-circuit was written in Quartus. Beginning with the transmit-signals: all the relevant LVDS transmit-signals that are physically connected to the HSMC (port A) connector of the FPGA were connected to a given clock signal. The PCB was then connected to the FPGA board, and the HDMI connectors were probed with the help of an oscilloscope and verified that there was an output signal on every HDMI-transmitter.
The PCB is now ready for connection with the host FPGA for further testing of the transmitter and receiver signals.

2.2 External loop-back test for the fiber-optic connector

To verify that the HDMI daughter card SFP-connector for fiber-optic communication is working correctly, an external loop-back test was conducted.

2.2.1 Purpose of test

- Test the dedicated SFP-connector on the HDMI-daughter card for fiber-optic communication and see that it is capable of sending and receiving information at speeds up to the Gigabit Transceiver (GBT)-standard of $4.8\mathrm{Gbit/s}$.

2.2.2 Experimental setup

A fiber-optic cable connected from the transmitter to the receiver using a fiber-module, forming an external loop through the cable, was connected to the SFP-connector of the HDMI-daughter card PCB. Using the GBT Quartus-example together with the In-system-source-and-probe editor and SignalTap II, it was possible to connect the transmitter to a internal counter that counted with increments of one. SignalTap II was then used to monitor and verify that the receiver line received the same incremented counter as the transmitter sent out.

2.2.3 Results

2.3 External loop-back test for the HDMI connectors

2.3.1 Purpose of tests

- Measure the quality of the signal at different frequencies up to $300\ \mathrm{MHz}$ and see how reflections affects the signal.
- Measure crosstalk between neighboring signal paths.
- Create a test environment using Quartus II in conjunction with SignalTap II to:
  - See if it is possible to sample the received signals at different frequencies up to $300\ \mathrm{MHz}$.
  - Investigate bit-error rate at different frequencies up to $300\ \mathrm{MHz}$.

2.3.2 Experimental setup

Each HDMI-connector has at least one transmitter- and receiver line. To simulate signal transmission over a distance, a HDMI cable was cut in half and the transmit- and receive lines were soldered together, creating an external loop-back. A pseudo-random generated bit-signal would travel out via one of the transmitters of the FPGA, out through a HDMI-connector, following the cable back into the same HDMI-connector into the receiver input.

2.3.3 Results

The following table sums up the cable-length and theoretical travel time versus the measured delay between the transmitted and received signal.

2.4 Conclusion and discussions

The measurement setup has a lot to say when it comes to measur