Chapter 1

HSMC-to-VLDB PCB Design

In order to test the GBTx chip, a Printed Circuit Board (PCB) that acts as a connecting bridge between the Field-Programmable Gate Array (FPGA) and the Versatile Link Demo Board (VLDB) is needed. As mentioned in **??**, the VLDB has a optical link which will provide connection to the FPGA in the counting room, and twenty e-links reachable through physical HDMI contacts, which will be available connections to the front-end detectors.

A basic test-setup would be to transmit test data from the FPGA to the Gigabit Transceiver (GBT)x via e-links. The data will represent data sent from the front-end detectors. The GBTx will then transmit the same data back to the FPGA via the fiber-optic cable, making it possible to analyze the received data and also compare it to the transmitted data.

Because of limited available physical Low-Voltage Differential Signaling (LVDS) connections on the FPGA board, the $320\ \mathrm{Mbit/s}$ data rate was chosen for the e-link connections. The required LVDS connections would thus be 20 receiver pairs and 10 transmitter pairs. As mentioned in section **??**, the High-Speed Mezzanine Card (HSMC) port A connection on the board has only 17 available LVDS channels, or 17 transmitter and 17 receiver pairs. Since the clock on each e-link will be the same during testing, the 10 clock pairs can be reduced to just one, reducing the total receiver pairs needed on the FPGA from 20 to just 11 pairs.

The resulting PCB has 10 individual High-Definition Multimedia Interface (HDMI) connector with each having a receiver and a transmitter pair. The J4 HDMI contact contains an additional receiver reserved for an input clock from the VLDB.

This chapter explains the design process of this PCB; beginning with the discussion of different design approaches, to the theory behind designing a high speed PCB. It then explains the final PCB design parameters and discusses the resulting product.

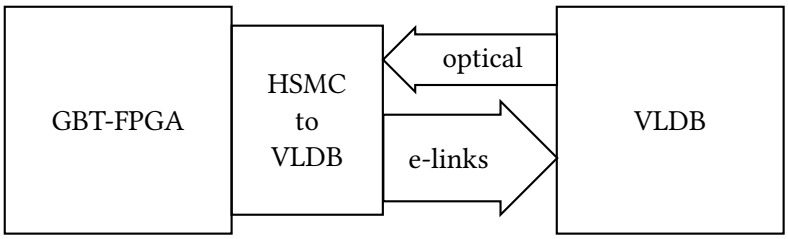


Figure 1.1: Block diagram showing the FPGA connected to the VLDB using the HSMC-to-VLDB PCB as a bridge.

1.1 Design Discussion

The design discussion and planning of the PCB was done together with Ph. D. Arild Velure.

The initial plan was to design a PCB with a male Small Form-Factor Pluggable HSMC board (SFP)-contact in one end connected with two HDMI connectors, one on each side of the PCB, making an adapter that can be plugged directly into the SFP-connectors on a SFP-board with HDMI cables connected to the VLDB. This design was quickly scratched as there was no loose male SFP connectors available on the marked, only female. The design plan was then changed to use only one PCB board with female SFPs-connectors on one side, wired to HDMI-connectors on the other side, acting as a middle joint between the SFP-board and the VLDB with SFP- and HDMI-cables connecting the three boards together.

The end result was a design that could be directly mounted on the FPGA through the HSMC connector. By copying one of the SFP-to-HSMC connections from the original SFP-board design files (the one concerning the Transceiver (XCVR)-protocol, see [**?**]), we found that we could remove the SFP-board completely from the connection chain and eliminate the resulting need for electrical SFP-cables. This would also remove the middle joint in the chain, reducing complexity and lowering the chance of signal reflections.

1.2 High Speed PCB Design

When transmitting signals through a conductor at high frequencies, the conductor no longer acts as an ideal wire. The signal voltage stops acting instantaneous across the conducting path, and factors like impedance mismatch and reflections becomes important for the quality of the signal to remain the same through the whole transmission. This section gives a brief explanation of high frequency signal behavior and the compensation methods that was practiced during the design of the HSMC-to-VLDB PCB.

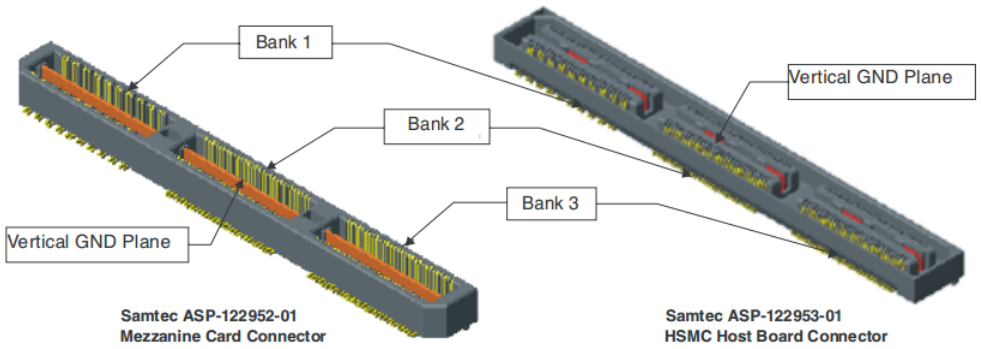


Figure 1.2: Male (ASP-122952) and female (ASP-122953) HSMC-connectors. The male type is to be connected at the bottom of the HSMC-to-VLDB PCB [**?** , Figure 2-1].

1.2.1 Transmission Lines

When signal rise/fall times becomes comparable with the propagation delay of the conductor, the signal no longer acts instantaneous. The conductor becomes what is known as a transmission line, with the signals voltage and current acting like waves propagation through the conductor. The general rule for determining if a signal is propagating along a transmission line is when the rise/fall time of the signal is less than 1/4 of the signal period, so that the high and low states are recognizable [**?**].

For an LVDS-protocol, with signal speeds reaching up to $3.125\ \mathrm{Gbit/s}$, the trace becomes a transmission line if the signal propagation time along the trace is less than 1/4 of the signal period, i.e $80\mathrm{ps}$.

The propagation velocity of a signal is given by:

$$v = \frac{c}{\sqrt{\epsilon_r}} \tag{1.1}$$

, where ϵ_r is the dielectric constant of the epoxy material FR4, often used as a material to separate the copper layers on the PCBs. ϵ_r has a value of around 4.05 @ $3\ \mathrm{GHz}$ [**?**]. A signal thus propagates through the conductor at a velocity of approximately $15\ \mathrm{mm/ns}$ [**?** , example 13.7].

Thus, by assuming a constant transmitting frequency of $3.125\ \mathrm{Gbit/s}$, a conductor becomes a transmission line if the length of the conductor stretches longer than $12\ \mathrm{mm}$ between transmitter and receiver. This short length is very difficult to avoid when designing a PCB with microstrip traces running from one connector out to eleven other connectors. The traces on the HSMC-to-VLDB PCB are therefore considered as transmission lines.

1.2.2 Reflections and Characteristic Impedance

Since the signals no longer acts instantaneous, the transmitter can not see what is connected at the receiving end at the time it sends a pulse down the conducting channel. All it sees is the channel impedance, called the characteristic impedance, Z_0, of the channel [**?**].

The type of trace that is used in the HSMC-to-VLDB PCB design is called a microstrip, which is when the signal traces run along traces on the outer layers of the PCB with the ground plane on the layer underneath.

A microstrip has a characteristic impedance that is given by:

$$Z_0 = \frac{60}{\sqrt{0.475\epsilon_r + 0.67}} \times \ln \frac{4h}{0.67(0.8w + t)} \tag{1.2}$$

, where ϵ_r is the dielectric constant, h is the height of the microstrip seen from the ground plane, i.e the thickness of the FR4 layer, w is the width of the microstrip, and t is the thickness of the copper [**?**].

It is important to match the impedance of the trace to that of the load impedance at the receiving end, or vice versa. With these being different, the energy of the signal cannot be fully absorbed at the receiving end, resulting in a partly reflection of the signal wave back to the transmitter. The ratio of the wave reflected back is given by:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1.3}$$

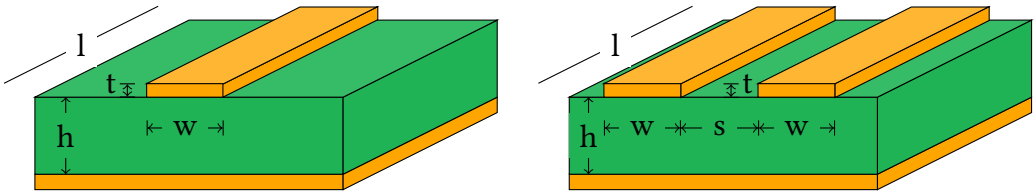
, where Z_L is the load impedance and Z_0 is the characteristic impedance.

Ideally the Z_L and Z_0 should be equal to avoid reflections. Impedance mismatch can cause waste of signal energy and interference with other signal pulses being transmitted through the channel [**?**].

When looking at the datasheet for cables with differential signals, such as HDMI-cables, it is often supplied a differential impedance between the cables instead of a characteristic impedance for each cable. Knowing the characteristic impedance, it is possible to calculate the corresponding differential impedance between two microstrip traces (or vice versa):

$$Z_{diff} = 2 \times Z_0[1 - 0.48e^{(-0.96 \times \frac{s}{h})}] \tag{1.4}$$

, where Z_0 is the characteristic impedance of the individual microstrips (assuming they are equal and have the same length), s is the spacing between the microstrips and h is the same as in the equation above [**?**].



(a) Single-ended. **(b)** Differential.

Figure 1.3: Microstrip, cross-section. The microstrip is the copper trace(s) on top, followed by a dielectric layer and a ground plane. h is the thickness of the dielectric, t is the copper thickness, l is the microstrip length, and w is the copper width. s is the spacing between the differential strips.

1.2.3 Routing

As mentioned in section **??**, differential signals have noise advantages over single ended signals. This is the case only if the pairs have *equal* path lengths and the individual wires in each pair are routed as close to one another as possible. In addition, to keep crosstalk to its minimum, individual pairs has to be routed a distance away from other wires (In reality, this only becomes a problem when dealing with wiring in the micro-scale domain). Twisting the individual wires in each pair to some extent will also contribute to common noise rejection [**?**]. This was taken into consideration when routing the PCB.

The individual wires in each pair was kept as close as possible, with a space constraint (See table 1.1) according to the required differential impedance Z_{diff} of approximately $100\ \Omega$ (See equation 1.6). When routing, twisting the wires (where possible) was achieved by purposely making the wires overlap at the viases. After routing the wires, attempts were made to separate the pairs a distance from one another, but this was not a critical stage.

1.3 PCB Design Parameters

The PCB schematic was designed using *Orcad Capture CIS* and the layout using *Orcad PCB Editor*, with design parameters meeting *Elprint's* capabilities [**?**]. The PCB layout was then exported into *Gerber-files* and imported into *Macaos* for further manufacture specification and validation. The PCB was then ordered from Elprint.

To avoid signal reflections, the PCB needed a characteristic impedance matching that of the cables and termination, in this case a single wire impedance of $50\ \Omega$, and a differential impedance of $100\ \Omega$. This was derived from the fact that the HDMI-cables were specified to have a differential impedance of approximately $100\ \Omega$, and that the individual transceiver lines from the FPGA has a characteristic impedance of $50\ \Omega$, with a selectable termination resistance at the receiving end of $100\ \Omega$, connected between the lines.

The PCB was chosen to be four layers, with signals running on the top and bottom copper layers, and the two middle planes for voltages and ground respectively.

For thicknesses of the different PCB copper layers and the FR4 in between, Elprint has a set of predefined *stack-ups* available in Macaos. It is possible to define custom stack-ups as well, but this will result in a more costly PCB. The 4036 pre-defined stack-up has a copper thickness of 18 µm on the two outer layers following an FR4 thickness of 65 µm between the outer layers and the power planes, with the power planes having a thickness of 35 µm. Between the power planes is another FR4 layer with a thickness of 1.4mm making the total PCB thickness of a standard 1.6mm. With a mircostrip width of 100 µm, the formula for characteristic impedance yields:

$$Z_0 = \frac{60}{\sqrt{(0.475 \times 4.05) + 0.67}} \ln 3.96 \tag{1.5}$$

, which gives a characteristic impedance Z_0 of $51.3\ \Omega$ @ 3 GHz. With a 300 µm spacing between the differential traces, the formula for differential impedance yields:

$$Z_{diff} = 2 \times 51.3\ \Omega[1 - 0.48e^{(-0.96 \times \frac{300}{65})}] \tag{1.6}$$

, which gives a differential impedance Z_{diff} of $102\ \Omega$ @ 3 GHz.

Table 1.1 shows data extracted from Orcad PCB Editor, which has a built-in impedance calculator that yields similar results as shown above:

	Layer	Type	t [µm]	ϵ_r	w [µm]	$Z_0[\Omega]$	Spacing [µm]	$Z_{diff}[\Omega]$
1	Surface	Air		1				
2	Top	Conductor	18		100	51.3	300	102
3		Dielectric	65	4.05				
4	Voltage	Plane	35					
5		Dielectric	1400	4.05				
6	Gnd	Plane	35					
7		Dielectric	65	4.05				
8	Bottom	Conductor	18		100	51.3	300	102
9	Surface	Air		1				

Table 1.1: The layers of the PCB and their traits, where t is the layer thickness and w is the width of the trace. The PCB has an overall thickness of 1.6 mm

1.4 Pads and Footprints

All pads and footprints were custom made using *Cadence Pad Designer*, with dimensions collected from datasheets of the different components. The only excepting was for the HSMC footprint and pads, which were acquired from the manufacturer. The pads were

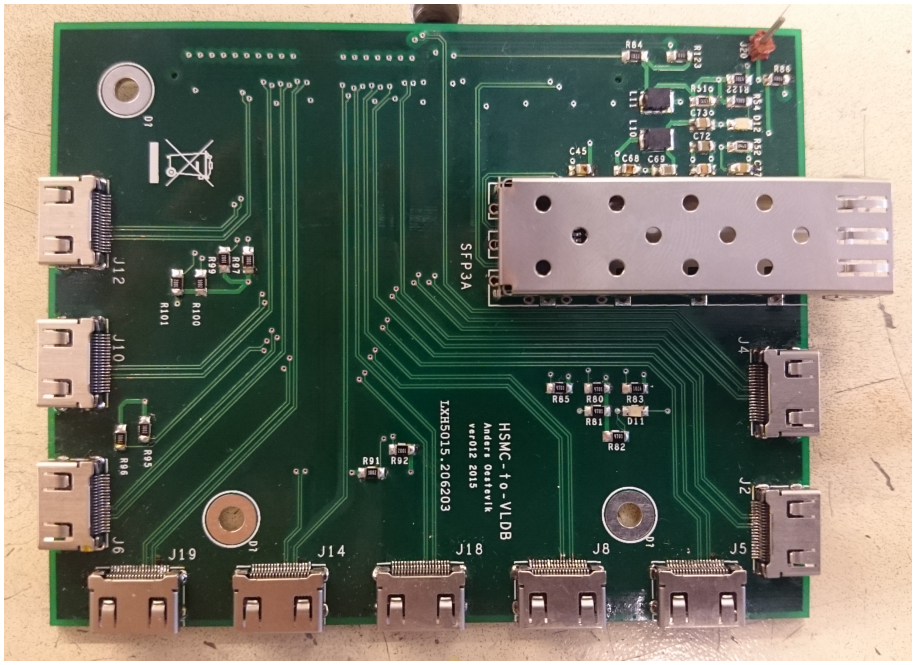


Figure 1.4: HDMI-to-VLDB PCB with components soldered on.

dimensioned a bit longer than the actual pins, making it a bit easier to make contact with the soldering iron when soldering by hand.

1.5 Soldering Process

All the components on the PCB was soldered by hand, with the exception of the ground pads underneath the HSMC, which had to be soldered by oven using solder paste. See **??** for more details about the soldering process.

The finished PCB is shown in figure 1.4. The HSMC contact is located at the bottom of the PCB.

1.6 PCB Faults and Compensations

During the process of hand soldering, it was discovered that the HSMC pads were dimensioned for the purpose of reflow soldering using a solder oven. This meant that the pads were dimensioned to match exactly that of the pins, making it very difficult to solder by hand. With 160 individual pins to be soldered to the PCB board, this resulted in a time-consuming work with a lot of effort trying to keep the pins from shorting. To ease the soldering process of the HSMC, the pads should be dimensioned a bit longer.

After receiving the PCBs, further inspection revealed that all viases had missing solder mask. This exposes the metal of the vias to the surface of the PCB and can possibly cause connection shorts between the viases and the pads and/or metallic casings when

soldering. The reason for the viases not to have a solder mask is because it was missing in the pad file. A solution to fix this in a future PCB print would obviously be to include a solder mask in the pad file. With the current PCB print, however, a temporary solution would be to apply thin *kapton tape* where most critical.

The exposed viases was later shown not to be as critical as first thought, due to the following points:

- The viases that are exposed underneath the HDMI casings are in fact connected to ground, making the possible shorts between the viases and the already ground connected casing not a critical problem.
- The exposed viases underneath the HSMC-connector could potentially connect to the ground pads when applying solder paste to the pads. This was avoided by carefully applying a thin line of solder paste in the middle of the ground pads. This prevented the solder paste to float over to the neighboring viases when melting it in the oven. A possible drawback to this would be bad connection between the ground pads and the HSMC-connector, but a quick check using a multimeter proved that the HSMC was indeed connected to all the ground pads.

In fact, when testing the PCB, the exposure of viases on the transmitter and receiver lines revealed to be quite useful probe points when using an oscilloscope to measure the signal integrity. Due to the lack of extra added probe points, measuring signals at the PCB viases became the most convenient way of directly measuring the signals on the transmitter and receiver lines (see subsection below). A lesson until next PCB-prototype is to include easily accessible probe points on lines that are relevant for oscilloscope measurement.

On the current version of the PCB, some of the receiver lines includes a $10\ \mathrm{k}\Omega$ pull-up resistor (R91, R92, R95, R96, R97, R99, R100 and R101 in figure 1.5). The reason why these are included could possibly be due to a misinterpretation of the SFP-schematic in which the design of the PCB was based on. This is concluded because two of the pull-up resistors (R100 and R101 in the schematic) are connected to receiver signals that are only used in the SFP-design, but not in this design. The pull-up resistor pads were therefore not soldered on the board, and the lines were left open.

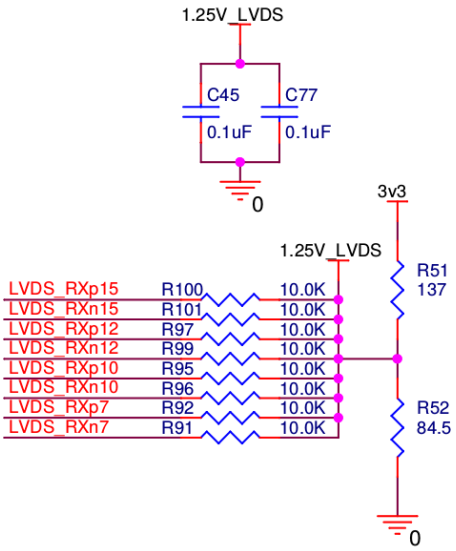


Figure 1.5: Pull-up resistors on some of the receiver lines.