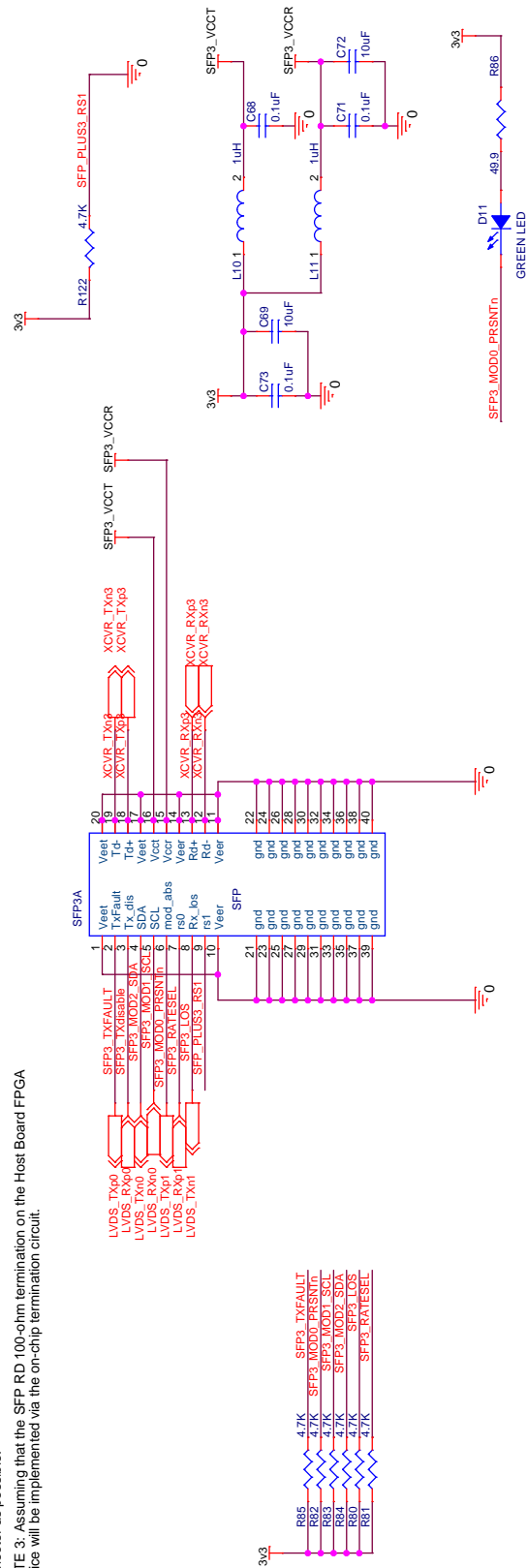


Chapter 1

Schematic and PCB Layout

The schematic of the HSMC-to-VLDB PCB is shown in figures 1.1, 1.2 and 1.3. The PCB layout is shown in figures 1.4 and 1.5. Notes: Do not solder *R91, R92, R95 – R97, R99 – R101*.

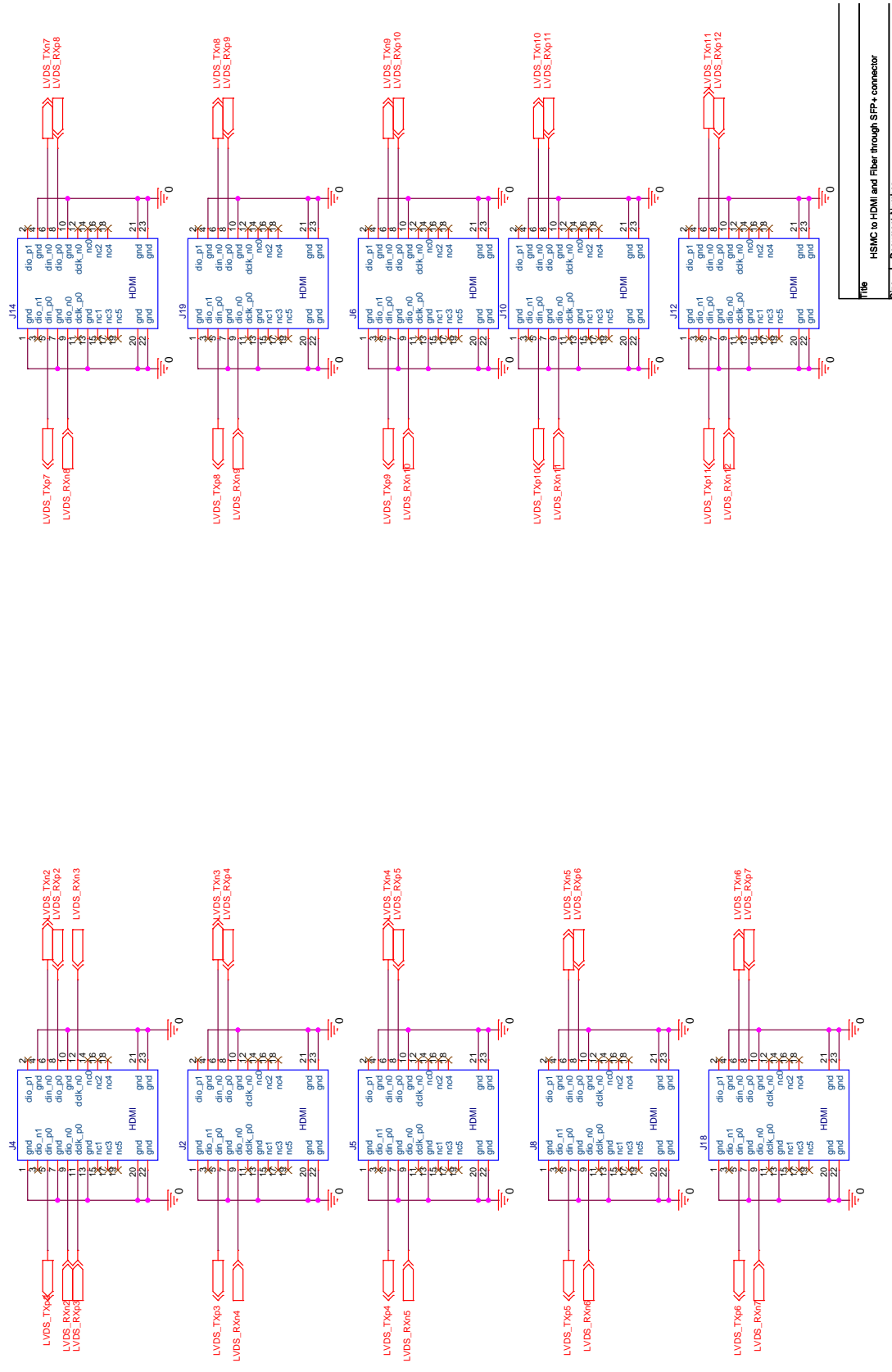


NOTE 1: 1uH ferrite bead should have a DC resistance of less than 1-ohm.

NOTE 2: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 3: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

Figure 1.1: PCB Schematic, SFP connector.



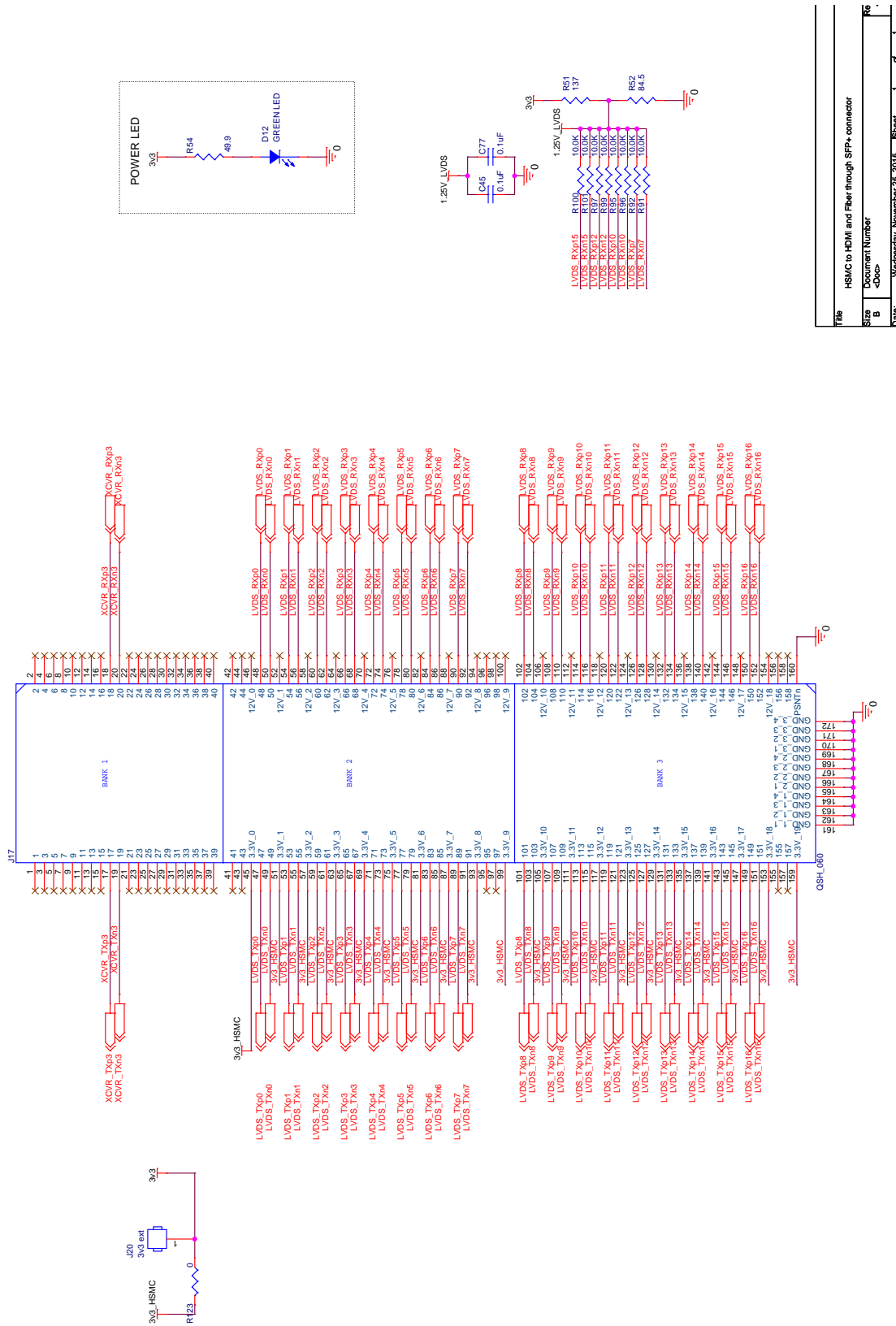
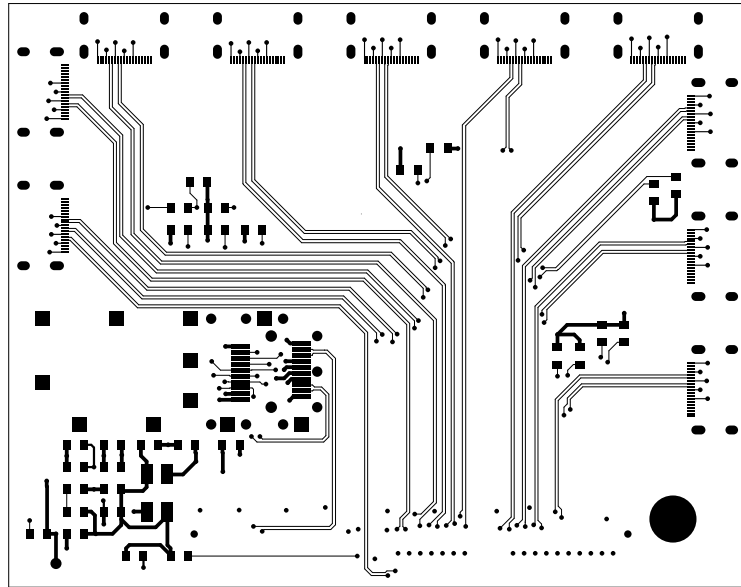
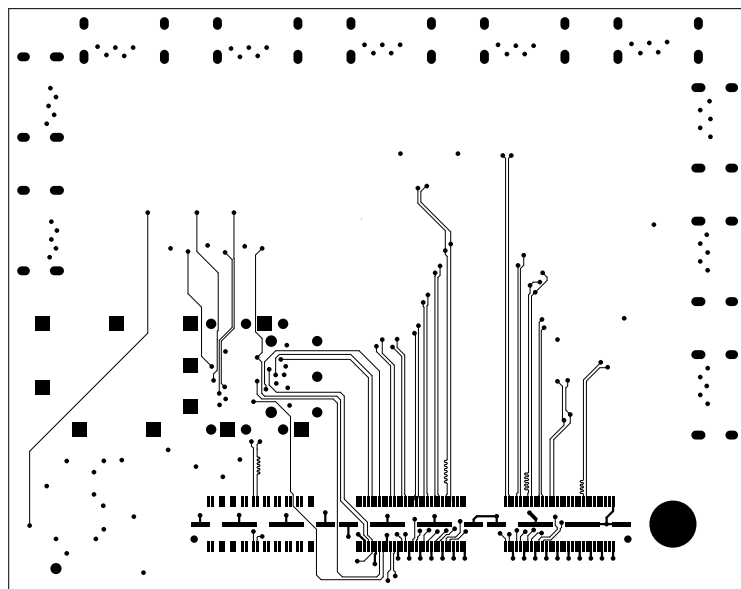


Figure 1.3: PCB Schematic, HSMC connector.

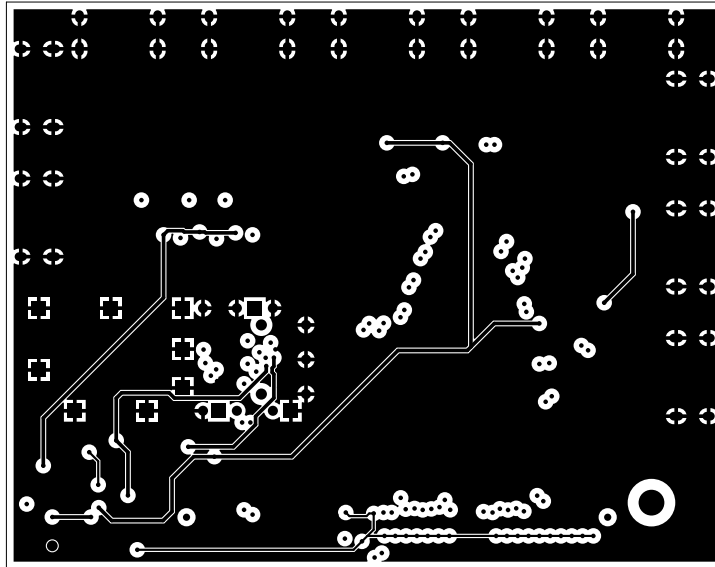


(a) Copper top.

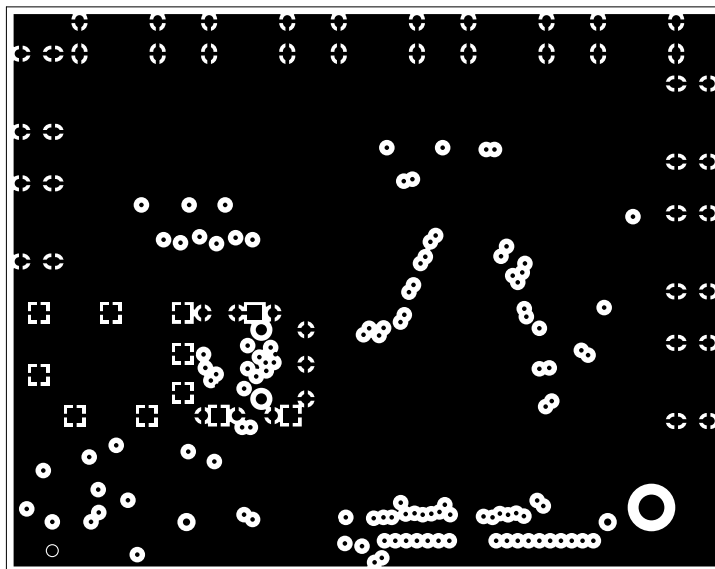


(b) Copper bottom.

Figure 1.4: PCB Layout, top and bottom layers.



(a) Inner layer: voltage.



(b) Inner layer: ground.

Figure 1.5: PCB Layout, inner layers.