Chapter 1

Introduction

1.1 Large Hadron Collider

The Large Hadron Collider (LHC) is the largest and most powerful particle collider in the world. It was built by the European Organization for Nuclear Research (CERN) [**?**] between 1998 and 2008, and had its first start-up on 10 September 2008. This massive machine lies 175 metres under ground, beneath the France–Switzerland border near Geneva, Switzerland; and consists of a 27 km long circular tunnel of superconductor magnets with additional accelerating structures. Its basic operation is to accelerate particles (protons and heavy ions, e.g. Pb) in bunches[1] to near the speed of light in opposite directions and collide them. The particle bunches are accelerated along two parallel beam lines running through the superconductor magnets, and collided at four locations were experiments like; ATLAS[**?**], ALICE[**?**], CMS[**?**] and LHCb[**?**] take place. As of 20 May 2015, the LHC can achieve beam energies up to 13 TeV, or 6.5 TeV per beam. Figure 1.1 shows an overall view of the LHC experiments.

1.2 High-Luminosity LHC

The future upgrade of the LHC accelerator, the High-Luminosity LHC (HL-LHC), has its goal of increasing the beam luminosity by ten times. This will lead to a corresponding growth of the amount of data to be treated by the data acquisition systems, and an increase in radiation. This will thus require high rate data links and Application Specific Integrated Circuits (ASICs) capable of tolerating high doses of radiation.

To address these needs, the GigaBit Transceiver (GBT) ASICs and transmission protocol was developed to provide a high radiation tolerant, high speed, optical transmission line capable of simultaneous transfer of readout data, timing and trigger signals in addition to slow control and monitoring data.

[1] The particles are accelerated in bunches to increase the probability that a collision will occur.

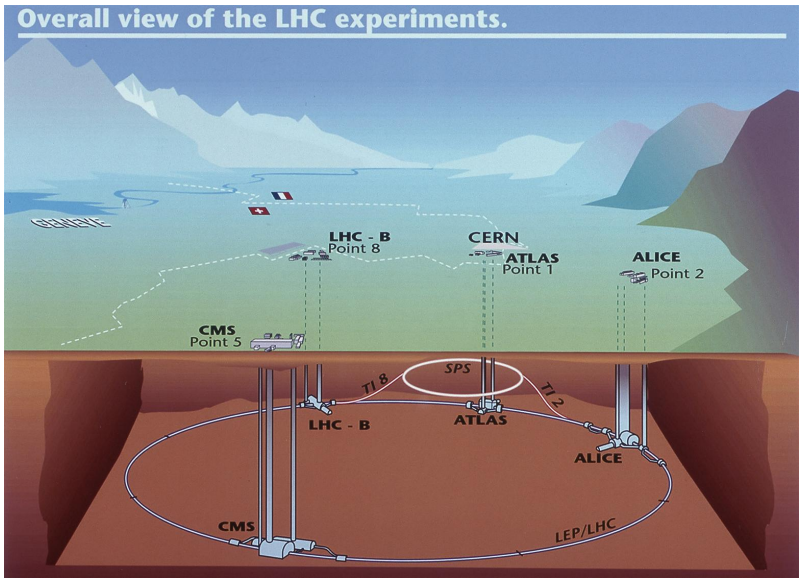

Figure 1.1: LHC overview [**?**].

1.3 The Gigabit Transceiver system

As illustrated in figure 1.2, the GBT system can be separated into two parts: The on-detector part, and the off-detector part of the system. The below sections gives a brief description of these:

1.3.1 On-detector

The on-detector part consists of radiation hard GBT ASICs that will provide interface and data transmission to the detectors and will thus be located in the radiation zone. These ASICs are used to implement bi-directional multipurpose 4.8 Gbit/s optical links for the high-energy physics experiments.

GBTx

The GBTx ASIC is a serializer-de-serializer chip responsible for the high speed bi-directional optical link. It has a bandwidth of $3.2 - 4.8$ Gbit/s, and combines three data paths for Trigger and Timing Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information in one physical link; using two optical fibers. The GBTx encodes and decodes this information into what is known as the GBT-Frame, and provides interface to the front end electronics embedded in the detectors. [**?**]

GBT frame formats

The GBTx transmits a 120-bit frame every 25 ns (40 MHz), which is triggered by LHC particle bunch crossings. The GBTx supports three different encoding modes:

"GBT-Frame", "8B/10B" and "Wide-Bus" mode. Figure 1.3 illustrates the "GBT-Frame" mode. The frame is divided into four parts: Header (H), Slow Control (SC), User Data (D) and Forward Error Correction (FEC). The Header field is a 4-bit field transmitted at the beginning of each frame, used to synchronize the data stream at the frame level. The header field can be set to "idle" (0110) or "data" (0101). The Slow Control field is a 4-bit field dedicated for routine and control operations that do not require precise timing. The User Data field is a 80-bit field reserved for generic transmission of data with a corresponding bandwidth of 3.2 Gbit/s. The remaining field reserves 32 bits for Forward Error Correction. This involves using Reed-Solomon encoding capable of correcting up to 16 concecutive corrupted bits. To achieve DC-balancing, a self-synchronizing scrambler distributes the 0's and 1's in the data stream.

The "8B/10B" and "Wide-Bus" mode share simularities with the "GBT-Frame" mode, but favors data width over reduced error correction (the "Wide-Bus" has none). Both modes are only available in the transmitter part of the GBTx, but requires less resources from the FPGA (1.3.2) than the "GBT-Frame". The "8B/10B" does not require scrambling because it is in itself DC-balanced [**?**]. These two modes are not yet available in the GBT FPGA example design. Both GBTx encoding and decoding operations can be done within a single clock cycle at 40 MHz.

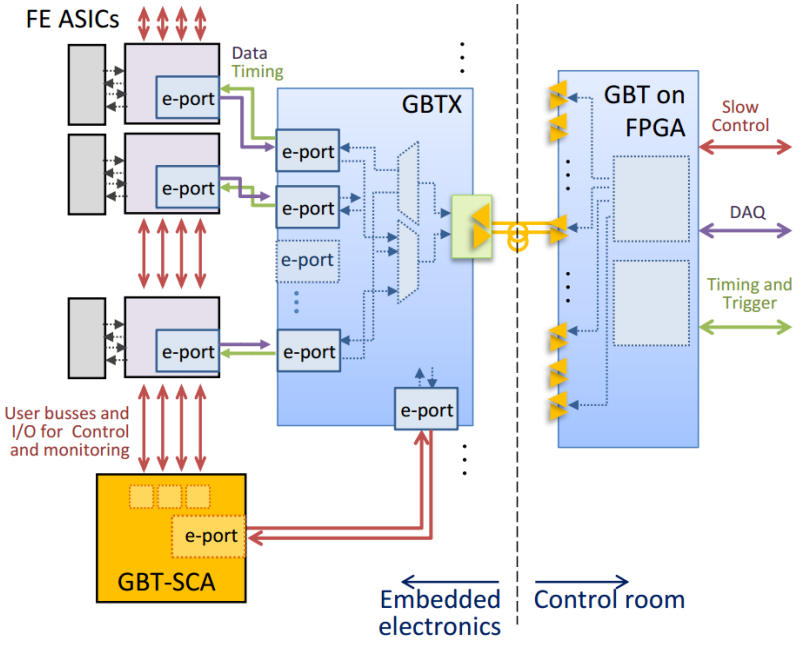

Figure 1.2: The GBT-link in its entirety. The on-detector (Embedded electronics) consists of custom made ASICs with an optical link connecting the off-detector (control room) Field-Programmable Gate Array (FPGA) with the GBT-FPGA implemented. [**?** , Figure 1].

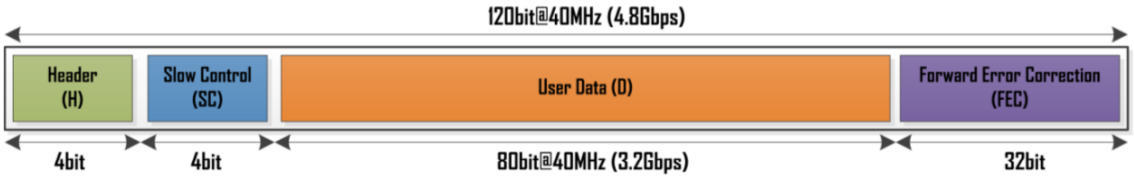

Figure 1.3: The GBT-Frame format. [**?** , Figure 4].

GBT-SCA

The GBT - Slow Control Adapter (GBT-SCA) ASIC is the part of the GBT chipset which distributes control and monitoring signals to the front-end electronics embedded in the detectors. It connects to the GBTx through a dedicated 80 Mbit/s e-link (1.5) and provides a number of user interface options for the front-end detectors, which includes: SPI, I2C, JTAG and a number of GPIOs [**?**].

All chips have been implemented using a commercial 130 nm process because of benefits regarding inherent resistance to ionising radiation [**?**].

1.3.2 Off-detector

The off-detector part is located in the counting room and consists of a Common Readout Unit (CRU), that will provide an interface between the detector ASICs and an online computer farm, with the GBTx as the middle joint. The CRU consists of Commercial Off-The-Shelf (COTS) components, mainly an FPGA, and will through optical links receive the data from the radiation detector.

FPGA - Cyclone V GT

Altera's Cyclone V GT FPGA board was chosen for use in this thesis. It was chosen mainly because of the on-board transceivers that are capable of reaching speeds that surpass the requirements of the GBT-FPGA Multi-Gigabit Transceiver (MGT), i.e 4.8 Gbit/s; "GT" indicates that the FPGA has transceivers that support speeds up to 6 Gbit/s [**?**].

Originally, a Terasic Cyclone V SX development board was aquired for use with this thesis. The Terasic board has advantages over the Cyclone V GT board in terms of communication with the outside world, such as an on-board Usb-to-Uart interface (more on this in chapter **??**). However, it was discovered that the transceivers on the Terasic board were not fast enough for the GBT MGT; maximum supported transceiver speed is only 3.125 Gbit/s [**?**]. Because of this, the more powerful Cyclone V GT FPGA development board was ordered, replacing the Terasic.

GBT-FPGA project

The GBT-FPGA project provides a firmware library for Altera and XilinX FPGAs for communication with the GBTx chipset. It allows for one or several GBT links of type "Standard" or "Latency-Optimized" (The latter providing low, fixed and deterministic latency). Each GBT link is composed of three components: a GBT Rx, a GBT Tx and a MGT. The GBT Rx is responsible for receiving, decoding and de-scrambling the data from the MGT. The GBT Tx is responsible for scrambling and encoding data before transmitting it through the MGT. The MGT is responsible for the actual transmitting, receiving, serialization and de-serialization of the GBT data. It is divided into a transmitter and a receiver: The transmitter shifts in 40 bit words from the GBT Tx, serializes the data and sends it out with the help of a dedicated PLL that generates a serial clock of 2400MHz. The receiver de-serializes the incoming data before shifting it to the GBT Rx. The receiver contains a Clock & Data Recovery (CDR) block to recover the clock signal directly from the incoming data stream [2]. The MGT requires an external clock of 120 MHz.
The GBT link supports all three encodings described in section 1.3.1. [**?**]

GBT-example design

The firmware library comes with an example design that incorporates a single GBT link of the "Standard" type. Included in the example is a pattern generator, connected to the GBT Tx; a pattern checker, connected to the GBT Rx; and a user control interface implemented using the In-System Source And Probe Editor. The example enables for external and internal loopback testing.

1.4 Versatile Link Demo Board

The Versatile Link Demo Board (VLDB) is the evaluation kit for the radiation hard optical link. It includes the main elements of the GBT Link, the radiation hard ASICs; GBTx, GBT-SCA and VTRx/VTTx (optical-link modules), in addition to radiation hard DC/DC converters. The VLDB has 20 e-links reachable through HDMI-connectors that connects to the front-end electronics, and a fiber-optical link that connects to the off-detector FPGA.

1.5 E-Links

E-links are electrical local duplex serial links suitable for transmission over PCBs or cables, within a distance of a few meters, and can operate at any data rate up to

[2]To be able to recover the clock using a CDR, it is important that the serial data has even transitions of 1's and 0's. This is one of the reasons why scrambling the data is important.

320 Mbit/s [3]. It was designed with the GBTx in mind, having radiation hard and single event upset (SEU) resistant transmitter and receiver blocks [**?**]. Each E-link consists of three differential signal lines: a clock line (dClk+/dClk-), a downlink output (dOut+/dOut-) and a uplink input (dIn+/dIn-).

The GBTx arranges e-links in 5 groups, with up to 8 e-links per group corresponding to 16 bits in the uplink and the downlink frames; making a total of 80 bits [**?**]. Each group can be programmed to data rates of 80 Mbit/s, with 8 e-links per group; 160 Mbit/s, with 4 e-links per group; or 320 Mbit/s, with 2 e-links per group. Faster data rates comes with the expense of less physical e-link connections available for the front-end detectors.

1.6 Primary objective

The primary objective of this thesis has been to design a CRU control interface software, along with the design of a Printed Circuit Board (PCB) that provides physical connection between the CRU (FPGA) and the VLDB card. The control interface was developed with the goal of one day replacing the Quartus-bound In-System Source And Probe Editor (ISSP), which is used today to manipulate the GBT control-signals; and instead introduce a cross-platform, open-source solution. The software is not completed, but well on its way to become usable. The PCB is completed, but some testing remains along with a full system test with the GBTx involved.

[3]The GBTx can only handle 320/160/80 Mbit/s

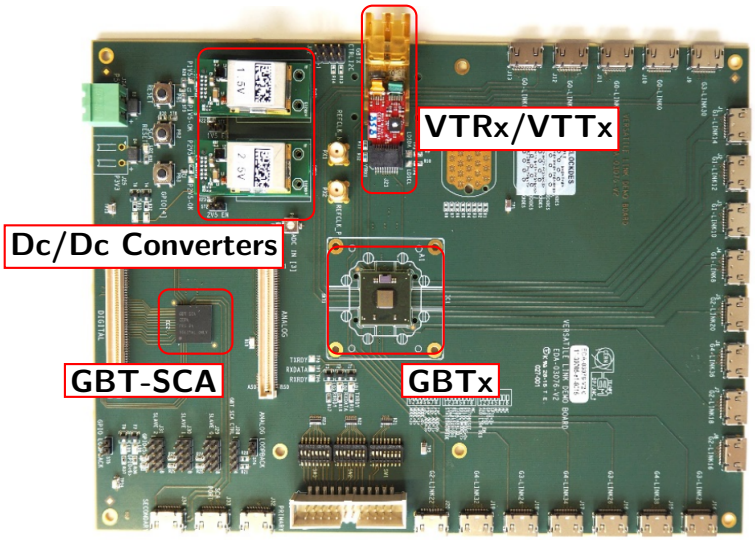

Figure 1.4: Versatile Link Demo Board overview [**?**].

1.7 Outline

This thesis is devided into six chapters, including this one. Chapter 2 gives a brief description of the transceiver technologies that enables communication between the GBTx and the CRU. Chapter 3 gives a brief overview over the process of designing a PCB that connects the FPGA and the VLDB togheter using e-links and optical link. Chapter 4 gives a brief overview of the development of the PC to CRU software design, both on the software and hardware side. Chapter 5 presents the different tests performed on the developed PCB, software and hardware. Because of a damaged FPGA board, not all results were retrieved. The chapter ends with suggestions of future tests to be performed on the system. Finally, chapter 6 summarizes and concludes the thesis.

Chapter 2

Cyclone V Transceiver Technology

For the FPGA to be able to transmit and receive serial data in the gigahertz domain, a high-speed transceiver is required. The Cyclone V GT-series supports a number of transceiver technologies through the High-Speed Mezzanine Card (HSMC) physical interface that can reach speeds up to 5.0 Gbit/s. This section gives a general description of some of these protocols.

2.1 Differential Signals

Common for all protocols described here is the fact that the signals are treated differentially. While a single ended signal involves one conductor between the transmitter and receiver, with the signal swinging from a given voltage to ground; differential signals involve a conductor pair of two signals that are identical, but with opposite polarity. The pair would ideally have equal path lenghts in order to have zero return currents, avoiding problems like Electromagnetic Interference (EMI). In addition, placing the signals as close as possible to one another will give benefits in terms of common-mode noise rejection [**?**].

When implemented correctly, differential signals have advantages over single ended signals such as effective isolation from power systems, minimized crosstalk and noise immunity through common-mode noise rejection. It also improves S/N ratio and effectively doubles the signal level at the output ($+v - (-v) = 2v$), which makes it especially useful in low level signal applications. The disadvantage comes in an increase in pin count and space required, since differential signals consists of two wires instead of one [**?**].

2.2 Low-Voltage Differential Signaling

Low-Voltage Differential Signaling (LVDS) is said to be the most commonly used differential interface. The interface offers a low power consumption with a voltage

swing of 350 mV and good noise immunity. With the right conditions, the standard can be able to deliver data rates up to 3.125 Gbit/s [**?**].

The Cyclone V GT board has 17 LVDS channels available on the HSMC port A connector. The channels have the ability to transmit and receive data at a rate up to 840 Mbit/s, with support for serialization and de-serialization through internal logic [**?**].

2.3 Current-Mode Logic

For data rates that exceeds 3.125 Gbit/s, Current-Mode Logic (CML) signaling is preferred. This is due to the fact that certain communication standards such as PCI-express, SATA and HDMI, shares consistency with CML in signal amplitude and reference to Vcc. CML can reach a data rate in excess of 10 Gbit/s, but has a higher power consumption than LVDS, with a voltage swing of approximately 800 mV [**?**].

The Cyclone V GT board has 4 Pseudo-CML (PCML) channels available on both port A and B HSMC connectors. The channels have the ability to transmit and receive data at a rate up to 5.0 Gbit/s, just over the 4.8 Gbit/s range required by the GBT MGT. [**?**]

Chapter 3

The Gigabit Transceiver

History, mg
Short about
the electron
components
gbt-sca, gbt

The GBT-FPGA project provides the firmware for the FPGA to communicate with the GBTx chipset over the versatile link.

3.1 GBT-FPGA Core

The following sections describe the different components that makes up the GBT-FPGA Core. The information was obtained from the GBT-FPGA User Guide [**?**].

3.1.1 GBT Bank

The GBT Bank is defined as the top module of the GBT-FPGA Core. It integrates up to four GBT Links and contains the ports required to operate the GBT Links.

3.1.2 GBT Link

The GBT Link is the actual channel of the link. It is composed of three components: GBT Tx, GBT Rx, and the MGT. The following subsections gives a brief description of these components.

GBT Tx

The GBT Tx component is responsible for scrambling and encoding data before transmitting it through the MGT.

GBT Rx

The GBT Rx component is responsible for receiving, decoding and de-scrambling the data through the MGT.

Multi-Gigabit Transceiver

The MGT is responsible for the transmitting, receiving, serialization and deserialization of the GBT data. It is divided into a transmitter and a receiver part.
The transmitter contains a PISO[1] with two input clocks; one for parallel data and one for serial data. It shifts in 40 bit words from the GBT Tx with a reference clock of 120 MHz, serializes the data and sends it out with the help of a dedicated Tx Phase-Locked Loop (PLL) that generates a serial clock of 2400MHz.
The receiver contains a CDR block, a SIPO[2], a RXRECCLK Phase Aligner block and a Barrel-shifter.

[1]Short for Parallel In Serial Out, a PISO is a shift-register circuit for serializing input parallel data.

[2]Short for Serial In Parallel Out, a SIPO is a shift-register circuit that converts input serial data into parallel data.