



Department of Physics and Technology

Master Thesis

**Interface Design for the
Gigabit Transceiver Common Readout Unit**

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Overview

Introduction

LHC Upgrade

Gigabit Transceiver System

Primary Objectives

PCB Design

Design Discussion

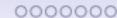
Transmission Lines

GBT Control Software

Hardware

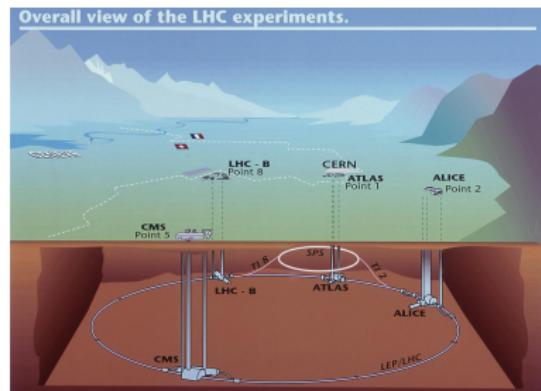
Software





LHC Upgrade

- Large Hadron Collider (LHC)
 - Particle accelerator
 - 27 km circular tunnel
 - 13 TeV
- High-Luminosity LHC
 - 10x beam luminosity
 - Increase in radiation and amount of data
 - → Gigabit Transceiver



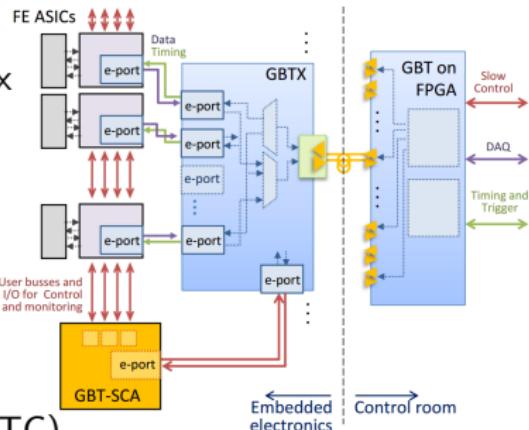
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Gigabit Transceiver System

- On-detector - Custom ASICs
 - GBTx, GBT-SCA, VTTx/VTRx
 - E-links
- Off-detector - Control room
 - CRU (FPGA)
 - > 4.8 Gbit/s transceivers
 - GBT-FPGA
- Optical communication
 - Timing and Trigger Control (TTC)
 - Data Acquisition (DAQ)
 - Slow Control (SC)



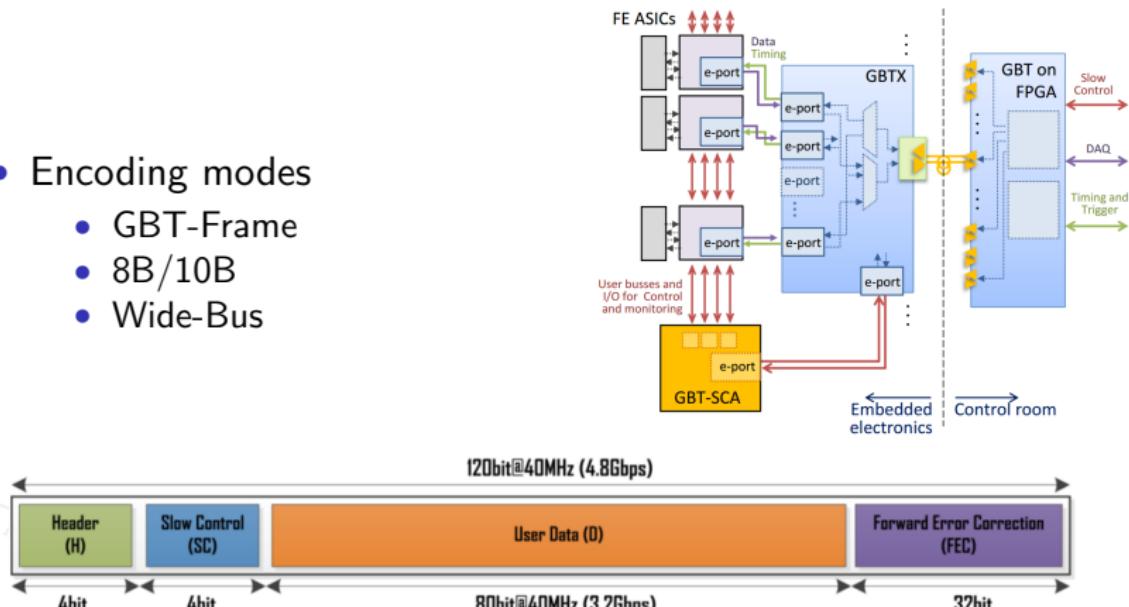
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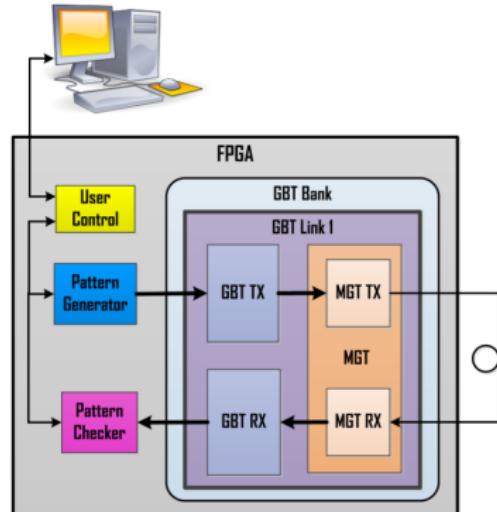
Gigabit Transceiver System

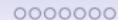
- Encoding modes
 - GBT-Frame
 - 8B/10B
 - Wide-Bus



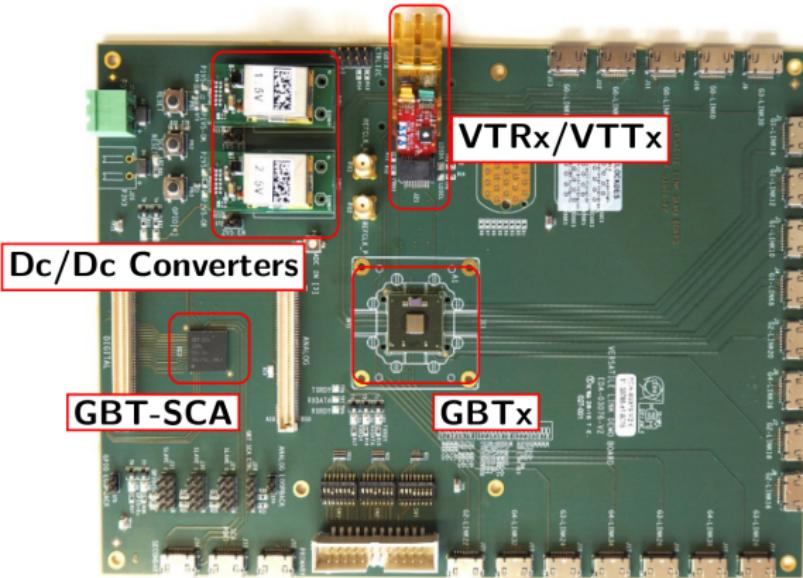
GBT-FPGA

- Firmware library for Altera/Xilinx FPGAs
- GBT Link
 - "Standard", "Latency-Optimized"
 - GBT Rx, GBT Tx, GBT MGT
- GBT-example Design





Versatile Link Demo Board



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Primary Objective

- Software Design
 - Serial communication between PC and CRU
 - Interface allowing control over CRU
- PCB Design
 - Connection between CRU and VLDB

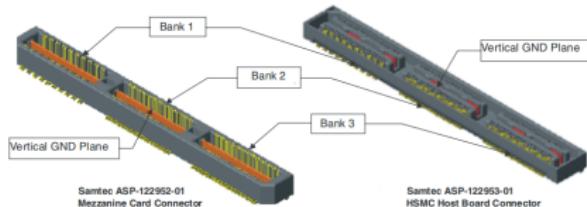


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PCB Design



Specifications:

- Connect to CRU using HSMC-connector
- E-links → 320 Mbit/s detector data → LVDS
- Optical-Fiber → 4.8 Gbit/s GBT data → PCML

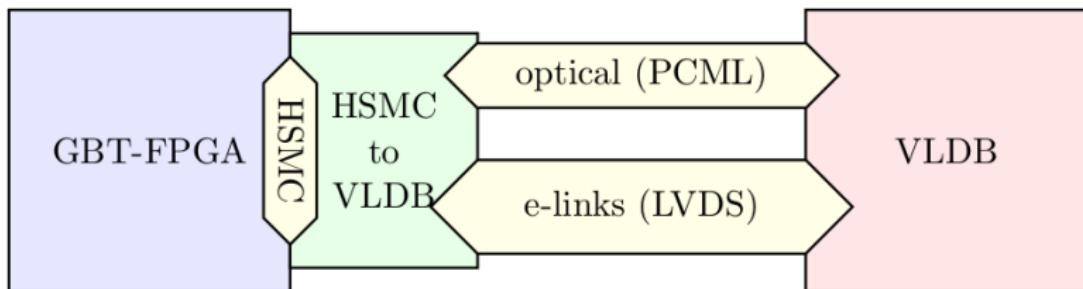


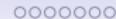
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PCB Design





Transmission Lines

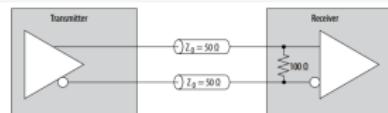
$$v = \frac{c}{\sqrt{\epsilon_r}}$$
$$\epsilon_r \approx 4$$

- $v = 15 \text{ cm/ns}$
- 4.8 Gbit/s (0.2 ns) → transmission line if trace < 3.1 cm
- Characteristic impedance, $Z_0 = 50$
- Differential impedance, $Z_{diff} = 100$



Figure 5-17: Differential Input OCT

The Cyclone V devices support OCT for differential LVDS and SLVS input buffers with a nominal resistance value of 100 Ω , as shown in this figure.



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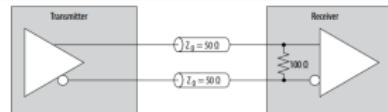
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Design Parameters

- Routing differential signals:
 - Equal trace lengths on each pair
 - As close as possible, but keep distance to other pairs
 - As straight paths as possible

Figure 5-17: Differential Input OCT

The Cyclone V devices support OCT for differential LVDS and SLVS input buffers with a nominal resistance value of 100Ω , as shown in this figure.

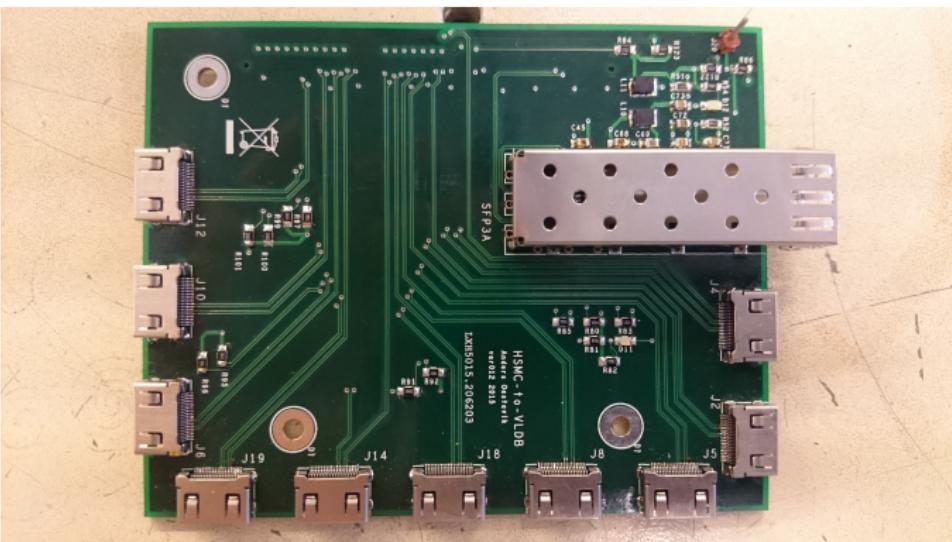


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Result

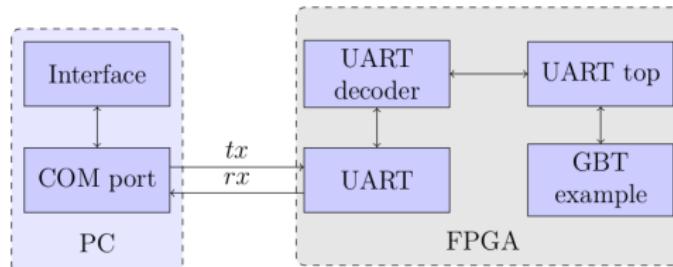


- Each HDMI has an input pair and an output pair
- J4 has an additional pair for input clock from VLDB

GBT Control Software

Specifications:

- Send/receive control signal information
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Hardware

Components:

- UART (RX, TX, Buffers, baudrate generator)
- Decoder
- GBT example (not implementet yet)



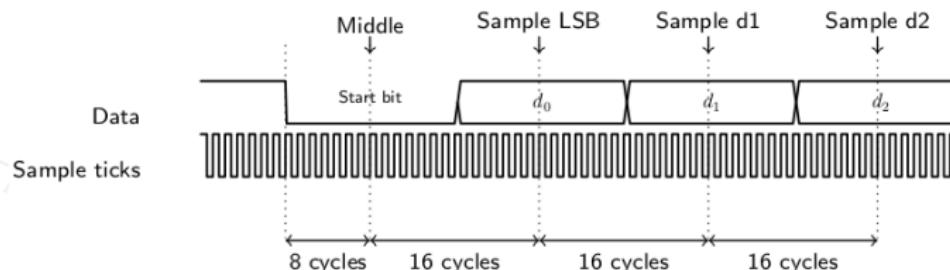
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UART

- Synchronisation → Oversampling
- $16 \times \text{baudrate}$
- Stores bytes in FIFO-buffers
- $19200 - 8 - N - 1 \rightarrow 307200$ sample clock



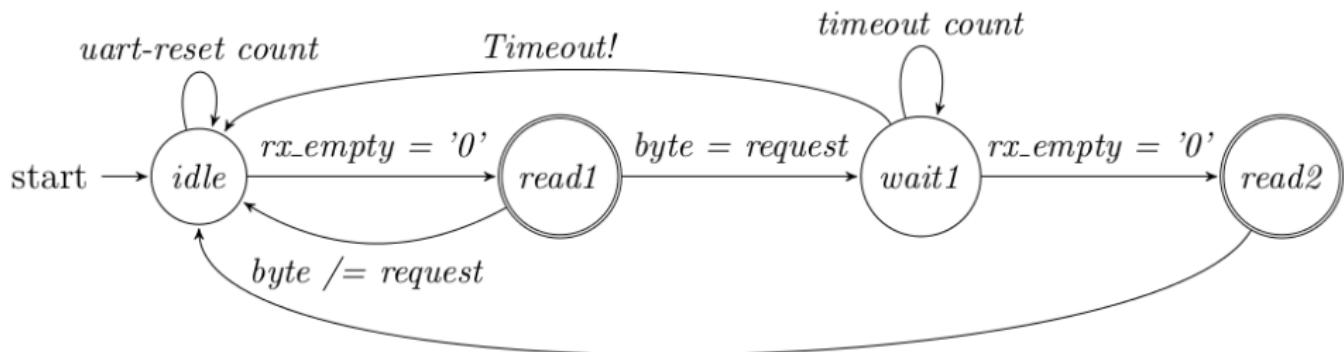
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Decoder

- Requests:
 - read → 0xDD
 - write 0 → 0xEE
 - write 1 → 0xFF
- Legal addresses:
 - 0x00 → 0x41
- Bytes sent to PC:
 - 0x00 → 0xC1



Conclusion

Hardware:

- UART + Decoder works
- Implementation into the GBT Example Design remains

Software:

- Send/Receive and User Interface modules works
- Both needs to be merged

Final testing of the system as a whole remains



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Software

Modules:

- Send/receive
- User Interface



Introduction

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PCB Design

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GBT Control Software

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Thank you!

