Chapter 1

Introduction

1.1 LHC

The Large Hadron Collider (LHC) is the largest and most powerful particle collider in the world. It was built by the European Organization for Nuclear Research (CERN) [**?**] between 1998 and 2008, and had its first start-up on 10 September 2008. This massive machine lies 175 metres deep beneath the France–Switzerland border near Geneva, Switzerland; and consists of a $27\ \mathrm{km}$ long circular tunnel of superconductor magnets with additional accelerating structures. Its basic operation is to accelerate particles (protons and heavy ions, e.g. Pb) to near the speed of light in opposite directions and collide them. The particles are accelerated along two parallel beam lines running through the superconductor magnets, and collided at four locations were experiments like ATLAS[**?**], ALICE[**?**], CMS[**?**] and LHCb[**?**] take place. As of 20 May 2015, the LHC can achieve beam energies up to $13\ \mathrm{T}e\mathrm{V}$, or $6.5\ \mathrm{T}e\mathrm{V}$ per beam.

1.2 SLHC

The future upgrade of the LHC accelerator, the Super Large Hadron Collider (SLHC), has its goal of increasing the beam luminosity by ten times. This will lead to a corresponding growth of the amount of data to be treated by the data acquisition systems, and an increase in radiation. This will thus require high rate data links and Application Specific Integrated Circuits (ASICs) capable of tolerating high doses of radiation.

To address these needs, the Gigabit Transceiver (GBT) architecture and transmission protocol was developed to provide a high radiation tolerant, high speed, optical transmission line capable with a simultaneous transfer of readout data, timing and trigger signals in addition to slow control and monitoring data.

1.3 GBT system

The GBT system can be described in two parts: The on-detector part, and the off-detector part of the system. The below sections gives a brief description of these:

1.3.1 On-detector

The on-detector part consists of radiation hard GBT ASICs that will act as detectors and will thus be located in the radioactive zone. These ASICs are used to implement bi-directional multipurpose $4.8\ \mathrm{Gbit/s}$ optical links for the high-energy physics experiments.

GBTx

The GBTx ASIC is a serializer-de-serializer chip responsible for the high speed bi-directional optical link. It has a bandwidth of $3.2 - 4.8\ \mathrm{Gbit/s}$, and combines three data paths for Trigger and Timing Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information in one physical link; using two optical fibers. The GBTx encodes and decodes this information into what is known as the GBT-Frame, and provides interface to the front end electronics embedded in the detectors. [**?**]

GBT frame formats

The GBTx transmits a 120-bit frame every $25\ \mathrm{ns}$ ($40\ \mathrm{MHz}$), which is triggered by LCH bunch crossings. The GBTx supports three different encoding modes: "GBT-Frame", "8B/10B" and "Wide-Bus" mode. Figure 1.1 illustrates the "GBT-Frame" mode: The Header (H) field is a 4-bit field transmitted at the beginning of each frame, used to synchronize the data stream at the frame level. The header field can be set to "idle" (0110) or "data" (0101). The Slow Control (SC) field is a 4-bit field dedicated for routine and control operations that do not require precise timing. The Data field is a 80-bit field reserved for generic transmission of data with a corresponding bandwidth of $3.2\ \mathrm{Gbit/s}$. The remaining field reserves 32 bits for Forward Error Correction (FEC). FEC involves using Reed-Solomon encoding capable of correcting up to 16 concecutive corrupted bits. To achieve DC-balancing, a self-synchronizing scrambler distributes the 0's and 1's in the data stream.

The "8B/10B" and "Wide-Bus" mode share simularities with the "GBT-Frame" mode, but favors data width over lesser grades of error correction (the "Wide-Bus" has none). Both modes are only available in the transmitter part of the GBTx, but requires less resources from the Field-Programmable Gate Array (FPGA) (receiving end) than the "GBT-Frame". The "8B/10B" does not require scrambling because it is in itself DC-balanced. [**?**]. These two modes are not yet available in the GBT FPGA example design.

Both GBTx encoding and decoding operations can be done within a single clock cycle at $40\ \mathrm{MHz}$.

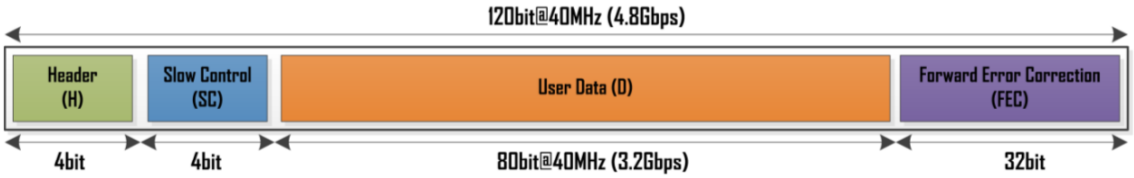

Figure 1.1: The GBT-Frame format. [**?** , Figure 4].

GBT-SCA

The GBT - Slow Control Adapter (GBT-SCA) ASIC is the part of the GBT chipset which distributes control and monitoring signals to the front-end electronics embedded in the detectors. It connects to the GBTx through a dedicated $80\ \mathrm{Mbit/s}$ e-link and provides a number of user interface options for the front-end detectors, which includes: SPI, Inter-Integrated Circuit (I2C), JTAG and a number of GPIOs [**?**].

All chips has been implemented using a commercial $130\ \mathrm{nm}$ process because of benefits regarding inherent resistance to ionising radiation [**?**].

1.3.2 Off-detector

The off-detector part is located in the counting room and consists of a Common Readout Unit (CRU), that will provide an interface between the detector ASICs and an online computer farm, with the GBTx as the middle joint. The CRU consists of Commercial Off-The-Shelf (COTS) components, mainly an FPGA, and will through optical links receive the data from the radiation detector.

FPGA - Cyclone V GT

Altera's Cyclone V GT FPGA board was chosen for use in this thesis. It was chosen mainly because of the on-board transceivers that are capable of reaching speeds that surpass the requirements of the GBT-FPGA Multi-Gigabit Transceiver (MGT), i.e $4.8\ \mathrm{Gbit/s}$; "GT" indicates that the FPGA has transceivers that support speeds up to $6\ \mathrm{Gbit/s}$ [**?**].
Originally, a Terasic Cyclone V GX development board was handed for use with this thesis. The Terasic board has advantages over the Cyclone V GT board in terms of communication with the outside world, such as on-board Usb-to-Uart (more on this in chapter **??**). However, it was discovered that the transceivers on the Terasic board were not fast enough for the GBT MGT; maximum supported transceiver speed is only $3.125\ \mathrm{Gbit/s}$ [**?**]. Because of this, the more powerful Cyclone V GT FPGA development board was ordered from the Altera web-pages, replacing the Terasic.

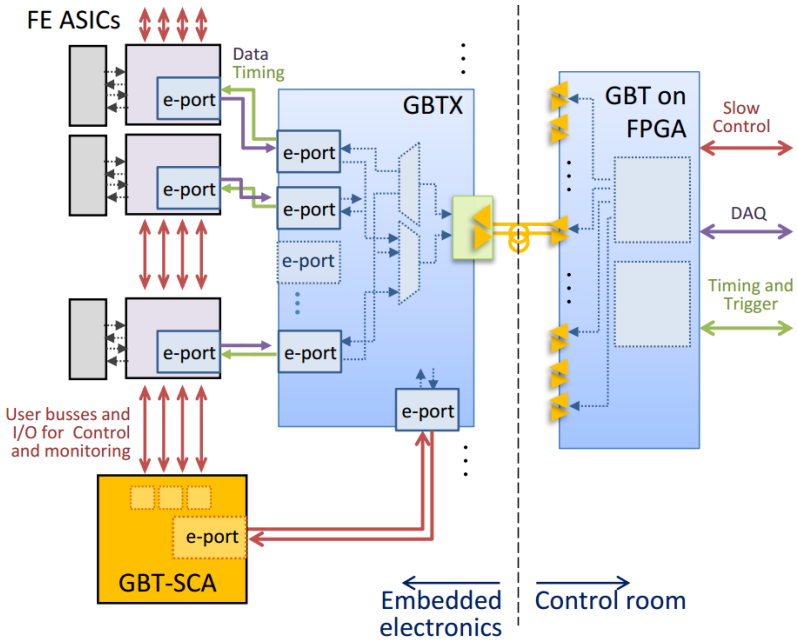

Figure 1.2: The GBT-link in its entirety. The on-detector consists of custom made ASICs with an optical link connecting the off-detector FPGA with the GBT-FPGA implemented. [? , Figure 1].

1.4 Versatile Link Demo Board

The Versatile Link Demo Board (VLDB) is the evaluation kit for the radiation hard optical link. It includes the main elements of the GBT Link, the radiation hard ASICs; GBTx, GBT-SCA and the VTRx/VTTx, in addition to radiation hard DC/DC converters. The VLDB has 20 e-links reachable through High-Definition Multimedia Interface (HDMI) connectors that connects to the front-end electronics, and a fiber-optic link that connects to the off-detector FPGA.

1.5 E-Links

An E-link is an electrical interface suitable for transmission Each E-link has three differential signal lines: a clock line (dClk+/dClk-), a downlink output (dOut+/dOut-) and a uplink input (dIn+/dIn-).

1.6 Primary objective

This thesis has its focus on the design of a CRU control interface software, and also a physical connection between the CRU and the VLDB card, where the radiation hard ASIC, the GBTx, is located. The control interface was developed with the goal of one day

replacing the Quartus-bound In-System Source And Probe Editor (ISSP), which is used today to manipulate the GBT control-signals; and instead introduce a cross-platform, open-source solution.

1.7 Outline

Chapter 2

Cyclone V Transceiver Technology

To be able to send serial data in the gigahertz domain, a high-speed transceiver is required. The Cyclone V GT-series FPGAs supports a number of transceiver technologies through the High-Speed Mezzanine Card (HSMC) physical interface that can reach speeds up to $6.144\ \mathrm{Gbit/s}$. This section gives a general description of some of these protocols.

2.0.1 Differential Signals

Common for all protocols described is the fact that the signals are treated differentially.

While a single ended signal involves one conductor between the transmitter and receiver, with the signal swinging from a given voltage to ground; differential signals involves a conductor pair with two signals that are identical, but with opposite polarity. The pair would ideally have equal path lenghts in order to have zero return currents, avoiding problems like *EMI*. In addition, placing the signals as close as possible to one another will give benefits in terms of common noise rejection [**?**].

When done correctly, differential signals have advantages over single ended signals such as effective isolation from power systems, minimized crosstalk and noise immunity through common-mode noise rejection. It also improves S/N ratio and effectively doubles the signal level at the output $(+v - (-v) = 2v)$, which makes it especially useful in low signal applications. The disadvantage comes in an increase in pin count and space required, since differential signals consists of two wires instead of one [**?**].

2.0.2 Low-Voltage Differential Signaling

Low-Voltage Differential Signaling (LVDS) is said to be the most commonly used differential interface. The interface offers a low power consumption with a voltage swing of $350\ \mathrm{mV}$ and good noise immunity. LVDS can deliver data rates up to $3.125\ \mathrm{Gbit/s}$ [**?**].

The Cyclone V GT board has 17 LVDS channels available on the HSMC port A connector. The channels have the ability to transmit and receive data at a rate up to

$840\ \mathrm{Mbit/s}$, with support for serialization and deserialization through internal logic. [**?**]

2.0.3 Current-Mode Logic

For data rates that exceeds $3.125\ \mathrm{Gbit/s}$, Current-Mode Logic (CML) signaling is preferred. This is due to the fact that certain communication standards such as PCIe, SATA and HDMI, shares consistency with CML in signal amplitude and reference to Vcc. CML can reach a data rate in excess of $10\ \mathrm{Gbit/s}$, but has a higher power consumption than LVDS, with a voltage swing of approximately $800\ \mathrm{mV}$ [**?**].

The Cyclone V GT board has 4 Pseudo-CML (PCML) channels available on both port A and B HSMC connectors. The channels have the ability to transmit and receive data at a rate up to $5.0\ \mathrm{Gbit/s}$, just over the $4.8\ \mathrm{Gbit/s}$ range required by the GBT MGT. [**?**]

Chapter 3

The Gigabit Transceiver

History, mg
Short about
the electron
components
gbt-sca, gbt

3.1 Encoding modes

The ”GBT-Frame” mode, which is Reed-Solomon Based; the ”8b10b” mode; and the ”Wide-Bus” mode which is without encoding.

3.2 GBT-FPGA Core

The following sections describe the different components that makes up the GBT-FPGA Core. The information was obtained by reading the GBT-FPGA User Guide [**?**].

3.2.1 GBT Bank

The GBT Bank is defined as the top module of the GBT-FPGA Core. It integrates up to four GBT Links and contains the ports required to operate the GBT Links.

3.2.2 GBT Link

The GBT Link is the actual channel of the link. It is composed of three components: GBT Tx, GBT Rx, and the MGT. The following subsections gives a brief description of these components.

GBT Tx

The GBT Tx component is responsible for scrambling and encoding data before transmitting it through the MGT.

GBT Rx

The GBT Rx component is responsible for receiving, decoding and de-scrambling the data through the MGT.

Multi-Gigabit Transceiver

The MGT is responsible for the transmitting, receiving, serialization and de-serialization of the GBT data. It is divided into a transmitter and a receiver part.
The transmitter contains a PISO with two input clocks; one for parallel data and one for serial data. It shifts in $40\ \mathrm{bit}$ words from the GBT Tx with a reference clock of $120\ \mathrm{MHz}$, serializes the data and sends it out with the help of a dedicated Tx Phase-Locked Loop (PLL) that generates a serial clock of $2400\mathrm{MHz}$.
The receiver contains a Clock & Data Recovery (CDR) block, a SIPO, a RXRECCLK Phase Aligner block and a Barrel-shifter.