Appendices

Index	Name	Description
P00	LATENCY-OPTIMIZED GBT LINK - TX	Indicates whether the Gigabit Transceiver (GBT) example design is using the latency optimized ('1') version or not ('0').
P01	LATENCY-OPTIMIZED GBT LINK - RX	Indicates whether the GBT example design is using the latency optimized ('1') version or not ('0').
P02	MGT TX PLL LOCKED	Shows the status of the MGT pll, and remains high ('1') if the pll is locked.
P03	TX_FRAMECLK PHASE ALIGNER - PLL LOCKED	Related to the latency optimized version.
P04	TX_FRAMECLK PHASE ALIGNER - PHASE SHIFT DONE	Related to the latency optimized version
P[05..12]	TX_WORDCLOCK MONITORING - STATS	Related to the latency optimized version
P13	TX_WORDCLOCK MONITORING - TX_WORDCLK PHASE OK	Related to the latency optimized version
P14	MGT READY	Asserted high ('1') to show that the MGT transceiver is ready.
P15	RX_WORDCLK READY	Asserted high ('1') to show that the RX_WORDCLK is ready.
P16	RX_FRAMECLK READY	Asserted high ('1') to show that the RX_FRAMECLK is ready.
P17	RX GBT READY	Asserted high ('1') to show that the receiver of the GBT-link is ready.
P[18..23]	RX BITSLIP NUMBER	Related to the latency optimized version, and must remain at "00h" to indicate that the RX and TX are properly aligned.
P24	RX HEADER IS DATA FLAG	Indicates whether the received data has a header of the frame that is idle ('0') or data ('1').
P25	RX GBT READY LOST FLAG	Indicates that the connection has been lost, and remains high until **S09** is asserted high.
P26	RX DATA ERROR SEEN FLAGS	Is asserted high ('1') if the pattern checker detects an indifference in the transmitted and received pattern.
P27	RX EXTRA DATA WIDE-BUS ERROR SEEN FLAG	Same as for **P26**, only related to the *wide-bus* mode.
P28	RX EXTRA DATA GBT8B10B ERROR SEEN FLAG	Same as for **P26**, only related to the *8B10B* mode.
P29	ISSP PLL Locked	Shows the status of the issp pll. This signal does not need to be monitored by the serial interface.

Table 1: GBT control signals overview, probes.

Index	Name	Description
S00	LOOPBACK	Select internal loopback inside the transceiver ('1'), or an external loopback via cabling ('0').
S01	GENERAL RESET	Main reset signal of the example design.
S02	MGT TX PLL RESET	Individual reset signal for the MGT pll.
S03	TX RESET	Individual reset signal for the transceiver.
S04	RX RESET	Individual reset signal for the receiver.
S[05..06]	PATTERN SELECT	Selects the pattern that is sent through the transmitter line. It can send a counter value ("1h") that increments by 1, or a static value ("2h").
S07	TX HEADER SELECTOR	Chooses the header of the frame: '0' for idle and '1' for data.
S08	RESET DATA & EXTRA DATA ERROR SEEN FLAGS	Resets **P26**.
S09	RESET RX GBT READY LOST FLAG	Resets **P25**.
S10	TX_FRAMECLK PHASE ALIGNER - MANUAL RESET	Related to the latency optimized version.
S[11..16]	TX_FRAMECLK PHASE ALIGNER - GBT LINK 1 STEPS	Related to the latency optimized version.
S17	TX_FRAMECLK PHASE ALIGNER - ENABLE	Related to the latency optimized version.
S18	TX_FRAMECLK PHASE ALIGNER - TRIGGER	Related to the latency optimized version.
S[19..26]	TX_WORDCLOCK MONITORING - THRESHOLD UP	Related to the latency optimized version.
S[27..34]	TX_WORDCLOCK MONITORING - THRESHOLD LOW	Related to the latency optimized version.
S35	TX_WORDCLOCK MONITORING - TX RESET ENABLE	Related to the latency optimized version.

Table 2: GBT control signals overview, switches.