Assignment 1, Part 3: Hardware Hiding

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# Introduction

Part 3 of Assignment 1 includes all the hardware hiding components of the pacemaker design. Hardware hiding has been implemented by noticing that all pacemaker modes have the same pacing and sensing procedure, so one component was made for each to deal directly with the hardware pins and exchange simplified information only when needed with the main software implementation.

# Variables

## Measured

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Units/Type** | **Description** | **Range** |
| t | ms | time since start of pulse | – |
| A\_pace\_start | boolean | Commence atrial pulse | {true, false} |
| V\_pace\_start | boolean | Commence ventricular pulse | {true, false} |
| ATR\_CMP\_DETECT | boolean | Atrial signal voltage higher than threshold | {true, false} |
| VENT\_CMP\_DETECT | boolean | Ventricular signal voltage higher than threshold | {true, false} |

## Constant

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Units/Type** | **Description** | **Range** |
| p\_mode | int | Pacemaker operational mode | {AOO,VOO,AAI,VVI} |
| p\_atr\_pulse\_amplitude | V | Desired amplitude of paced atrial pulses | 0.5–7.0 ± 12% |
| p\_vent\_pulse\_amplitude | V | Desired amplitude of paced ventricular pulses | 0.5–7.0 ± 12% |
| p\_atr\_pulse\_width | ms | Desired pulse width of paced atrial pulses | 0.05–1.9 ± 0.2 ms |
| p\_vent\_pulse\_width | ms | Desired pulse width of paced ventricular pulses | 0.05–1.9 ± 0.2 ms |

## Controlled

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Units/Type** | **Description** | **Range** |
| h\_atr\_pulse\_detected | boolean | Pulse detected in atrium | {true, false} |
| h\_vent\_pulse\_detected | boolean | Pulse detected in ventricle | {true, false} |
| PACE\_CHARGE\_CTRL | boolean | PWM connected to primary capacitor | {true, false} |
| ATR\_PACE\_CTRL | boolean | Atrial ring connected to primary capacitor | {true, false} |
| VENT\_PACE\_CTRL | boolean | Ventricular ring connected to primary capacitor | {true, false} |
| ATR\_GND\_CTRL | boolean | Atrial ring connected to ground | {true, false} |
| VENT\_GND\_CTRL | boolean | Ventricular ring connected to ground | {true, false} |
| PACE\_GND\_CTRL | boolean | Atrial and Ventricular tip connected to blocking capacitor | {true, false} |
| Z\_ATR\_CTRL | boolean | Impedance circuit connected to atrial ring | {true, false} |
| Z\_VENT\_CTRL | boolean | Impedance circuit connected to ventricular ring | {true, false} |
| PACING\_REF\_PWM | % | Reference PWM for primary capacitor | 0–100 |
| ATR\_CMP\_REF\_PWM | % | Reference PWM for atrial signal comparator | 0–100 |
| VENT\_CMP\_REF\_PWM | % | Reference PWM for ventricular signal comparator | 0–100 |
| FRONTEND\_CTRL | boolean | Sensing circuit connected to leads | {true, false} |

## Internal

No internal variables

# Interfaces

## **Pacing**

### Description

The pacing component controls the pacing reference pulse width modulation and the control signals in the pacing circuitry. It has two input signals, A\_pace\_start and V\_pace\_start which are both normally false. When a 1 ms pulse is detected on either, the appropriate control signals are set to pace the appropriate chamber.

### Variables

#### Measured

|  |  |  |
| --- | --- | --- |
| **Name** | **Abbreviation** | **Reference** |
| t | – | 2.1 |
| A\_pace\_start | – | 2.1 |
| V\_pace\_start | – | 2.1 |

#### Constant

|  |  |  |
| --- | --- | --- |
| **Name** | **Abbreviation** | **Reference** |
| p\_mode | – | 2.2 |
| p\_atr\_pulse\_amplitude | – | 2.2 |
| p\_vent\_pulse\_amplitude | – | 2.2 |
| p\_atr\_pulse\_width | – | 2.2 |
| p\_vent\_pulse\_width | – | 2.2 |

#### Controlled

|  |  |  |
| --- | --- | --- |
| **Name** | **Abbreviation** | **Reference** |
| PACE\_CHARGE\_CTRL | – | 2.3 |
| ATR\_PACE\_CTRL | – | 2.3 |
| VENT\_PACE\_CTRL | – | 2.3 |
| ATR\_GND\_CTRL | – | 2.3 |
| VENT\_GND\_CTRL | – | 2.3 |
| PACE\_GND\_CTRL | – | 2.3 |
| Z\_ATR\_CTRL | – | 2.3 |
| Z\_VENT\_CTRL | – | 2.3 |
| PACING\_REF\_PWM | – | 2.3 |

#### Internal

No internal values

### Initial values

ATR\_PACE\_CTRL = false

VENT\_PACE\_CTRL = false

ATR\_GND\_CTRL = false

VENT\_GND\_CTRL = false

Z\_ATR\_CTRL = false

Z\_VENT\_CTRL = false

PACE\_CHARGE\_CTRL = true

PACE\_GND\_CTRL = true

### Requirements

Z\_ATR\_CTRL = false

Z\_VENT\_CTRL = false

|  |  |
| --- | --- |
| **p\_mode** | **PACING\_REF\_PWM** |
| AOO | p\_atr\_pulse\_amplitude/0.05 |
| VOO | p\_vent\_pulse\_amplitude/0.05 |
| AAI | p\_atr\_pulse\_amplitude/0.05 |
| VVI | p\_vent\_pulse\_amplitude/0.05 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A pace start** | **V pace start** | **A pace start-1** | **V pace start-1** | **PACE CHARGE CTRL** | **ATR PACE CTRL** | **VENT PACE CTRL** | **ATR GND CTRL** | **VENT GND CTRL** |
| false | false | false | true | true | false | false | false | true |
| true | false | true | false | false | true | false |
| true | X | X | false | false | true | false | false |
| true | false | X | X | false | true | false | false | false |
| true | X | X | ILLEGAL INPUTS | | | | |

### State Transitions

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | INITIAL | C22\_Charge | Buffer | A\_pacing | C21\_Discharge\_A | V\_pacing | C21\_Discharge\_V |
| INITIAL | – | Automatic | – | – | – | – | – |
| C22\_Charge | – | – | ~A\_pace\_start  ~V\_pace\_start | – | – | – | – |
| Buffer | – | – | – | A\_pace\_start | – | V\_pace\_start | – |
| A\_pacing | – | – | – | – | t=p\_atr\_pulse\_width | – | – |
| C21\_Discharge\_A | – | Automatic | – | – | – | – | – |
| V\_pacing | – | – | – | – | – | – | t=p\_vent\_pulse\_width |
| C21\_Discharge\_V | – | Automatic | – | – | – | – | – |

### State details

|  |  |
| --- | --- |
| **State** | **Description** |
| INITIAL | Sets initial values |
| C22\_Charge | Starts charging pacing capacitor |
| Buffer | Waits until pace start signals are low |
| A\_pacing | Paces atrium |
| C21\_Discharge\_A | Discharges blocking capacitor through atrium |
| V\_pacing | Paces ventricle |
| C21\_Discharge\_V | Discharges blocking capacitor through ventricle |

### Design details

The buffer state is necessary to make sure the pacing doesn’t loop.

### Future changes

Eventually, dual pacing modes will have to be implemented. The states will have to modified to change pacing between the atrium and ventricle.

### Stateflow Screenshot

Diagram

Description automatically generated

### Testing

|  |  |  |  |
| --- | --- | --- | --- |
| **Test Case** | **Expected Result** | **Actual Result** | **Pass/Fail** |
| p\_mode: AOO  p\_lower\_rate\_limit: 60 BPM | Pacing at 60 BPM | Pacing at 60 BPM | Pass |
| p\_mode: VOO  p\_lower\_rate\_limit: 60 BPM | Pacing at 60 BPM | Pacing at 60 BPM | Pass |

Test 1

Chart, box and whisker chart

Description automatically generated

Test 2

A picture containing chart

Description automatically generated

## **Sensing**

### Description

The sensing component controls the atrial and ventricular comparator reference pulse width modulations and the control signal for the sensing circuitry.

### Variables

#### Measured

|  |  |  |
| --- | --- | --- |
| **Name** | **Abbreviation** | **Reference** |
| ATR\_CMP\_DETECT | – | 2.1 |
| VENT\_CMP\_DETECT | – | 2.1 |

#### Constant

|  |  |  |
| --- | --- | --- |
| **Name** | **Abbreviation** | **Reference** |
| p\_mode | – | 2.2 |
| p\_atr\_pulse\_amplitude | – | 2.2 |
| p\_vent\_pulse\_amplitude | – | 2.2 |

#### Controlled

|  |  |  |
| --- | --- | --- |
| **Name** | **Abbreviation** | **Reference** |
| h\_atr\_pulse\_detected | – | 2.3 |
| h\_vent\_pulse\_detected | – | 2.3 |
| ATR\_CMP\_REF\_PWM | – | 2.3 |
| VENT\_CMP\_REF\_PWM | – | 2.3 |
| FRONT\_END\_CTRL | – | 2.3 |

#### Internal

No internal variables

### Initial Values

No initial values

### Requirements

h\_atr\_pulse\_detected = ATR\_CMP\_DETECT

h\_vent\_pulse\_detected = VENT\_CMP\_DETECT

|  |  |  |  |
| --- | --- | --- | --- |
| **p\_mode** | **ATR\_CMP\_REF\_PWM** | **VENT\_CMP\_REF\_PWM** | **FRONT\_END\_CTRL** |
| AOO | 0 | 0 | false |
| VOO | 0 | 0 | false |
| AAI | p\_atr\_pulse\_amplitude/0.05 | 0 | true |
| VVI | 0 | p\_vent\_pulse\_amplitude/0.05 | true |

### Design details

Due to the discrete clock, the PWM ON time is calculated and rounded to the nearest amount of clock cycles and then subtracted from the PWM period so that the period is not affected by rounding errors.

### Future changes

More modes will have to be implemented as they are designed. For dual sensing modes both atrial and ventricular paces will have to be monitored.

### Stateflow Screenshot

No Stateflow necessary for Sensing.

### Testing

|  |  |  |  |
| --- | --- | --- | --- |
| **Test Case** | **Expected Result** | **Actual Result** | **Pass/Fail** |
| p\_mode: AAI  p\_lower\_rate\_limit: 60 BPM  Atrium PW: 10.0 ms  Heart Rate: 60 BPM | No pacing | No pacing | Pass |
| p\_mode: VVI  p\_lower\_rate\_limit: 60 BPM  Ventricle PW: 10.0 ms  Heart Rate: 60 BPM | No pacing | No pacing | Pass |

Test 1

Chart

Description automatically generated

Test 2

A picture containing chart

Description automatically generated