Atlys BSB Support Files for AXI-based Designs

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Overview

This package will integrate board support for the Atlys Spartan-6 FPGA Development Board into Xilinx EDK tools. It includes board definition files for creating AXI-based MicroBlaze embedded designs in the Base System Builder (BSB). It also includes cores for custom peripherals such as the Digilent USB-EPP interface, the 16MB Quad SPI Flash Memory and AC97. With these files the BSB can be used to create Platform Studio projects initialized with cores that are properly configured to control the on-board peripherals. The currently supported cores are outlined in Table 1.

TABLE 1. BSB SUPPORTED PERIPHERALS

Peripheral	Supported Interface	Core name(s)	Notes
128MB DDR (cached)	AXI4	axi_s6_ddrx	--
8 User Switches	AXI4-Lite	axi_gpio	--
5 User Push Buttons	AXI4-Lite	axi_gpio	--
8 LED outputs	AXI4-Lite	axi_gpio	--
UART	AXI4-Lite	axi_uartlite/axi_uart16550	--
16-MB Quad-SPI PCM	AXI4-Lite	d_qspi_axi	Custom core; supports 1X, 2X and 4X modes
AC-97	AXI4-Lite	d_ac97_axi	Custom core
USB-EPP	AXI4-Lite	d_usb_epp_dstm_axi	Custom core
10/100/1000 Mbps PHY	AXI4-Lite	axi_ethernet	Requires license
10/100 Mbps PHY	AXI4-Lite	axi_ethernetlite	--

For additional information on using these cores, please refer to their PDF datasheets

Using the BSB Support Files

Note: In order to use the custom cores from the BSB Support Files, first install the "Digilent_AXI_IPCore_Support" package (from Digilent website).
The "Digilent_AXI_IPCore_Support" adds core and bus definitions in IPXACT standard to the EDK installation directory.

1. Start Platform Studio and create a new project in Base System Builder. Choose AXI system in the "Create New XPS Project Using BSB Wizard" window.
2. Click on the "Browse" button beside the "Set Project Peripheral Repository Search Path" box and browse to the path containing the .\lib subfolder from the BSB Support Files folder, then press OK.
   The BSB window should look like in figure below:

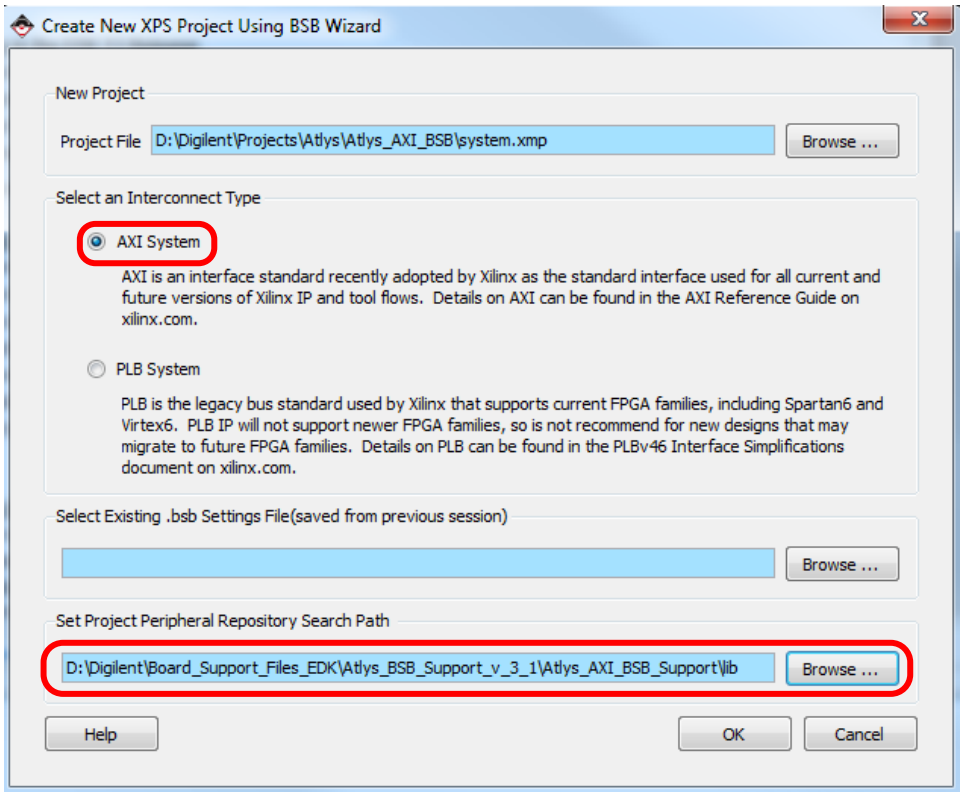

Figure 1. BSB window with specifying the Peripheral Repository Search Path

Click OK. You should now be able to select the Digilent Spartan-6 Atlys as your development board further in the Board Selection window.

Using Interrupt for the Digilent USB-EPP interface

EPP requests for the USB-EPP interface come from the USB port. If there is no answer in 100mS, the PC application will signal a timeout. Therefore, it is recommended that Epp requests are handled with an interrupt service routine instead of continuously polling the interface status.

The demo applications include examples for using the USB-EPP interface in both polling and interrupt mode.

In order to use interrupt service routines, the interrupt request signal for the Digilent USB-EPP has to be connected to either an interrupt controller or the Microblaze processor interrupt input.

If the “Use Interrupt” option is selected for any core in BSB, then the Base System Builder will add an interrupt controller to the system.

For example, to select the “Use Interrupt” option for the Digilent_Usb_Epp peripheral in BSB, in the “Peripheral Configuration” window click on the “Digilent_Usb_Epp” peripheral and select “Use Interrupt” like is shown in Figure 2 below.

Note that because the USB-EPP interface is a custom core, its interrupt output is not automatically connected by BSB and the user will have to make the connection manually, as described in the section “Using the Digilent USP-EPP interface controller” below.

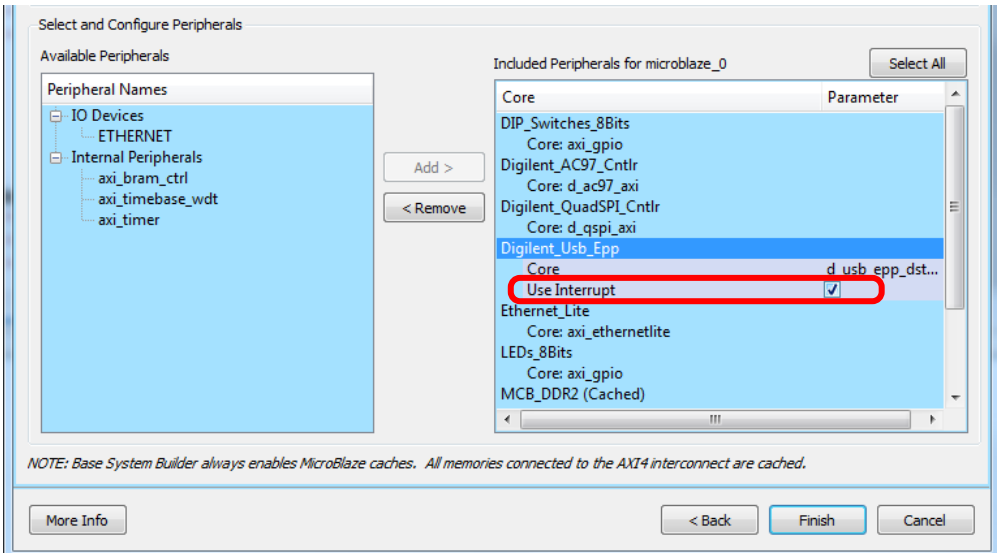

Figure 2. Selecting the “Use Interrupt” option for the Digilent_Usb_Epp interface in Base System Builder.

Using the custom cores

Although the “Digilent_AXI_IPCore_Support” package installs the IPXACT definitions for custom cores, the internal and external connections for the custom cores are not automatically made by BSB (except for AXI4-Lite bus connections). Therefore, the user must manually make the connections when using any of the custom cores. The following sections describe how to manually create these connections for each custom core.

Using the Digilent USB-EPP interface controller

If the Digilent USB-EPP interface controller is present in the system, the following connections have to be made:

a. Go to the “Ports” tab in XPS and expand *Digilent_Usb_Epp* core instance. Connect **S_AXI_ACLK** to **clk_100_0000MHzPLL0** then make the ports under “(IO_IF) usb_epp_ext” external, like Figure 3 below shows:

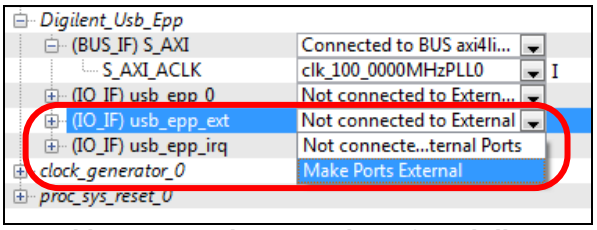

Figure 3. Making external connections for Digilent_Usb_Epp

If the "Use Interrupt" option was selected in BSB for the Digilent USB-EPP controller interface, the USB-EPP Interrupt output has to be connected to the interrupt controller:

b. On the "Ports" tab, in XPS, expand the *microblaze_0_intc* instance and click on the "Net" of "Intr" port. An "Interrupt Connection Dialog" appears. Select the interrupt port: **Digilent_Usb_Epp:IRQ_EPP**, shown in Figure 4 below, click on the "->" arrow to add the connection then press OK.

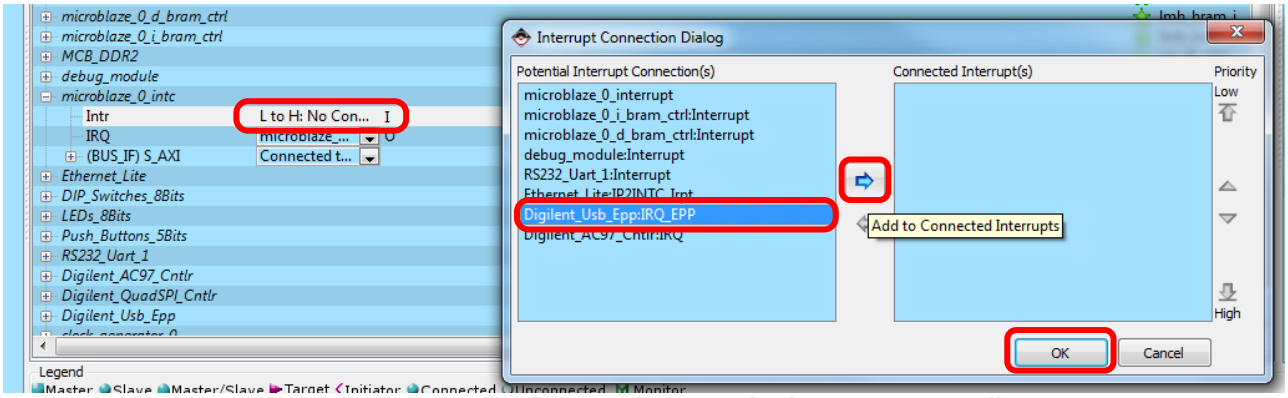

Figure 4. Connecting interrupt port to the interrupt controller

Connecting Digilent Quad-SPI controller

Expand *Digilent_QuadSPI_Cntlr* core instance. Connect **S_AXI_ACLK** to **clk_100_0000MHzPLL0** and make external the ports under "(IO_IF) qspi_ext".

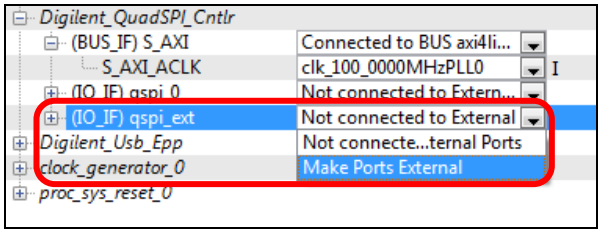

Figure 5. Making external connections for Digilent_QuadSPI_Cntlr

Connecting Digilent AC97 controller

Expand *Digilent_AC97_Cntlr* core instance. Connect **S_AXI_ACLK** to **clk_100_0000MHzPLL0** and make external the ports under "(IO_IF) ac97_ext".

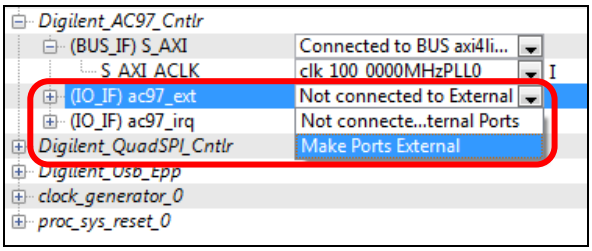

Figure 6. Making external connections on Digilent_AC97_Cntlr