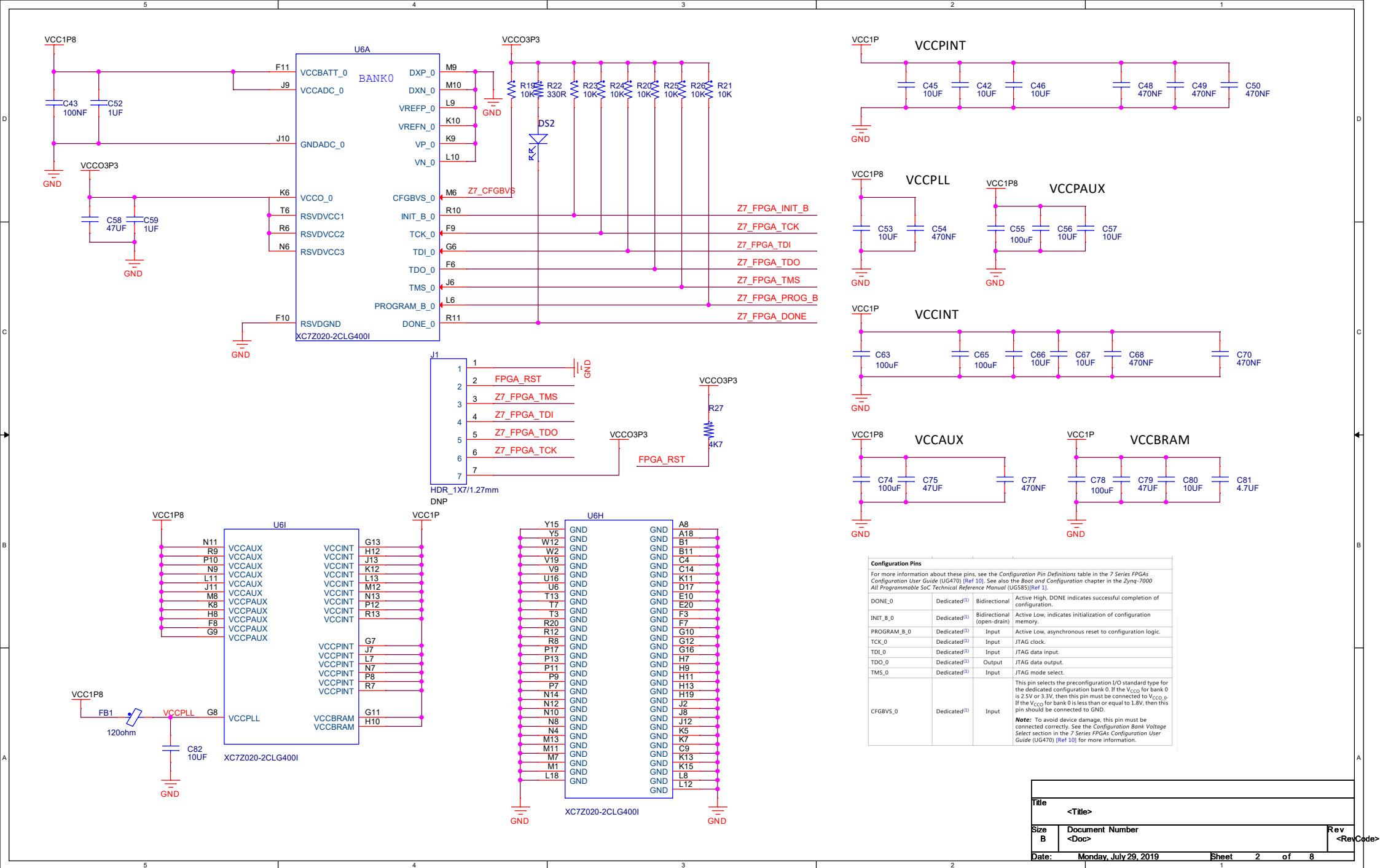
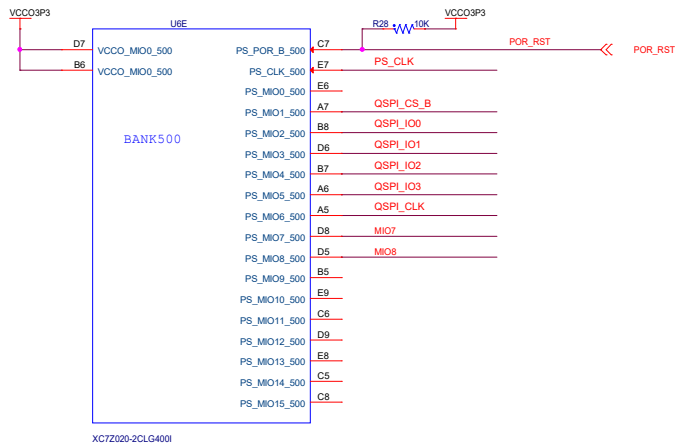
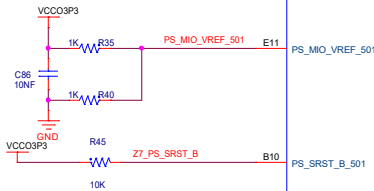
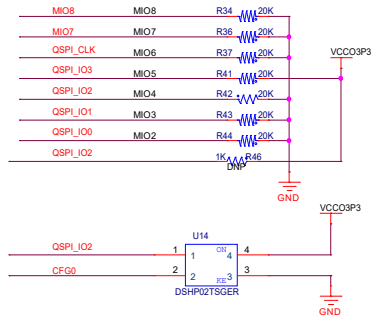
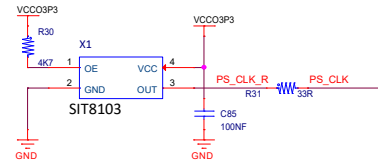
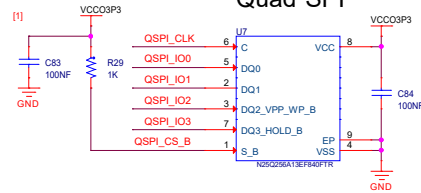


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Quad SPI



Value	0	1
QSPI_IO2	Default: SPI	SD Card

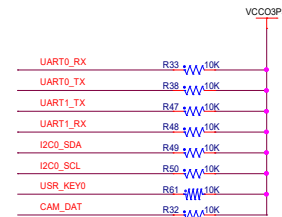
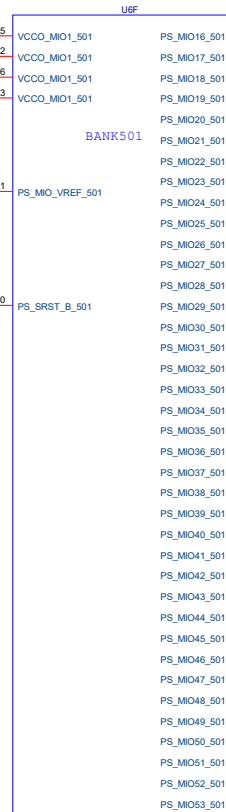


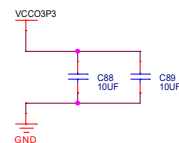
Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common ⁽¹⁾				0	0	0	JTAG Chain Routing ⁽²⁾ 0: Cascade mode 1: Independent mode
NOR Boot ⁽³⁾				0	0	1	
NAND				0	1	0	
Quad-SPI ⁽³⁾				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage ⁽⁴⁾							
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

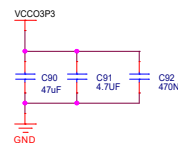
Notes:

- JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
- For secure mode, JTAG is not enabled and MIO[2] is ignored.
- The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
- Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

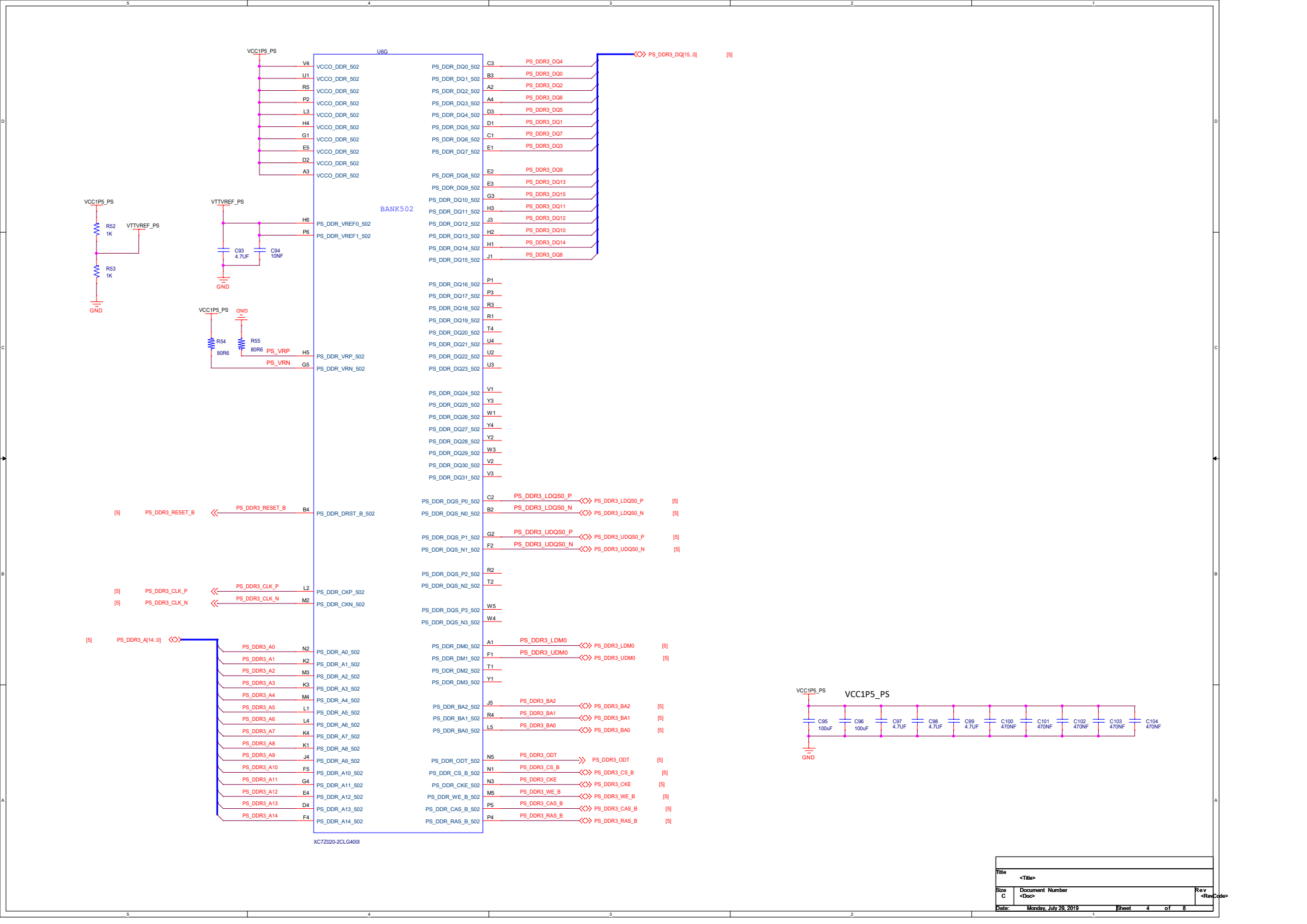
VCCO_MIO0

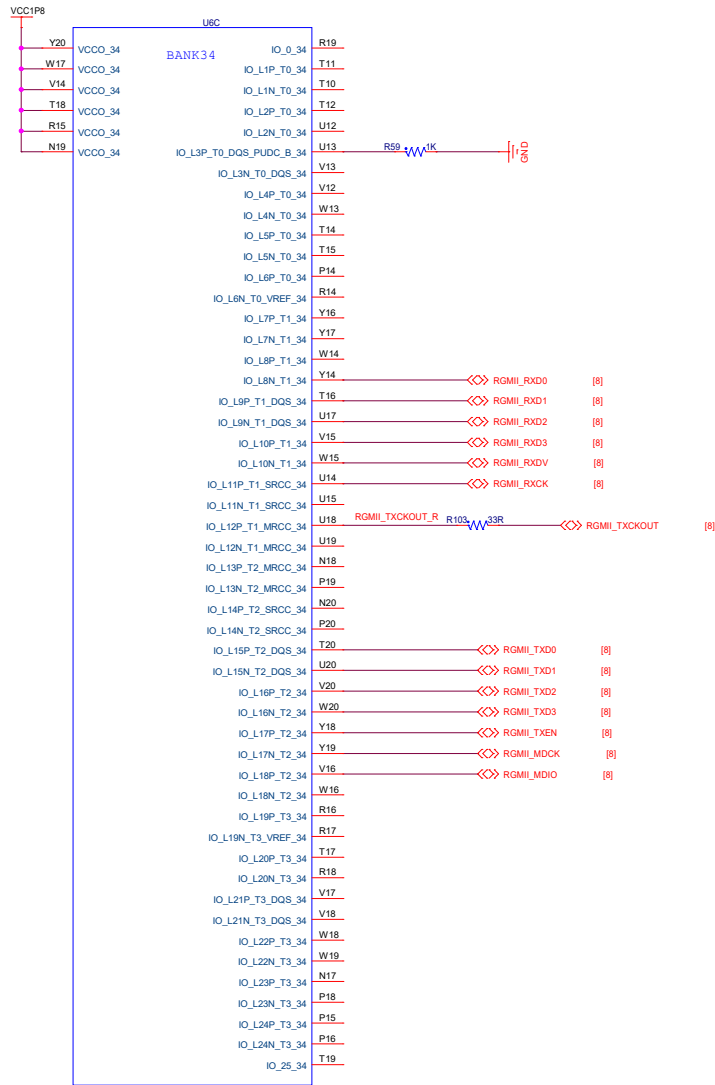


VCCO_MIO1

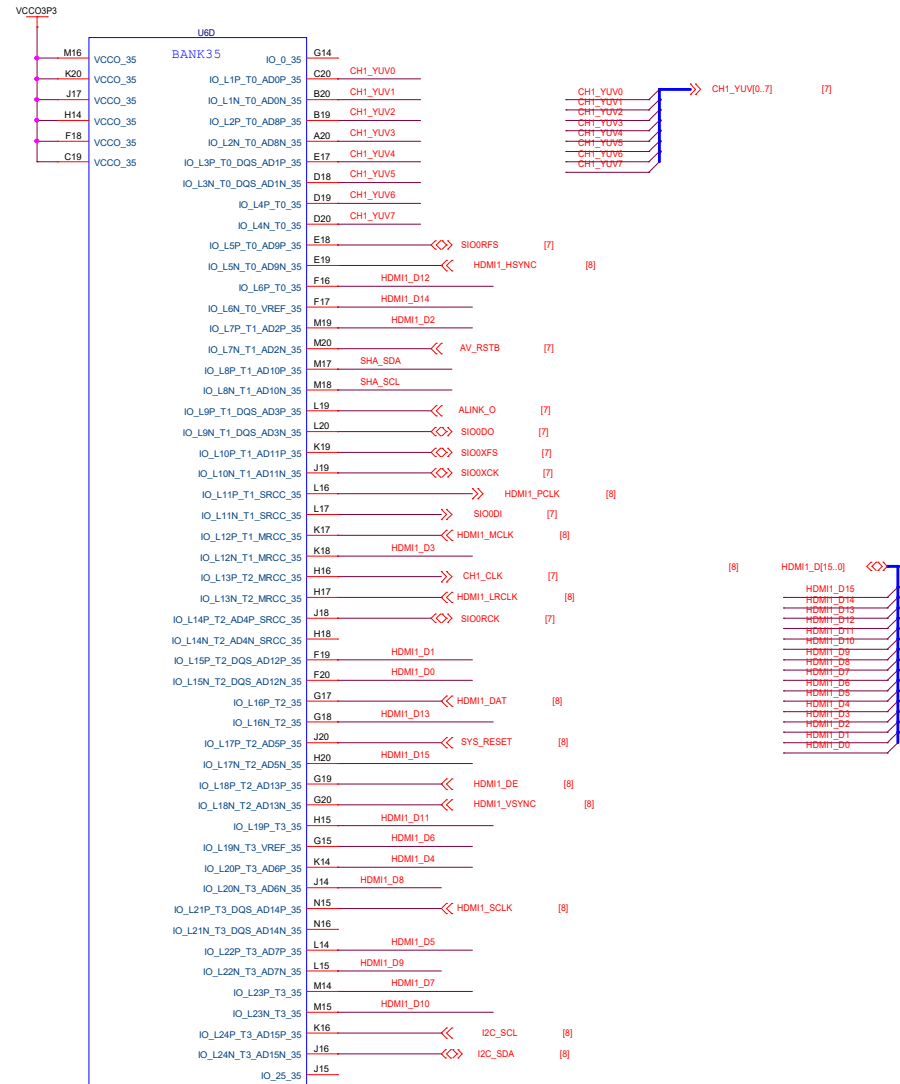
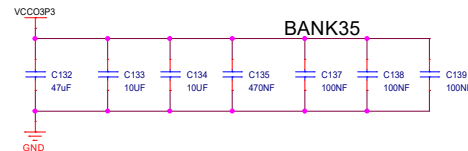
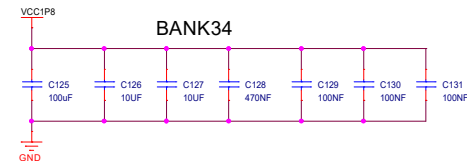


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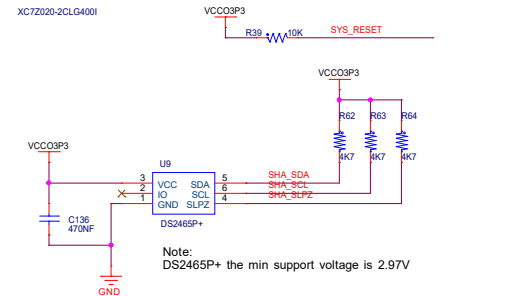




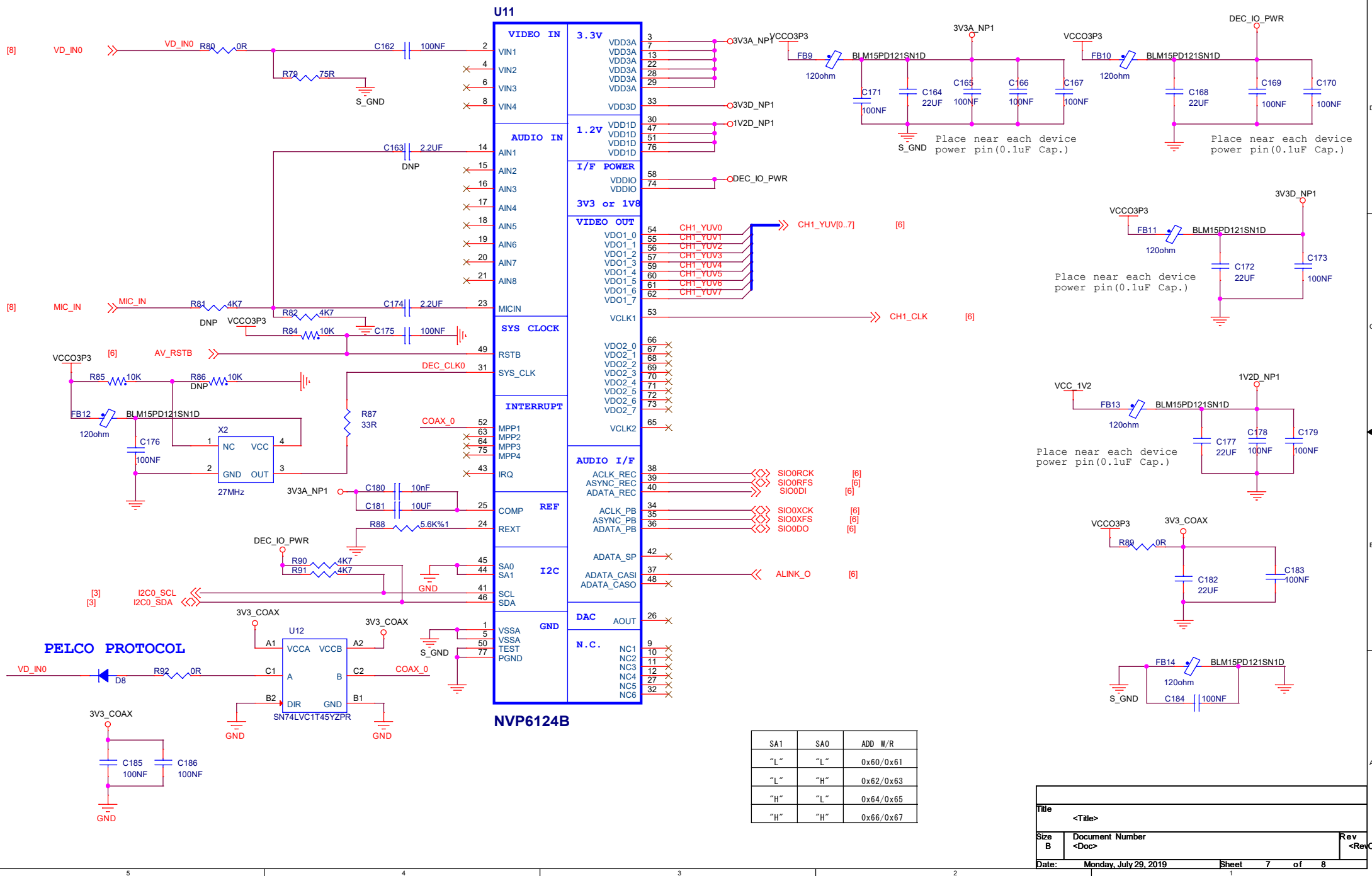
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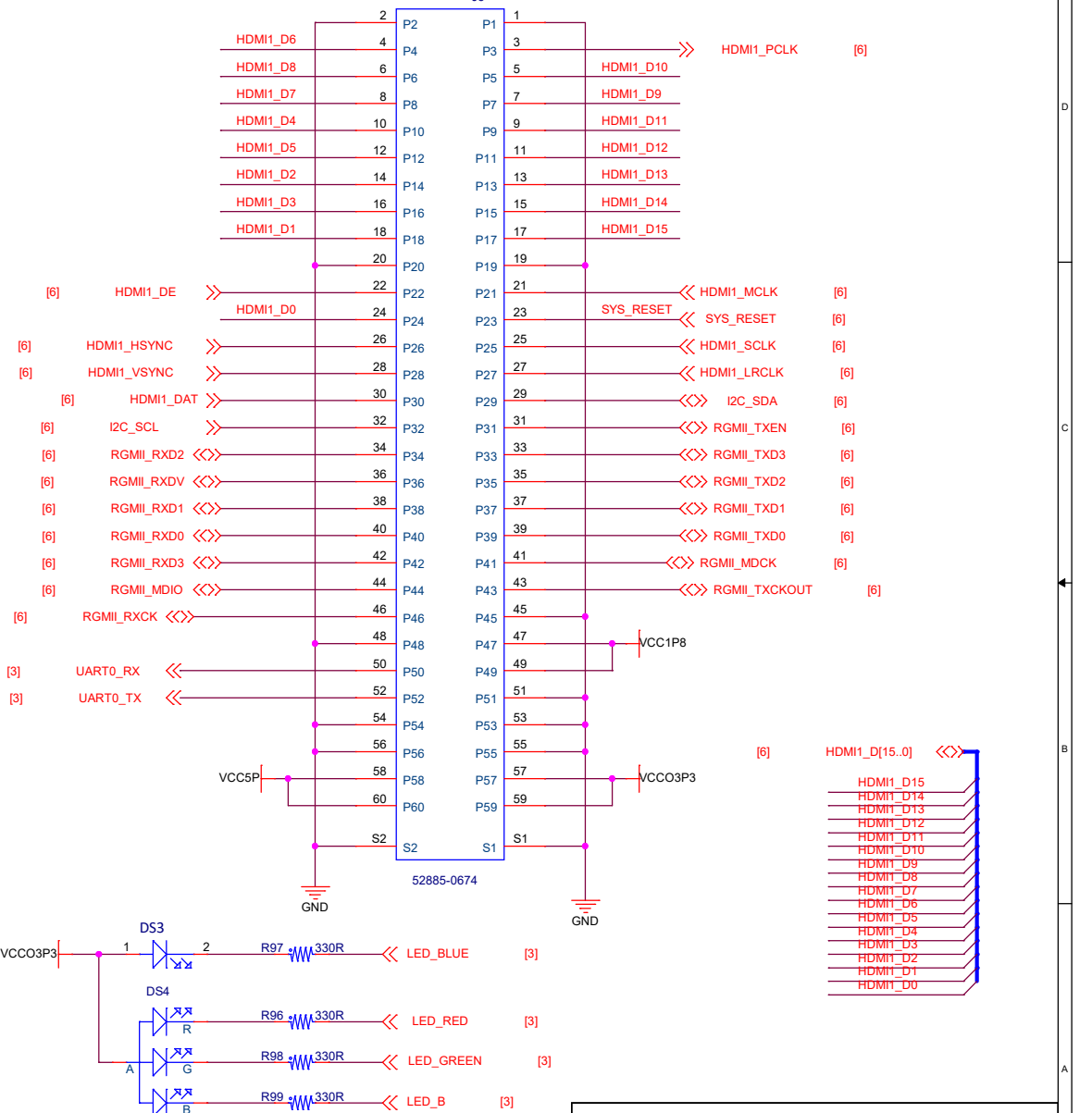
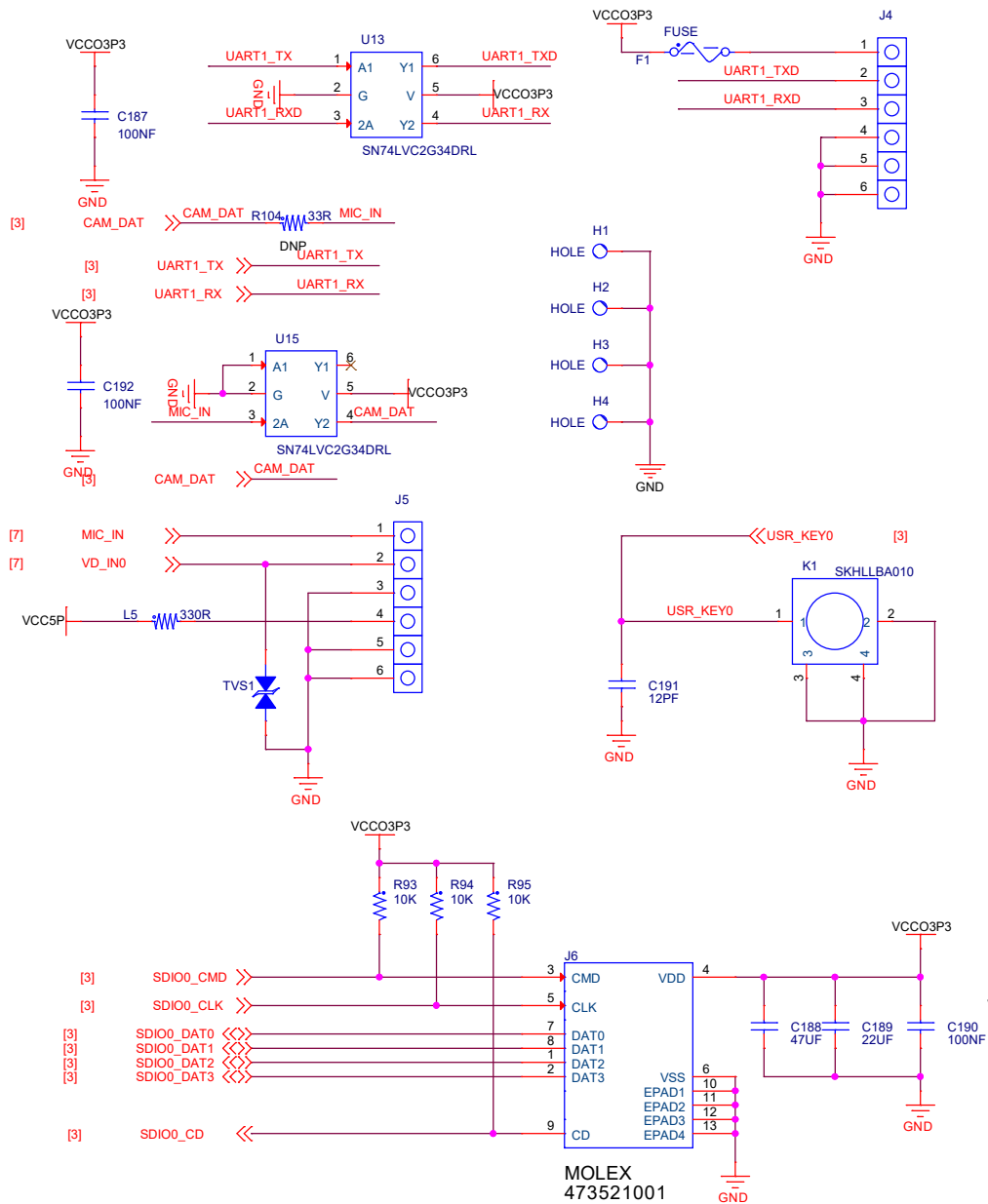


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