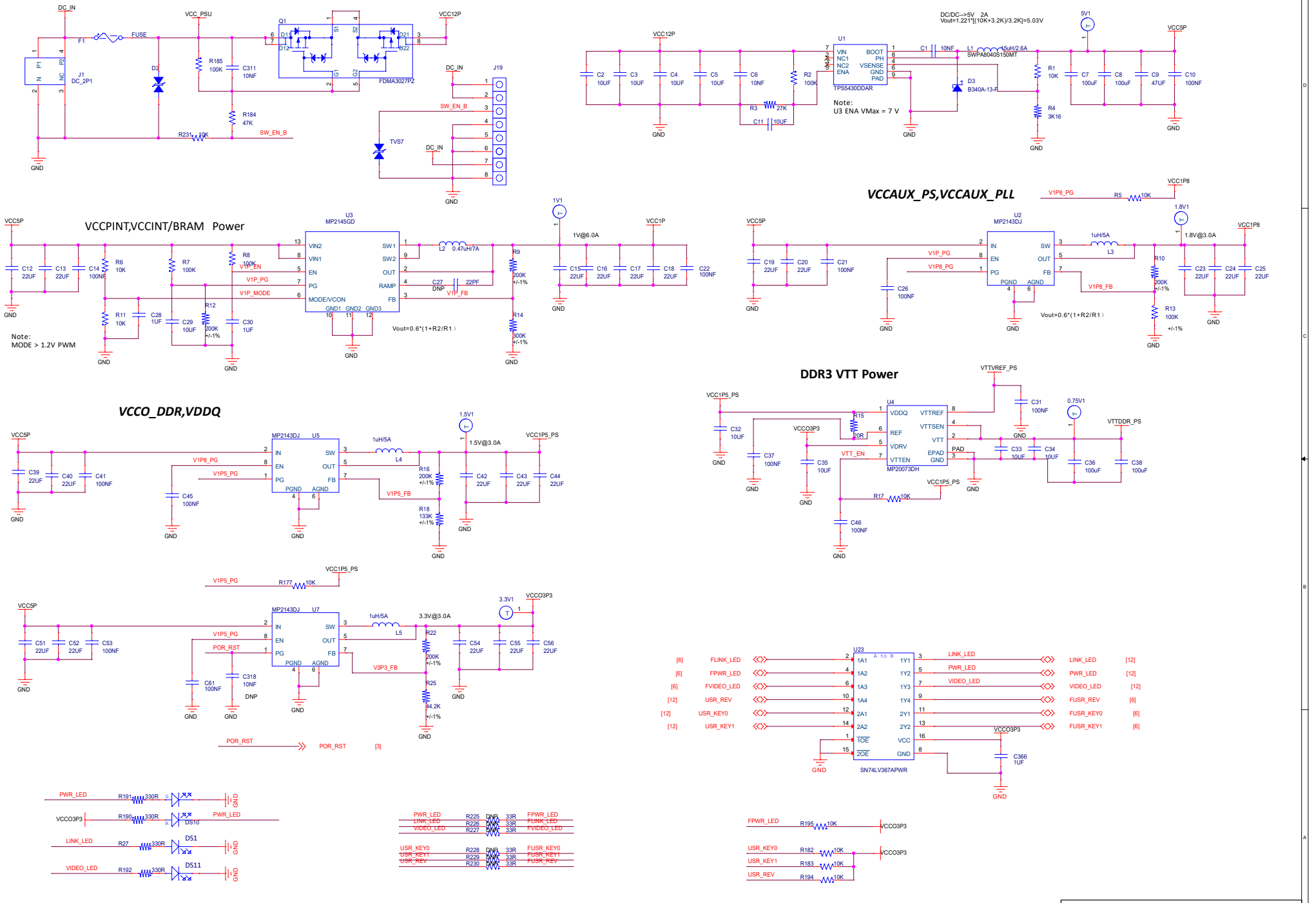
DC_IN
VCC_PSU
VCC12P
FUSE
F1
J1
DC_2P1
D2
R185
100K
C311
10NF
Q1
FDMA3027P2
R184
47K
R231
10K
SW_EN_B
TVS7
J19
GND
DC/DC-->5V 2A
Vout=1.221*[(10K+3.2K)/3.2K]=5.03V
U1
TPS5430DDAR
C1
10NF
L1
5uH/2.6A
SWPA8040S150MT
D3
B340A-13-F
R1
10K
R4
3K16
C7
100uF
C8
100uF
C9
47UF
C10
100NF
VCC5P
5V1
C2
10UF
C3
10UF
C4
10UF
C5
10UF
C6
10NF
R2
100K
R3
27K
C11
10UF
Note:
U3 ENA VMax = 7 V
VCCPINT,VCCINT/BRAM Power
U3
MP2145GD
VIN2
VIN1
EN
PG
MODE/VCON
SW1
SW2
OUT
RAMP
FB
GND1
GND2
GND3
L2
0.47uH/7A
C27
DNP
22PF
R6
10K
R7
100K
R8
100K
R11
10K
C28
1UF
C29
10UF
R12
200K
+/-1%
C30
1UF
R9
200K
+/-1%
R14
300K
+/-1%
V1P_EN
V1P_PG
V1P_MODE
V1P_FB
C12
22UF
C13
22UF
C14
100NF
C15
22UF
C16
22UF
C17
22UF
C18
22UF
C22
100NF
1V1
1V@6.0A
VCC1P
Vout=0.6*(1+R2/R1)
Note:
MODE > 1.2V PWM
VCCAUX_PS,VCCAUX_PLL
U2
MP2143DJ
IN
EN
PG
SW
OUT
FB
PGND
AGND
L3
1uH/5A
R5
10K
V1P8_PG
V1P8_FB
R10
200K
+/-1%
R13
100K
+/-1%
C19
22UF
C20
22UF
C21
100NF
C26
100NF
C23
22UF
C24
22UF
C25
22UF
VCC1P8
1.8V1
1.8V@3.0A
Vout=0.6*(1+R2/R1)
VCCO_DDR,VDDQ
U5
MP2143DJ
L4
1uH/5A
1.5V1
1.5V@3.0A
VCC1P5_PS
R16
200K
+/-1%
R18
133K
+/-1%
C39
22UF
C40
22UF
C41
100NF
C45
100NF
C42
22UF
C43
22UF
C44
22UF
V1P5_PG
V1P5_FB
DDR3 VTT Power
U4
MP20073DH
VDDQ
REF
VDRV
VTTEN
VTTREF
VTTSEN
VTT
EPAD
GND
PAD
R15
20R
VTT_EN
R17
10K
C46
100NF
C32
10UF
C37
100NF
C35
10UF
C31
100NF
C33
10UF
C34
10UF
C36
100uF
C38
100uF
VTTVREF_PS
VTTDDR_PS
0.75V1
VCC1P5_PS
VCCO3P3
U7
L5
1uH/5A
3.3V1
3.3V@3.0A
R22
200K
+/-1%
R25
44.2K
+/-1%
C51
22UF
C52
22UF
C53
100NF
C54
22UF
C55
22UF
C56
22UF
C61
100NF
C318
10NF
DNP
V3P3_FB
POR_RST
R177
10K
V1P5_PG
POR_RST
[3]
U23
SN74LV367APWR
1A1
1A2
1A3
1A4
2A1
2A2
1OE
2OE
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
VCC
GND
C366
1UF
[6] FLINK_LED
[6] FPWR_LED
[6] FVIDEO_LED
[12] USR_REV
[12] USR_KEY0
[12] USR_KEY1
LINK_LED [12]
PWR_LED [12]
VIDEO_LED [12]
FUSR_REV [6]
FUSR_KEY0 [6]
FUSR_KEY1 [6]
PWR_LED
LINK_LED
VIDEO_LED
R191
330R
R190
330R
R27
330R
R192
330R
DS10
DS1
DS11
R225 DNP 33R FPWR_LED
R226 DNP 33R FLINK_LED
R227 DNP 33R FVIDEO_LED
R228 DNP 33R FUSR_KEY0
R229 DNP 33R FUSR_KEY1
R230 DNP 33R FUSR_REV
FPWR_LED
R195
10K
USR_KEY0
USR_KEY1
USR_REV
R182
10K
R183
10K
R194
10K
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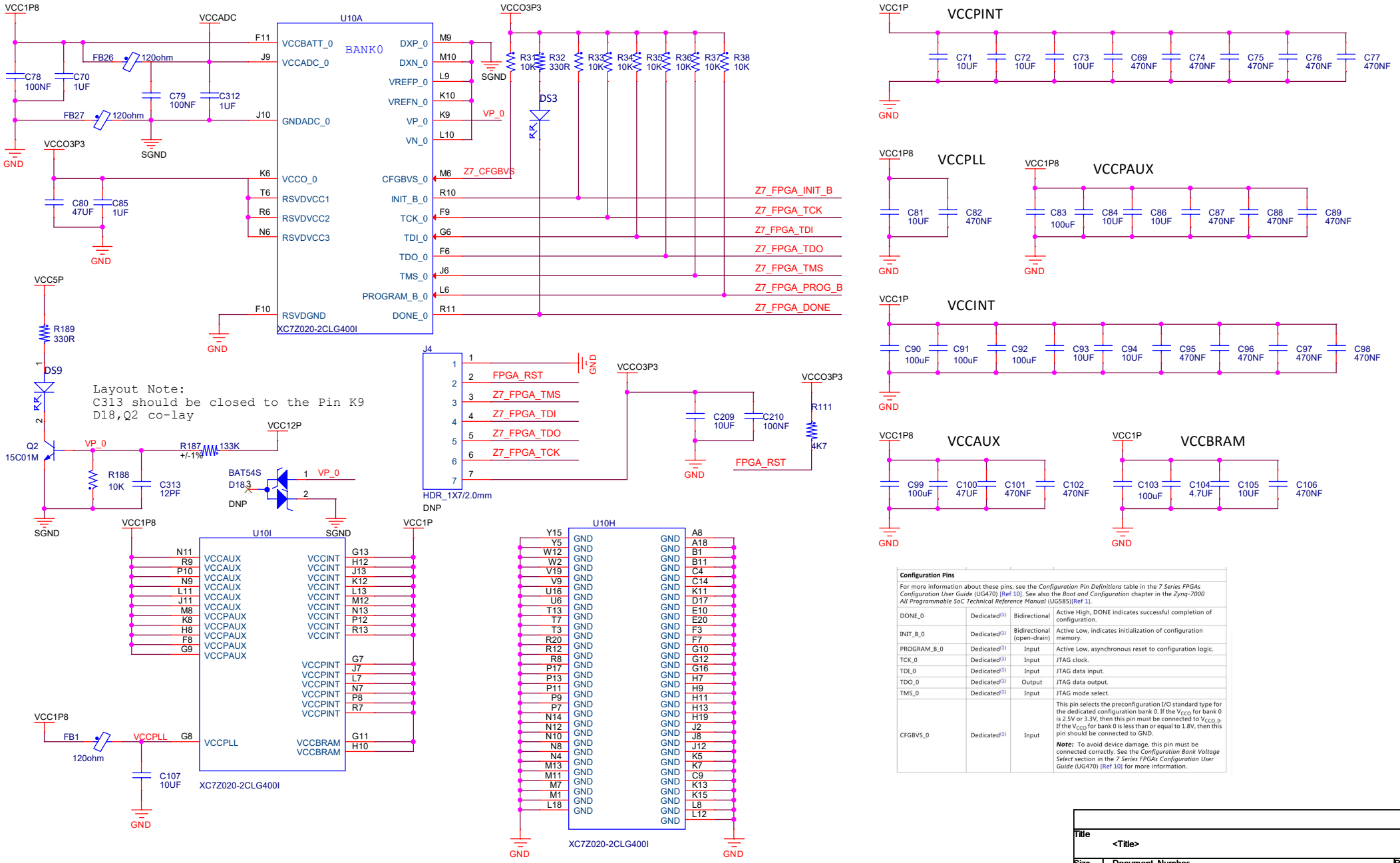

Configuration Pins			
For more information about these pins, see the *Configuration Pin Definitions* table in the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 10]. See also the *Boot and Configuration* chapter in the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)[Ref 1].			
DONE_0	Dedicated(1)	Bidirectional	Active High, DONE indicates successful completion of configuration.
INIT_B_0	Dedicated(1)	Bidirectional (open-drain)	Active Low, indicates initialization of configuration memory.
PROGRAM_B_0	Dedicated(1)	Input	Active Low, asynchronous reset to configuration logic.
TCK_0	Dedicated(1)	Input	JTAG clock.
TDI_0	Dedicated(1)	Input	JTAG data input.
TDO_0	Dedicated(1)	Output	JTAG data output.
TMS_0	Dedicated(1)	Input	JTAG mode select.
CFGBVS_0	Dedicated(1)	Input	This pin selects the preconfiguration I/O standard type for the dedicated configuration bank 0. If the V_{CCO} for bank 0 is 2.5V or 3.3V, then this pin must be connected to V_{CCO_0}. If the V_{CCO} for bank 0 is less than or equal to 1.8V, then this pin should be connected to GND. ***Note:*** To avoid device damage, this pin must be connected correctly. See the *Configuration Bank Voltage Select* section in the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 10] for more information.

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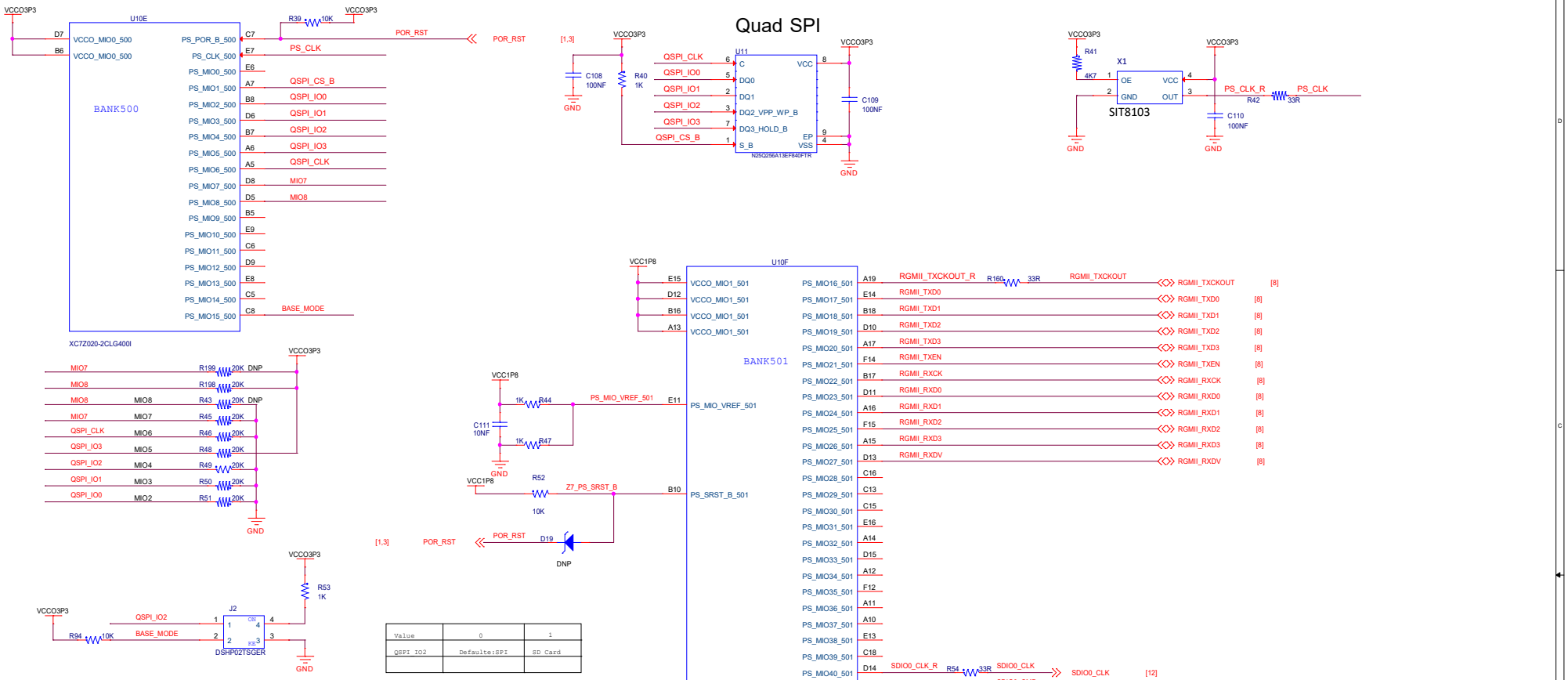

Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common(1)				0	0	0	**JTAG Chain Routing**(2) 0: Cascade mode 1: Independent mode
NOR Boot(3)				0	0	1	
NAND				0	1	0	
Quad-SPI(3)				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage(4)							

	Bank 1	Bank 0	
2.5 V, 3.3 V	0	0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.
1.8 V	1	1	

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

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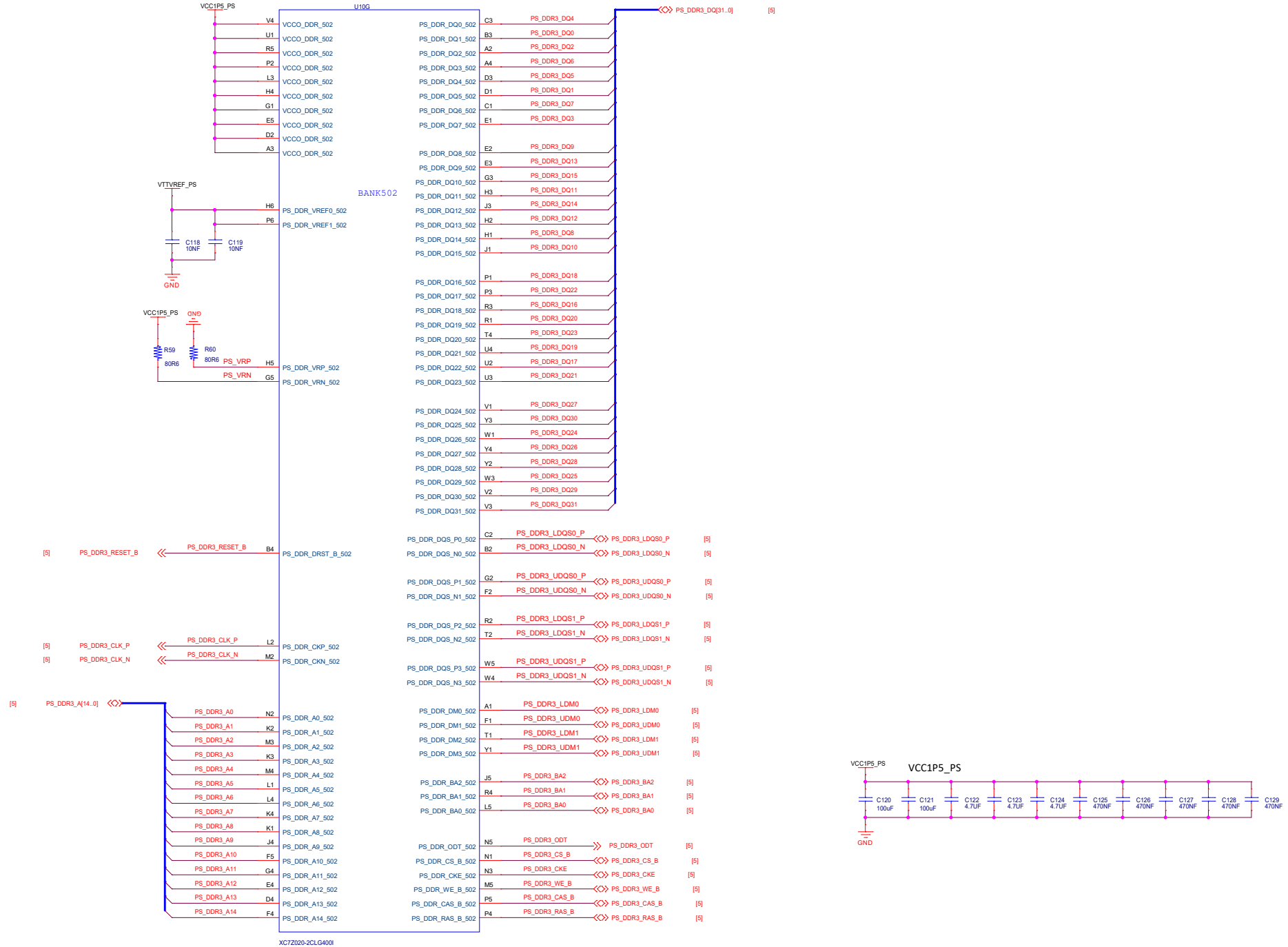

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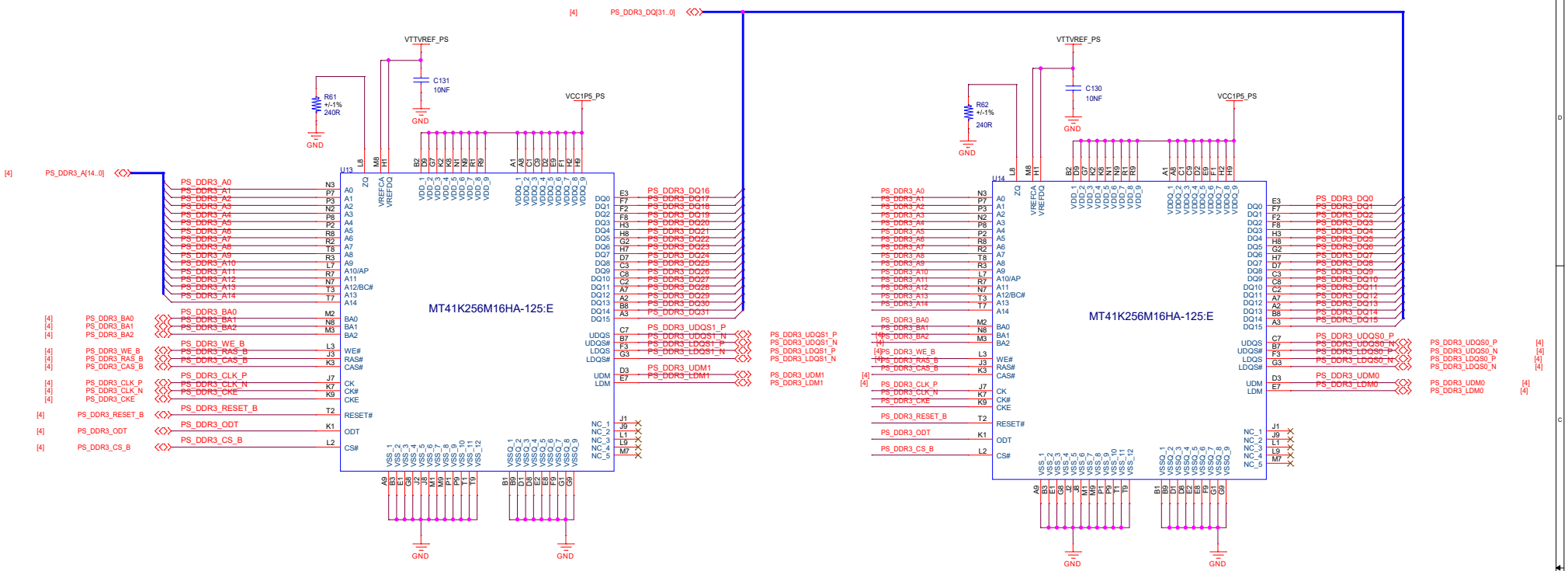
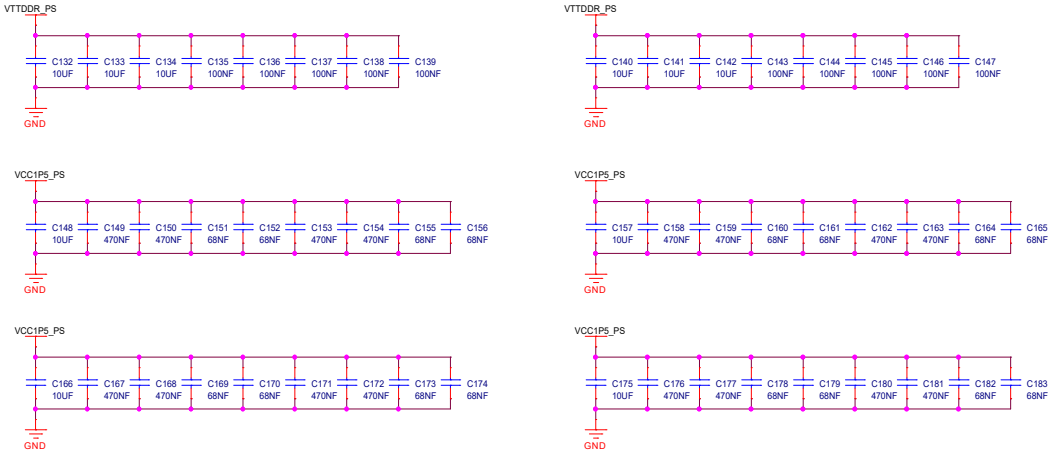
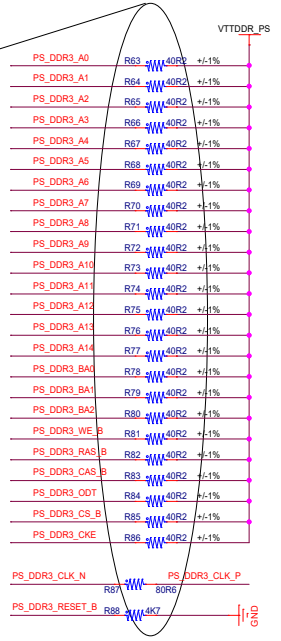




Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms



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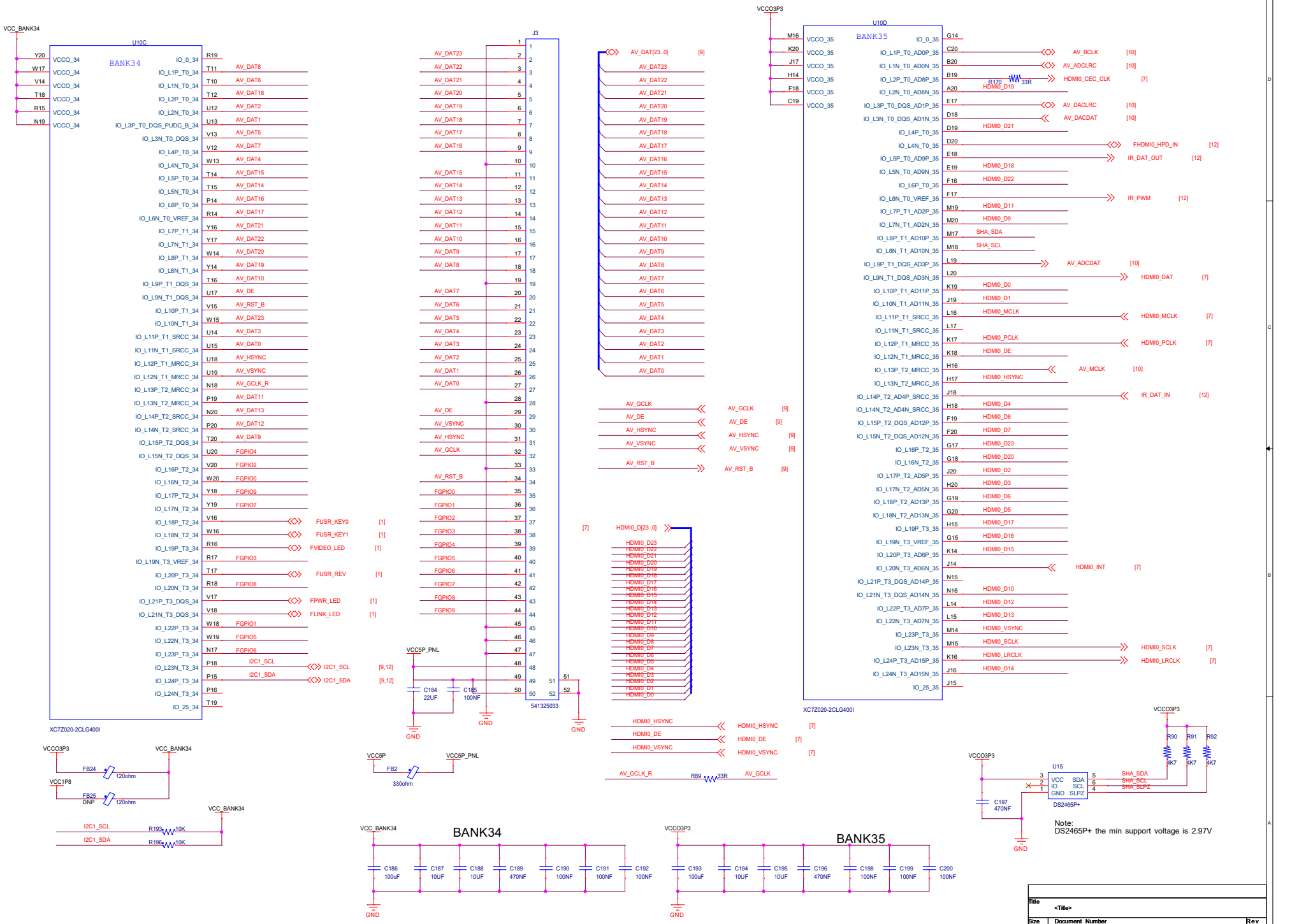
U10C
BANK34
XC7Z020-2CLG400I
U10D
BANK35
XC7Z020-2CLG400I
J3
541325033
VCC_BANK34
VCCO3P3
VCC5P_PNL
VCC5P
VCC1P8
GND
FB24
FB25
DNP
120ohm
330ohm
R193
R196
10K
R89
33R
R170
U15
DS2465P+
R90
R91
R92
4K7
C197
470NF
BANK34
BANK35
C184
22UF
C185
100NF
C186
100uF
C187
10UF
C188
10UF
C189
470NF
C190
100NF
C191
100NF
C192
100NF
C193
100uF
C194
10UF
C195
10UF
C196
470NF
C198
100NF
C199
100NF
C200
100NF
Note:
DS2465P+ the min support voltage is 2.97V
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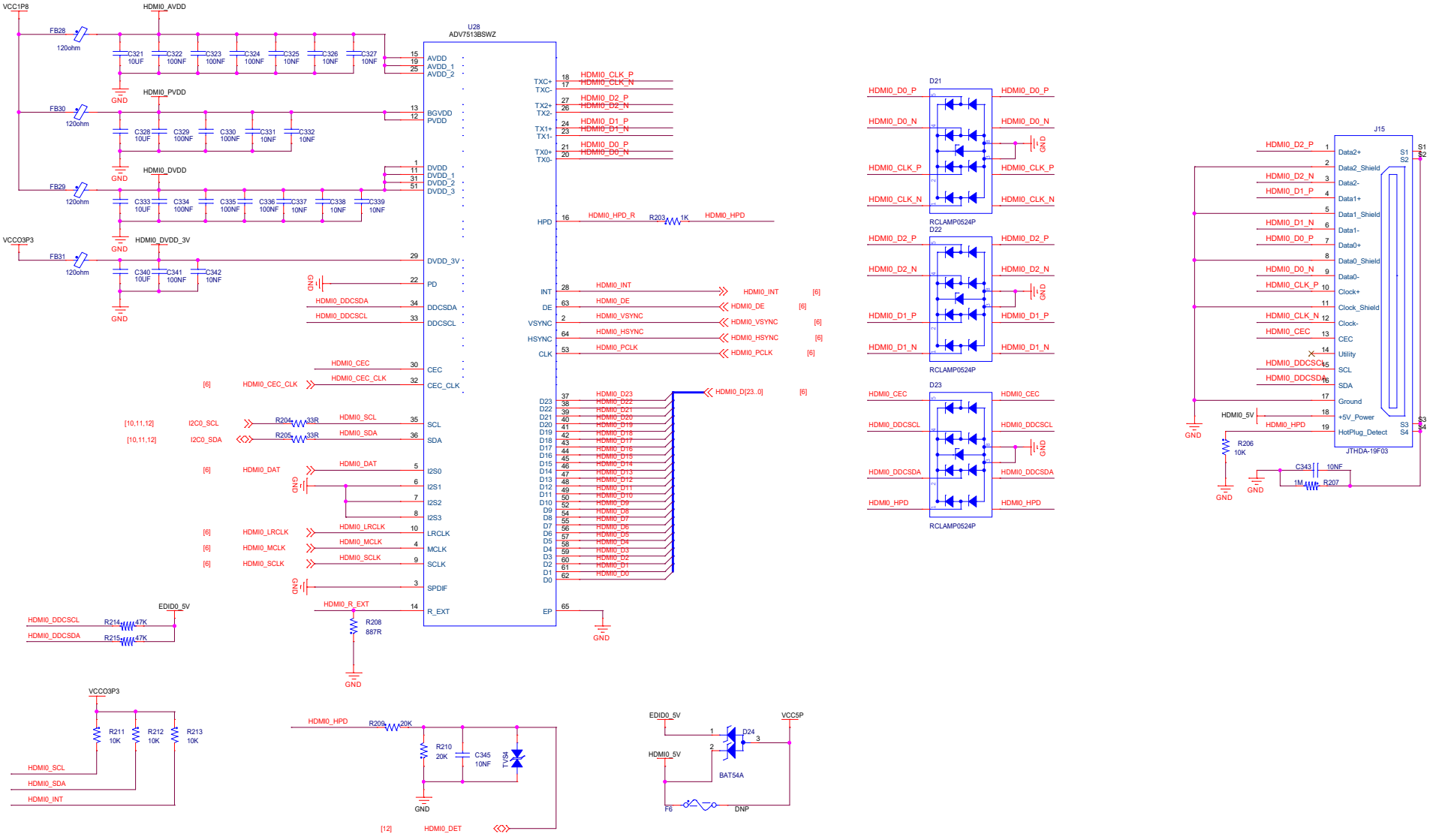

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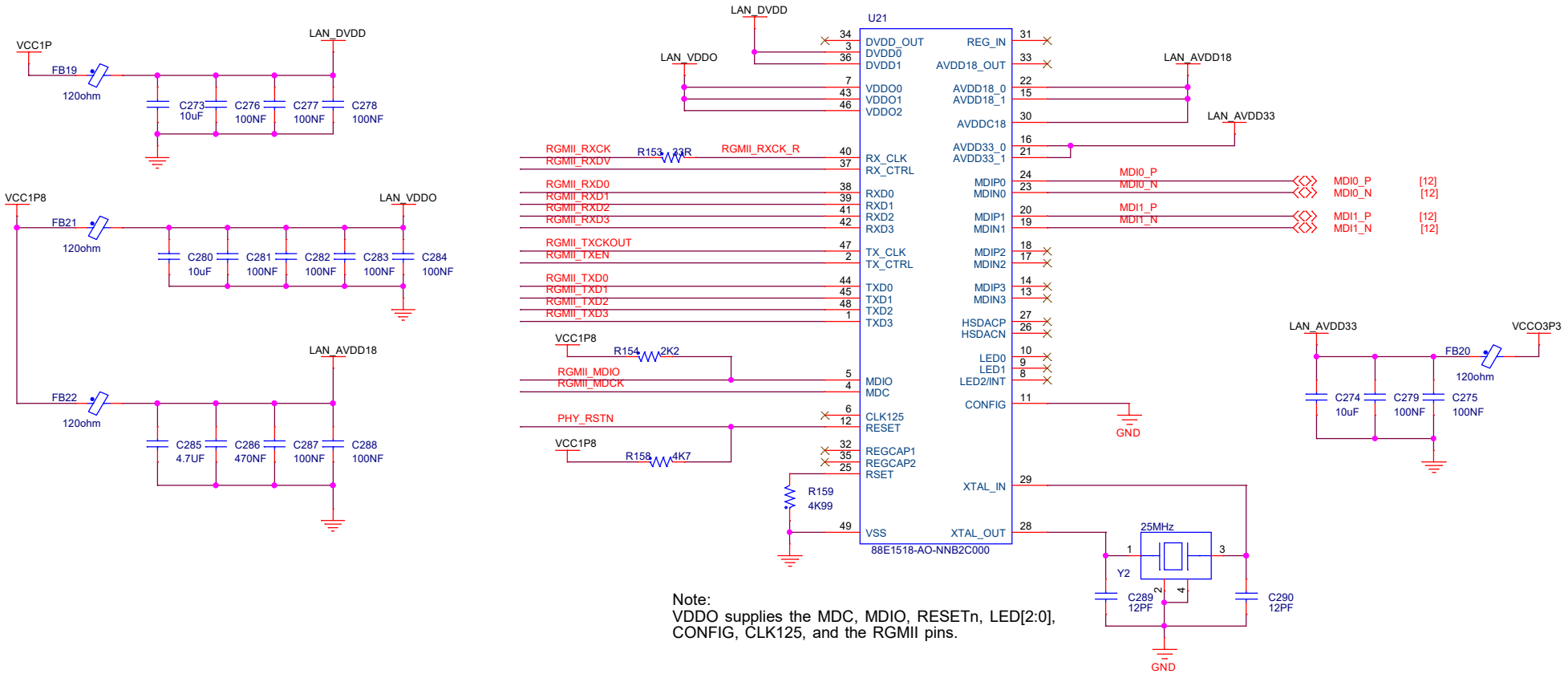

Note:
VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, and the RGMII pins.

RGMII_TXCKOUT <> RGMII_TXCKOUT [3]
RGMII_TXD0 <> RGMII_TXD0 [3]
RGMII_TXD1 <> RGMII_TXD1 [3]
RGMII_TXD2 <> RGMII_TXD2 [3]
RGMII_TXD3 <> RGMII_TXD3 [3]
RGMII_TXEN <> RGMII_TXEN [3]

RGMII_MDIO <> RGMII_MDIO [3]
RGMII_MDCK <> RGMII_MDCK [3]
PHY_RSTN <> PHY_RSTN [3]

RGMII_RXCK <> RGMII_RXCK [3]
RGMII_RXD0 <> RGMII_RXD0 [3]
RGMII_RXD1 <> RGMII_RXD1 [3]
RGMII_RXD2 <> RGMII_RXD2 [3]
RGMII_RXD3 <> RGMII_RXD3 [3]
RGMII_RXDV <> RGMII_RXDV [3]

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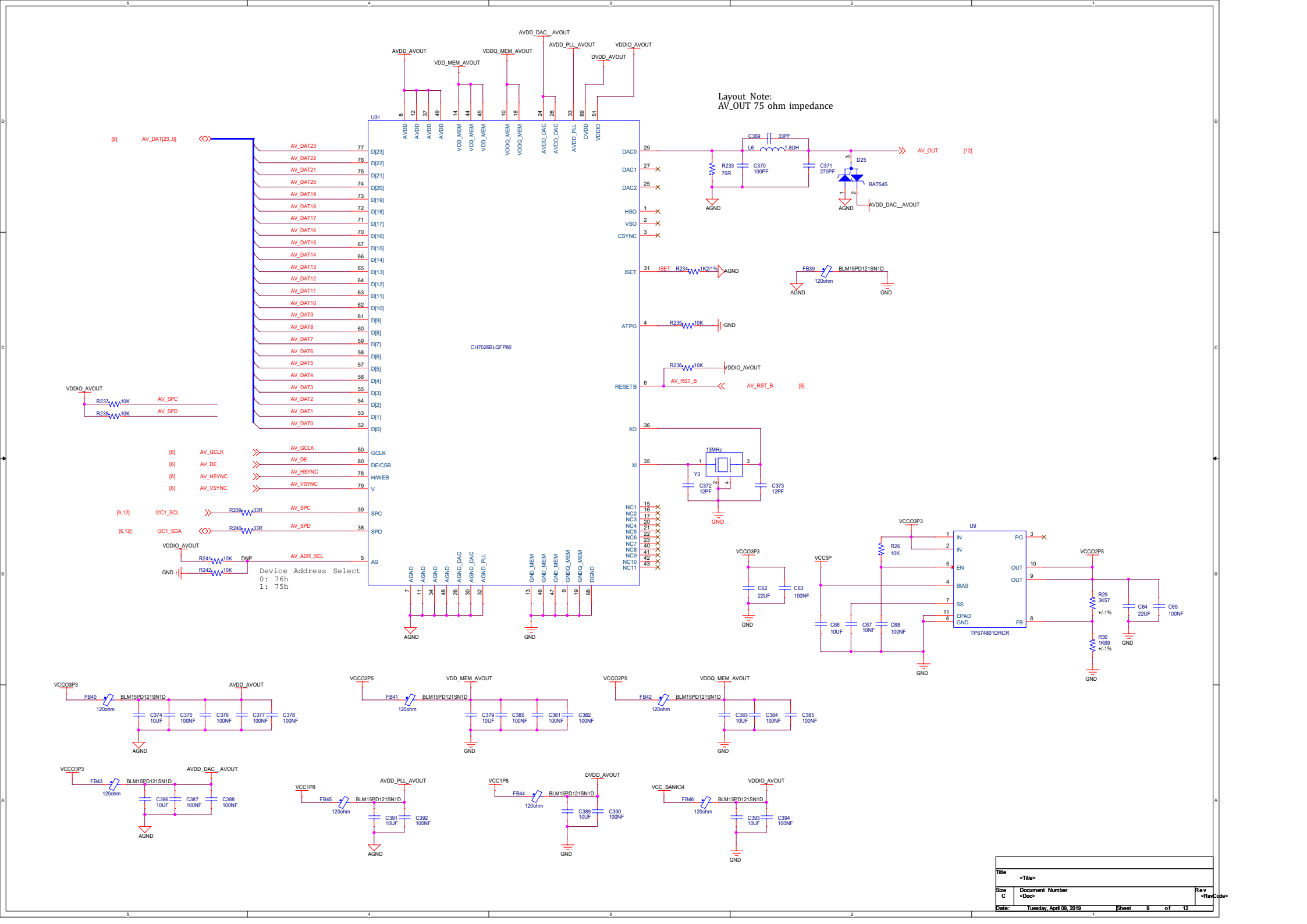
Layout Note:
AV_OUT 75 ohm impedance
U31
CH7026BLQFP80
AVDD_AVOUT
VDD_MEM_AVOUT
VDDQ_MEM_AVOUT
AVDD_DAC__AVOUT
AVDD_PLL_AVOUT
DVDD_AVOUT
VDDIO_AVOUT
AV_DAT[23..0]
AV_GCLK
AV_DE
AV_HSYNC
AV_VSYNC
I2C1_SCL
I2C1_SDA
AV_SPC
AV_SPD
AV_ADR_SEL
AV_OUT
AV_RST_B
ISET
R234 1K2/1%
R235 10K
R236 10K
R237 10K
R238 10K
R239 33R
R240 33R
R241 10K DNP
R242 10K
R233 75R
C369 33PF
L6 1.8UH
C370 100PF
C371 270PF
D25 BAT54S
FB39 BLM15PD121SN1D 120ohm
13MHz
Y3
C372 12PF
C373 12PF
Device Address Select
0: 76h
1: 75h
U9
TPS74801DRCR
R26 10K
R29 3K57 +/-1%
R30 1K69 +/-1%
C62 22UF
C63 100NF
C64 22UF
C65 100NF
C66 10UF
C67 10NF
C68 100NF
FB40 BLM15PD121SN1D 120ohm
C374 10UF
C375 100NF
C376 100NF
C377 100NF
C378 100NF
FB41 BLM15PD121SN1D 120ohm
C379 10UF
C380 100NF
C381 100NF
C382 100NF
FB42 BLM15PD121SN1D 120ohm
C383 10UF
C384 100NF
C385 100NF
FB43 BLM15PD121SN1D 120ohm
C386 10UF
C387 100NF
C388 100NF
FB45 BLM15PD121SN1D 120ohm
C391 10UF
C392 100NF
FB44 BLM15PD121SN1D 120ohm
C389 10UF
C390 100NF
FB46 BLM15PD121SN1D 120ohm
C393 10UF
C394 100NF
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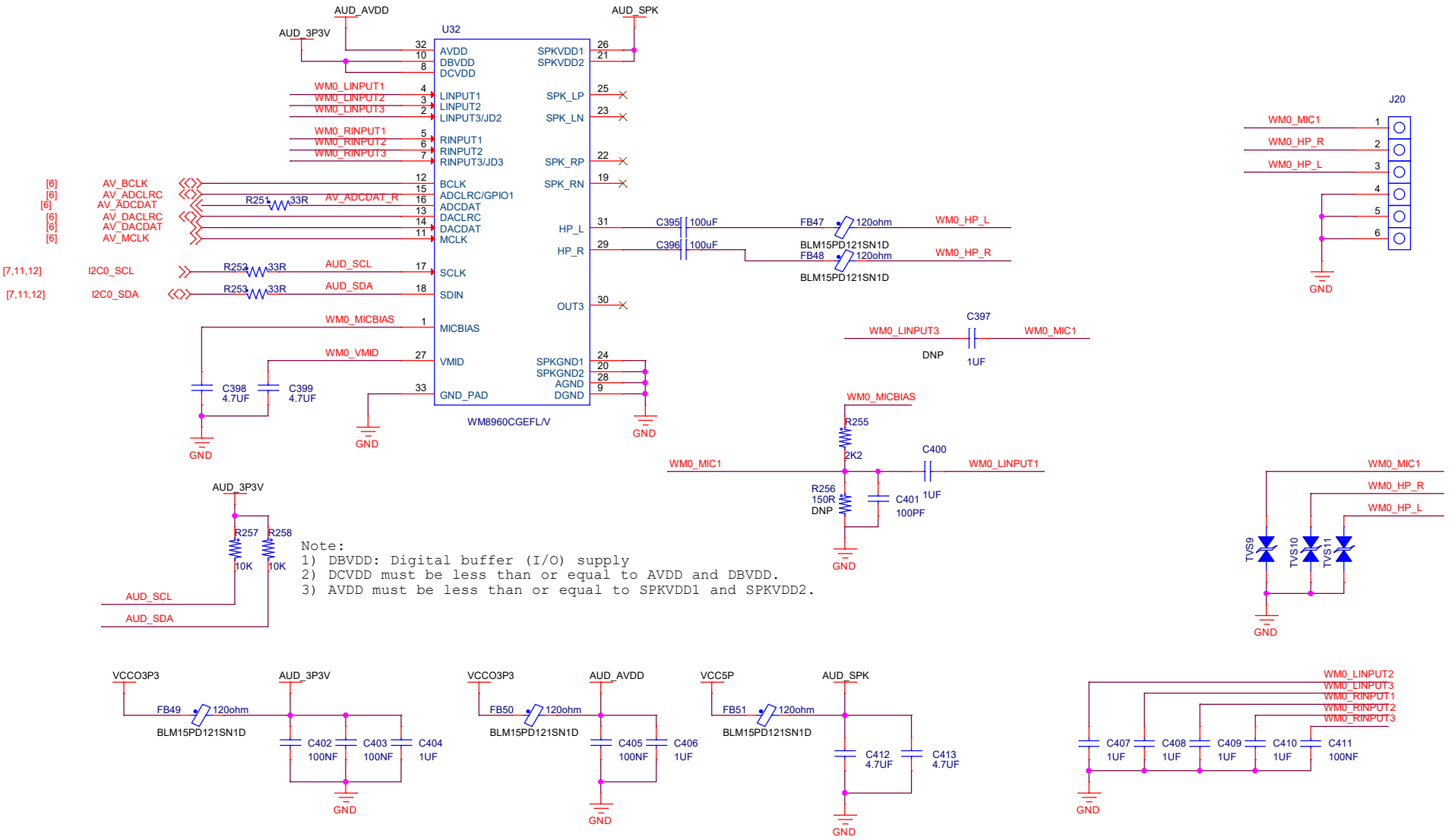

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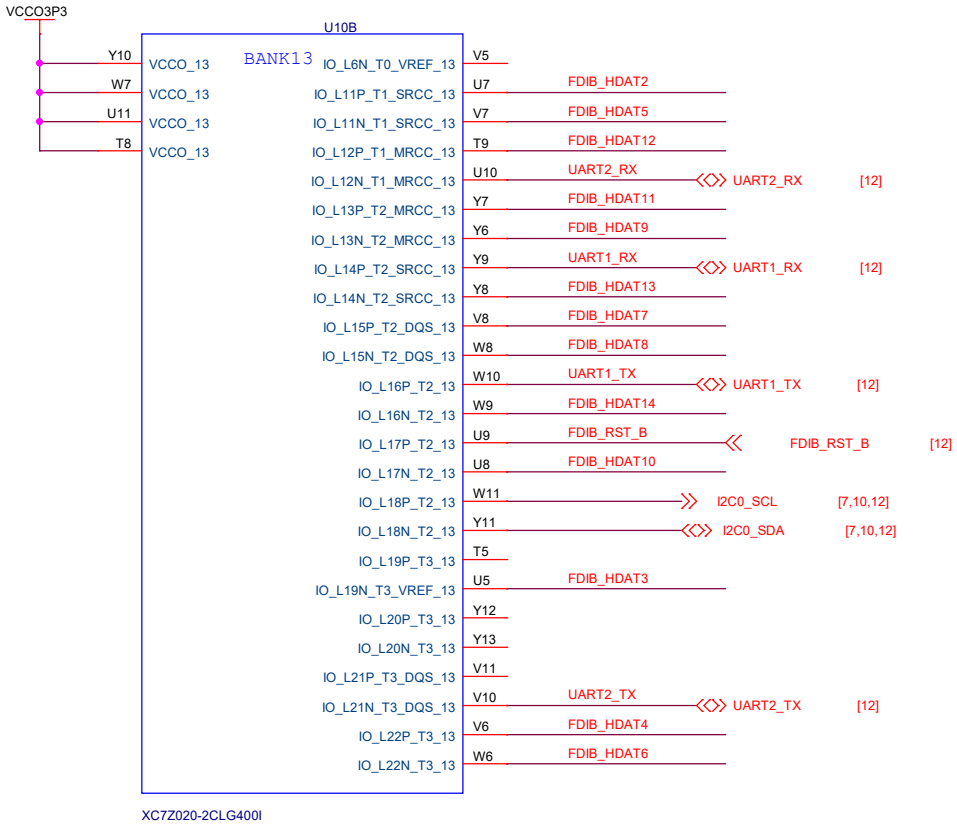

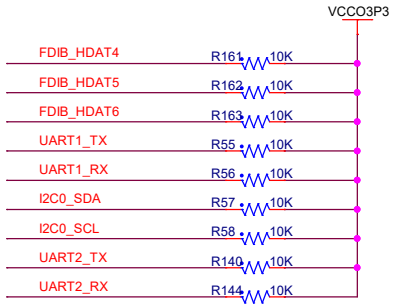

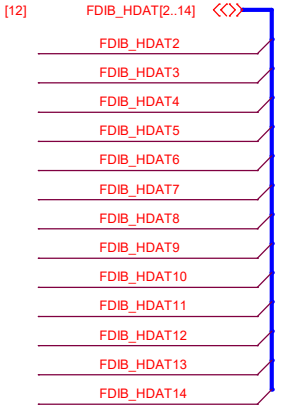

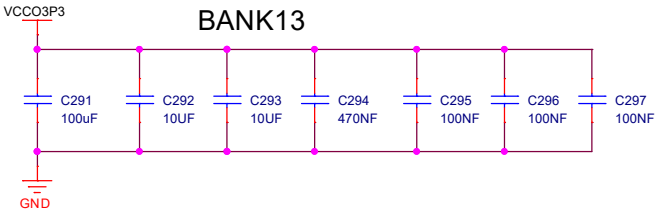

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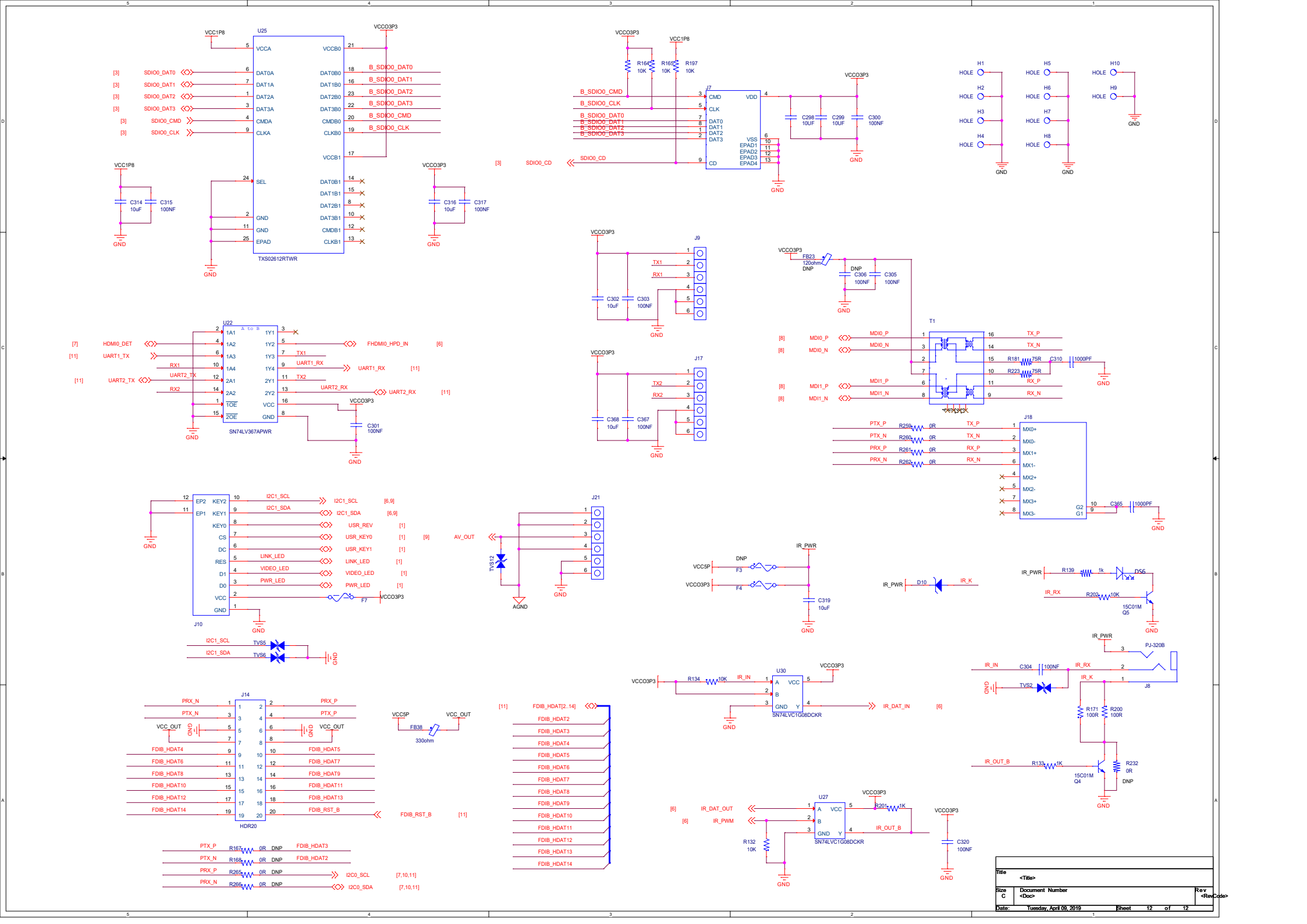
U25
TXS02612RTWR
VCC1P8
VCCO3P3
SDIO0_DAT0
SDIO0_DAT1
SDIO0_DAT2
SDIO0_DAT3
SDIO0_CMD
SDIO0_CLK
B_SDIO0_DAT0
B_SDIO0_DAT1
B_SDIO0_DAT2
B_SDIO0_DAT3
B_SDIO0_CMD
B_SDIO0_CLK
C314 10uF
C315 100NF
C316 10uF
C317 100NF
GND
J7
SDIO0_CD
R164 10K
R165 10K
R197 10K
C298 10UF
C299 10UF
C300 100NF
H1 HOLE
H2 HOLE
H3 HOLE
H4 HOLE
H5 HOLE
H6 HOLE
H7 HOLE
H8 HOLE
H10 HOLE
H9 HOLE
U22
SN74LV367APWR
HDMI0_DET
UART1_TX
UART2_TX
UART2_RX
RX1
RX2
FHDMI0_HPD_IN
UART1_RX
TX1
TX2
C301 100NF
J9
J17
C302 10uF
C303 100NF
C368 10uF
C367 100NF
FB23 120ohm DNP
C306 100NF
C305 100NF
T1
MDI0_P
MDI0_N
MDI1_P
MDI1_N
TX_P
TX_N
RX_P
RX_N
R181 75R
R223 75R
C310 1000PF
J18
MX0+
MX0-
MX1+
MX1-
MX2+
MX2-
MX3+
MX3-
PTX_P
PTX_N
PRX_P
PRX_N
R259 0R
R260 0R
R261 0R
R262 0R
C365 1000PF
J10
I2C1_SCL
I2C1_SDA
USR_REV
USR_KEY0
USR_KEY1
LINK_LED
VIDEO_LED
PWR_LED
F7
TVS5
TVS6
J21
AV_OUT
TVS12
AGND
IR_PWR
DNP
VCC5P
F3
F4
C319 10uF
D10
IR_K
R139 1k
DS6
IR_RX
R202 10K
15C01M
Q5
PJ-320B
IR_IN
C304 100NF
TVS2
J8
R171 100R
R200 100R
IR_OUT_B
R133 1K
R232 0R
Q4
R134 10K
U30
SN74LVC1G08DCKR
IR_DAT_IN
U27
IR_DAT_OUT
IR_PWM
R201 1K
R132 10K
C320 100NF
J14
HDR20
VCC_OUT
FB38 330ohm
FDIB_HDAT2
FDIB_HDAT3
FDIB_HDAT4
FDIB_HDAT5
FDIB_HDAT6
FDIB_HDAT7
FDIB_HDAT8
FDIB_HDAT9
FDIB_HDAT10
FDIB_HDAT11
FDIB_HDAT12
FDIB_HDAT13
FDIB_HDAT14
FDIB_RST_B
R167 0R DNP
R168 0R DNP
R265 0R DNP
R266 0R DNP
I2C0_SCL
I2C0_SDA
Title
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