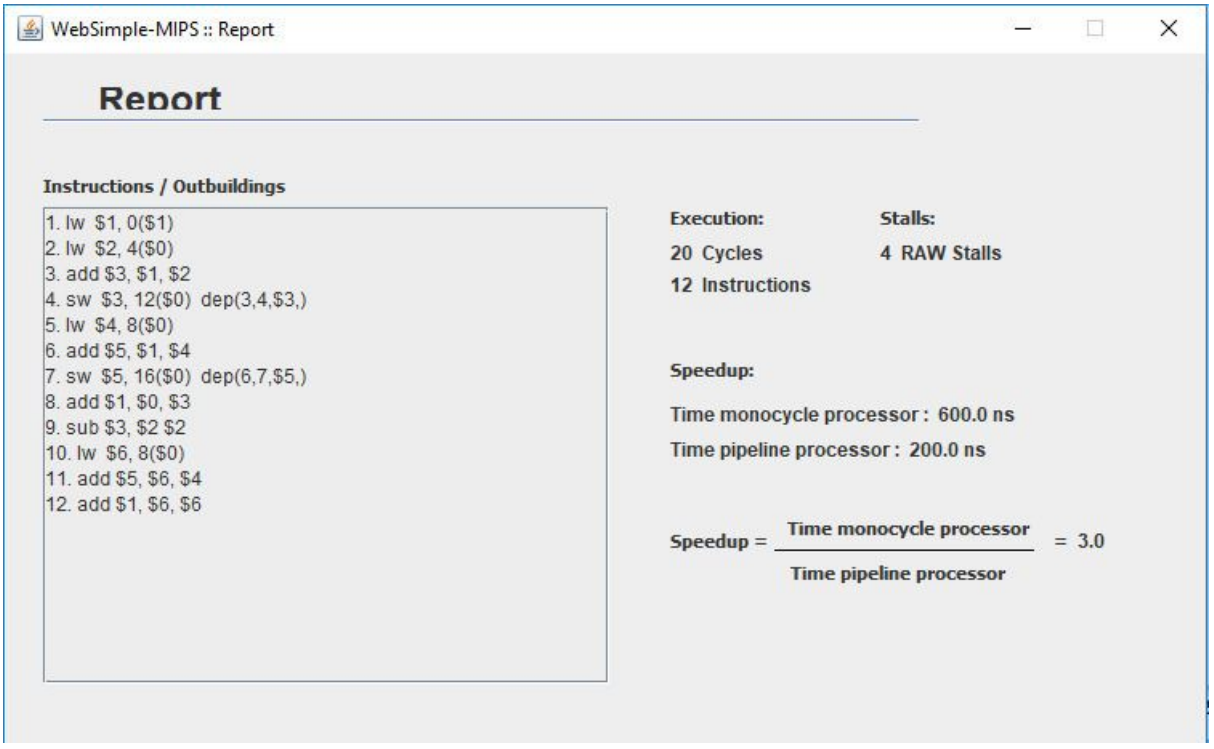
UNIVERSIDADE FEDERAL DA BAHIA
INSTITUTO DE MATEMÁTICA E ESTATÍSTICA
DEPARTAMENTO DE CIÊNCIA DA COMPUTAÇÃO
DISCIPLINA: MATA48 – Arquitetura de Computadores
PROFESSOR: Marcos Ennes Barreto SEMESTRE: 2019.1
ALUNOS: Artur Oscar e Luíz Cláudio

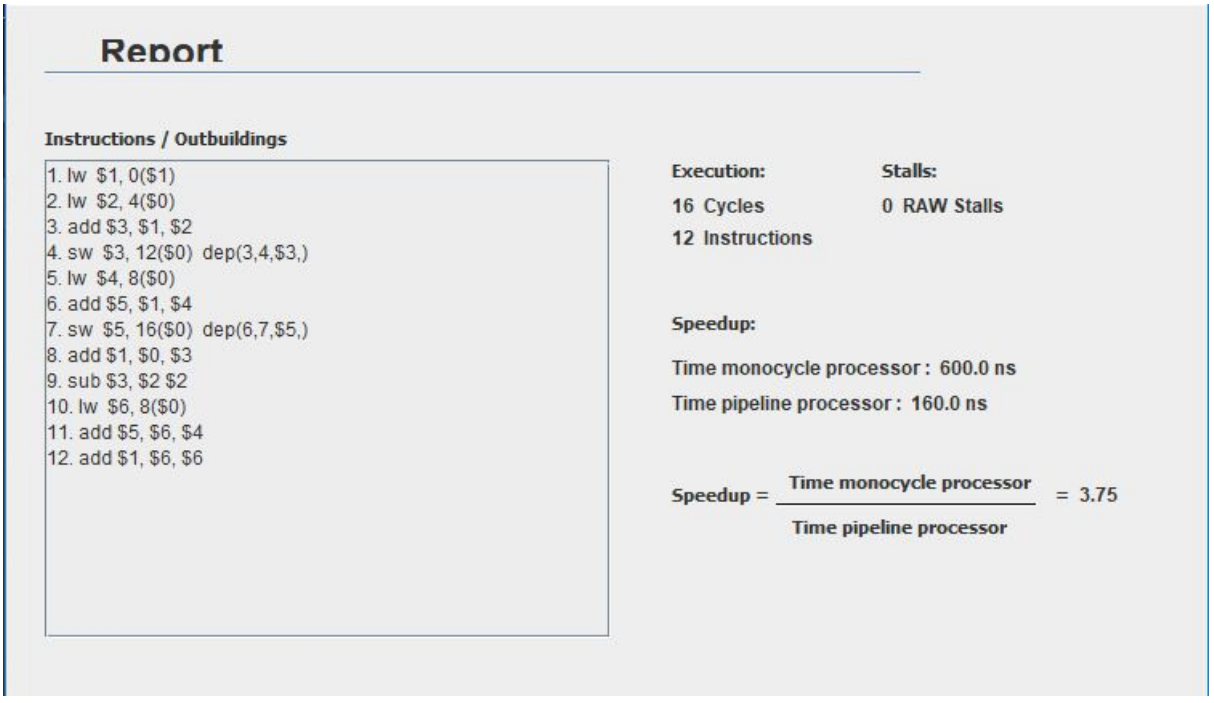
TRABALHO PRÁTICO II

2019

a)


WebSimple-MIPS :: Report
Report
Instructions / Outbuildings
1. lw $1, 0($1)
2. lw $2, 4($0)
3. add $3, $1, $2
4. sw $3, 12($0) dep(3,4,$3,)
5. lw $4, 8($0)
6. add $5, $1, $4
7. sw $5, 16($0) dep(6,7,$5,)
8. add $1, $0, $3
9. sub $3, $2 $2
10. lw $6, 8($0)
11. add $5, $6, $4
12. add $1, $6, $6
Execution:
20 Cycles
12 Instructions
Stalls:
4 RAW Stalls
Speedup:
Time monocycle processor : 600.0 ns
Time pipeline processor : 200.0 ns
Speedup = Time monocycle processor / Time pipeline processor = 3.0

b)


Report
Instructions / Outbuildings
1. lw $1, 0($1)
2. lw $2, 4($0)
3. add $3, $1, $2
4. sw $3, 12($0) dep(3,4,$3,)
5. lw $4, 8($0)
6. add $5, $1, $4
7. sw $5, 16($0) dep(6,7,$5,)
8. add $1, $0, $3
9. sub $3, $2 $2
10. lw $6, 8($0)
11. add $5, $6, $4
12. add $1, $6, $6
Execution:
16 Cycles
12 Instructions
Stalls:
0 RAW Stalls
Speedup:
Time monocycle processor : 600.0 ns
Time pipeline processor : 160.0 ns
Speedup = Time monocycle processor / Time pipeline processor = 3.75

c)

Report

Instructions / Outbuildings

1. lw $1, 0($1)
2. lw $2, 4($0)
3. add $3, $1, $2
4. sw $3, 12($0) dep(3,4,$3,)
5. lw $4, 8($0)
6. add $5, $1, $4
7. sw $5, 16($0) dep(6,7,$5,)
8. add $1, $0, $3
9. sub $3, $2 $2
10. lw $6, 8($0)
11. add $5, $6, $4
12. add $1, $6, $6

Execution: **Stalls:**

18 Cycles 2 RAW Stalls

12 Instructions

Speedup:

Time monocycle processor : 600.0 ns

Time pipeline processor : 180.0 ns

$$\text{Speedup} = \frac{\text{Time monocycle processor}}{\text{Time pipeline processor}} = 3.333$$

d)

Report

Instructions / Outbuildings

1. lw $1, 0($1)
2. lw $2, 4($0)
3. add $3, $1, $2
4. sw $3, 12($0) dep(3,4,$3,)
5. lw $4, 8($0)
6. add $5, $1, $4
7. sw $5, 16($0) dep(6,7,$5,)
8. add $1, $0, $3
9. sub $3, $2 $2
10. lw $6, 8($0)
11. add $5, $6, $4
12. add $1, $6, $6

Execution: **Stalls:**

20 Cycles 4 RAW Stalls

12 Instructions

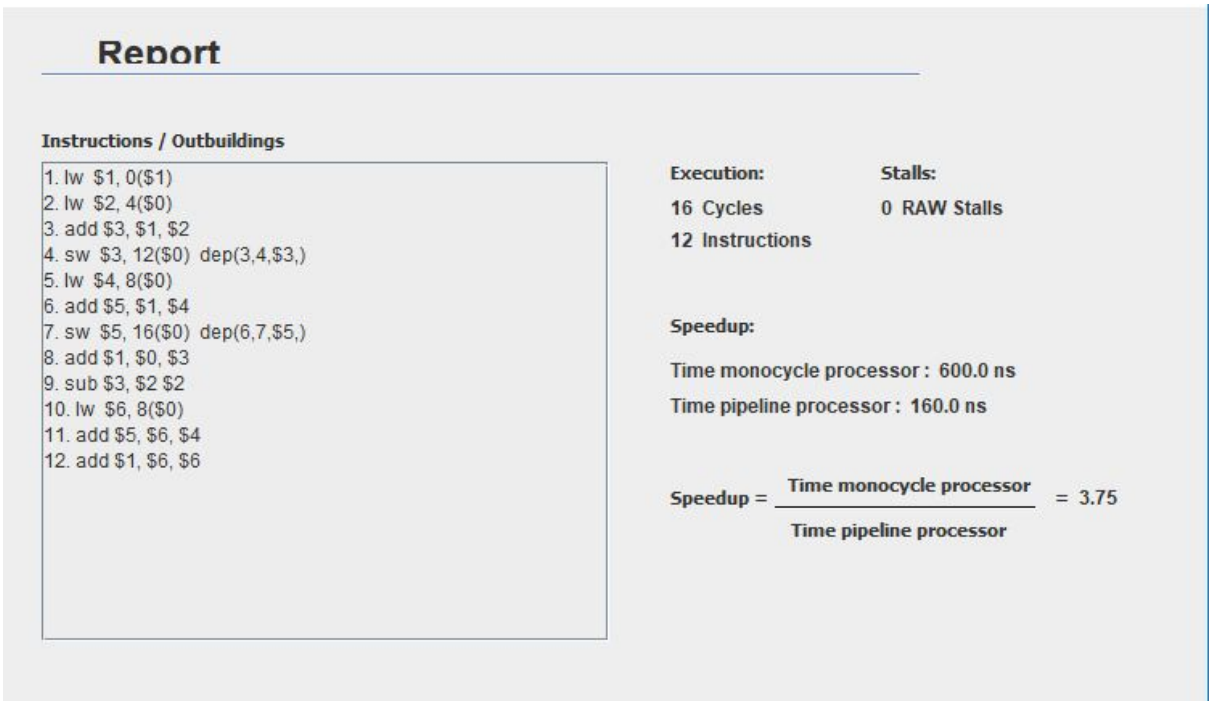
Speedup:

Time monocycle processor : 600.0 ns

Time pipeline processor : 200.0 ns

$$\text{Speedup} = \frac{\text{Time monocycle processor}}{\text{Time pipeline processor}} = 3.0$$

e)



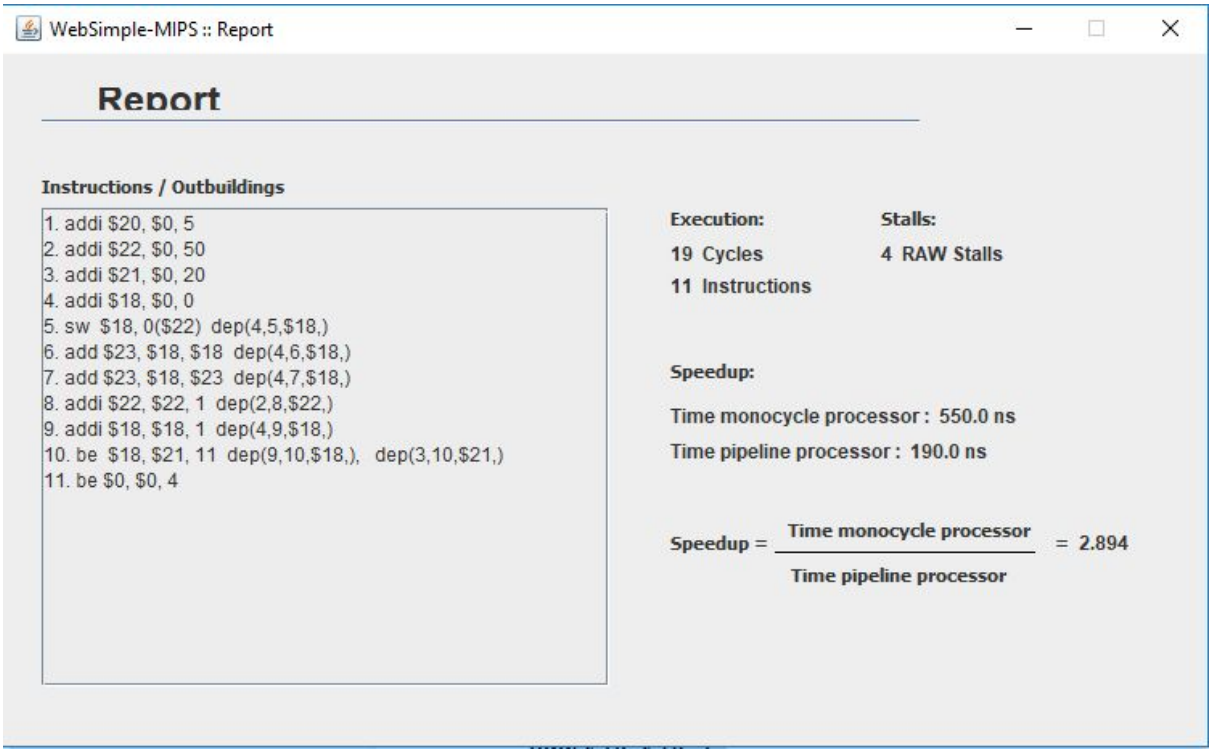
f) Não é viável tecnicamente utilizar forwarding MEM->EX e WB->EX ao mesmo tempo, pois duas informações conflitantes podem ser enviadas para o estágio EX, vindas do estágio WB e do estágio MEM ao mesmo tempo. Como há de ser escolhida uma dentre as três configurações de forwarding, é melhor optar pelo forwarding MEM->EX, pois o resultado da instrução anterior pode ser enviado para o EX uma iteração antes do que no tipo de forwarding WB->EX. Dentre os resultados das questões b a d, esse tipo de forwarding foi o que provocou maior speedup.

g)

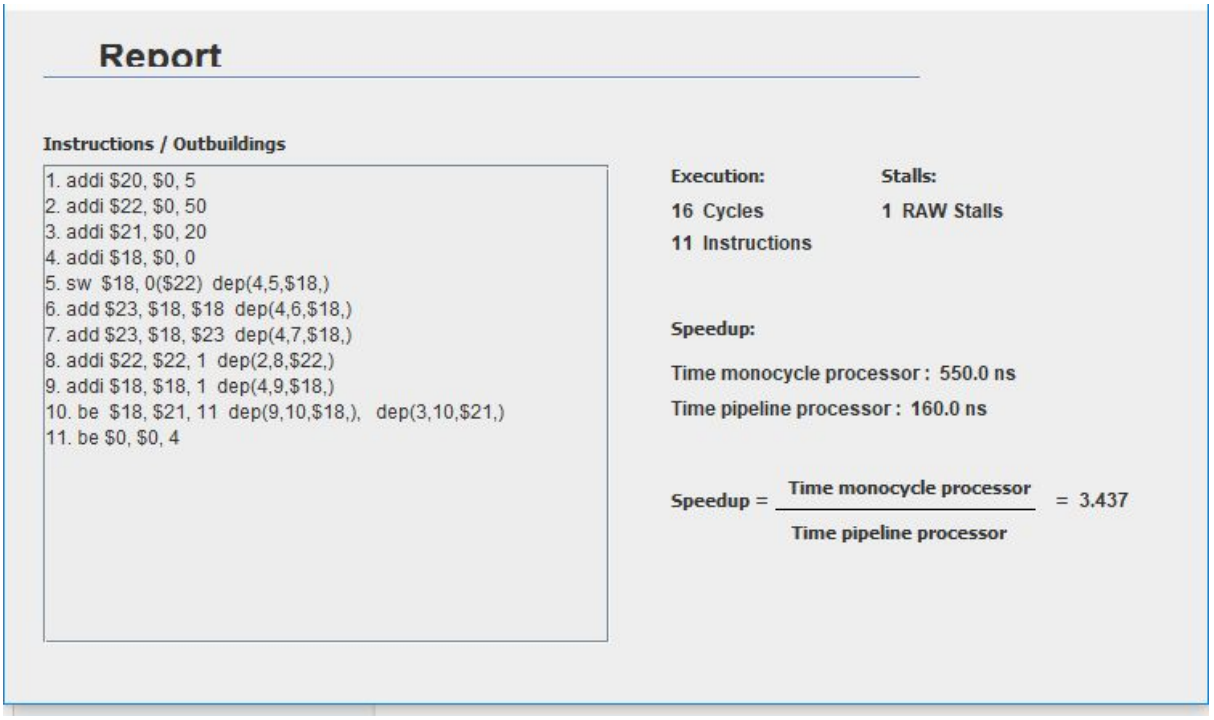
Trecho 1 ADAPTADO:

```
addi $20, $0, 5
addi $22, $0, 50
addi $21, $0, 20
addi $18, $0, 0
sw  $18, 0($22)
add $23, $18, $18
add $23, $18, $23
addi $22, $22, 1
addi $18, $18, 1
be  $18, $21, 11
be $0, $0, 4
```

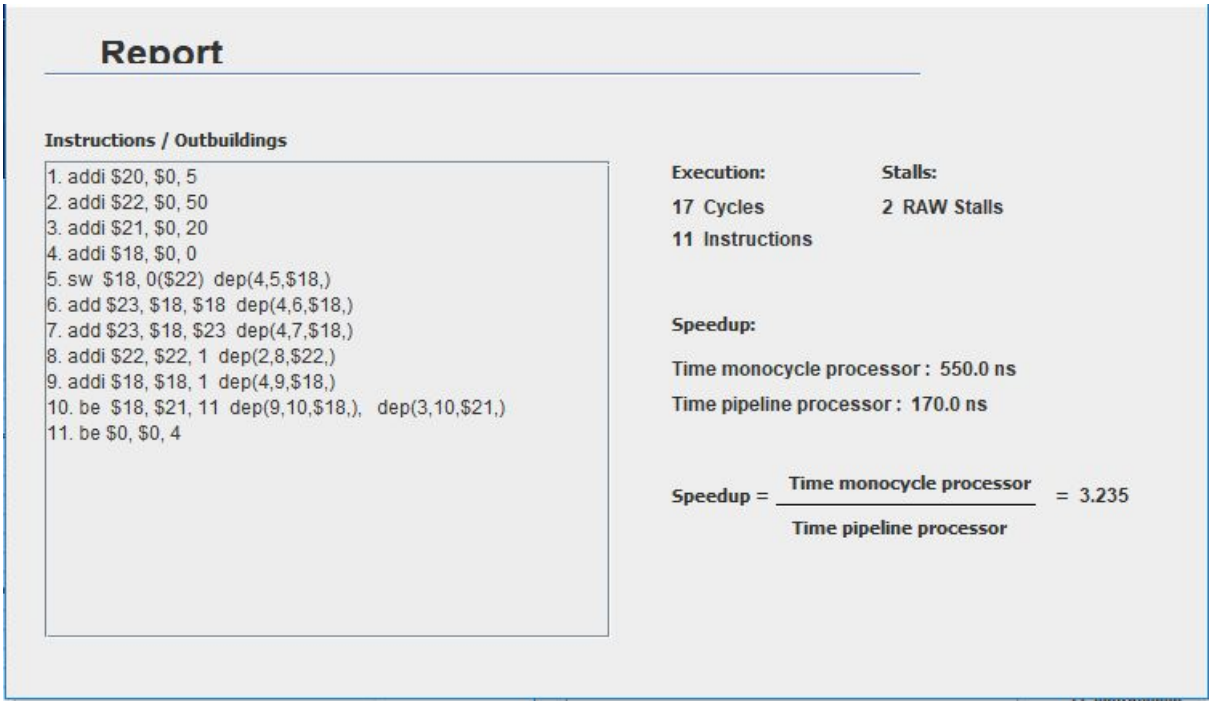
Trecho 1, relatório a)



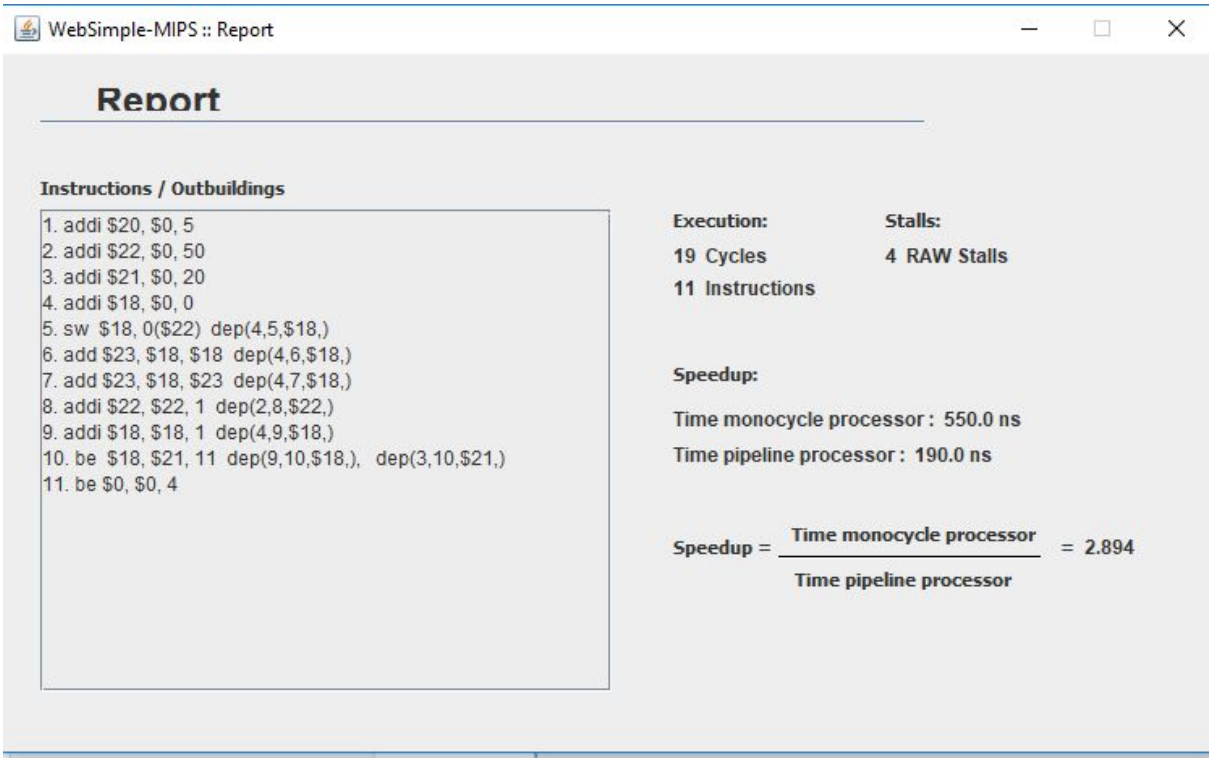
Trecho 1, relatório b)



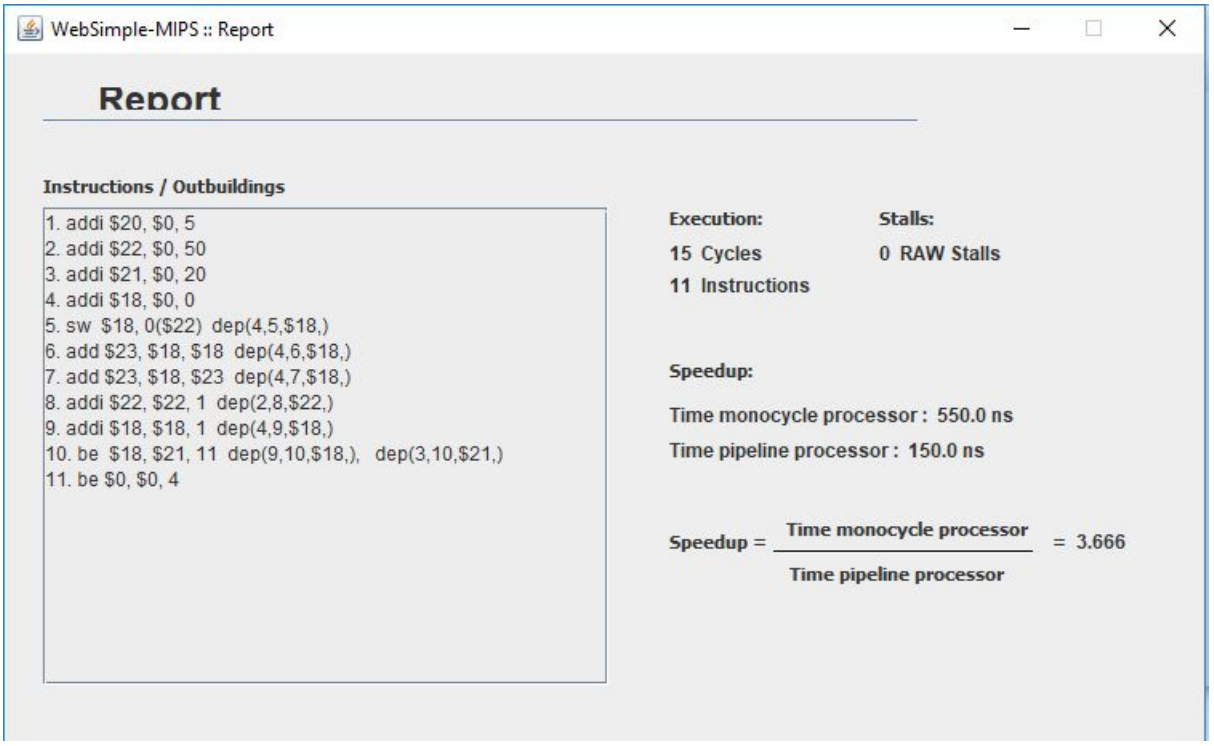
Trecho 1, relatório c)



Trecho 1, relatório d)



Trecho 1, relatório e)



Trecho 2 ADAPTADO:

```
lw  $20,  0($1)
lw   $18, 1($1)
lw  $19, 2($1)
mul $19, $20, 2
add $19, $19 ,$18
sub $18, $18, 1
add $20, $23, $20
add $20, $2, $0
blt $20, $0, 3
```

Trecho 2, relatório a)

Report

Instructions / Outbuildings

1. lw $20, 0($1)
2. lw $18, 1($1) dep(1,2,)
3. lw $19, 2($1)
4. mul $19, $20, 2
5. add $19, $19 ,$18
6. sub $18, $18, 1
7. add $20, $23, $20
8. add $20, $2, $0
9. blt $20, $0, 3

Execution: Stalls:

15 Cycles 2 RAW Stalls

9 Instructions

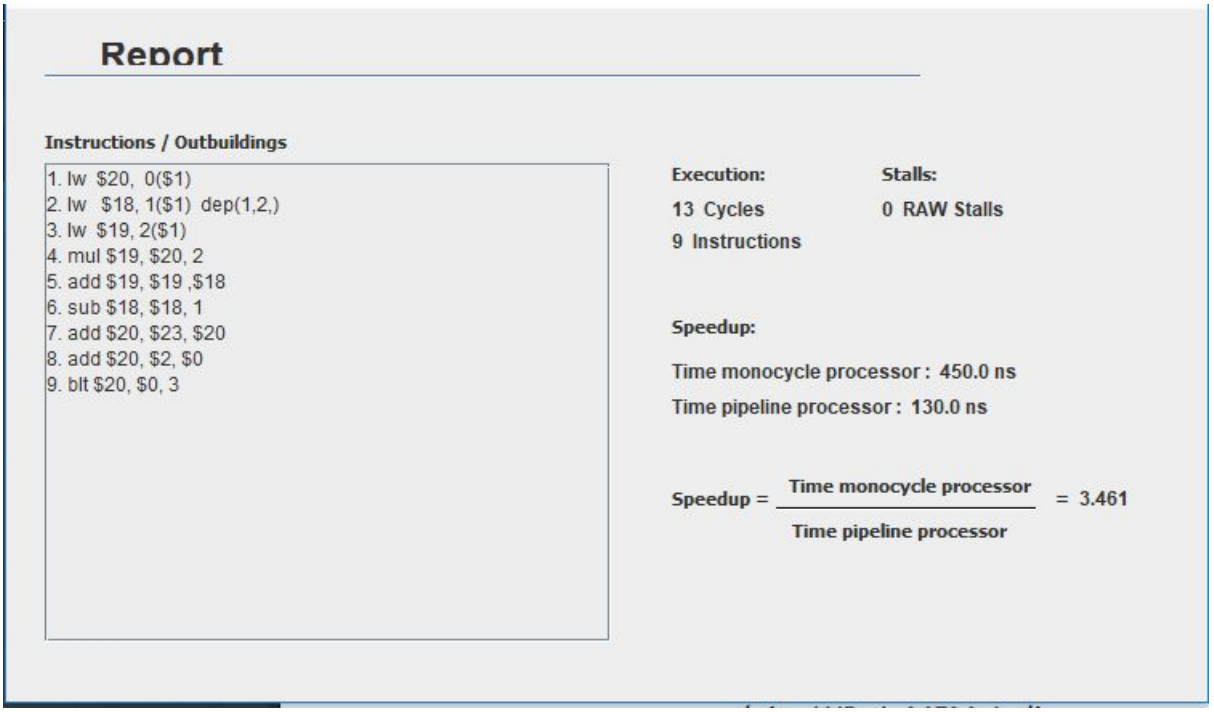
Speedup:

Time monocycle processor : 450.0 ns

Time pipeline processor : 150.0 ns

$$\text{Speedup} = \frac{\text{Time monocycle processor}}{\text{Time pipeline processor}} = 3.0$$

Trecho 2, relatório b)



Report

Instructions / Outbuildings

1. lw $20, 0($1)
2. lw $18, 1($1) dep(1,2,)
3. lw $19, 2($1)
4. mul $19, $20, 2
5. add $19, $19 ,$18
6. sub $18, $18, 1
7. add $20, $23, $20
8. add $20, $2, $0
9. blt $20, $0, 3

Execution: Stalls:

13 Cycles 0 RAW Stalls

9 Instructions

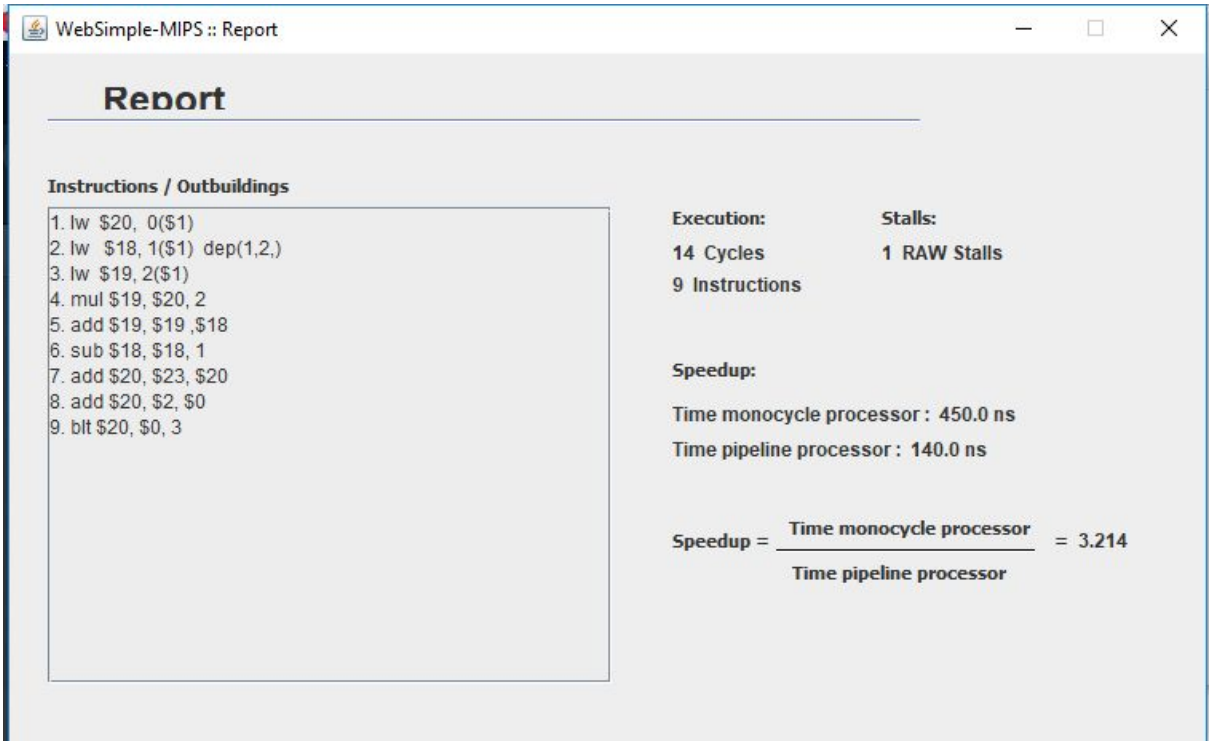
Speedup:

Time monocycle processor : 450.0 ns

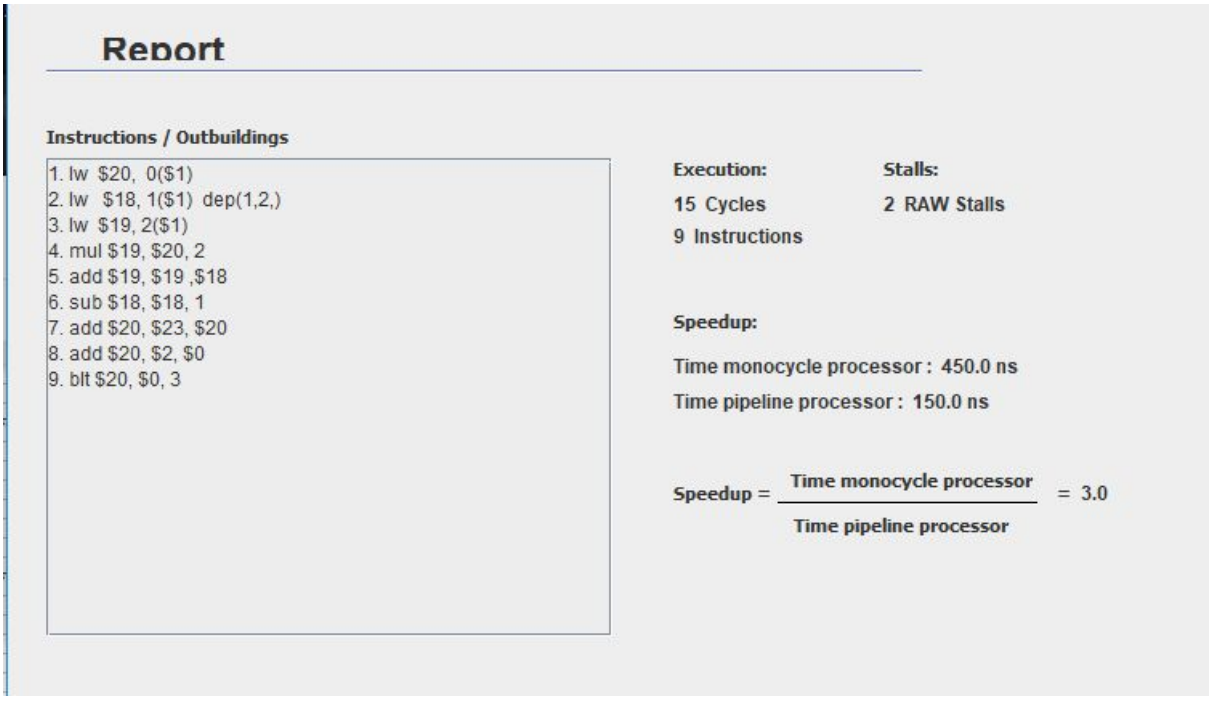
Time pipeline processor : 130.0 ns

$$\text{Speedup} = \frac{\text{Time monocycle processor}}{\text{Time pipeline processor}} = 3.461$$

Trecho 1, relatório c)



Trecho 1, relatório d)



Trecho 2, relatório e)