

# Sine Wave generation with desired number of ON-OFF cycles and initial phase using on-board MCP4921 DAC on Xenon FPGA Board

## 1 Introduction

The system is designed to produce a sine wave with desired number of ON and OFF cycles. The system accepts two input values through the DIP switches of the Xenon board. Pin 7 to pin 4 is used for entering the number of ON cycles and pin 3 to pin 0 is used for entering the number of OFF cycles. The Max 10 FPGA on the Xenon Board communicates with the on board MCP4921 DAC through Serial Peripheral Interface(SPI) communication protocol.

## 2 Working

### 2.1 Pin description of MCP4921 DAC

MCP4921 DAC has the following pins-

- Positive Power Supply Input (VDD) - VDD is the positive power supply input. The input power supply is relative to AVSS and can range from 2.7V to 5.5V.
- Chip Select (CS') - CS' is the chip select input, which requires an active-low signal to enable serial clock and data functions.
- Serial Clock Input (SCK) - SCK is the SPI compatible serial clock input.
- Serial Data Input (SDI) - SDI is the SPI compatible serial data input.
- Latch DAC Input (LDAC') - LDAC' (the latch DAC synchronization input) transfers the input latch registers to the DAC registers (output latches) when low.
- Analog Ground (AVSS) - analog ground pin.
- DAC voltage reference input - The analog signal on these pins is utilized to set the reference voltage on the string DAC. The input signal can range from AVSS to VDD.
- DAC output - Output of DAC.

These pins are already connected to the IO pins of the Xenon board and the pin numbers of the same are available in the [Xenon user manual](#).

### 2.2 Communication using SPI

- The FPGA communicates with the onboard MCP4921 DAC using Serial Peripheral Interface (SPI) communication protocol.
- Commands and data are sent to the device via the SDI pin, with data being clocked-in on the rising edge of SCK.
- The CS' pin must be held low for the duration of a write command. The write command consists of 16 bits and is used to configure the DAC's control and data latches.

<b>Upper Half:</b>								
W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x
$\overline{A/B}$	BUF	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8	
bit 15								bit 8

Figure 1: Write command register upper half

<b>Lower Half:</b>								
W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
D7	D6	D5	D4	D3	D2	D1	D0	
bit 7								bit 0

Figure 2: Write command register lower half

- The write command consists of 16 bits and is used to configure the DAC's control and data latches
- Bit 15 to bit 11 of the write command register are configuration bits (are set to 0011 for our application) followed by 12 data bits from bit 11 to bit 0.
- The write command is initiated by driving the CS' pin low, followed by clocking the four configuration bits and the 12 data bits into the SDI pin on the rising edge of SCK. The CS' pin is then raised, causing the data to be latched into the selected DAC's input registers.
- Then the LDAC' pin is set to low state, so that the values held in the DAC's input registers are transferred into the DAC's output registers. The outputs will transition to the value and held in the DAC register.

### 2.3 Algorithm used to generate sine wave with required number of ON and OFF cycles using VHDL

- Look up table based logic is used for sine wave generation using the onboard MCP4921 DAC on the Xenon board.
- Two look-up tables are used, one which contains 24 12-bit data samples corresponding to one cycle of sine wave and another empty look-up table which contains 24 12-bit 0 values corresponding to one OFF cycle.
- The write command register frame for the DAC is generated and sent to the write command register of the DAC serially using finite state machine logic in VHDL.
- The FSM contains 7 states. States-1 is reset state, state-2 to state-4 are involved in generation of ON cycles and state-5 to state-7 are involved in generation of OFF cycles.
  - State-1- reset state- CS' and LDAC' are set to '1' and the configuration bits of the write register frame are set to their default value. Also the bit count (variable which keeps the count of the number of bits sent serially to the DAC register) is reset to 0. The FSM unconditionally goes to state 2 after this state.
  - State-2- In this state, the 12 bit data sample from the sine wave LUT is loaded into the write register frame. The FSM unconditionally goes to state 3 after this state.
  - state-3- In this state the data of the write register frame created in the previous state is serially sent to the write register of the DAC through the DAC input pin. The CS' pin is kept at logic '0' during this process. After the all the 16 bits of the frame are sent, a counter counting the number of ON cycles is updated. This value is then compared with

- the required number of ON cycles (which is given as input), and if both the values are equal then the next state will be state 7, and if it is not equal then the next state will be state 4.
- state-4- In this state, the LDAC' pin is changed to logic '0' in order to transfer data from the DAC input register to the DAC output register. The FSM unconditionally goes to state 2 after this state.
  - state-5- In this state, the 12 bit data sample from the empty LUT is loaded into the write register frame(for OFF cycles). The FSM unconditionally goes to state 6 after this state.
  - state-6- In this state the data of the write register frame created in the previous state is serially sent to the write register of the DAC through the DAC input pin. The CS' pin is kept at logic '0' during this process. After the all the 16 bits of the frame are sent, a counter counting the number of OFF cycles is updated. This value is then compared with the required number of OFF cycles (which is given as input), and if both the values are equal then the next state will be state 4, and if it is not equal then the next state will be state 7.
  - state-7- In this state, the LDAC' pin is changed to logic '0' in order to transfer data from the DAC input register to the DAC output register. The FSM unconditionally goes to state 5 after this state.

## 2.4 Setting the frequency of generated sine wave

The DAC is being operated at a clock frequency of 25 MHz. So in order to get a sine wave of desired frequency, the data in the input register of the DAC will have to be sent to the output register of the DAC after a specific number of clock cycles. This means that the loading of the register frame from the LUT will also have to be done after a specific number of clock cycles.

Let n be the number of clock cycles after which we are supposed to load the DAC register frame.

Hence, number of cycles after which data in the input register has to be shifted to output register =  $n + \text{total cycles needed to send the frame data serial into DAC input register} + \text{total cycles needed for sending data from input register to output register}$  =  $n+16+1$

No. of cycles after which data in input register has to be shifted to output register =  $n+17$

Let f be the required frequency of the sine wave.

Since the clock frequency is 25 MHz and the total number of samples in the frame are 24,

$$\frac{1}{25MHz} * (n + 17) * 24 = \frac{1}{fKHz}$$

Hence,

$$n = \frac{1042}{fKHz} - 17$$

This value should be changed in the VHDL code in order to get the desired sine wave frequency.

## 2.5 About Xenon Board

- Here is a picture of the xenon board-

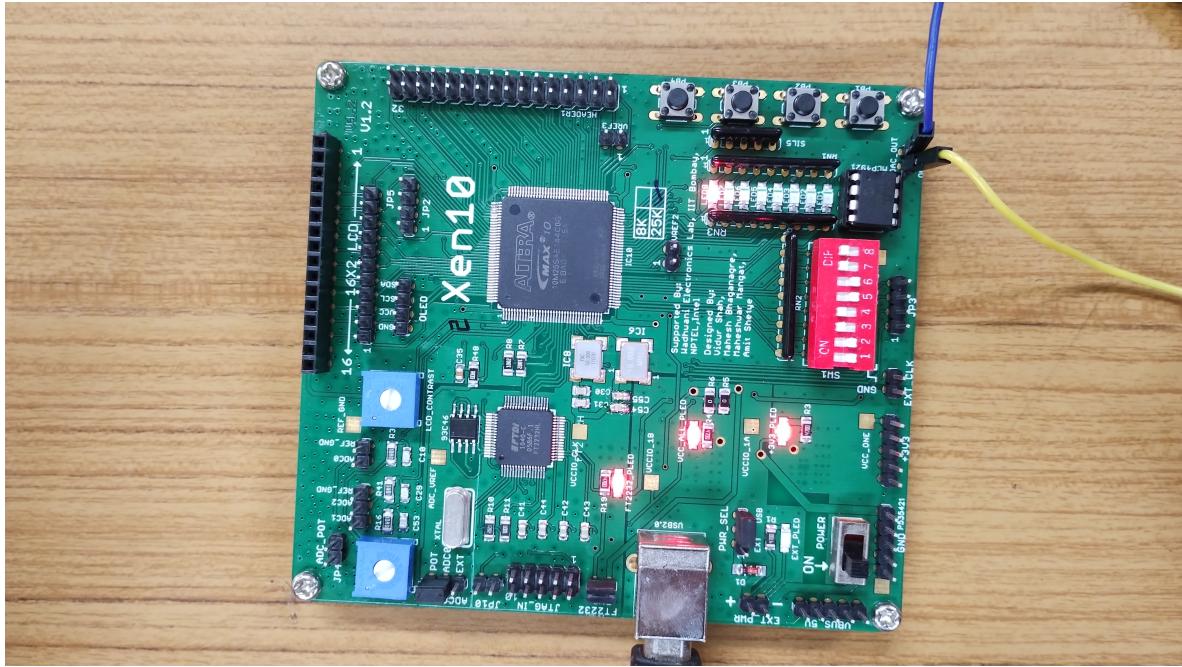


Figure 3: Xenon Board

- A JTAG cable is used to connect the Xenon board to USB port of a laptop/desktop.  
The USB connector of the Xenon board is shown in the below image-

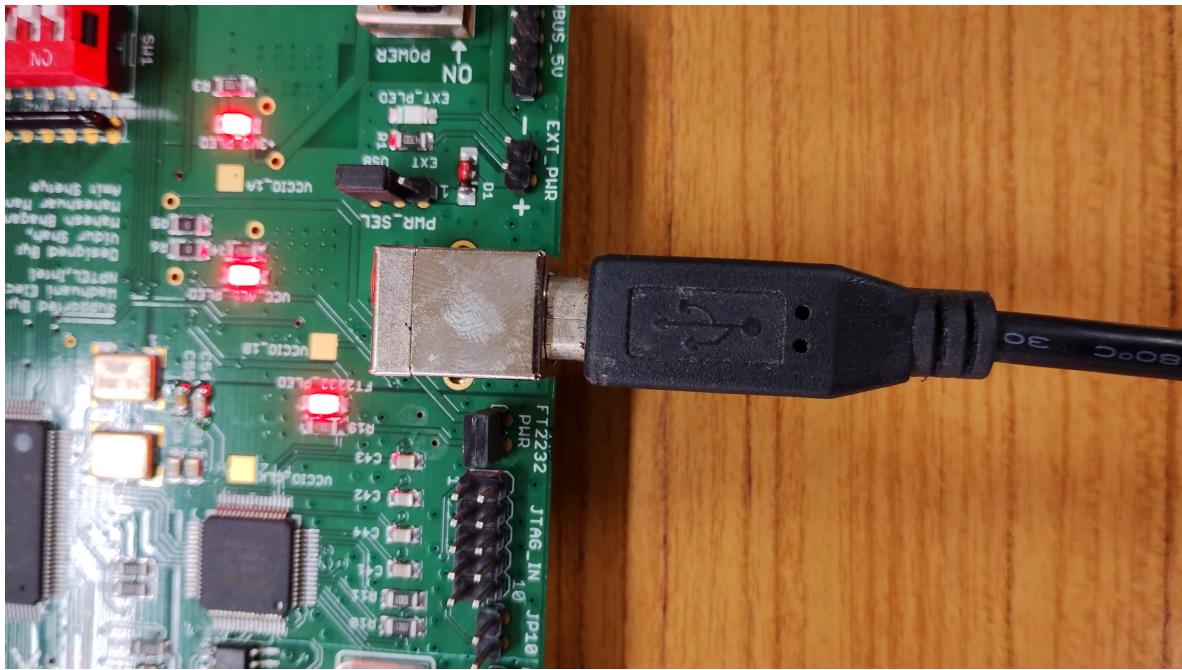


Figure 4: JTAG cable connected to the USB connector of Xenon board

- The DIP switches, DAC chip and the DAC output pins are shown in the figure below. The DAC

chip is encircled in yellow colour, DIP switches are encircled in blue colour and the DAC output pins are encircled in red colour.

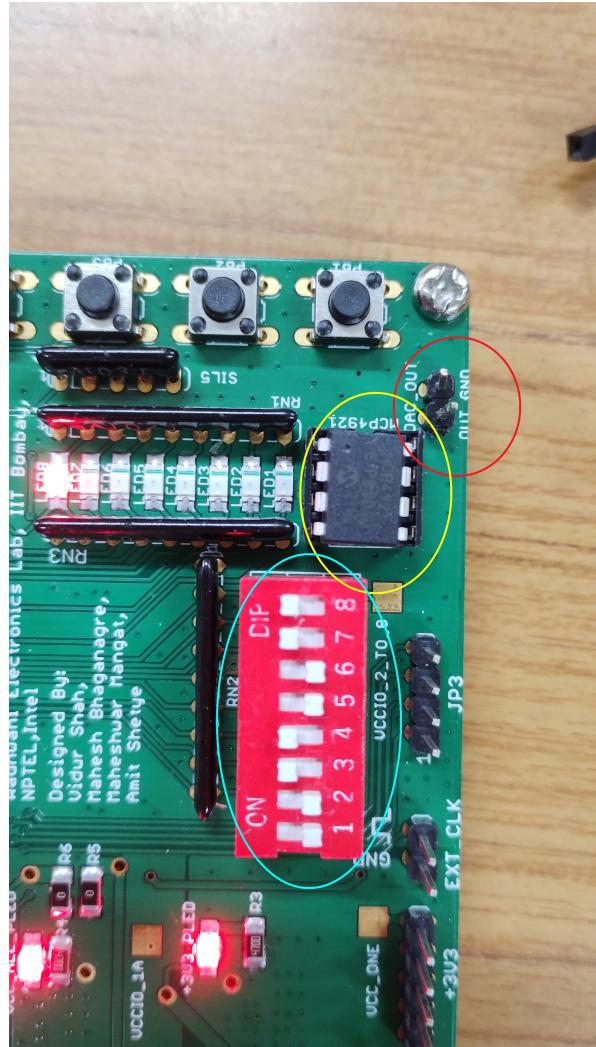


Figure 5: DIP switches, DAC chip and DAC output pins

- PIN 1 to PIN 4 of the DIP switches are used to select the number of ON cycles (PIN 1 being the most significant bit and PIN 4 being the least significant bit). And PIN 5 to PIN 8 of the DIP switches are used to select the number of OFF cycles (PIN 5 being the most significant bit and PIN 8 being the least significant bit). For Eg: to get 6 ON cycles and 5 OFF cycles, the positions of the DIP switches should be OFF-ON-ON-OFF-OFF-ON-OFF-ON.

## 2.6 ON-OFF cycles and Initial Phase adjustment

In the VHDL code there is a variable declared as phase which can take values from 0 to 23. There are 24 steps covering from 0 to 360 degrees, this corresponds to 15 degrees in each step. Lets say the phase is set to a value 5(6th step), the resultant output waveform would have a phase shift of 90 degrees. The DAC output pins are connected to an oscilloscope to observe the output waveform for different input values given through the DIP switch.

- For 2 ON Cycles and 1 OFF cycle with initial phase of 30 degrees



Figure 6: Input for 2 ON cycles and 1 OFF cycle



Figure 7: Output for 2 ON cycles and 1 OFF cycle and initial phase of 30 degrees

- For 3 ON Cycles and 2 OFF cycles and initial phase of 30 degrees

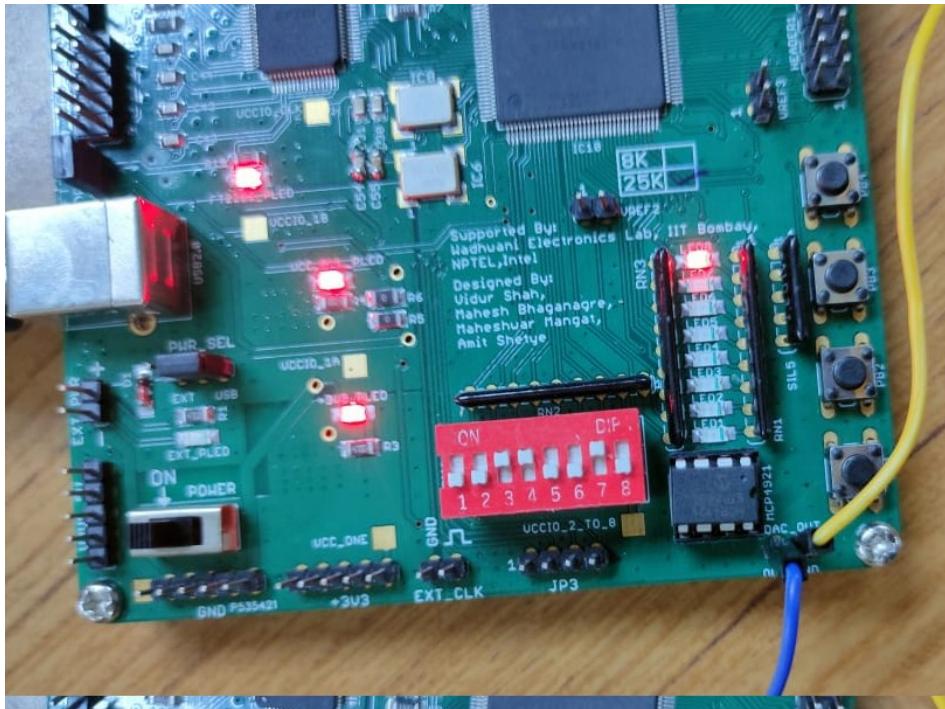


Figure 8: Input for 3 ON cycles and 2 OFF cycles

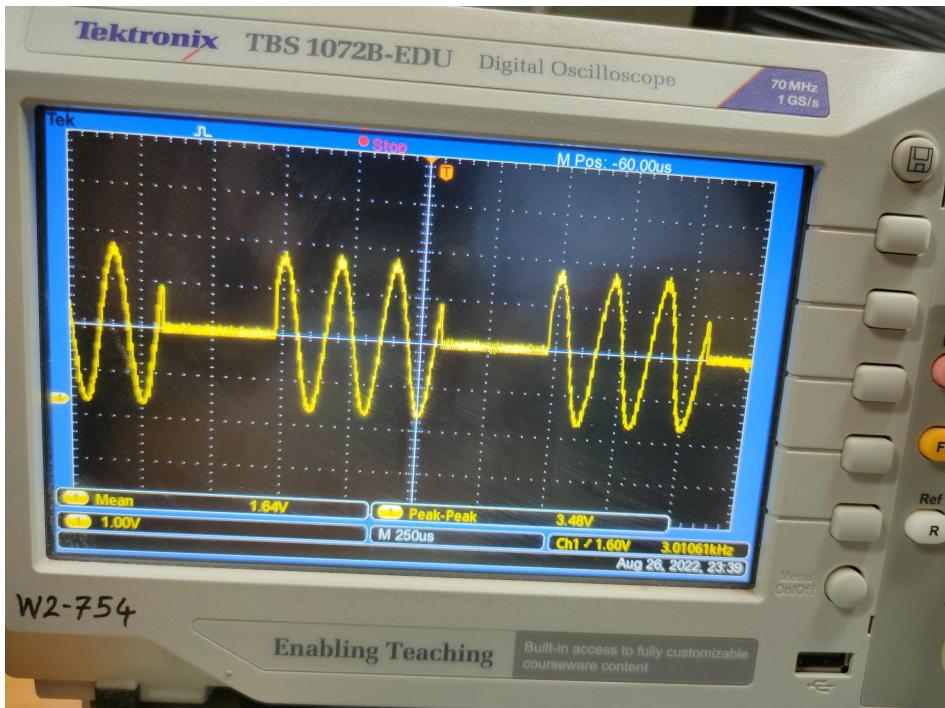


Figure 9: Output for 3 ON cycles and 2 OFF cycles and with initial phase of 30 degrees

- For 3 ON and 2 OFF cycles with initial phase of 270 degrees

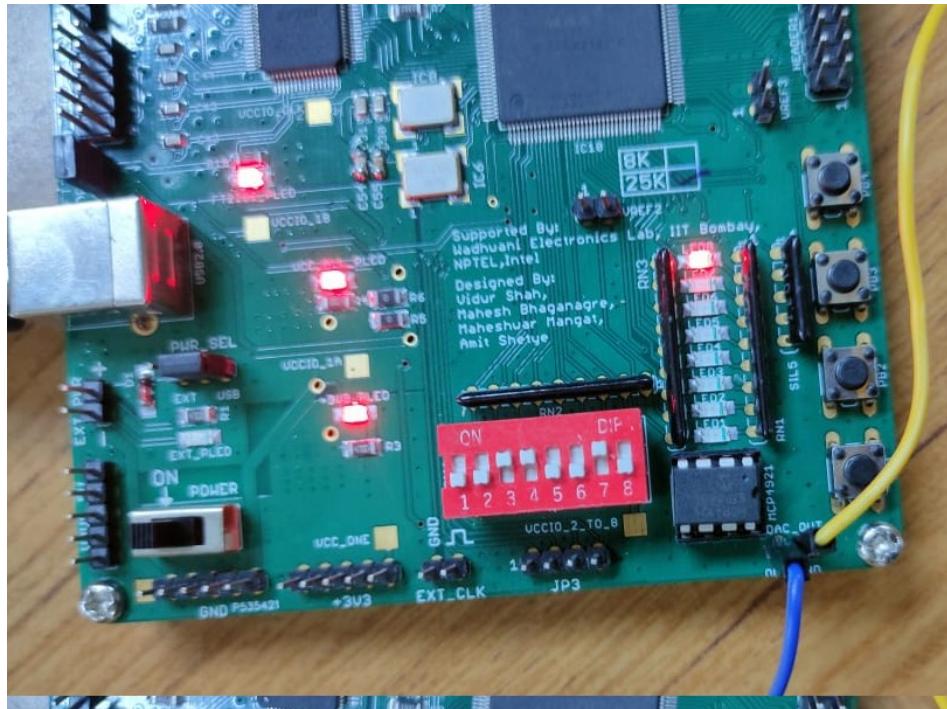


Figure 10: Input for 3 ON cycles and 2 OFF cycles

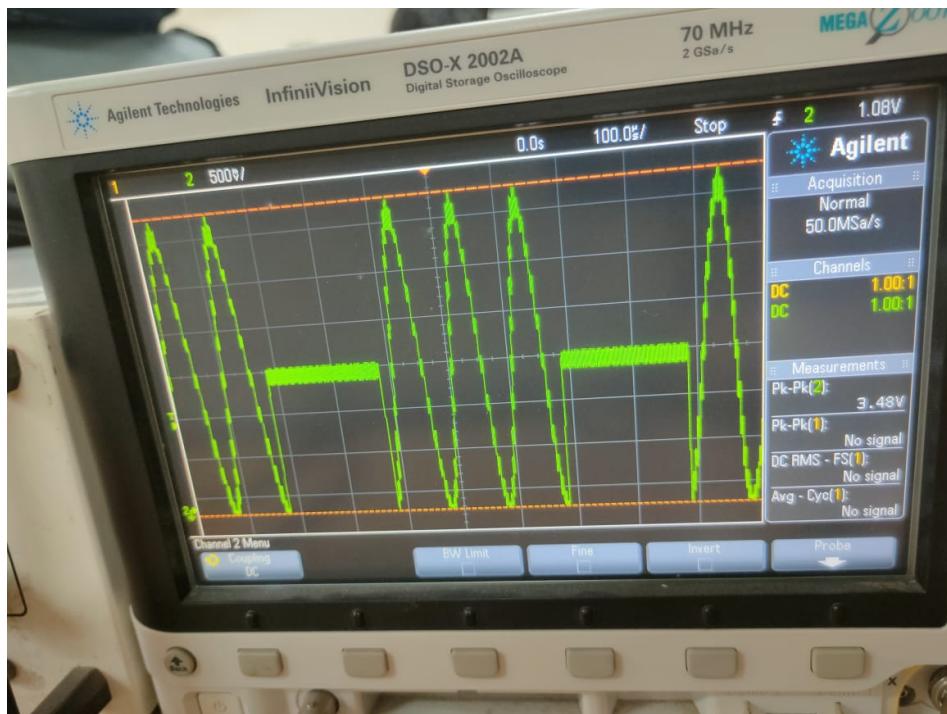


Figure 11: Output for 3 ON cycles and 2 OFF cycle and with initial phase of 270 degrees

- For 11 ON and 3 OFF cycles with initial phase of 270 degrees

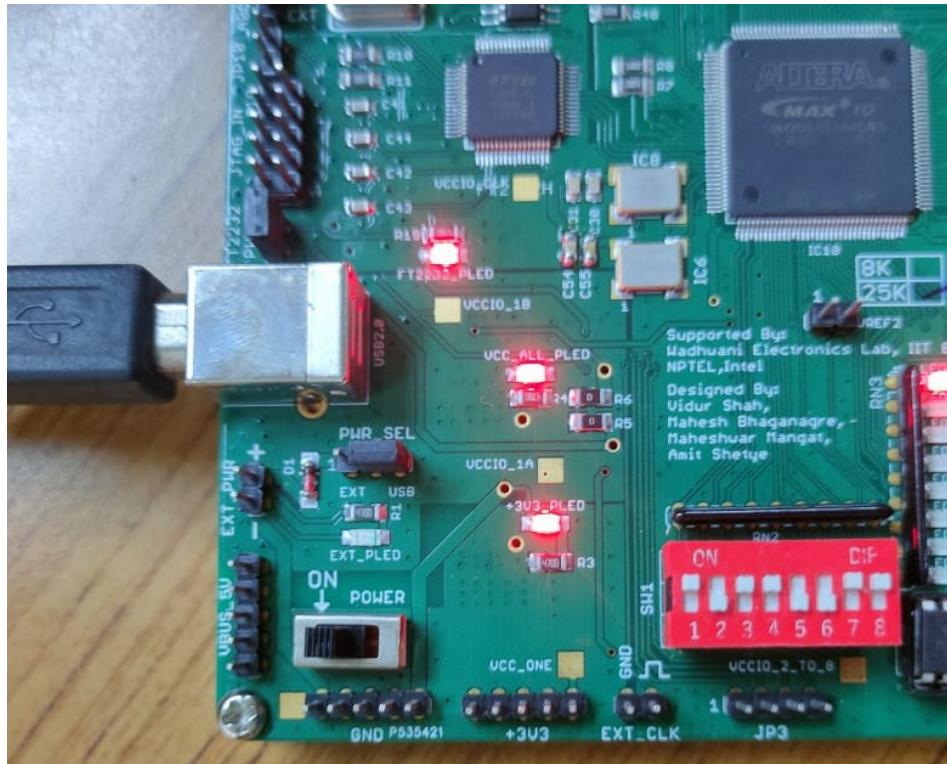


Figure 12: Input for 11 ON cycles and 3 OFF cycles



Figure 13: Output for 11 ON cycles and 3 OFF cycle and with initial phase of 270 degrees

- For 3 ON and 3 OFF cycles with initial phase of 60 degrees

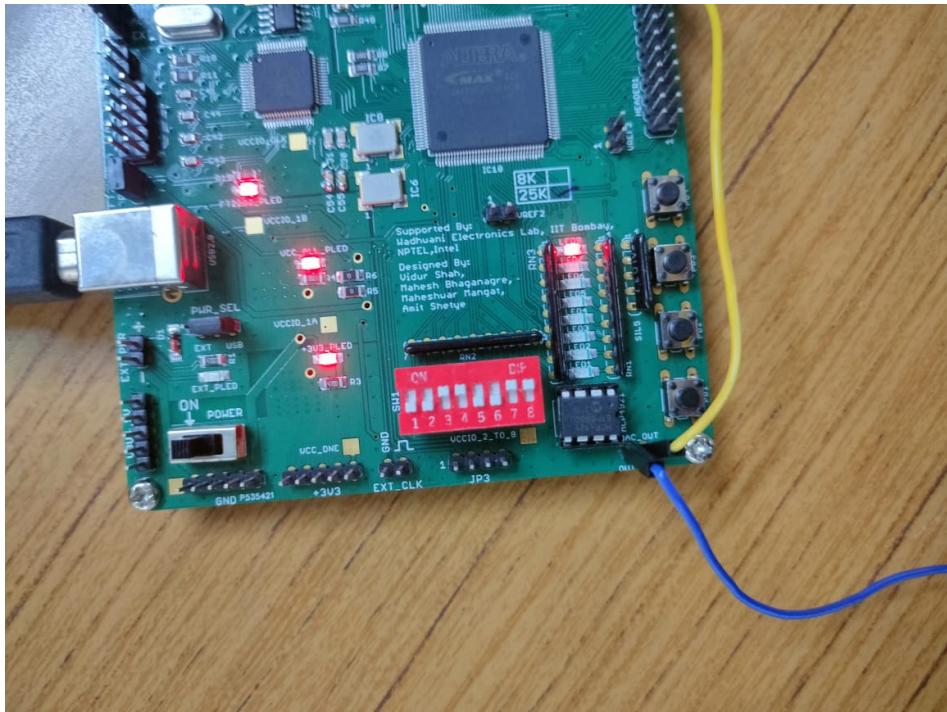


Figure 14: Input for 3 ON cycles and 3 OFF cycles

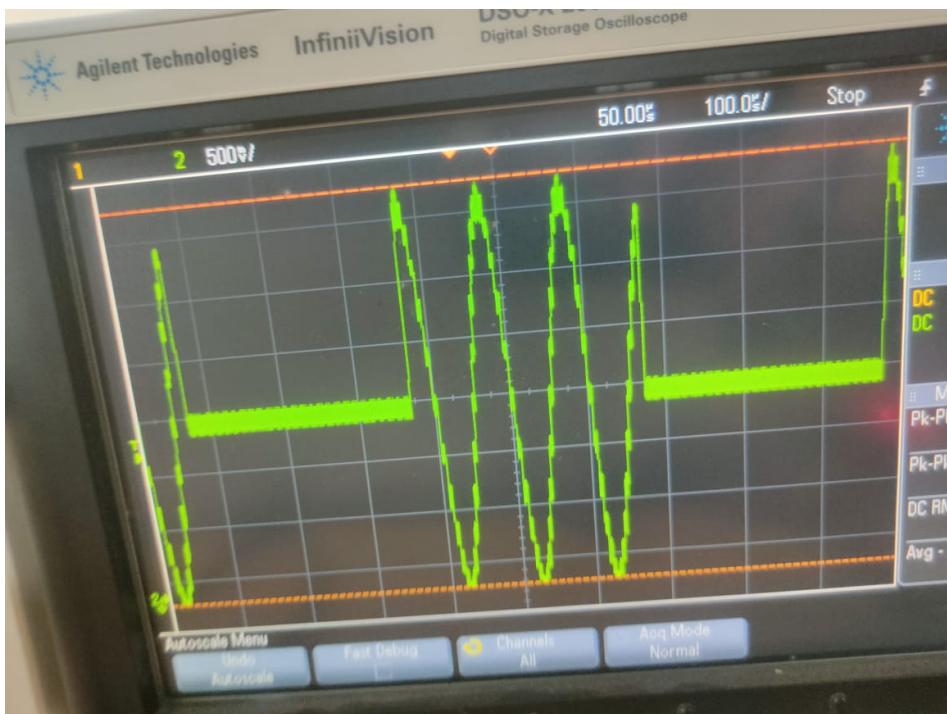


Figure 15: Output for 3 ON cycles and 3 OFF cycle and with initial phase of 60 degrees

- Generation of 5 KHz sine wave by setting off cycles to zero. Frequency is controlled using vhdl code

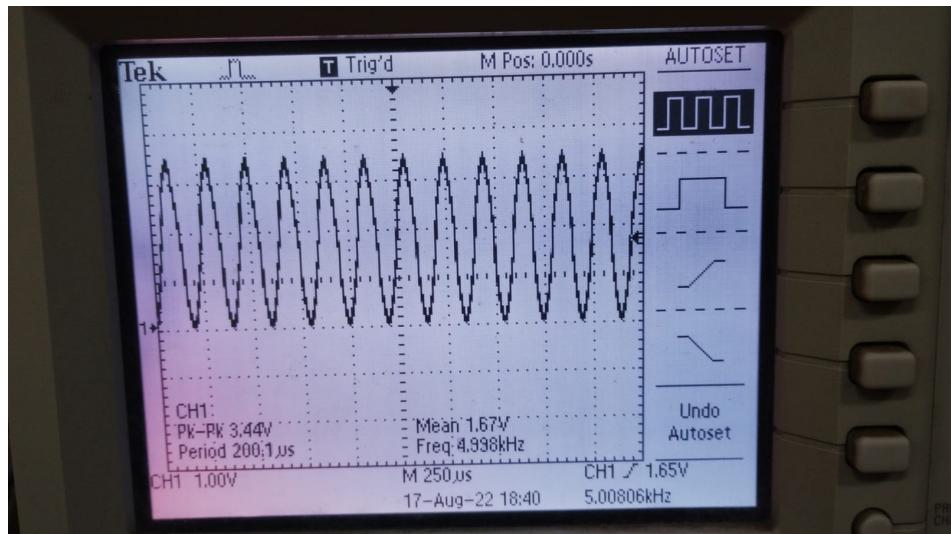


Figure 16: 5 KHz sine wave

- Generation of 10 KHz sine wave by setting off cycles to zero. Frequency is controlled using vhdl code

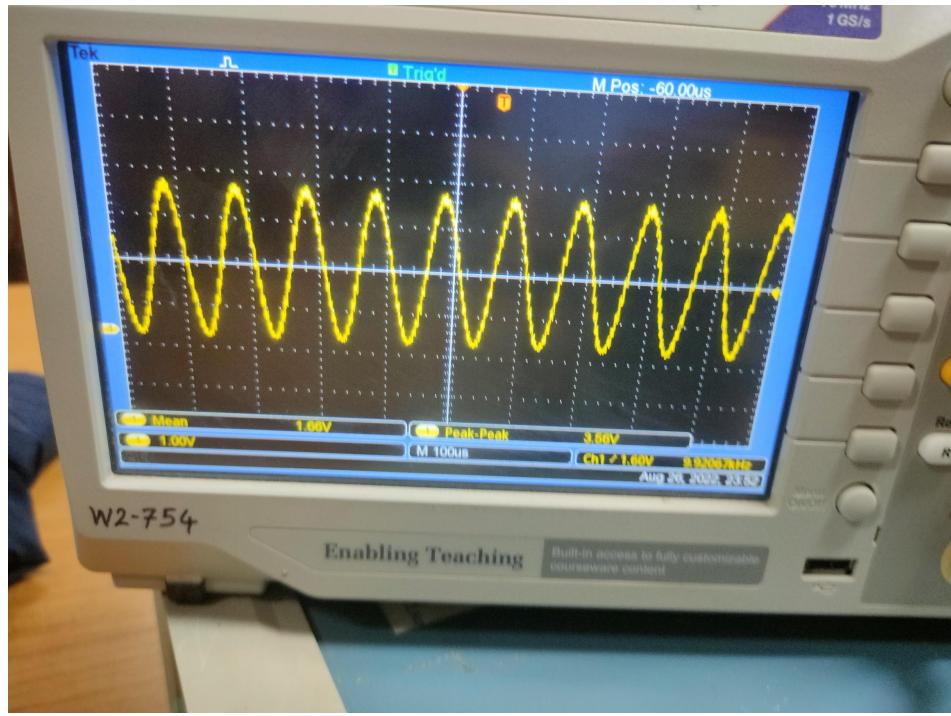


Figure 17: 10 KHz sine wave

## 2.7 Getting Xenon board to work with your PC (via USB interface)

- Plug in the USB cable to the USB connector on the Xen10 board, and the other end of the cable to a USB port on your PC. Turn on the power switch.
- You will need to install the drivers for Xen10 the first time it is connected to your PC.
- Once you connect Xen10 to your PC and power it on, Windows 7 and higher versions automatically search for available drivers. If no drivers are available, a desktop notification showing Device driver was NOT successfully installed will pop up. In such case, follow the below steps.
- Download the CMD MAX10.zip file and extract it to the desired directory. Zip file is available on resource [drive](#).
- Open the device manager by right clicking on This PC / Computer - Properties - Device Manager.
- Inside Device Manager, under other devices you will see 2 uninstalled devices named Dual RS232-HS with yellow warning (Ensure the Xen10 board is connected to the host as given in step 1). Right click on the first one and select Update driver. Now select Browse the computer for driver software, and click Next. Now, provide the path to the folder CMD MAX10 (which you extracted in step 4). Click Next.
- The installation should now begin. After this is complete a dialogue box will appear displaying successfully installed USB serial converter A, repeat step 6 for the second uninstalled device Dual RS232-HS. Similar dialogue box displaying successfully installed USB serial converter B will appear. Xen10 is now ready to be used.