Alisha Patel

I pledge my honor that I have abided by the Stevens Honor System.

Signal Name	Signal Value	0 ns 20.0	μs 40.0 μs	60.0 µs	80.0 µs	100.0	104.8 μs	120.0 µs	140.0 µs
⊡ clock_r	0	0 1 0 1 0	1 0 1 0 1	0 1 0 1 0	1 0 1 0	\int_1 0	1 0 1	0 1 0	$\int 1 \int 0 \int 1$
RegData	0000 0100	0000 010	0						
> RegWrite	1	0		1					
❷ WriteReg[01	00	01						
2- ReadReg	01	00		01					
2- ReadReg	00	00							
∰ X0[70]	0000 0000	0000 0000							
🗇 X1[70]	0000 0100	0000 0000							
∰ X2[70]	0000 0000	0000 0000							
∰ X3[70]	0000 0000	0000 0000							
RegData1	0000 0100	0000 0000		0000 0	0100				
RegData2	0000 0000	0000 0000							

The output changes based on two factors, the data input, and when the clock rises(turns on) then, it will be actually written in the register. As soon as the ReadReg1 and ReadReg2 change, it is read instantly (because that's a combinational logic), but when it comes to writing the data to a register, it uses sequential logic as a clock turning on and off again. As shown in the diagram above, when the RegDataW is changed, neither the RegData1 or RegData2 changes. Even after enabling the RegWrite to start operating and changing the ReadReg1, there is a slight delay. The delay is when the clock finally starts back again after, thus it will then finally start writing the output simultaneously in the register itself and the RegData1. Thus, the data is written when the clock restarts to overwrite the value in both registers and the data output.