ANURAG PALLAPROLU

Ph.D. Candidate in Electrical and Computer Engineering

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in linkedin.com/in/apallapr *Country of Origin:* India *Date of Birth:* 18 Feb 1995

EXPERIENCE

University of California, Santa Barbara

Graduate Teaching/Research Assistant, Electrical and Computer Engg.

- Research on wireless sensing with off-the-shelf WiFi devices at the RF Sensing and Robotic Networks Lab, advised by Prof. Yasamin Mostofi.
- Teaching Assistant for ECE 146A/B which covered digital communication fundamentals and communication systems design. I conducted weekly 3-hour lab sessions that introduced students to MATLAB and enabled them to explore some basic ideas in analog and digital modulation.
- Teaching and Lab Assistant for ECE 10A/AL which covered introductory circuits and network analysis. Member of a team of 7 TAs who concurrently managed online course management and evaluation. Out of 22 students under my purview, 16 students achieved > 90% grade, while 4 students achieved perfect scores.
- Teaching Assistant for ECE 139 which covered elementary probability theory and statistics. Out of 25 students in my section, 17 students scored > 90% in the final, while 5 students achieved perfect scores.

September 2019 – Present Santa Barbara, USA.

Qualcomm CDMA Technologies

VLSI CAD Engineer

- Developed the hierarchical extraction flow using the Synopsys StarRC extractor that was piloted successfully on 11nm and 8nm SoC contexts.
- Enabled fill-DEF back-annotation with Mentor Graphics' Calibre FDI.
- Developed a technique to reduce buffer count in post-route hold fix ECO cycles through intelligent net rerouting.
- Developed a technique for systematic die overdrive voltage margin assessment for improved yield and power metrics on a 7nm MDM solution.
- Maintained a parser suite for LEF to GDS conversion for computational geometry operations on route obstruction shapes.
- Enabled flow to ascertain block level OTC RDL content from SoC context RDL data (presented at Mentor Forum 2019).
- Supported multiple SoC tapeouts (7nm, 8nm, 11nm, 14nm) through various timing critical sign-off violation debugging iterations.

August 2017 – September 2019 Bengaluru, India.

STMicroelectronics N.V.

Research Intern

Developed and characterized the Muller C element for 40nm CMOS and 28FDSOI asynchronous logic library. Did a detailed study of self-timed circuits and their analysis techniques such as CSP and partially implemented a clock-pausing based fast-to-slow data synchronizer that leverages local asynchronous clock generation.

January 2017 – July 2017 Noida, India.

Physical Research Laboratory

Summer Research Fellow

Worked under the mentorship of Dr. Namit Mahajan, on the topic of Large N analysis of scalar field theories with elementary perturbations. Picked up a little about elementary cyclic cosmology and accelerator magnet design also.

May 2016 – July 2016 Ahmedabad, India.

LIFE PHILOSOPHY

"., I seem to have been only like a boy playing on the seashore, and diverting myself now and then in finding a smoother pebble or prettier shell than ordinary, while the great ocean of truth lay all undiscovered before me.."

ACHIEVEMENTS

- **3 x Outstanding TA Award**
  ECE Department, UC Santa Barbara.
- **Winner, New Venture Competition**
  Technology Management Program, UC Santa Barbara, 2020.
- **Graduate Record Examination**
  324/340 = 168 Q + 156 V + 5 AWA
- **Test Of English as Foreign Language**
  116/120 = 29 R + 29 L + 28 S + 30 W
- **10 x Qualstar**
  Qualcomm, Bengaluru, 2017-2019.
- **Graduate Aptitude Test in Engineering**
  Score: 574, Rank: 3295, Paper : ECE
- **Summer Research Fellowship**
  PRL, Ahmedabad. 2016.
- **Summer Research Fellowship**
  Indian Academy of Sciences, Bengaluru. 2015.
- **INSPIRE Fellowship**
  Deparment of Science and Technology, Govt. of India. 2012.

EDUCATION

Masters in Electrical and Computer Engineering

UC Santa Barbara, CA, USA

December 2020 GPA: 3.97/4

Bachelors in Electrical Engineering and Masters in Physics

Birla Institute of Technology & Science, Pilani, Rajasthan

July 2017 GPA: 8.14/10

Secondary School

Delhi Public School, Hyderabad

July 2010 GPA: 9.8/10

PROJECT WORK

Short Baseline Positioning System Design

Imaging Systems (ECE 278C) Final Project, UCSB

We construct a simulator to show the workings of the short baseline architecture widely used in underwater acoustics. With the help of FMCW transmissions and a symmetric receiver configuration one is able to perform both range and bearing angle estimation in one shot, thereby allowing complete inertial mapping of the surroundings.

Feb 2020 – March 2020 Santa Barbara, USA

Joint Precoding and Power Control Design in Massive MIMO: A Game Theoretic Approach

Non-Cooperative Game Theory (ECE 270) Final Project, UCSB

To counter interference driven SINR reduction, subscriber mobile stations are liable to use maximum TX power as a worst case strategy that leads to some of them receiving lower overall link quality. However, if the base station can provide feedback to the users through a capacity-limited noiseless channel, we can design power usage policies that helps us attain Pareto-efficiency or Socio-optimal Nash equilibrium. We use the Price of Anarchy (PoA) of this configuration as a metric to design base station policies for more equitable SINR allocation.

October 2019 – December 2019 Santa Barbara, USA

Design of an Asynchronous "Wake-Up" Flip Flop for Faster Memory Power Cycles

Standard Cells Team, STMicroelectronics

Constructed a low power "Wake-Up" flop, called so because of the characteristic absence of the data input, which made it to the 28nm test-chip of 1Q'17. What makes the design challenging is that it is neither fully asynchronous nor fully clocked. It's rising edge characteristic is more like a flip-flop, but it's falling edge nature shows an outright combinational structure. The device would aid in quick power-down and safe power-up of register arrays with its novel behavior of fast high-to-low and clocked low-to-high transitions when the reset pin is toggled, thereby improving the power efficiency of memories.

January 2017 – June 2017 Noida, India

PUBLICATIONS

Wiffract: A New Foundation for RF Imaging via Edge Tracing

ACM MobiCom 2022, DOI:10.1145/3495243.3514261

Co-authors: Dr. Belal Korany, Prof. Yasamin Mostofi, UC Santa Barbara.

October 2022 Sydney, NSW, Australia

Floquet topological phase transitions in a kicked Haldane-Chern insulator

arXiv:1709.08354, Phys. Rev. B 97, 085405

Co-authors: Dr. Tridev Mishra, Dr. Tapomoy G. Sarkar, Dr. Jayendra N. Bandyopadhyay, BITS Pilani.

September 2017 Pilani, India

Topological phase transitions in Graphene under periodic kicking

arXiv:1702.00995

Co-authors: Dr. Tridev Mishra, Dr. Tapomoy G. Sarkar, Dr. Jayendra N. Bandyopadhyay, BITS Pilani.

February 2017 Pilani, India

MASTERS THESIS

Topological Modifications Of Graphene Under Periodic Kicking

Quantum mechanical study of Graphene when subjected to "single" and "double kicking" is the main focus of the thesis. These terms refer to the special kind of perturbations that are applied to the "unkicked" Graphene Hamiltonian. The approach to study kicked Graphene taken in this work is different and is topological in nature. Important ideas are taken from Floquet Theory and an analytic expression for the mass term and the curvature tensor are derived for the singly kicked case and an approximate expression for the mass term is derived for the doubly kicked one. These expressions are verified using computer assisted proving with Mathematica and important phase transitions are noted.

PROGRAMMING

Python (NumPy, PyTorch, Keras, SKLearn) | LaTeX | C, C++ | R | Scheme | Haskell | Verilog | Perl | Scripting (Bash, TCL) | HTML5/CSS | NodeJS/PHP

TOOLS

Ansys HFSS | REMCOM Wireless InSite | Altair WinProp/FEKO | Git | MATLAB, Simulink, GNU Octave, GNUPlot | FreeFEM++ | Cadence Virtuoso Design Suite | Synopsys Design Compiler/IC Compiler II Suite | Cadence Genus/Innovus Suite | Calibre DRV | Synopsys Primetime-StarRC-XT

SKILLS

- Experience with Linux/UNIX
- Raspberry Pi/Arduino Prototyping
- Antenna Array/SAR Assembly
- Manufacturing Power Tools

LANGUAGES

English (Full Proficiency)
Hindi (Full Proficiency)
Telugu (Mother Tongue)