APARAJITA MEHROTRA Bangalore, India
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SUMMARY

- 11 years of experience in Physical Design Synthesis and front-end Implementation
- Hands-on experience in implementing 5G Low-Power Modem designed for smartphones and wearables
- Team lead responsible for driving Modem project - hard macros and top-level
- Experience in deep-submicron foundry technology process nodes (TSMC N3, SF 5LPE), currently working on TSMC 2nm
- Expert in Synopsys Implementation tool-suite

SKILLS

- Strong understanding of IC design, device physics, VLSI circuit design, physical design flow, chip level integration, block timing closure, design trade-offs between power, performance, and reliability
- **Design:** RTL-to-GDSII, Synthesis, Static Timing Analysis, Timing Constraints, FrontEnd Design Checks, Formal Verification (LEC, Formality), Conformal Low Power, Custom Datapath, Place and Route, Hierarchical Design, Constraint Management, Power Performance Area (PPA) improvement, QoR improvement, Low-Power Flow Development, FDSoI, SoC interconnect (NoC)
- **EDA Software:** Fusion Compiler, Design Compiler, IC Compiler II, Formality, RTLA, Conformal LowPower, PrimeTime
- Programming/Scripting: Tcl, Python, Verilog, Perl, shell scripting

PUBLICATIONS and AWARDS

- "Split and Conquer: Left-Shifting Placement to Synthesis with Split Session Flow" in QCPO 2022
- SNPS CEFO Achievement Award for driving a key RTLA initiative to successful deployment with positive business outcome in Q1 2021
- SNPS Above and Beyond leadership award for successful RTL Architect engagement and DC Runtime Inoculation campaign
- Multiple spot awards for reducing the pipelining stages on FPU block at Broadcom
- Won the 1st place in paper presentations at various IEEE student conferences organized by IIT Delhi, BITS Pilani, DTU
- Paper accepted for the 6th International Conference on Microwaves ICMARS – 2010

WORK EXPERIENCE

Staff Engineer, Qualcomm, Bangalore, India Jun'21-Present

- Successfully led three projects to deliver netlists with optimized PPA metrics. 8-9% improvement in stdcell area achieved across all the HMs. Improved the design flow to pull in the project timelines by 2 months.
- Project lead driving collaboration with RTL, DV, DFT, MBIST, CAD, PD teams, SOC integration teams, program management teams to deliver the collaterals within tight timelines
- Responsible for setting schedules for each stage of the project and quality drops for PD, implement feedback in the design constraints and timing/congestion to ensure best-in-class PPA
- Integrate and present weekly status in progress reports, highlight issues and risks to the schedule to leadership and program management team
- Mentored and upskilled the team comprising of 25 engineers by delivering focused sessions on Fusion Compiler debug techniques
- Developed and deployed a split-flow creation to reduce cycle time by devising a methodology to integrate incremental floorplans into synthesis flow
- Presented this work through a paper titled "Split and Conquer: Left-Shifting Placement to Synthesis with Split Session Flow" in Qualcomm internal conference QCPO
- Undertook initiatives to improve the flow debug, design automation, correlation with backend flows and out of the box Power Performance Area (PPA)

Sr. Application Engineer, Synopsys, Bangalore, India Jan'17-Jun'21

- Collaborated with customers on cutting-edge technologies (16nm-5nm) and market-critical projects
- Key focus on delivering innovative generic automated flow/methodologies that deliver best performance and runtime
- Instrumental in tool usage proliferation
- Delivered multiple best-practice sessions to designers to enhance end-user tool expertise
- **Key Contributions:**
  - Led a successful RTL Architect engagement with a search engine company, collaborated with various R&D and sales teams across the globe to make this the first win in India
  - Successfully defended DC at a Korean mobile OEM on two critical projects with 86% better QoR
  - Successfully led the DC Inoculation campaign at a Korean mobile OEM resulting in 40% runtime and 99% QoR improvement
  - Created a novel automated testcase packaging methodology and scriptware for a complex flow at a Korean mobile OEM to increase efficiency, 3 hours of TAT reduced to 10mins
  - Won critical benchmarks at Korean mobile OEM on two key designs which played a pivotal role in contract renewal
  - Developed a full implementation flow for 8nm design from place to route to deliver best performance and area
  - Developed ICC2 flip chip methodology on a tight schedule

Sr. IC Design Engineer, Broadcom, Santa Clara, CA Jul'13 – Dec'16

- Synthesis to tapeout-closure implementation for Floating-point unit in 16FF tech node for Vulcan CPU

- Project completed and taped out on time, successful bring up on tested, no design issues in FPU
- Challenges: performance critical and congested CPU block
- Register retimed the design during synthesis and integrated it into the design flow
- **Key Contributions:**
  - Floorplan: Evaluated macro placement for the design and managed the interblock paths to meet timing
  - Synthesis: register retiming, optimal placement, and custom solution for timing critical paths
  - Constraint management: used top level timing report to derive block level timing, closed the critical paths to the FPU macro
  - Clocking: Evaluated different MCTS configurations for reducing wirelength and power and get optimal solution for the multipoint grid. Implemented Multipoint CTS clocking solution to achieve minimal insertion delay while utilizing useful skew to push for high speed
  - Place and route: Designed custom datapath in Floating point unit running at 3+ GHz
  - Physical verification: solved PV violations using Calibre DRC and LVS in time sensitive environment for multiple hard macros
  - Design closure: including fixing EM/IR, noise, LVS, EM, IR, transition violations

Graduate Technical Intern in Real Intent, Sunnyvale, CA Jan'13 - July'13

- Automated a solution to create thousands of unit tests for testing their formal verification tool. Created the metadata used by the R&D
- Meridian CDC: Potential problems that lead to structural errors in clock domain crossing designs were identified and implemented possible solutions to resolve these errors

EDUCATION

MS Electrical Engg., Viterbi School of Engineering, University of Southern California, Los Angeles Aug'11 - May'13

- Research student with the BioRC (Biomimetic Real-Time Cortex) project led by Prof. Alice Parker, USC
- Design of a multicore processor with a Network-on-Chip on 45nm Technology
- Design of a 1K-bit SRAM and implementation of a Noise Reduction procedure used in Digital Image Processing

B.Tech (Electronics and Communication), Jamia Millia Islamia, New Delhi, India Jul'07 – May'11

Research work: Centre for Applied Research in Electronics (CARE), IIT Delhi Jan'10 - Jan'11

Worked with Prof. Shiban K. Koul to develop a conceptual design along with fabrication and testing to successfully complete the following projects. Published two technical papers on them:

- Broad Stopband Lowpass Filter utilizing Defected Ground Structure on Microstrip and Suspended Stripline
- Design and Analysis of Parallel Coupled Bandpass Filter, Lowpass Filter and Branch Line Directional Coupler