**EEE 529 Fall 2017**

***Prof. Shimeng Yu***

**Lab #1 SRAM Stability Analysis**

***Due Sep 15, 11:59pm submission by Blackboard (Friday)***

Please run HSPICE simulations using the 32 nm high-performance PTM model to finish following questions. More information about PTM is available on the website as below.

[http://ptm.asu.edu](http://ptm.asu.edu/)

**Please use following conditions in your simulations.**

Transistor minimum width=35 nm

Transistor minimum gate length=30 nm

Nominal VDD=0.9 V

Rise time=30 ps

Fall time=30 ps

WL pulse width=500 ps

BL capacitance=100 fF

The default ratio of the SRAM cell is 2:1:1 (PD:PG:PU), which means the size of the PD transistor is two times larger than the minimum width while the PG and the PU transistors are the same as the minimum width. Use the default ratio (unless specified to other values in Part I Q2(2)) in all the following problems in this lab.

## Part I: Statics Stability Analysis (50pts)

1. Please plot the butterfly curve (read mode) of a SRAM cell as in Figure 1. (5pts).



Figure 1. SRAM Schematic

2. Read the following paper and answer the question.

Evert Seevinck et al., “Static-Noise Margin Analysis of MOS SRAM Cells”, *IEEE JSSC, SC-22*, No. 5, 1987.

1. Assume the ratio of the SRAM cell is 2:1:1 (PD:PG:PU), please use the method proposed in this paper to measure static noise margin for the READ operation (This means the pass gate is included for Cicuit F1 and F2 in Fig. 6). The read SNM should be transformed similarly as in Fig 5 in the paper (5 pts).
2. Assume the ratio of the SRAM cell is x:1:1 (PD:PG:PU), please sweep x from 2 to 3, 4, and 5, and redo problem 2(1). Plot read SNM vs. x and explain you results (10 pts).
3. If the SRAM requires at least 80 mV SNM to make sure the circuit is reliable, what is the lowest VDD if scaling VDD from 0.9 V to 0.3 V? Please plot read SNM vs. VDD and explain you result (10 pts).

3. Read the following paper and answer the question.

Jiajing Wang et al., “Analyzing Static and Dynamic Write Margin for Nanometer SRAMs”, *ACM/IEEE International Symposium on* *Low Power Electronics and Design (ISLPED),* pp. 129-134. IEEE, 2008.

1. Please show similar result as in Figure 2(b) from the paper to find out the static write margin (by sweeping BL voltage) of a SRAM cell from previous question (10 pts). (Note: there is a typo in Figure 2’s caption of this paper, which is BLB instead of BL)
2. Please plot a diagram of the static write margin (by sweeping BL voltage) vs. VDD (10 pts).

## Part II: Dynamic Stability Analysis (50pts)

1. Read the following paper and answer the question.

Wei Dong et al., “SRAM dynamic stability: theory, variability and analysis.” *IEEE/ACM ICCAD*, pp. 378-385, 2008.

1. Plot the dynamic read operation timing to show the waveform of the storage nodes (Q and QB) and BL/BLN voltages. (10 pts).

**Critical charge is the minimal amount of charge injected by the noise leads to a READ failure. If noise (current source) is added to storage node Q as in** Figure 2**.**

1. Assume the noise has a magnitude of 20 uA. Please plot the simulation results (waveform of (Q and QB) by sweeping the noise duration from 30 ps to 500 ps with a step of 10 ps. Is the READ operation successful or failed? If the READ failure is incurred, please find the critical charge (20 pts).
2. Repeat step (2) with noise magnitude of 35 uA. (20 pts)

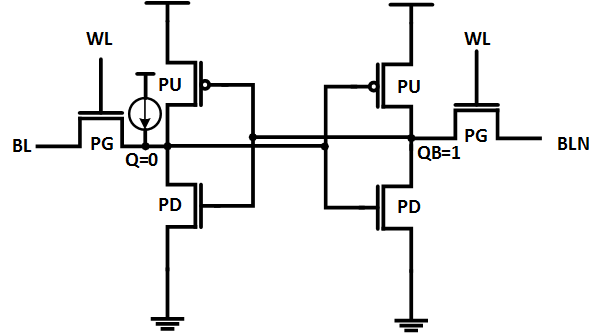


Figure 2. SRAM with current source noise and initial state.

## Report:

***Everything must be on white background with colored images, and clearly readable for credit.***

Please submit a concise report on your work and results using the link in Blackboard system.

Include your HSPICE files (including netlist and testbench) in the Appendix section of your report.