2-bit adder Datasheet

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Clock frequency = 2GHz
Clock period = 500ps

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Area = 176.92992 um2
Length = 13.652 um
Width = 12.96 um

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Core Utilization = 95%

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A1	A0	B1	B0	Sum1	Sum0	Cout
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	1	0	1	1
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Truth Table for 2 bit adder

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Top 3 Best case slack timing: 132.4ps, 93.7ps, 93.7ps
Top 3 Worst case slack timing: 24.6ps, 33.4ps, 34.6ps

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Power

Power Units = 1mW

Time Units = 1e-12 secs

Total Power

Total Internal Power:	0.02670523	68.6455%
Total Switching Power:	0.01218265	31.3153%
Total Leakage Power:	0.00001525	0.0392%
Total Power:	0.03890312	

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.009628	0.0007958	3.644e-06	0.01043	26.8
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.01708	0.01139	1.16e-05	0.02848	73.2
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.02671	0.01218	1.525e-05	0.0389	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
vdd	0.7	0.02671	0.01218	1.525e-05	0.0389	100

Power Distribution Summary:

Highest Average Power:	g191 (INVx13_ASAP7_75t_R):	0.005504
Highest Leakage Power:	FE_OFC4_n_14 (BUFx12f_ASAP7_75t_R):	7.991e-07

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Total capacitance: 9.7032 e-14 F

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Schematic View: