APR Report

Complete Clock Synthesis Tree report

```
#####################################################################
#  Generated by:      Cadence Encounter 14.27-s035_1
#  OS:                Linux x86_64(Host ID eecad44.eas.asu.edu)
#  Generated on:      Sat Apr 22 19:16:01 2017
#  Design:            conv_pool
#  Command:           reportClockTree -report final.ctsrpt
#####################################################################
#####################################################################
# Complete Clock Tree Timing Report
#
# CLOCK: clk
#
# Mode: preRoute
#
# Delay Corner information
# Analysis View      : default_setup_view
# Delay Corner Name   : delayCorner_slow
# RC Corner Name     : RC_corner_25
# Analysis View      : default_hold_view
# Delay Corner Name   : delayCorner_fast
# RC Corner Name     : RC_corner_25
#####################################################################


Nr. of Subtrees             : 1
Nr. of Sinks                : 864
Nr. of Buffer               : 0
Nr. of Level (including gates) : 0
Root Rise Input Tran        : 0.1(ps)
Root Fall Input Tran        : 0.1(ps)
No Driving Cell Specified!
Max trig. edge delay at sink(R): f2_af01_reg[7]/CLK 807.3(ps)
Min trig. edge delay at sink(R): f1_img16_reg[7]/CLK 0.3(ps)

                         (Actual)          (Required)
Rise Phase Delay            : 0.3~807.3(ps)       0~10(ps)
Fall Phase Delay            : 0.3~807.3(ps)       0~10(ps)
Trig. Edge Skew             : 807(ps)             14(ps)
Rise Skew                   : 807(ps)
Fall Skew                   : 807(ps)
Max. Rise Buffer Tran       : 0(ps)               200(ps)
Max. Fall Buffer Tran       : 0(ps)               200(ps)
Max. Rise Sink Tran         : 1290.5(ps)          200(ps)
Max. Fall Sink Tran         : 1290.5(ps)          200(ps)
Min. Rise Buffer Tran       : 0(ps)               0(ps)
Min. Fall Buffer Tran       : 0(ps)               0(ps)
Min. Rise Sink Tran         : 6.3(ps)             0(ps)
Min. Fall Sink Tran         : 6.3(ps)             0(ps)
```

view default_setup_view : skew = 807ps (required = 14ps)
view default_hold_view : skew = 807ps (required = 14ps)

verifyGeometry Report

```
############################################################
#  Generated by:      Cadence Encounter 14.27-s035_1
#  OS:                Linux x86_64(Host ID eecad44.eas.asu.edu)
#  Generated on:      Sat Apr 22 19:21:06 2017
#  Design:            conv_pool
#  Command:           verifyGeometry
############################################################

Begin Summary ...
  Cells      : 0
  SameNet    : 0
  Wiring     : 0
  Antenna    : 0
  Short      : 0
  Overlap    : 0
End Summary

No DRC violations were found
```

verifyConnectivity Report

```
############################################################
#  Generated by:      Cadence Encounter 14.27-s035_1
#  OS:                Linux x86_64(Host ID eecad44.eas.asu.edu)
#  Generated on:      Sat Apr 22 19:21:01 2017
#  Design:            conv_pool
#  Command:           verifyConnectivity
############################################################
Verify Connectivity Report is created on Sat Apr 22 19:21:01 2017

Begin Summary
   Found no problems or warnings.
End Summary
```

APR_Report

Athi Narayanan Parameswaran
ASU ID: 1211377931

Gate Count and Area

encounter 7> reportGateCount
Gate area 0.6998 um^2
[0] conv_pool Gates=56492 Cells=21832 Area=39535.6 um^2

Post-Route summary

```
#####################################################################
#  Generated by:      Cadence Encounter 14.27-s035_1
#  OS:                Linux x86_64(Host ID eecad44.eas.asu.edu)
#  Generated on:      Sat Apr 22 17:02:53 2017
#  Design:            conv_pool
#  Command:           optDesign -postRoute -hold -incr
#####################################################################

------------------------------------------------------------
    optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|         WNS (ns):|  0.001  |  0.001  |  0.165  |
|         TNS (ns):|  0.000  |  0.000  |  0.000  |
|   Violating Paths:|    0    |    0    |    0    |
|        All Paths:|   872   |   662   |   210   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |   5851 (6114)    |   -0.217   |   5851 (6122)    |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 77.308%
Total number of glitch violations: 0
------------------------------------------------------------
```

APR_Report **Athi Narayanan Parameswaran**
ASU ID: 1211377931

Post-Route hold summary

```
#####################################################################
#  Generated by:      Cadence Encounter 14.27-s035_1
#  OS:                Linux x86_64(Host ID eecad44.eas.asu.edu)
#  Generated on:      Sat Apr 22 17:02:53 2017
#  Design:            conv_pool
#  Command:           optDesign -postRoute -hold -incr
#####################################################################

------------------------------------------------------------
    optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|         WNS (ns):|  0.027  |  0.027  |  0.051  |
|         TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|         All Paths:|   872   |   662   |   210   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |   5851 (6114)    |   -0.217   |   5851 (6122)    |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 77.308%
Total number of glitch violations: 0
------------------------------------------------------------
```

Post Layout power after Prime-Time

Information: Running averaged power analysis... (PWR-601)
Information: Running power calculation with 4 threads. (PWR-602)
****
Report : Averaged Power
Design : conv_pool
Version: K-2015.06-SP1
Date : Mon Apr 24 12:58:36 2017
****

Attributes
---
i - Including register clock pin internal power
u - User defined power group

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
clock_network	9.010e-04	0.0000	0.0000	9.010e-04 (13.07%)	i
register	4.575e-04	4.012e-04	4.455e-07	8.592e-04 (12.46%)	
combinational	2.865e-03	2.268e-03	2.463e-06	5.135e-03 (74.47%)	
sequential	0.0000	0.0000	0.0000	0.0000 (0.00%)	
memory	0.0000	0.0000	0.0000	0.0000 (0.00%)	
io_pad	0.0000	0.0000	0.0000	0.0000 (0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000 (0.00%)	

Net Switching Power = 2.669e-03 (38.70%)
Cell Internal Power = 4.224e-03 (61.25%)
Cell Leakage Power = 2.908e-06 (0.04%)

Total Power = 6.895e-03 (100.00%)

1

APR_Report **Athi Narayanan Parameswaran**
ASU ID: 1211377931

Top 3 worst-case timing paths

Setup:

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -nets
        -slack_lesser_than 60.000000
        -max_paths 50
        -sort_by slack
Design : conv_pool
Version: K-2015.06-SP1
Date   : Mon Apr 24 12:58:35 2017
****************************************


 Startpoint: f1_img7_reg[0]
        (rising edge-triggered flip-flop clocked by clk)
 Endpoint: f2_af06_reg[11]
        (rising edge-triggered flip-flop clocked by clk)
 Path Group: clk
 Path Type: max

 Point                          Fanout      Incr      Path
 ---------------------------------------------------------------------------
 clock clk (rise edge)                        0.000000   0.000000
 clock network delay (ideal)                  0.000000   0.000000
 f1_img7_reg[0]/CLK (DFFHQNx4_ASAP7_75t_R)    0.000000   0.000000 r
 f1_img7_reg[0]/QN (DFFHQNx4_ASAP7_75t_R)     61.018219 &
                                              61.018219 f
 n_1544 (net)                    9
 g21605/Y (INVx13_ASAP7_75t_R)                60.860199 &
                                              121.878418 r
 img7[0] (net)                  34
 a0_mul_468_19/g12728/Y (NAND2xp67_ASAP7_75t_R)  72.340088 &
                                              194.218506 f
 a0_mul_468_19/n_128 (net)                2
 a0_mul_468_19/g12666/Y (NAND2x1_ASAP7_75t_R)    29.628067 &
                                              223.846573 r
 a0_mul_468_19/n_193 (net)                2
 a0_mul_468_19/g12548/Y (NOR2x1_ASAP7_75t_R)     12.823730 &
                                              236.670303 f
 a0_mul_468_19/n_260 (net)                2
 a0_mul_468_19/g12540/Y (INVx1_ASAP7_75t_R)      10.457733 &
                                              247.128036 r
 a0_mul_468_19/n_261 (net)                2
 a0_mul_468_19/g12501/Y (OA21x2_ASAP7_75t_R)     14.168564 &
                                              261.296600 r
 a0_mul_468_19/n_297 (net)                2
```

```
a0_mul_468_19/g12465/Y (OA21x2_ASAP7_75t_R)       14.727661 &
                                    276.024261 r
a0_mul_468_19/n_322 (net)                 3
a0_mul_468_19/g12457/Y (INVx1_ASAP7_75t_R)        6.122223 & 282.146484 f
a0_mul_468_19/n_323 (net)                 1
a0_mul_468_19/g12413/Y (NAND3x1_ASAP7_75t_R)      7.113220 & 289.259705 r
a0_mul_468_19/n_356 (net)                 1
a0_mul_468_19/g12388_dup/Y (OA21x2_ASAP7_75t_R)   21.806396 &
                                    311.066101 r
a0_mul_468_19/FE_RN_10 (net)              2
a0_mul_468_19/FE_RC_2138_0/Y (A2O1A1Ixp33_ASAP7_75t_R_v1)
                                  16.909698 &
                                    327.975800 f
a0_mul_468_19/FE_RN_454_0 (net)           1
a0_mul_468_19/FE_RC_798_0/Y (INVx2_ASAP7_75t_R)   20.561859 &
                                    348.537659 r
a0_mul_468_19/n_390 (net)                 4
a0_mul_468_19/g12323/Y (NOR2x1_ASAP7_75t_R)       9.436859 & 357.974518 f
a0_mul_468_19/n_414 (net)                 1
a0_mul_468_19/g12318/Y (NOR2x1_ASAP7_75t_R)       7.262909 & 365.237427 r
a0_mul_468_19/n_93 (net)                  1
a0_mul_468_19/FE_OCPC842_n_93/Y (BUFx6f_ASAP7_75t_R)
                                  11.703156 &
                                    376.940582 r
a0_mul_468_19/FE_OCPN842_n_93 (net)       5
a0_mul_468_19/g12310/Y (OA21x2_ASAP7_75t_R)       11.260498 &
                                    388.201080 r
a0_mul_468_19/n_424 (net)                 1
a0_mul_468_19/FE_RC_1486_0/Y (XNOR2xp5_ASAP7_75t_R_v2)
                                  14.330536 &
                                    402.531616 r
a0_mul_468_19/FE_RN_812_0 (net)           1
a0_mul_468_19/FE_RC_1487_0/Y (INVx1_ASAP7_75t_R)  8.562103 & 411.093719 f
a0_mul_468_19/Z[11] (net)                 1
f2_af06_reg[11]/D (DFFHQNx4_ASAP7_75t_R)          0.006439 & 411.100159 f
data arrival time                                   411.100159

clock clk (rise edge)                       420.000000 420.000000
clock network delay (ideal)                   0.000000   420.000000
clock reconvergence pessimism                 0.000000   420.000000
f2_af06_reg[11]/CLK (DFFHQNx4_ASAP7_75t_R)                420.000000 r
library setup time                          -7.631978  412.368022
data required time                                  412.368022
-----------------------------------------------------------------------------
data required time                                  412.368022
data arrival time                                  -411.100159
-----------------------------------------------------------------------------
slack (MET)                                         1.267863


Startpoint: f1_img7_reg[0]
```

```
        (rising edge-triggered flip-flop clocked by clk)
Endpoint: f2_af06_reg[10]
        (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                 Fanout      Incr      Path
-------------------------------------------------------------------------------
clock clk (rise edge)                              0.000000   0.000000
clock network delay (ideal)                        0.000000   0.000000
f1_img7_reg[0]/CLK (DFFHQNx4_ASAP7_75t_R)          0.000000   0.000000 r
f1_img7_reg[0]/QN (DFFHQNx4_ASAP7_75t_R)           61.018219 &
                                                   61.018219 f
n_1544 (net)                           9
g21605/Y (INVx13_ASAP7_75t_R)                      60.860199 &
                                                   121.878418 r
img7[0] (net)                         34
a0_mul_468_19/g12728/Y (NAND2xp67_ASAP7_75t_R)     72.340088 &
                                                   194.218506 f
a0_mul_468_19/n_128 (net)                  2
a0_mul_468_19/g12666/Y (NAND2x1_ASAP7_75t_R)       29.628067 &
                                                   223.846573 r
a0_mul_468_19/n_193 (net)                  2
a0_mul_468_19/g12548/Y (NOR2x1_ASAP7_75t_R)        12.823730 &
                                                   236.670303 f
a0_mul_468_19/n_260 (net)                  2
a0_mul_468_19/g12540/Y (INVx1_ASAP7_75t_R)         10.457733 &
                                                   247.128036 r
a0_mul_468_19/n_261 (net)                  2
a0_mul_468_19/g12501/Y (OA21x2_ASAP7_75t_R)        14.168564 &
                                                   261.296600 r
a0_mul_468_19/n_297 (net)                  2
a0_mul_468_19/g12465/Y (OA21x2_ASAP7_75t_R)        14.727661 &
                                                   276.024261 r
a0_mul_468_19/n_322 (net)                  3
a0_mul_468_19/g12457/Y (INVx1_ASAP7_75t_R)         6.122223 & 282.146484 f
a0_mul_468_19/n_323 (net)                  1
a0_mul_468_19/g12413/Y (NAND3x1_ASAP7_75t_R)       7.113220 & 289.259705 r
a0_mul_468_19/n_356 (net)                  1
a0_mul_468_19/g12388_dup/Y (OA21x2_ASAP7_75t_R)    21.806396 &
                                                   311.066101 r
a0_mul_468_19/FE_RN_10 (net)               2
a0_mul_468_19/FE_RC_2138_0/Y (A2O1A1Ixp33_ASAP7_75t_R_v1)
                                      16.909698 &
                                                   327.975800 f
a0_mul_468_19/FE_RN_454_0 (net)            1
a0_mul_468_19/FE_RC_798_0/Y (INVx2_ASAP7_75t_R)    20.561859 &
                                                   348.537659 r
a0_mul_468_19/n_390 (net)                  4
a0_mul_468_19/g12323/Y (NOR2x1_ASAP7_75t_R)        9.436859 & 357.974518 f
a0_mul_468_19/n_414 (net)                  1
```

```
a0_mul_468_19/g12318/Y (NOR2x1_ASAP7_75t_R)       7.262909 & 365.237427 r
a0_mul_468_19/n_93 (net)                  1
a0_mul_468_19/FE_OCPC842_n_93/Y (BUFx6f_ASAP7_75t_R)
                                  11.703156 &
                                        376.940582 r
a0_mul_468_19/FE_OCPN842_n_93 (net)         5
a0_mul_468_19/FE_OCPC4560_n_93/Y (HB1xp67_ASAP7_75t_R)
                                  10.196808 &
                                        387.137390 r
a0_mul_468_19/FE_OCPN4560_n_93 (net)        1
a0_mul_468_19/g12312/Y (XNOR2xp5_ASAP7_75t_R_v2)    9.913483 & 397.050873 f
a0_mul_468_19/Z[10] (net)                 1
f2_af06_reg[10]/D (DFFHQNx4_ASAP7_75t_R)          0.009430 & 397.060303 f
data arrival time                                   397.060303

clock clk (rise edge)                       420.000000 420.000000
clock network delay (ideal)                   0.000000   420.000000
clock reconvergence pessimism                 0.000000   420.000000
f2_af06_reg[10]/CLK (DFFHQNx4_ASAP7_75t_R)                420.000000 r
library setup time                          -18.952885 401.047115
data required time                                  401.047115
--------------------------------------------------------------------------------
data required time                                  401.047115
data arrival time                                  -397.060303
--------------------------------------------------------------------------------
slack (MET)                                         3.986813


Startpoint: f1_img7_reg[0]
        (rising edge-triggered flip-flop clocked by clk)
Endpoint: f2_af06_reg[8]
        (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                             Fanout      Incr      Path
--------------------------------------------------------------------------------
clock clk (rise edge)                       0.000000   0.000000
clock network delay (ideal)                   0.000000   0.000000
f1_img7_reg[0]/CLK (DFFHQNx4_ASAP7_75t_R)         0.000000   0.000000 r
f1_img7_reg[0]/QN (DFFHQNx4_ASAP7_75t_R)          61.018219 &
                                        61.018219 f
n_1544 (net)                              9
g21605/Y (INVx13_ASAP7_75t_R)                   60.860199 &
                                        121.878418 r
img7[0] (net)                            34
a0_mul_468_19/g12728/Y (NAND2xp67_ASAP7_75t_R)     72.340073 &
                                        194.218491 f
a0_mul_468_19/n_128 (net)                 2
a0_mul_468_19/g12666/Y (NAND2x1_ASAP7_75t_R)       29.628067 &
                                        223.846558 r
```

```
a0_mul_468_19/n_193 (net)                2
a0_mul_468_19/g12548/Y (NOR2x1_ASAP7_75t_R)       12.823730 &
                                          236.670288 f
a0_mul_468_19/n_260 (net)                2
a0_mul_468_19/g12540/Y (INVx1_ASAP7_75t_R)        10.457733 &
                                          247.128021 r
a0_mul_468_19/n_261 (net)                2
a0_mul_468_19/g12501/Y (OA21x2_ASAP7_75t_R)       14.168549 &
                                          261.296570 r
a0_mul_468_19/n_297 (net)                2
a0_mul_468_19/g12465/Y (OA21x2_ASAP7_75t_R)       14.727661 &
                                          276.024231 r
a0_mul_468_19/n_322 (net)                3
a0_mul_468_19/g12457/Y (INVx1_ASAP7_75t_R)        6.122253 & 282.146484 f
a0_mul_468_19/n_323 (net)                1
a0_mul_468_19/g12413/Y (NAND3x1_ASAP7_75t_R)      7.113220 & 289.259705 r
a0_mul_468_19/n_356 (net)                1
a0_mul_468_19/g12388_dup/Y (OA21x2_ASAP7_75t_R)   21.806366 &
                                          311.066071 r
a0_mul_468_19/FE_RN_10 (net)             2
a0_mul_468_19/FE_RC_2138_0/Y (A2O1A1Ixp33_ASAP7_75t_R_v1)
                                  16.909698 &
                                          327.975769 f
a0_mul_468_19/FE_RN_454_0 (net)          1
a0_mul_468_19/FE_RC_798_0/Y (INVx2_ASAP7_75t_R)   20.561890 &
                                          348.537659 r
a0_mul_468_19/n_390 (net)                4
a0_mul_468_19/g12326/Y (OA21x2_ASAP7_75t_R)       16.940186 &
                                          365.477844 r
a0_mul_468_19/n_411 (net)                2
a0_mul_468_19/FE_OCPC4985_n_411/Y (BUFx6f_ASAP7_75t_R)
                                  9.015930 & 374.493774 r
a0_mul_468_19/FE_OCPN4985_n_411 (net)    1
a0_mul_468_19/g12314/Y (XOR2x1_ASAP7_75t_R)       15.722717 &
                                          390.216492 r
a0_mul_468_19/Z[8] (net)                 1
FE_OCPC957_a06_8_/Y (BUFx12f_ASAP7_75t_R)         14.680206 &
                                          404.896698 r
FE_OCPN957_a06_8_ (net)                  1
f2_af06_reg[8]/D (DFFHQNx4_ASAP7_75t_R)           0.211609 & 405.108307 r
data arrival time                                 405.108307

clock clk (rise edge)                    420.000000 420.000000
clock network delay (ideal)                0.000000   420.000000
clock reconvergence pessimism              0.000000   420.000000
f2_af06_reg[8]/CLK (DFFHQNx4_ASAP7_75t_R)          420.000000 r
library setup time                       -5.404984  414.595016
data required time                                 414.595016
-------------------------------------------------------------------------------
data required time                                 414.595016
data arrival time                                 -405.108307
```

```
--------------------------------------------------------------------------------
slack (MET)                                9.486710
```

Hold:

```
****************************************
Report : timing
        -path_type full
        -delay_type min
        -nets
        -slack_lesser_than 60.000000
        -max_paths 50
        -sort_by slack
Design : conv_pool
Version: K-2015.06-SP1
Date   : Mon Apr 24 12:58:35 2017
****************************************


 Startpoint: f1_img6_reg[0]
        (rising edge-triggered flip-flop clocked by clk)
 Endpoint: f2_af31_reg[3]
        (rising edge-triggered flip-flop clocked by clk)
 Path Group: clk
 Path Type: min

 Point                          Fanout      Incr      Path
 -------------------------------------------------------------------------------
 clock clk (rise edge)                      0.000000   0.000000
 clock network delay (ideal)                0.000000   0.000000
 f1_img6_reg[0]/CLK (DFFHQNx4_ASAP7_75t_R)  0.000000   0.000000 r
 f1_img6_reg[0]/QN (DFFHQNx4_ASAP7_75t_R)   30.360809 &
                                            30.360809 f
 n_1552 (net)                           1
 FE_OCPC424_n_1552/Y (BUFx12f_ASAP7_75t_R)  24.588715 &
                                            54.949524 f
 FE_OCPN424_n_1552 (net)                17
 a0_mul_493_19/g12679/Y (AOI22xp33_ASAP7_75t_R)  20.858231 &
                                            75.807755 r
 a0_mul_493_19/n_166 (net)                  1
 a0_mul_493_19/g12578/Y (OA22x2_ASAP7_75t_R)  21.231117 &
                                            97.038872 r
 a0_mul_493_19/n_237 (net)                  2
 a0_mul_493_19/g12497/Y (NOR2x1_ASAP7_75t_R)  9.342171 & 106.381042 f
 a0_mul_493_19/n_299 (net)                  2
 a0_mul_493_19/g12481/Y (NOR2x1_ASAP7_75t_R)  7.683624 & 114.064667 r
 a0_mul_493_19/n_307 (net)                  1
 a0_mul_493_19/g12941/Y (XNOR2xp5_ASAP7_75t_R_v2)  55.195709 &
                                            169.260376 r
 a0_mul_493_19/Z[3] (net)                   1
```

```
f2_af31_reg[3]/D (DFFHQNx2_ASAP7_75t_R)          0.465958 & 169.726334 r
data arrival time                                169.726334

clock clk (rise edge)                    0.000000   0.000000
clock network delay (ideal)              0.000000   0.000000
clock reconvergence pessimism            0.000000   0.000000
f2_af31_reg[3]/CLK (DFFHQNx2_ASAP7_75t_R)                0.000000 r
library hold time                      166.473663 166.473663
data required time                               166.473663
-------------------------------------------------------------------------------
data required time                               166.473663
data arrival time                               -169.726334
-------------------------------------------------------------------------------
slack (MET)                                      3.252670


Startpoint: f1_img6_reg[0]
        (rising edge-triggered flip-flop clocked by clk)
Endpoint: f2_af31_reg[4]
        (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Point                          Fanout      Incr      Path
-------------------------------------------------------------------------------
clock clk (rise edge)                    0.000000   0.000000
clock network delay (ideal)              0.000000   0.000000
f1_img6_reg[0]/CLK (DFFHQNx4_ASAP7_75t_R)        0.000000   0.000000 r
f1_img6_reg[0]/QN (DFFHQNx4_ASAP7_75t_R)         30.360809 &
                                         30.360809 f
n_1552 (net)                          1
FE_OCPC424_n_1552/Y (BUFx12f_ASAP7_75t_R)        24.588715 &
                                         54.949524 f
FE_OCPN424_n_1552 (net)                 17
a0_mul_493_19/g12679/Y (AOI22xp33_ASAP7_75t_R)    20.858231 &
                                         75.807755 r
a0_mul_493_19/n_166 (net)               1
a0_mul_493_19/g12578/Y (OA22x2_ASAP7_75t_R)       21.231117 &
                                         97.038872 r
a0_mul_493_19/n_237 (net)               2
a0_mul_493_19/g12497/Y (NOR2x1_ASAP7_75t_R)       9.342163 & 106.381035 f
a0_mul_493_19/n_299 (net)               2
a0_mul_493_19/g12493/Y (INVx1_ASAP7_75t_R)        6.232048 & 112.613083 r
a0_mul_493_19/n_300 (net)               1
a0_mul_493_19/g12465/Y (OA21x2_ASAP7_75t_R)       15.272003 &
                                         127.885086 r
a0_mul_493_19/n_322 (net)               3
a0_mul_493_19/g12414/Y (XNOR2xp5_ASAP7_75t_R_v2)  61.267593 &
                                         189.152679 r
a0_mul_493_19/Z[4] (net)                1
f2_af31_reg[4]/D (DFFHQNx3_ASAP7_75t_R)          0.449799 & 189.602478 r
```

```
data arrival time                                   189.602478

clock clk (rise edge)                          0.000000   0.000000
clock network delay (ideal)                    0.000000   0.000000
clock reconvergence pessimism                  0.000000   0.000000
f2_af31_reg[4]/CLK (DFFHQNx3_ASAP7_75t_R)                 0.000000 r
library hold time                            177.403076 177.403076
data required time                                  177.403076
-----------------------------------------------------------------------------
data required time                                  177.403076
data arrival time                                  -189.602478
-----------------------------------------------------------------------------
slack (MET)                                         12.199402


Startpoint: f1_img11_reg[3]
          (rising edge-triggered flip-flop clocked by clk)
Endpoint: f2_af09_reg[5]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Point                                Fanout      Incr      Path
-----------------------------------------------------------------------------
clock clk (rise edge)                          0.000000   0.000000
clock network delay (ideal)                    0.000000   0.000000
f1_img11_reg[3]/CLK (DFFHQNx4_ASAP7_75t_R)     0.000000   0.000000 r
f1_img11_reg[3]/QN (DFFHQNx4_ASAP7_75t_R)      28.350830 &
                                               28.350830 r
n_1643 (net)                          1
FE_OCPC2576_n_1643/Y (BUFx12f_ASAP7_75t_R)     20.886581 &
                                               49.237411 r
FE_OCPN2576_n_1643 (net)              17
a0_mul_471_20/g12685/Y (AOI22xp33_ASAP7_75t_R)  17.671745 &
                                               66.909157 f
a0_mul_471_20/n_177 (net)             2
a0_mul_471_20/g12597/Y (OA22x2_ASAP7_75t_R)    21.791176 &
                                               88.700333 f
a0_mul_471_20/n_220 (net)             3
a0_mul_471_20/FE_RC_911_0/Y (NAND2xp5_ASAP7_75t_R)  8.411606 & 97.111938 r
a0_mul_471_20/FE_RN_512_0 (net)       1
a0_mul_471_20/FE_RC_909_0/Y (NAND2x1_ASAP7_75t_R)   10.506363 &
                                               107.618301 f
a0_mul_471_20/n_288 (net)             2
a0_mul_471_20/g12446/Y (NOR2x1_ASAP7_75t_R)    9.173393 & 116.791695 r
a0_mul_471_20/n_335 (net)             2
a0_mul_471_20/g12445/Y (INVx1_ASAP7_75t_R)     5.739128 & 122.530823 f
a0_mul_471_20/n_336 (net)             1
a0_mul_471_20/g12423/Y (NAND2xp5_ASAP7_75t_R)  7.918274 & 130.449097 r
a0_mul_471_20/n_350 (net)             1
a0_mul_471_20/g12395/Y (XNOR2xp5_ASAP7_75t_R_v2)    57.791031 &
```

	188.240128 r
a0_mul_471_20/Z[5] (net)	1
f2_af09_reg[5]/D (DFFHQNx3_ASAP7_75t_R)	0.507782 & 188.747910 r
data arrival time	188.747910
clock clk (rise edge)	0.000000 0.000000
clock network delay (ideal)	0.000000 0.000000
clock reconvergence pessimism	0.000000 0.000000
f2_af09_reg[5]/CLK (DFFHQNx3_ASAP7_75t_R)	0.000000 r
library hold time	169.820709 169.820709
data required time	169.820709
---	---
data required time	169.820709
data arrival time	-188.747910
---	---
slack (MET)	18.927200

Final Results:

Latency – 0.027569 ms
Power – 6.895 mW
Length – 0.2263 mm
Width - 0.2284 mm
Area – 0.051709 mmsq
Density – 0.77308