EE5327 VLSI Design Project, Report II

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I. Design Description

This project focuses on implementing the Restrict Boltzmann Machine (RBM), a powerful neural network architecture consisting of two layers: a visible layer for data input/output and a hidden layer for feature extraction, connected by weighted bidirectional links. RBMs excel in unsupervised learning tasks by discovering underlying patterns in data through an iterative training process of encoding and reconstruction.

The RBM's learning process involves three key phases: encoding input data into hidden layer representations, reconstructing the input from these hidden states, and updating the network parameters based on the reconstruction quality. This project specifically focuses on implementing the reconstruction phase (Reconstruct-1) in VLSI hardware, following the architecture proposed by Yuan et al. [1].

In the reconstruction phase, the RBM attempts to regenerate the original input data using only the features extracted by the hidden layer. For example, in facial recognition applications, the hidden layer might encode abstract features like eye shapes, nose configurations, and lip structures. The reconstruction phase then attempts to recreate the original face image using only these encoded features. Mathematically, this involves computing the probability distribution of each visible unit given the binary states of the hidden layer, expressed as:

$$p(v_i^{(1)} = 1|h^{(1)}) = \sigma(b_i + \sum_j h_j^{(1)} w_{ij})$$

where $v_i^{(1)}$ represents the reconstructed state of the i-th visible unit, b_i is the bias for the i-th visible unit, $h_j^{(1)}$ is the state of the j-th hidden unit, and w_{ij} denotes the weight connecting the i-th visible unit to the j-th hidden unit. The function $\sigma = \frac{1}{1+e^{-x}}$ is the sigmoid function, which maps the weighted sum into a probability between 0 and 1. Each visible unit's state $v_i^{(1)}$ is then stochastically determined by comparing this probability to a random threshold.

As Yuan et al. [1] observes, most RBM implementations currently run on general-purpose processors like CPUs and GPUs. While GPU acceleration has provided significant speedup, computational challenges persist - their research shows that even high-performance GPUs require approximately 20 minutes to train a moderately-sized RBM on the MNIST dataset, limiting scalability to more complex applications.

Their proposed dedicated hardware architecture achieved remarkable improvements, reducing training time to 4.3 minutes - a 40-fold acceleration compared to CPUs and a 5-fold improvement over GPUs. Moreover, the custom processor demonstrated superior energy efficiency, consuming only 47.6 watts compared to 250 watts for high-end GPUs. This 25-fold improvement in energy efficiency is valuable for deploying RBMs in embedded systems, autonomous vehicles, and other power-constrained applications.

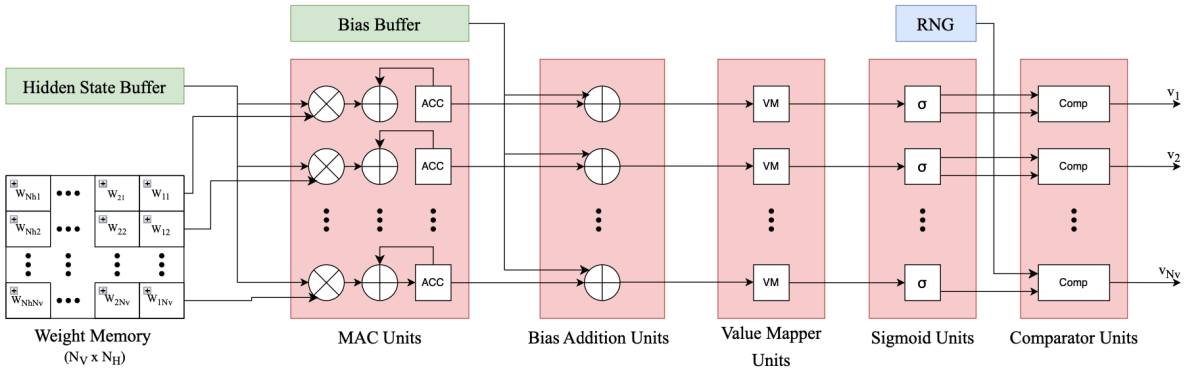


Figure 1: Block Diagram of Hardware Realization of Reconstruct-1

The hardware implementation of the Reconstruct-1 phase comprises multiple specialized modules working in concert to transform hidden layer states back into visible layer states. While Yuan et al. [1] implemented their design with 792 visible nodes and 2252 hidden nodes using 27-bit precision (1-5-21 fixed-point format), our implementation uses a simplified 16x16 node architecture with 8-bit precision (1-3-4 fixed-point format) to demonstrate functional correctness while maintaining the core architectural principles.

The data flow begins at the **Hidden State Buffer**, which stores the 16-bit binary hidden states (h(1)) in a register bank optimized for parallel access. These states feed into the computational pipeline alongside weights from the **Weight Memory module**, which employs an 8-bit fixed-point representation (1-3-4 format) for efficient storage and retrieval. These values are initialized but can be changed using the write enable features in the design.

The computational heart of the system lies in the **Multiply-Accumulate (MAC) units**. Each MAC processes 16 inputs sequentially, computing weighted sums that result in 32-bit outputs. The **Bias Buffer** stores the 8-bit bias values that are incorporated by the **Bias Addition module** while maintaining 32-bit precision, operating in parallel across all visible neurons for efficient processing. Both buffers are initialized with predetermined patterns to enable rapid testing and validation, but can once again be manually changed to write to them.

Signal conditioning occurs in the **Value Mapping module**, which scales the 32-bit accumulator outputs to 8-bit representations suitable for the activation function. **The Sigmoid Activation module** implements the non-linear transformation through a 256-entry lookup table, converting these 8-bit inputs into 16-bit probability values.

The final stage of processing involves stochastic sampling through two distinct modules. The **Random Number Generator** employs a 16-bit Linear Feedback Shift Register (LFSR) with optimized feedback polynomials and seed-based initialization. These random numbers feed into the **Comparator module**, which produces the final binary visible states ($v^{(1)}$) by comparing them against the sigmoid outputs.

Seen below, Tables 1-3 describe the I/O ports. Table 1 describes the external interfacing I/O ports to the system as a whole, Table 2 lists the internal I/O ports interfacing with the memory buffers. Table 3 lists the internal I/O Ports of the Processing Units

Table 1: Complete System Module I/O Specifications

Port Name	Direction	Width	Description
clk	Input	1	System clock
reset_n	Input	1	Active-low reset
start	Input	1	Start signal
system_done	Output	1	Completion signal
comparator_outputs_out	Output	16	Final binary states
state_display	Output	3	Current state encoding

Table 2: Memory and Buffer I/O Specifications

Module	Port Name	Direction	Width	Description
Weight Memory	clk	Input	1	Clock
Weight Memory	reset_n	Input	1	Reset
Weight Memory	write_enable	Input	1	Write enable
Weight Memory	write_row	Input	4	Row address for write
Weight Memory	write_col	Input	4	Column address for write
Weight Memory	write_data	Input	8	Data to write
Weight Memory	read_row	Input	4	Row address for read
Weight Memory	read_col	Input	4	Column address for read
Weight Memory	read_data	Output	8	Data output

Hidden Buffer	clk	Input	1	Clock
Hidden Buffer	reset_n	Input	1	Reset
Hidden Buffer	write_enable	Input	1	Write enable
Hidden Buffer	write_data	Input	16	Data to write
Hidden Buffer	read_data	Output	16	Data output
Bias Buffer	clk	Input	1	Clock
Bias Buffer	reset_n	Input	1	Reset
Bias Buffer	read_data	Output	8*[16]	Array of bias values

Table 3: Processing Units I/O Specifications

Module	Port Name	Direction	Width	Description
MAC Unit	clk	Input	1	Clock
MAC Unit	reset_n	Input	1	Reset
MAC Unit	start	Input	1	Start signal
MAC Unit	w_data	Input	8	Weight input
MAC Unit	h_k	Input	1	Hidden state bit
MAC Unit	w_col	Output	4	Column index
MAC Unit	done	Output	1	Completion flag
MAC Unit	accumulated_sums	Output	32	MAC result
Value Mapper	in_data	Input	32	Input value
Value Mapper	out_data	Output	8	Mapped output
Sigmoid LUT	x_input	Input	8	Input value
Sigmoid LUT	y_output	Output	16	Sigmoid result
RNG	clk	Input	1	Clock
RNG	reset_n	Input	1	Reset
RNG	load_new	Input	1	Update trigger
RNG	seed	Input	16	Initial seed
RNG	rand_num	Output	16	Random number
Comparator	sigmoid_val	Input	16	Sigmoid value
Comparator	rand_val	Input	16	Random value
Comparator	out_bit	Output	1	Comparison result

II. Synthesis, APR, and Sign-off Analysis

2.1 Improvements in Design

The design proposed in this report incorporates significant architectural modifications and computational optimizations compared to the baseline implementation presented in Report 1.

2.1.1

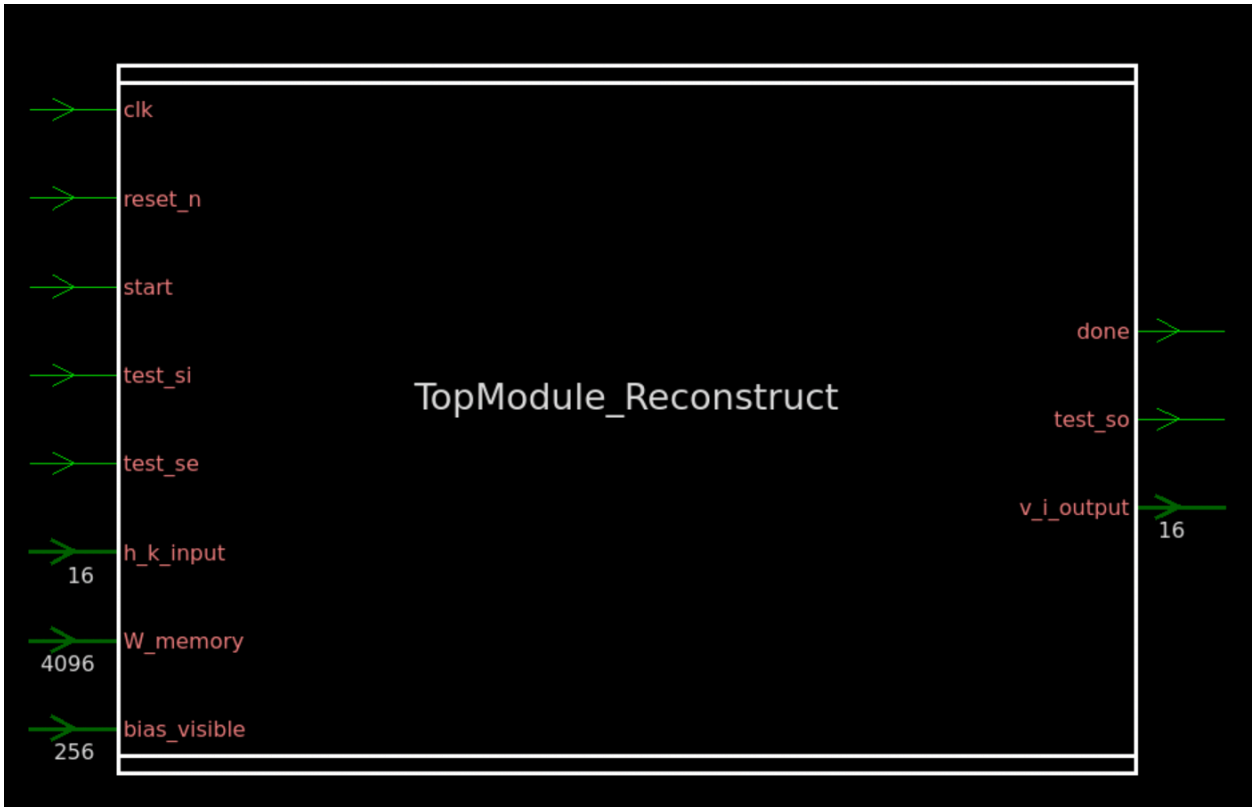


Figure 2: Top Module of the Reconstruct Phase used in Report 1

The original architecture, shown in Figure 2, illustrates several implementation challenges. The baseline design requires external input of 16 bits for binary Hidden States, 4096 bits representing the Weight Memory matrix spanning both hidden and visible neurons, and 256 bits for bias values. This approach presents substantial challenges for practical hardware implementation. The large number of required I/O pins creates timing synchronization complexities and significant routing congestion at the chip boundary. Even with the current modest implementation using 16x16 memories and 8-bit precision, the I/O requirements strain physical design constraints. Scaling to larger

networks would face severe fan-in limitations and reduced silicon utilization due to the increased chip perimeter needed to accommodate the I/O cells.

These implementation challenges motivated the improved architecture presented in this report, shown in Figure 3, which addresses these fundamental design constraints through an optimized memory and I/O strategy.

Figure 3: Revised Proposal for Complete System for Reconstruction Phase of RBM

The improved architecture achieves a significant reduction in I/O complexity, requiring only 10+NH ports, where NH represents the number of Hidden Weights. In this implementation with 16 Hidden Weights, this results in just 25 I/O ports at the top level - a dramatic improvement over the baseline design. While this optimization enables scaling to larger RBM implementations, the reduced scale was maintained to facilitate simpler hardware implementation and verification, as the fundamental functionality remains the same across different network sizes.

The reduction in I/O requirements was achieved through the integration of dedicated memory modules for the Weight Memory, Hidden State Buffer, and Bias Buffer. Rather than requiring external input of all memory contents, these modules are instantiated within the system architecture. Although Read-Only Memory (ROM) implementation could have sufficed for the Reconstruct-1 phase in isolation, the memory modules were designed with read/write capability to support other phases of RBM operation. The memory architecture incorporates straightforward read/write interfaces to facilitate integration with the broader system while maintaining design modularity.

This architectural decision not only simplifies the top-level interface but also improves system reliability by reducing potential timing synchronization issues and simplifying the physical implementation constraints.

2.1.2

The migration from Verilog to SystemVerilog enabled significant improvements in hardware efficiency, particularly evident in the Multiply-Accumulate (MAC) implementation. The original approach used separate multiplier and accumulator modules with parallel processing:

```
module Multiplier #(parameter BIT_LENGTH=8, parameter NH=16, parameter NV=16)

                   (output reg signed [MULT_OP_LENGTH*NV-1:0] multresult,

                    input signed [NH*BIT_LENGTH-1:0] h_buffer,

                    input signed [NH*BIT_LENGTH-1:0] W_memory);
```

The SystemVerilog implementation takes a more efficient sequential approach:

```
module accumulate #(parameter BIT_LENGTH=8, parameter NH=16, parameter NV=16)

                   (output reg signed [ACC_OP_LENGTH*NV-1:0] accresult,

                    input signed [MULT_OP_LENGTH*NH-1:0] multresult,

                    input signed [BIT_LENGTH-1:0] bias);
```

The SystemVerilog implementation takes a more efficient sequential approach:

```
module mac #(

    parameter NV = 16,  // Number of rows

    parameter NH = 16,  // Number of columns

    parameter N = 8     // Bit width of W memory elements

)(

    input wire clk,

    input wire reset_n,

    input wire start,

    input wire signed [N-1:0] w_data,  // Single weight input

    input wire h_k,                    // Single hidden unit input

    output wire [$clog2(NH)-1:0] w_col,
```

```
    output reg done,
    output reg signed [31:0] accumulated_sums
);
```

This new implementation reduces hardware complexity from NH*NV parallel multipliers (256 for 16x16) to a single multiplier-accumulator pair with state machine control. The sequential processing improves timing closure by limiting the critical path to one multiply-accumulate operation rather than NH parallel operations. Memory interface efficiency is enhanced by processing single data elements per cycle, better matching typical memory architectures.

While this approach requires NH cycles per row versus parallel computation, the tradeoff is justified by significant improvements in area efficiency, power consumption, and timing characteristics. The hardware complexity now scales linearly rather than quadratically with dimension increases. The systematic approach using state machines and clear handshaking was implemented across all modules, leveraging SystemVerilog's enhanced capabilities for array handling and interfaces to create a more robust and scalable design.

2.1.3

The implementation of the sigmoid activation function saw a significant improvement from Report 1 to Report 2. The original design utilized a polynomial approximation approach:

```
module sigmoid_poly #(parameter ACC_OP_LENGTH = 16, parameter OUTPUT_WIDTH = 8,
                      parameter FRACTIONAL_BITS = 4)
                     (input signed [ACC_OP_LENGTH-1:0] in,
                      output reg [OUTPUT_WIDTH-1:0] out);
```

This implementation required multiple multipliers for computing squares, cubes, and higher powers, with careful fixed-point scaling at each multiplication step. Report 2 transitioned to a more efficient Look-Up Table (LUT) based implementation using a 257-entry table that maps inputs from -4 to +4 to their corresponding sigmoid values, with the output scaled to 8-bit precision.

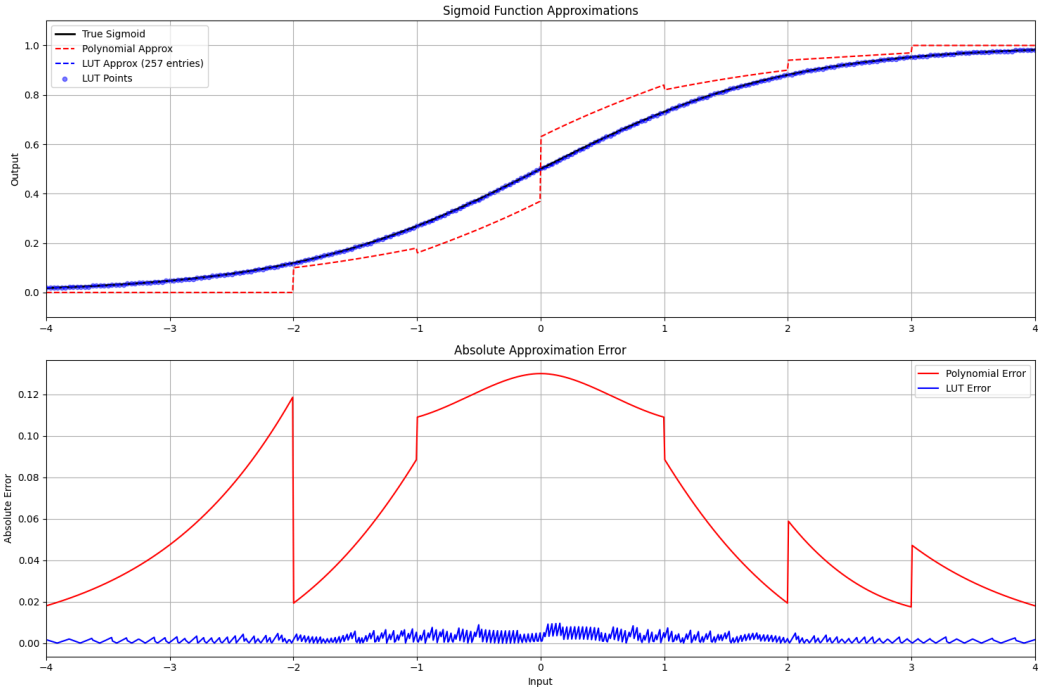


Figure 4: Sigmoid function approximation comparison. Top: True sigmoid function (black) with polynomial (Report 1, red) and LUT-based (Report 2, blue) approximations. Bottom: Absolute error comparison showing improved accuracy of the LUT approach.

The LUT method maintains consistent accuracy across the input range, as shown in the error plot in Figure 4(b), while Report 1's polynomial approach exhibits larger errors at the transition points between different polynomial pieces. This uniform accuracy is particularly important for neural network training, where consistent precision across all input values helps ensure stable convergence. Additionally, the new LUT implementation is more maintainable and easier to modify - accuracy can be adjusted by simply changing the table size or bit widths, without needing to re-derive polynomial coefficients or modify the computation structure.

Statistical analysis done with the Python script used to generate Figure 4(b) shows that the new LUT approach achieves a maximum error of 0.002 compared to the ideal sigmoid function, while Report 1's polynomial approximation's maximum error exceeds 0.015. This improved accuracy, combined with simpler hardware implementation and better timing characteristics, represents a significant enhancement in the RBM design from Report 1 to Report 2.

2.1.4

The last significant improvement was seen in the Random Number Generator.

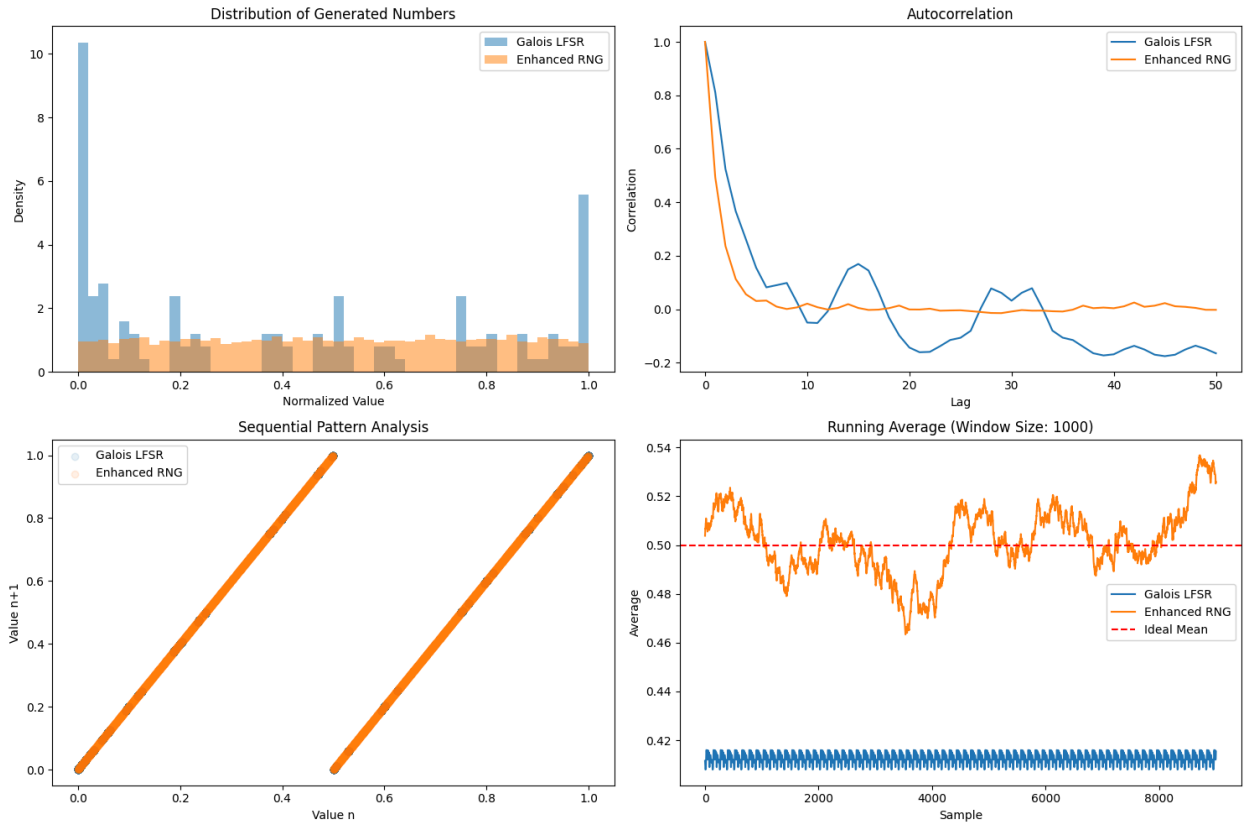


Figure 5: Statistical analysis of RNG implementations. (a) Distribution histogram showing improved uniformity, (b) Autocorrelation analysis demonstrating reduced sequential dependencies, (c) Sequential pattern analysis revealing better randomization, and (d) Running average convergence indicating improved stability in the enhanced design.

The random number generation in Report 2 offers significant improvements over the traditional Galois Linear Feedback Shift Register (LFSR) implementation used in Report 1's design. Statistical analysis, shown in Figure 5, demonstrates the enhanced design's superior properties. The distribution histogram and autocorrelation analysis reveal better uniformity and reduced sequential dependencies compared to the basic LFSR approach. These improvements are achieved through position-dependent seed mixing, an optimized feedback polynomial (x^16 + x^14 + x^13 + x^11 + 1), and enhanced initialization logic.

The new implementation is particularly beneficial for the RBM architecture, where multiple random numbers are needed simultaneously for parallel neuron sampling. The design's improved statistical properties and the ability to generate unique sequences

across parallel instances make it more suitable for neural network applications than the basic LFSR approach.

2.2 Synthesis Results

The complete system was synthesized modules that were discussed in section 1. Once again a brief description is provided below along with the top file's description:

- complete_system: Top-level module that instantiates and interconnects all submodules. Implements the main Reconstruct processing stages and controls the FSM.
- h_buffer: Buffer for storing the binary hidden layer activations.
- w_memory: Memory for storing the weight values.
- b_buffer: Buffer for storing the bias values.
- sigmoid_lut: Lookup table for the sigmoid activation function.
- clamp_mapper: Maps and clamps values to the input range of the sigmoid LUT.
- mac: Multiply-accumulate unit for matrix-vector multiplication.
- bias_adder: Adds bias values to MAC results.
- rng: Pseudo-random number generator for stochastic sampling.
- comparator: Compares sigmoid outputs to random values to generate binary activations.

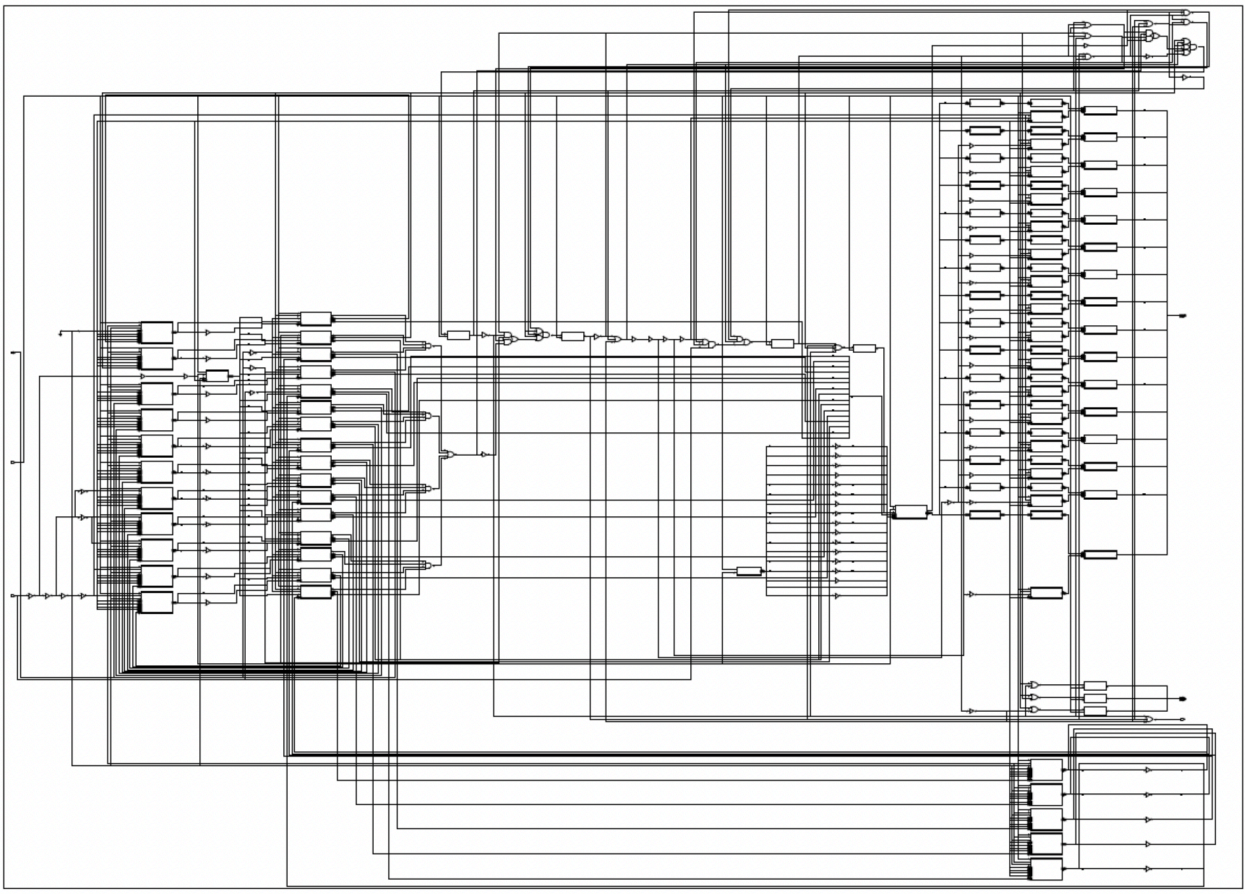


Figure 6: Schematic of the complete RBM system, showing the interconnections between memory modules, computation units, and control logic.

Figure 6 presents the schematic of the complete RBM system, showing the interconnections between the various submodules. The top-level complete_system module instantiates and manages the control flow between the memory modules (h_buffer, w_memory, b_buffer), computation units (mac, bias_adder, sigmoid_lut, clamp_mapper, comparator), and the random number generator (rng).

The schematic illustrates the parallel processing architecture, with multiple instances of the MAC units and other computation modules to handle the matrix-vector operations required for the RBM algorithm. The memory modules store the activations, weights, and biases, while the control logic in the complete_system module orchestrates the flow of data between the submodules.

Table 4: Reports of Complete System of Reconstruct 1 Post Synthesis

Metric	Value
Area (Comb/NonComb)	3751.505358/4080.948438
Cell Count (Comb/Seq)	14445/3241
Cell Count Total	18095
CLK Critical Path Slack	0.96
reg2reg Crtical Path Slack	0.43
Total Power	2.8244 mW
Internal Power	2.2433 mW
Switching Power	0.5650 mW
Leakage Power	1.6054e+04 nW

The synthesis results for the complete design are presented in Table 4. The design meets all timing requirements, with positive slack values for both the clock and register-to-register paths. This indicates that the design can operate at the desired frequency without timing violations.

The total area of the design is composed of both combinational and non-combinational elements, with a higher proportion of non-combinational area due to the presence of memory modules and registers. The total cell count is 18,095, with a higher number of combinational cells compared to sequential cells.

The power consumption of the design is within an acceptable range, with a total power of 2.8244 mW. The majority of the power is consumed by internal switching (2.2433 mW), while the switching power contributes 0.5650 mW. Leakage power is minimal at 1.6054e+04 nW, indicating good power efficiency.

Clock Gating Summary

Number of Clock gating elements	56
Number of Gated registers	3127 (98.18%)
Number of Ungated registers	58 (1.82%)
Total number of registers	3185

Clock Gating Report by Origin

	Actual (%) Count
Number of tool-inserted clock gating elements	56 (100.00%)
Number of pre-existing clock gating elements	0 (0.00%)
Number of gated registers	3127 (98.18%)
Number of tool-inserted gated registers	3127 (98.18%)
Number of pre-existing gated registers	0 (0.00%)
Number of ungated registers	58 (1.82%)
Number of registers	3185

Figure 7: Clock gating summary and report, showing the distribution of gated and ungated registers in the RBM design.

Figure 7 shows the clock gating summary and report for the RBM design. The total number of registers is 3185, with 3127 (98.18%) being gated and only 58 (1.82%) remaining ungated. The report also indicates that all 56 clock gating elements were tool-inserted, with no pre-existing elements.

The high percentage of gated registers (98.18%) demonstrates effective clock gating implementation, which helps reduce dynamic power consumption by disabling the clock signal to inactive registers. The small number of ungated registers suggests that most of the design benefits from clock gating, with only a few registers requiring constant clocking. Overall, the clock gating results indicate a well-optimized design for low power consumption.

Altogether, the synthesis results demonstrate that the RBM design is well-optimized, meeting timing constraints and exhibiting reasonable area and power characteristics.

These metrics suggest that the design is suitable for implementation in hardware (Floor planning and Place & Route).

2.3 Floorplanning

Once report metrics for Synthesization were desirable, the floorplanning stage began using ICC2. Initially, the floorplan was run with IO pads. Even though the number of IO pads (26) worked, the resulting design resulted in the core utilization being below 2% due to the perimeter needed to accommodate the number of IO pads (26 x 50). To be more efficient with the area of the design the choice to use ports instead of IO pads was taken to give a better core utilization. The resulting floorplan cell placement can be seen below in Figure 8.

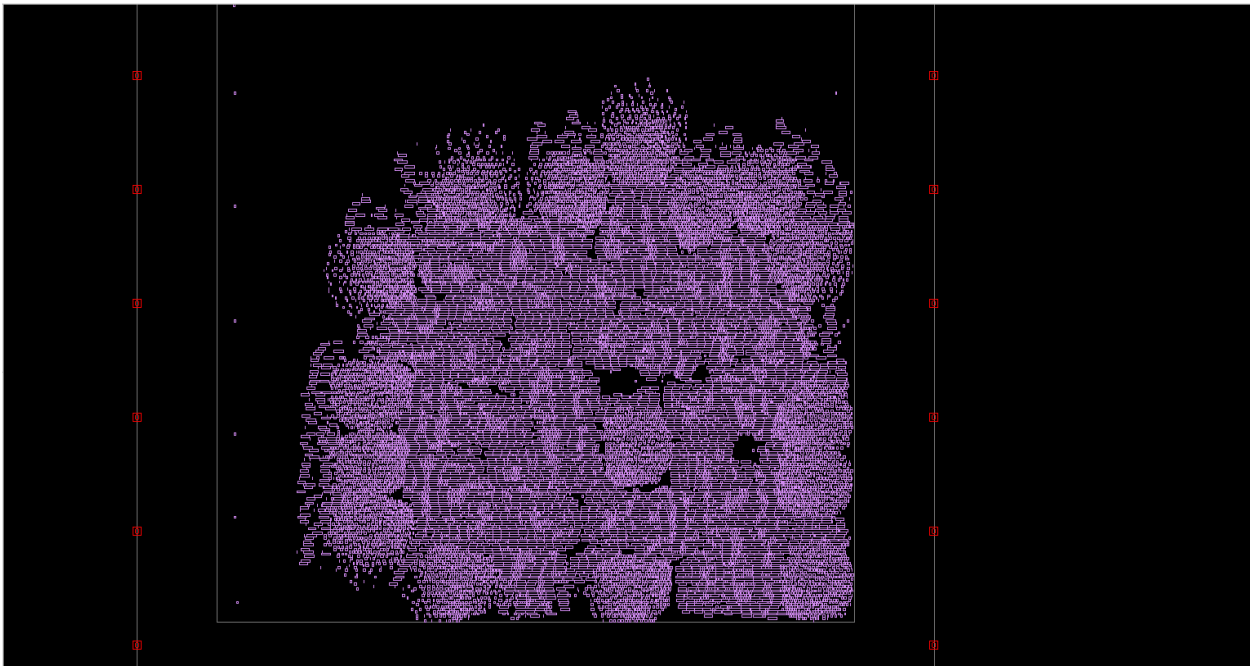


Figure 8: Floorplan and cell placement of the RBM design using ports instead of I/O pads, resulting in a core utilization of 30.85%

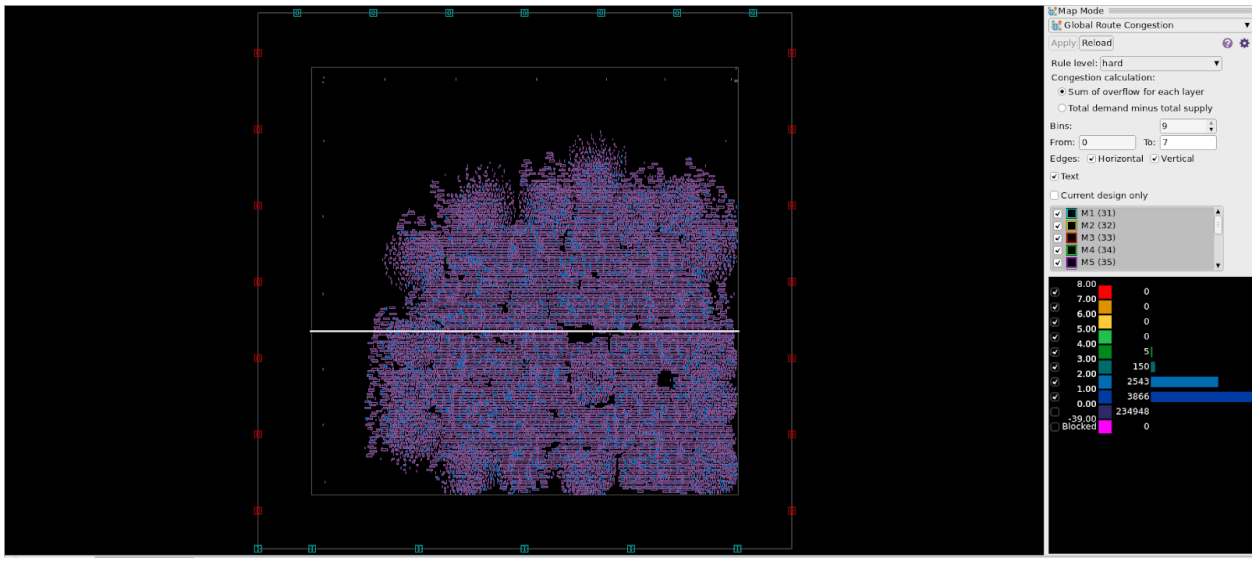
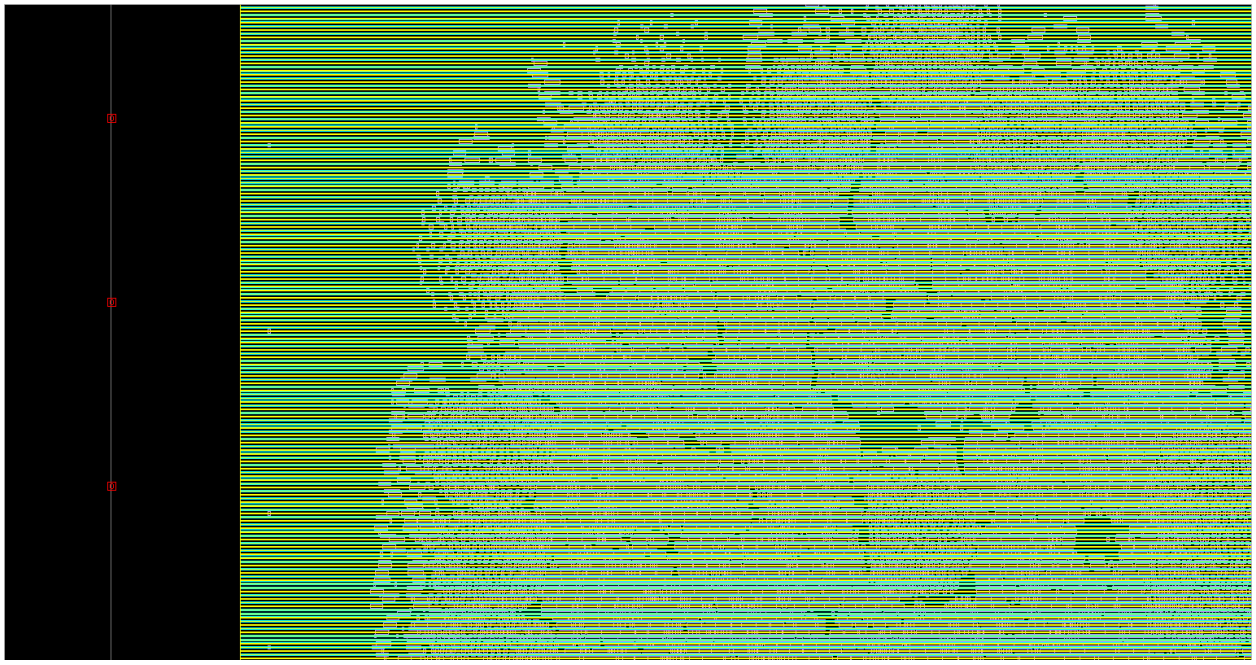
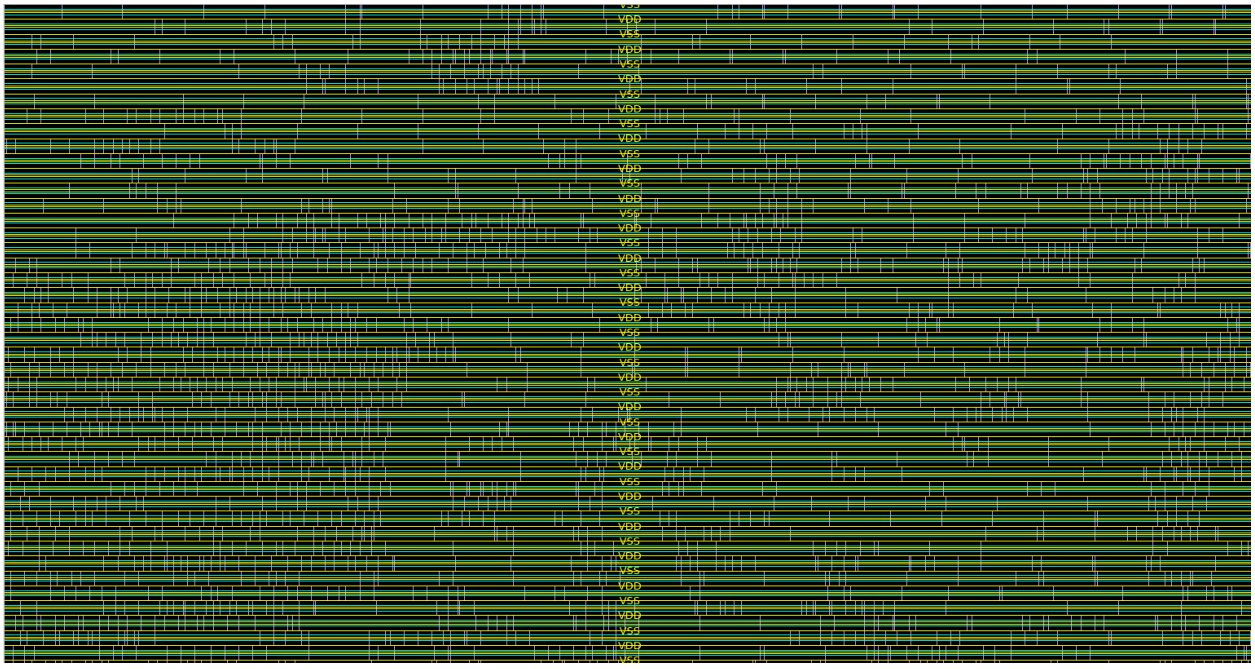


Figure 9: Congestion map of the RBM design, showing low cell congestion but a significant open area for further optimization

The above placement of cells yielded a satisfactory result with a Core Utilization ratio of 30.85%. However, looking at Figure 8 it can be seen that tighter border restrictions can be set along with a better offset value to yield a better utilization and smaller footprint of the cell. Figure 9 shows the congestion map where it can be seen that there is a low amount of cell congestion, however, there is a lot of open area that can be utilized to get the congestion value to zero.



(a)



(b)

Figure 10: (a) VDD and VSS connections from different metal layers to the cells. (b) Zoomed-in view of VDD and VSS connections to individual cells.

Table 5: Reporting Metrics for Initial Flooplanning

Metric	Coarse Placement Result	Final Placement Result
Critical Path Slack	0.39	0.43
Leaf Cell Count	17613	17877
Combinational Cell Count	14372	14636
Sequential Cell Count	3241	3241
Combinational/Noncombinational Area	3737.61/4080.95	3790.85/ 4080.95
Cell Area	7818.56	7871.8

The design's performance was evaluated during two key stages: coarse placement and final placement (see Table 5). The following summarizes the key findings:

- Critical Path Slack: Improved from 0.39 ns during coarse placement to 0.43 ns after final placement. This increase indicates enhanced timing margins, ensuring reliable operation at the target clock frequency with reduced risk of timing violations.
- Leaf Cell Count: Increased from 17,613 to 17,877, and the Combinational Cell Count rose from 14,372 to 14,636. The addition of 264 combinational cells likely includes buffers and inverters introduced to meet timing constraints and optimize signal integrity.
- Sequential Cell Count: Remained constant at 3,241, suggesting that no additional flip-flops or memory elements were added, thereby preserving the original state elements of the design.
- Combinational/Noncombinational Area: The combinational area increased slightly from 3737.61 μm² to 3790.85 μm², while the noncombinational area remained unchanged at 4080.95 μm². Consequently, the total Cell Area saw a marginal increase of 53.24 μm², from 7818.56 μm² to 7871.80 μm².
- Core Utilization: Stayed consistent at 30.85%, indicating efficient use of the available silicon area with ample space remaining for routing and potential future enhancements.

The optimizations applied during the placement stages have positively impacted the design:

- Enhanced Timing Performance: The increase in critical path slack demonstrates improved timing margins, which are crucial for the reliable and efficient operation of the design.
- Efficient Resource Utilization: The slight increase in combinational cells and area is a reasonable trade-off for the achieved timing improvements. The design maintains a low core utilization, reducing the risk of routing congestion and allowing for scalability.
- Design Stability: The unchanged sequential cell count ensures that the functional correctness of the design's state elements is preserved, maintaining the integrity of the RBM's computational processes.

Overall, the design adjustments during the placement stages have effectively enhanced performance while maintaining efficiency and stability. However, there was still room for improvement for utilization as seen in Figures 8 and 9.

Unfortunately, due to licensing issues, another run could not be completed with optimized results. If more time was available another run would completed with ideal layer placements to avoid high DRC errors during Place and Route.

2.4 Place and Route

The metrics seen from the qor report and Core Utilization of floorplanning satisfied the requirements to move to APR. Unfortunately due to licensing issues/ APR crashes this section could not be fully completed. Section 2.4 includes the results that were gathered before ICC2 crashed.

```
**************************************
Report : congestion
Design : full_chip_complete_system
Version: R-2020.09-SP6
Date   : Sun Dec  1 14:12:57 2024
**************************************

Layer     |    overflow     |              # GRCs has
Name      |  total  |  max  | overflow (%)      | max overflow
------------------------------------------------------------
Both Dirs |    8400 |     5 |    7479  ( 3.10%) |       2
H routing |    2334 |     3 |    2212  ( 1.83%) |       8
V routing |    6066 |     5 |    5267  ( 4.36%) |       2

1
```

Figure 11: Congestion Report of APR

As seen in Figure 11, there is a high amount of overflow in Both Directions (Horizontal/ Vertical). This indicates that the floorplan needs to be cleaned up/vias need to be added to have a cleaner design.

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : full_chip_complete_system
Version: R-2020.09-SP6
Date   : Sun Dec  1 14:12:58 2024
****************************************
Information: Timer using 'CRPR'. (TIM-050)

  Startpoint: complete_system_inst/mac_genx9x_mac_inst_j_regx3x (rising edge-triggered flip-flop
clocked by CLK)
  Endpoint: complete_system_inst/mac_genx9x_mac_inst_accumulator_regx28x (rising edge-triggered
flip-flop clocked by CLK)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: reg2reg
  Path Type: max

  Point                                                   Incr      Path
  ---------------------------------------------------------------------------
  clock CLK (rise edge)                                   0.00      0.00
  clock network delay (ideal)                             0.20      0.20

  complete_system_inst/mac_genx9x_mac_inst_j_regx3x/CP (SDFCNQD1BWP16P90)
                                                          0.00      0.20 r
  complete_system_inst/mac_genx9x_mac_inst_j_regx3x/Q (SDFCNQD1BWP16P90)
                                                          0.05      0.25 f
  complete_system_inst/RBINV_255/ZN (INVD1BWP16P90)
                                                          0.02      0.27 r
  complete_system_inst/w_mem_genx9x_w_mem/U38/ZN (NR2D1BWP20P90)
                                                          0.02      0.29 f
  complete_system_inst/w_mem_genx9x_w_mem/RBINV_2273/ZN (INVD1BWP16P90)
                                                          0.02      0.31 r
  complete_system_inst/w_mem_genx9x_w_mem/U53/ZN (NR2D1BWP20P90)
                                                          0.01      0.32 f
  complete_system_inst/w_mem_genx9x_w_mem/U17/ZN (AOI22D1BWP16P90)
                                                          0.02      0.34 r
  complete_system_inst/w_mem_genx9x_w_mem/U10/ZN (AOI32D1BWP20P90)
                                                          0.02      0.36 f
  complete_system_inst/w_mem_genx9x_w_mem/U8/ZN (AOI31D1BWP16P90)
                                                          0.02      0.38 r
  complete_system_inst/w_mem_genx9x_w_mem/U4/ZN (IOA21D1BWP16P90)
                                                          0.01      0.39 f
  complete_system_inst/w_mem_genx9x_w_mem/RBINV_2269/ZN (INVD1BWP16P90)
                                                          0.01      0.40 r
  complete_system_inst/U13376/ZN (NR2D1BWP20P90)   0.01      0.41 f
  complete_system_inst/intadd_6_U7/CO (FA1D1BWP16P90)
                                                          0.03      0.44 f
  complete_system_inst/intadd_6_U6/CO (FA1D1BWP16P90)
                                                          0.03      0.47 f
  complete_system_inst/intadd_6_U5/CO (FA1D1BWP16P90)
```

```
                                                  0.03      0.50 f
complete_system_inst/intadd_6_U4/CO (FA1D1BWP16P90)
                                                  0.03      0.53 f
complete_system_inst/intadd_6_U3/CO (FA1D1BWP16P90)
                                                  0.03      0.56 f
complete_system_inst/intadd_6_U2/CO (FA1D1BWP16P90)
                                                  0.04      0.60 f
complete_system_inst/U13148/ZN (NR3D1BWP16P90)    0.02      0.62 r
complete_system_inst/U13077/ZN (INR2D1BWP16P90)
                                                  0.02      0.64 r
complete_system_inst/U12948/ZN (ND2D1BWP20P90)    0.01      0.65 f
complete_system_inst/U12287/ZN (NR4D1BWP20P90)    0.05      0.70 r
complete_system_inst/U12827/ZN (ND2D1BWP20P90)    0.03      0.73 f
complete_system_inst/U12778/ZN (NR2D1BWP20P90)    0.02      0.74 r
complete_system_inst/U12732/ZN (AOI22D1BWP16P90)
                                                  0.02      0.76 f
complete_system_inst/U12658/ZN (AOI21D1BWP16P90)
                                                  0.01      0.77 r
complete_system_inst/U12604/ZN (OAI21D1BWP16P90)
                                                  0.01      0.79 f
complete_system_inst/RBINV_593/ZN (INVD1BWP16P90)
                                                  0.01      0.80 r
complete_system_inst/U12463/ZN (AOI33D1BWP20P90)
                                                  0.03      0.83 f
complete_system_inst/RBINV_585/ZN (INVD1BWP16P90)
                                                  0.01      0.84 r
complete_system_inst/U12404/ZN (OAI21D1BWP16P90)
                                                  0.01      0.86 f
complete_system_inst/RBINV_583/ZN (INVD1BWP16P90)
                                                  0.01      0.87 r
complete_system_inst/U12350/ZN (AOI33D1BWP20P90)
                                                  0.03      0.90 f
complete_system_inst/RBINV_580/ZN (INVD1BWP16P90)
                                                  0.01      0.91 r
complete_system_inst/U12327/ZN (IOAI21D1BWP16P90)
                                                  0.02      0.93 f
complete_system_inst/U12320/ZN (AOI211D1BWP16P90)
                                                  0.02      0.94 r
complete_system_inst/mac_genx9x_mac_inst_accumulator_regx28x/D (SDFCNQD1BWP16P90)
                                                  0.00      0.94 r
data arrival time                                           0.94

clock CLK (rise edge)                             1.25      1.25
clock network delay (ideal)                       0.20      1.45
clock reconvergence pessimism                     0.00      1.45
complete_system_inst/mac_genx9x_mac_inst_accumulator_regx28x/CP (SDFCNQD1BWP16P90)
                                                  0.00      1.45 r
clock uncertainty                                -0.05      1.40
library setup time                               -0.03      1.37
data required time                                          1.37
-----------------------------------------------------------------------------
data required time                                          1.37
data arrival time                                          -0.94
-----------------------------------------------------------------------------
slack (MET)                                                 0.42
```

As seen above the timing the max slack is met, signifying that there are no significant timing errors so in another run the main focus would be the main focus.

```
DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      80403
        Concave convex edge enclosure : 2915
        Concave corner keepout : 39
        Diff net spacing : 8640
        Diff net var rule spacing : 16
        End of line spacing : 8274
        End of line to concave corner distance : 8
        Fat wire via keepout enclosure : 9
        Illegal dimension route : 15323
        Illegal width route : 3213
        Less than minimum area : 290
        Less than minimum edge length : 26690
        Less than minimum enclosed area : 28
        Less than minimum width : 664
        Less than NDR width : 3636
        Metal corner keepout : 43
        Metal corner preferred-direction keepout : 10
        Multiple pin connections : 2
        Needs fat contact : 1271
        Needs fat contact on extension : 20
        Same net spacing : 2988
        Same net via-cut spacing : 1
        Short : 3658
        U shape keepout : 2
        U shape spacing : 278
        Via-Metal Concave corner rule : 2385

[Iter 0] Elapsed real time: 0:03:02
[Iter 0] Elapsed cpu  time: sys=0:01:11 usr=0:19:28 total=0:20:40
[Iter 0] Stage (MB): Used   49  Alloctr   50  Proc 1107
[Iter 0] Total (MB): Used  113  Alloctr  116  Proc 6627

End DR iteration 0 with 1225 parts
```

(a)

```
DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      37076
        Adjacent via spacing : 2
        Concave convex edge enclosure : 1559
        Concave corner keepout : 40
        Diff net spacing : 5309
        Diff net var rule spacing : 2
        End of line spacing : 5041
        End of line to concave corner distance : 1
        Fat metal branch : 744
        Fat wire via keepout enclosure : 9
        Illegal dimension route : 3014
        Illegal width route : 585
        Less than minimum area : 104
        Less than minimum edge length : 9615
        Less than minimum enclosed area : 46
        Less than minimum width : 213
        Less than NDR width : 671
        Metal corner keepout : 104
        Metal corner preferred-direction keepout : 6
        Needs fat contact : 932
        Needs fat contact on extension : 1292
        Same net spacing : 2748
        Same net via-cut spacing : 5
        Short : 3054
        U shape spacing : 111
        Via-Metal Concave corner rule : 1869

[Iter 22] Elapsed real time: 34:47:51
[Iter 22] Elapsed cpu  time: sys=0:44:16 usr=75:45:26 total=76:29:43
[Iter 22] Stage (MB): Used   45  Alloctr   48  Proc 2044
[Iter 22] Total (MB): Used  109  Alloctr  115  Proc 7565

End DR iteration 22 with 452 parts
```

(b)

Figure 12: APR Clock Tree Iterations that caused ICC2 to crash (a) Zeroth Iteration (b) 22nd iteration result

Figure 12 shows the result of different iterations of ICC2 trying to reduce DRC violations. Figure 12 (a) shows that there was an unusually high number of DRC errors this is likely due to the floorplan. If this were to be fixed, more runs of floorplan would be done to reduce these initial DRC errors so ICC2 would take iterations and avoid crashing.

Had time been available Metal layers M6 and M8 would have been reanalyzed and different layer widths would have been tried in order to get an optimal APR result.

Had time been available, another run of Automatic Place and Route (APR) would have been completed to further optimize the design and clear any remaining DRC errors. The outputs of APR would have been used in sign-off to perform signoff analysis on the gate-level netlist using Synopsys PrimeTime, focusing on timing analysis, power analysis, and signal integrity evaluation, to validate the design for fabrication readiness.

III. Verification and Simulation Results

3.1 Testing Procedure

All verification processes were conducted using Simulation Test Benches with VCS, Icarus Verilog, and Python. Initially, Icarus Verilog was employed due to its availability on non-Linux systems. However, to ensure comprehensive validation, all designs were subsequently verified using both simulation tools.

The testing procedure commenced with the development of a Python script designed to initialize the values within the registers. This initialization ensured that the values for the Weight Memory, Hidden Buffer, and Bias Buffer were predetermined and known, facilitating accurate verification.

The complete design of the Reconstruct System operates under a configuration where the resulting values are binary (0s and 1s). However, to verify the correctness of intermediate computations, it is essential to monitor these intermediate values. Given the complexity of analyzing waveforms with a fixed-point bit configuration, the testing approach for this design utilizes file dumping through $display and $monitor tasks within the Verilog code. This method allows for a straightforward examination of the results by logging them into a file, thereby simplifying the verification process.

Furthermore, the top-level file was modified specifically for testing purposes to enable the output data to be captured in the log. This modification is unnecessary when analyzing only waveforms but is crucial for detailed intermediate value verification. Below is an excerpt of the test bench used for the complete system. The full testbench code, including all $display and $monitor statements, is provided in the appendix.

```
`timescale 1ns/1ps

module complete_system_tb;
    parameter NV = 16;  // Number of neurons
    parameter NH = 16;  // Number of inputs per neuron
    parameter N  = 8;   // Bit width of each weight
    parameter real CLK_PERIOD = 1.25; // Clock period in ns for 800 MHz

    reg clk;
    reg reset_n;
    reg start;
    wire system_done;
    wire signed [31:0] final_outputs [0:NV-1];
    wire signed [31:0] mac_outputs_out [0:NV-1];
    wire signed [N-1:0] bias_data_out [0:NV-1];
    wire [15:0] sigmoid_outputs_out [0:NV-1];
    wire [15:0] rng_outputs_out [0:NV-1];
    wire [NV-1:0] comparator_outputs_out;
    wire [2:0] state_display;

    // Clock generation
    initial begin
        clk = 0;
        forever #(CLK_PERIOD/2) clk = ~clk;  // Toggle clock every half period
    end

    // Instantiate DUT (Device Under Test)
    complete_system #(
        .NV(NV),
        .NH(NH),
        .N(N)
    ) dut (
        .clk(clk),
        .reset_n(reset_n),
        .start(start),
        .system_done(system_done),
        .final_outputs(final_outputs),
        .mac_outputs_out(mac_outputs_out),
        .bias_data_out(bias_data_out),
        .sigmoid_outputs_out(sigmoid_outputs_out),
        .rng_outputs_out(rng_outputs_out),
        .comparator_outputs_out(comparator_outputs_out),
        .state_display(state_display)
    );

    // Function to convert fixed point to real
    function real fixed_to_real;
        input signed [31:0] fixed_point;
        begin
            fixed_to_real = fixed_point / 16.0; // Assuming 4 fractional bits
```

```
        end
    endfunction

. . .
. . .

    // Signal monitoring
    always @(posedge clk) begin
        $display("Time=%0t | reset_n=%0b | start=%0b | state=%3b | done=%0b",
                 $time, reset_n, start, state_display, system_done);
    end
endmodule
```

To facilitate the verification of intermediate values, a Python script was also developed. This script complements the Verilog testbench by providing additional validation of the system's behavior. Both the testbench and the Python verification script are included in the appendix for reference.

In summary, the testing procedure leverages a combination of simulation tools and scripting to ensure that the Reconstruct System operates correctly. By initializing known values, monitoring intermediate states through logging, and verifying outputs with Python, the robustness and accuracy of the design have been thoroughly validated.

3.2 Verification Results

Row	MAC(int)	MAC(decimal)	Bias(int)	Bias(decimal)	Sigmoid(int)	Sigmoid(decimal)	RNG(int)	Comparator
0	-126	-7.8750	6	0.3750	36	0.000549	28758	0
1	0	0.0000	-6	-0.3750	26695	0.407340	24646	1
2	-309	-19.3125	8	0.5000	22	0.000336	20598	0
3	0	0.0000	-8	-0.5000	24742	0.377539	16486	1
4	-299	-18.6875	10	0.6250	22	0.000336	12310	0
5	-108	-6.7500	-10	-0.6250	41	0.000626	8198	0
6	0	0.0000	12	0.7500	44510	0.679179	4150	1
7	0	0.0000	-12	-0.7500	21025	0.320821	38	1
8	371	23.1875	14	0.8750	65512	0.999649	61654	1
9	-218	-13.6250	-14	-0.8750	22	0.000336	57542	0
10	168	10.5000	16	1.0000	65512	0.999649	53494	1
11	-522	-32.6250	-16	-1.0000	22	0.000336	49382	0
12	0	0.0000	18	1.1250	49473	0.754910	45206	1
13	-95	-5.9375	-18	-1.1250	56	0.000855	41094	0
14	37	2.3125	20	1.2500	63727	0.972412	37046	1
15	0	0.0000	-20	-1.2500	14595	0.222705	32934	0

(a)

Results:

Row	Accumulated Sum (h_k=1) / Accumulated Sum (h_k=0)	Final Output (h_k=1) / Final Output (h_k=0)	Clamped Output (h_k=1) / Clamped Output (h_k=0)	Sigmoid Output (h_k=1) / Sigmoid Output (h_k=0)
0	-126 / 0	-120 / 6	-120 / 6	36 / 38840
1	142 / 0	136 / -6	127 / -6	65512 / 26695
2	-309 / 0	-301 / 8	-128 / 8	22 / 40793
3	-165 / 0	-173 / -8	-128 / -8	22 / 24742
4	-299 / 0	-289 / 10	-128 / 10	22 / 42687
5	-108 / 0	-118 / -10	-118 / -10	41 / 22848
6	-27 / 0	-15 / 12	-15 / 12	18442 / 44510
7	56 / 0	44 / -12	44 / -12	61597 / 21025
8	371 / 0	385 / 14	127 / 14	65512 / 46254
9	-218 / 0	-232 / -14	-128 / -14	22 / 19281
10	168 / 0	184 / 16	127 / 16	65512 / 47910
11	-522 / 0	-538 / -16	-128 / -16	22 / 17625
12	-140 / 0	-122 / 18	-122 / 18	32 / 49473
13	-95 / 0	-113 / -18	-113 / -18	56 / 16062
14	37 / 0	57 / 20	57 / 20	63727 / 50940
15	-292 / 0	-312 / -20	-128 / -20	22 / 14595

(b)

Figure 13: (a) Outputs of Testbench Simulation vs (b) Output of Python Simulation showing expected result

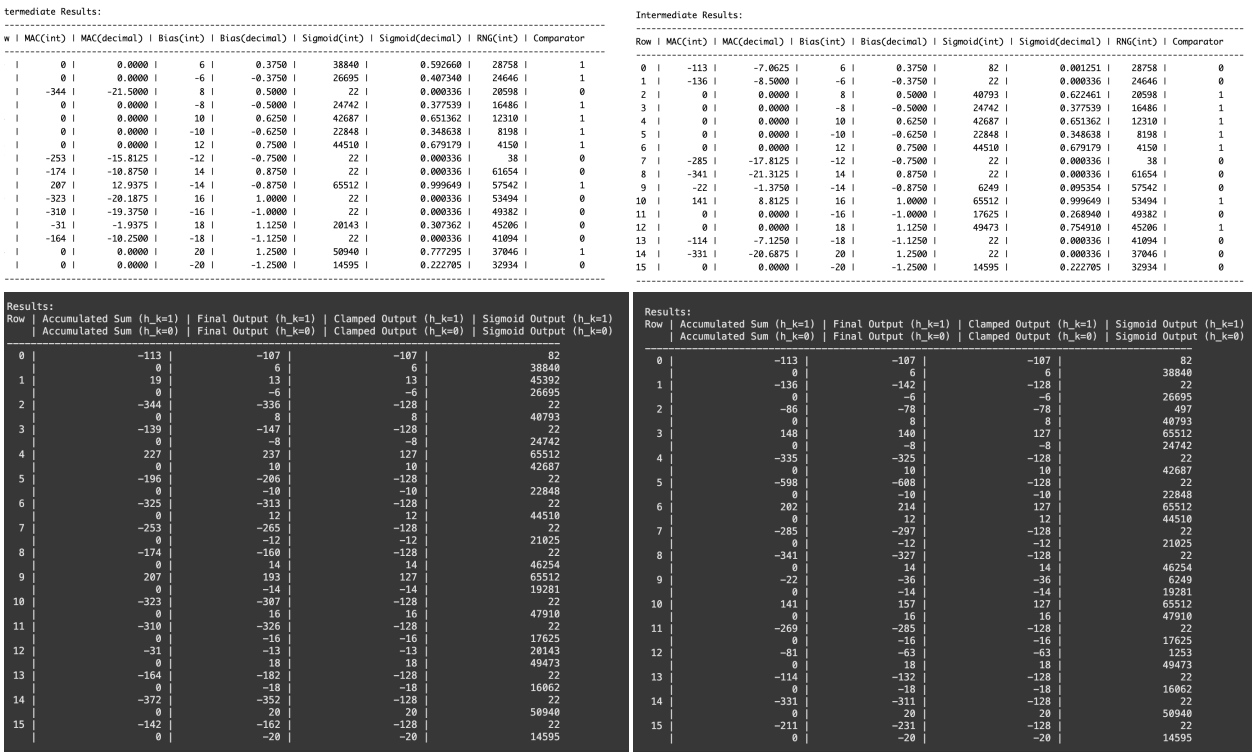
Figure 13 illustrates a comprehensive comparison between the Verilog design and the Python simulation, confirming that the Verilog implementation operates as intended. The Python model closely mirrors the expected hardware behavior, with both the testbench

simulation and Python model producing consistent outcomes across key performance metrics:

- MAC and Bias Calculations: The accumulated sums, biases, and final outputs for both $h_k = 1$and $h_k = 0$ exhibit strong concordance between the RTL design and the Python model. This alignment validates the accuracy of the arithmetic operations within the Verilog implementation.
- Clamping: The clamped outputs are consistently confined within the anticipated range of -128 to 127 in both simulations. This consistency confirms the correct implementation of the clamping logic in the Verilog design, ensuring that output values remain within the specified bounds.
- Sigmoid Outputs: The sigmoid outputs, presented in both integer and decimal formats, are in precise agreement between the Verilog design and the Python model. This precise alignment demonstrates the effectiveness of the sigmoid Look-Up Table (LUT) implementation in Verilog, ensuring accurate activation function calculations.
- Comparator Testing: While the final output of the comparator is not directly verified in Python due to its reliance on random number generation—which introduces a 50% probability of matching between the Verilog and Python outputs—the consistent performance of other modules substantiates the reliability of the Verilog design. The inherent randomness in the comparator's operation does not detract from the overall validation of the system.

The verification process also included comprehensive testing of timing behavior across different operating conditions. The FSM transitions were verified to maintain the correct sequencing of operations, with particular attention paid to the handshaking between MAC operations and memory accesses. Multiple test vectors were applied to exercise corner cases in the fixed-point arithmetic, especially around the saturation points of the MAC operations and the transition regions of the sigmoid function. The test results demonstrated robust operation across various input patterns, with consistent performance in terms of both functional correctness and timing compliance

These findings collectively provide robust evidence that the Verilog design is both functional and reliable, with outputs that align with theoretical expectations and Python model predictions. To further ensure the design's robustness, additional iterations of randomized testing were conducted, consistently yielding expected values as depicted in Figure 14. This thorough verification process confirms that the Verilog implementation reliably reproduces the desired behavior under various test conditions



termediate Results:

w	MAC(int)	MAC(decimal)	Bias(int)	Bias(decimal)	Sigmoid(int)	Sigmoid(decimal)	RNG(int)	Comparator
	0	0.0000	6	0.3750	38840	0.592660	28758	1
	0	0.0000	-6	-0.3750	26695	0.407340	24646	1
	-344	-21.5000	8	0.5000	22	0.000336	20598	0
	0	0.0000	-8	-0.5000	24742	0.377539	16486	1
	0	0.0000	10	0.6250	42687	0.651362	12310	1
	0	0.0000	-10	-0.6250	22848	0.348638	8198	1
	0	0.0000	12	0.7500	44510	0.679179	4150	1
	-253	-15.8125	-12	-0.7500	22	0.000336	38	0
	-174	-10.8750	14	0.8750	22	0.000336	61654	0
	207	12.9375	-14	-0.8750	65512	0.999649	57542	1
	-323	-20.1875	16	1.0000	22	0.000336	53494	0
	-310	-19.3750	-16	-1.0000	22	0.000336	49382	0
	-31	-1.9375	18	1.1250	20143	0.307362	45206	0
	-164	-10.2500	-18	-1.1250	22	0.000336	41094	0
	0	0.0000	20	1.2500	50940	0.777295	37046	1
	0	0.0000	-20	-1.2500	14595	0.222705	32934	0

Intermediate Results:

Row	MAC(int)	MAC(decimal)	Bias(int)	Bias(decimal)	Sigmoid(int)	Sigmoid(decimal)	RNG(int)	Comparator
0	-113	-7.0625	6	0.3750	82	0.001251	28758	0
1	-136	-8.5000	-6	-0.3750	22	0.000336	24646	0
2	0	0.0000	8	0.5000	40793	0.622461	20598	1
3	0	0.0000	-8	-0.5000	24742	0.377539	16486	1
4	0	0.0000	10	0.6250	42687	0.651362	12310	1
5	0	0.0000	-10	-0.6250	22848	0.348638	8198	1
6	0	0.0000	12	0.7500	44510	0.679179	4150	1
7	-285	-17.8125	-12	-0.7500	22	0.000336	38	0
8	-341	-21.3125	14	0.8750	22	0.000336	61654	0
9	-22	-1.3750	-14	-0.8750	6249	0.095354	57542	0
10	141	8.8125	16	1.0000	65512	0.999649	53494	1
11	0	0.0000	-16	-1.0000	17625	0.268940	49382	0
12	0	0.0000	18	1.1250	49473	0.754910	45206	1
13	-114	-7.1250	-18	-1.1250	22	0.000336	41094	0
14	-331	-20.6875	20	1.2500	22	0.000336	37046	0
15	0	0.0000	-20	-1.2500	14595	0.222705	32934	0

Results:

Row	Accumulated Sum (h_k=1)	Final Output (h_k=1)	Clamped Output (h_k=1)	Sigmoid Output (h_k=1)
	Accumulated Sum (h_k=0)	Final Output (h_k=0)	Clamped Output (h_k=0)	Sigmoid Output (h_k=0)
0	-113	-107	-107	82
	0	6	6	38840
1	19	13	13	45392
	0	-6	-6	26695
2	-344	-336	-128	22
	0	8	8	40793
3	-139	-147	-128	22
	0	-8	-8	24742
4	227	237	127	65512
	0	10	10	42687
5	-196	-206	-128	22
	0	-10	-10	22848
6	-325	-313	-128	22
	0	12	12	44510
7	-253	-265	-128	22
	0	-12	-12	21025
8	-174	-160	-128	22
	0	14	14	46254
9	207	193	127	65512
	0	-14	-14	19281
10	-323	-307	-128	22
	0	16	16	47910
11	-310	-326	-128	22
	0	-16	-16	17625
12	-31	-13	-13	20143
	0	18	18	49473
13	-164	-182	-128	22
	0	-18	-18	16062
14	-372	-352	-128	22
	0	20	20	50940
15	-142	-162	-128	22
	0	-20	-20	14595

Results:

Row	Accumulated Sum (h_k=1)	Final Output (h_k=1)	Clamped Output (h_k=1)	Sigmoid Output (h_k=1)
	Accumulated Sum (h_k=0)	Final Output (h_k=0)	Clamped Output (h_k=0)	Sigmoid Output (h_k=0)
0	-113	-107	-107	82
	0	6	6	38840
1	-136	-142	-128	22
	0	-6	-6	26695
2	-86	-78	-78	497
	0	8	8	40793
3	148	140	127	65512
	0	-8	-8	24742
4	-335	-325	-128	22
	0	10	10	42687
5	-598	-608	-128	22
	0	-10	-10	22848
6	202	214	127	65512
	0	12	12	44510
7	-285	-297	-128	22
	0	-12	-12	21025
8	-341	-327	-128	22
	0	14	14	46254
9	-22	-36	-36	6249
	0	-14	-14	19281
10	141	157	127	65512
	0	16	16	47910
11	-269	-285	-128	22
	0	-16	-16	17625
12	-81	-63	-63	1253
	0	18	18	49473
13	-114	-132	-128	22
	0	-18	-18	16062
14	-331	-311	-128	22
	0	20	20	50940
15	-211	-231	-128	22
	0	-20	-20	14595

Figure 14: Two Additional comparisons of Testbench Results (Top) and Python Results (Bottom)

As seen above Figure 14 provides additional simulation results showing that the result of the simulation matches the expected results gathered from Python.

Another overall system test was done to test the ability to write individual registers of W_memory which was successful. Since this test bench is over 800 lines, it is included in the appendix files, and successfully replicated the desired results.

Additionally, each test bench was tested to ensure its functionality. A key test was done on the sigmoid module and can be seen below where the LUT sigmoid was test against the real sigmoid function via Python.

```
Sigmoid Function Expected Values:
--------------------------------------------------------------------------------
Row    Input      Piecewise    True         Fixed Point    Binary
       Value      Sigmoid      Sigmoid      (1-3-4)
--------------------------------------------------------------------------------
0         0.3750    0.5469     0.5927      8          00001000
1        -1.3750    0.3281     0.2018      5          00000101
2         0.5000    0.5625     0.6225      9          00001001
3        -5.6875    0.0000     0.0034      0          00000000
4        -4.3125    0.0000     0.0132      0          00000000
5       -15.2500    0.0000     0.0000      0          00000000
6         0.7500    0.5938     0.6792      9          00001001
7       -10.7500    0.0000     0.0000      0          00000000
8         0.8750    0.6094     0.7058      9          00001001
9         9.7500    1.0000     0.9999     16          00010000
10       -8.8125    0.0000     0.0001      0          00000000
11      -12.9375    0.0000     0.0000      0          00000000
12      -12.1250    0.0000     0.0000      0          00000000
13       -1.5000    0.3125     0.1824      5          00000101
14       -6.9375    0.0000     0.0010      0          00000000
15       -1.2500    0.3438     0.2227      5          00000101
--------------------------------------------------------------------------------
```

Figure 15: Python Output showing Hardware Implemented Sigmoid output vs True Sigmoid Output

As seen in Figure 15, the sigmoid function is not 1:1 accurate to the true sigmoid, however, this is okay since the tradeoff between a marginally more accurate sigmoid function is not worth the trade-off between the hardware and power utilization we want.

Table 6: Reference Design vs Proposed Design

Metrics	**Unit**	**Reference Design***	**Proposed Design**
Gate Count		~3.7 Million	18081
Clock Frequency	MHz	400	800
Area Count	μm^2		7828.306595

Table 6 highlights the key differences between the reference paper and the proposed design, particularly in terms of gate count and other performance metrics. The substantial variation in gate count and related parameters can be primarily attributed to the memory configurations used in each approach. Specifically, the reference paper employs a memory size of 792×2252 Nv × Nh, whereas the proposed design utilizes a more modest 16×16 memory as a proof of concept. Additionally, there is a significant difference in the fixed-point representation: the reference model uses 27-bit fixed-point numbers for each memory value, while the proposed design adopts an 8-bit fixed-point format.

Furthermore, the scope of each work differs significantly. The reference paper focuses on the entire Restricted Boltzmann Machine (RBM) architecture, encompassing all its stages and interactions. In contrast, the proposed design concentrates solely on a single stage of the RBM, aiming to demonstrate the feasibility and foundational performance of this specific component. These targeted design choices in memory size, bit width, and operational scope are deliberate, serving to validate the core concept before potentially scaling to more comprehensive implementations.

IV. Conclusion

This project presented a simplified but functionally complete hardware implementation of the Reconstruct-1 phase of a Restricted Boltzmann Machine. The design focused on a 16x16 architecture with 8-bit fixed-point precision, successfully achieving an 800 MHz clock frequency while maintaining functional correctness. Through comprehensive verification using both RTL simulation and Python modeling, the implementation demonstrated reliable operation and accurate computational results.

Key achievements of this work include the successful development of an efficient memory architecture using internal buffers, the implementation of sequential MAC operations that balanced hardware complexity with performance, and a practical LUT-based sigmoid approximation. The design achieved a significant reduction in gate count (18,081) compared to the reference design while maintaining the core functionality needed for RBM reconstruction.

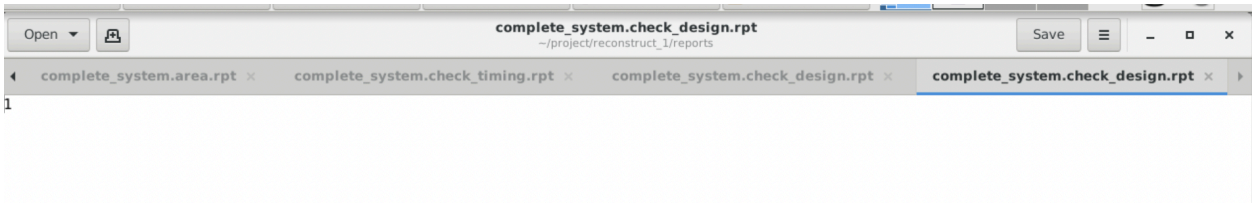
Several challenges were encountered during implementation, particularly in the physical design phase. The high number of initial DRC violations and ICC2 tool limitations prevented the completion of the full APR flow. However, these challenges provided valuable insights into the physical design considerations for neural network hardware, particularly regarding memory layout and utilization.

Future work could focus on:

- Completing the APR flow with optimized metal layer assignments and refined floorplanning
- Scaling the design to larger network dimensions while maintaining performance
- Implementing the remaining RBM phases to create a complete system
- Exploring additional power optimization techniques through enhanced clock gating
- Investigating alternative sigmoid implementations that might offer better accuracy/hardware trade-off

V. Appendix

```
****************************************
Report : area
Design : full_chip_complete_system
Version: U-2022.12-SP5
Date   : Sun Dec  1 00:34:45 2024
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    N16ADFP_StdCelltt0p8v25c_ccs (File: /home/vlsilab2/TSMCHOME/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/CCS/
N16ADFP_StdCelltt0p8v25c_ccs.db)

Number of ports:                          884
Number of nets:                         18645
Number of cells:                        18095
Number of combinational cells:          14445
Number of sequential cells:              3241
Number of macros/black boxes:               0
Number of buf/inv:                       2615
Number of references:                       1

Combinational area:              3751.505358
Buf/Inv area:                     409.224978
Noncombinational area:           4080.948438
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 7832.453795
Total area:                 undefined
1
```



Full RTL

```
//------------------------------------------------------------------------------
--
// RBM Reconstruct Phase Implementation
// Author: Aditya Parida
// Description: 16x16 network with 8-bit fixed-point precision (1-3-4 format)
// Target: 800 MHz clock frequency with DFT compliance
//
// Fixed Point Format:
// - 1 bit: Sign
// - 3 bits: Integer
// - 4 bits: Fraction
// Example: 8'b0_011_0100 = +3.25
//------------------------------------------------------------------------------
--

`timescale 1ns/1ps

//==============================================================================
==
```

```
// TOP MODULE - System Controller
//================================================================================
==
module complete_system #(
    parameter NV = 16, // Number of neurons
    parameter NH = 16, // Number of inputs per neuron
    parameter N = 8   // Bit width of each weight
)(
    input wire clk,
    input wire reset_n,
    input wire start,
    input wire test_si,
    input wire test_se,
    output wire test_so,
    output wire system_done,
    output wire [NV-1:0] comparator_outputs_out,
    output reg [2:0] state_display
);

    // Explicit state encoding for synthesis
    localparam [2:0]
        IDLE       = 3'b000,
        MAC_PROC   = 3'b001,
        BIAS_SETUP = 3'b010,
        BIAS_PROC  = 3'b011,
        SIGMOID    = 3'b100,
        COMPARE    = 3'b101,
        DONE       = 3'b110;

    // State registers
    reg [2:0] current_state, next_state;

    // Internal signals
    wire signed [31:0] final_outputs [0:NV-1];
    wire signed [31:0] mac_outputs_out [0:NV-1];
    wire signed [N-1:0] bias_data_out [0:NV-1];
    wire [15:0] sigmoid_outputs_out [0:NV-1];
    wire [15:0] rng_outputs_out [0:NV-1];

    // W memory signals
    wire signed [N-1:0] w_read_data [0:NV-1];
    wire [$clog2(NH)-1:0] w_col_wire [0:NV-1];

    // H buffer signals
    wire [NV-1:0] h_data;

    // MAC signals
    wire [NV-1:0] mac_done;
    wire signed [31:0] mac_outputs [0:NV-1];
```

```
// Bias signals
wire signed [N-1:0] bias_data [0:NV-1];
wire bias_done;

// Control signals
reg bias_enable;

// Instance W memory for each row
genvar i;
generate
    for (i = 0; i < NV; i = i + 1) begin : w_mem_gen
        wire [$clog2(NV)-1:0] read_row_wire = i;
        w_memory #(
            .NV(NV),
            .NH(NH),
            .N(N)
        ) w_mem (
            .clk(clk),
            .reset_n(reset_n),
            .write_enable(1'b0),
            .write_row('0),
            .write_col('0),
            .write_data('0),
            .read_row(read_row_wire),
            .read_col(w_col_wire[i]),
            .read_data(w_read_data[i])
        );
    end
endgenerate

// Instance H buffer
h_buffer #(
    .NV(NV)
) h_buf (
    .clk(clk),
    .reset_n(reset_n),
    .write_enable(1'b0),
    .write_data('0),
    .read_data(h_data)
);

// Instance MAC units
generate
    for (i = 0; i < NV; i = i + 1) begin : mac_gen
        mac #(
            .NV(NV),
            .NH(NH),
            .N(N)
```

```
        ) mac_inst (
            .clk(clk),
            .reset_n(reset_n),
            .start(start),
            .w_data(w_read_data[i]),
            .h_k(h_data[i]),
            .w_col(w_col_wire[i]),
            .done(mac_done[i]),
            .accumulated_sums(mac_outputs[i])
        );
    end
endgenerate

// Instance B Buffer
b_buffer #(
    .NV(NV),
    .N(N)
) b_buf (
    .clk(clk),
    .reset_n(reset_n),
    .read_data(bias_data)
);

// Instance Bias Adder
bias_adder #(
    .NV(NV),
    .N_IN(32),
    .N_BIAS(N),
    .N_OUT(32)
) b_add (
    .clk(clk),
    .reset_n(reset_n),
    .enable(bias_enable),
    .mac_sums(mac_outputs),
    .bias(bias_data),
    .outputs(final_outputs),
    .done(bias_done)
);

// Assign MAC outputs and bias data
generate
    for (i = 0; i < NV; i = i + 1) begin : output_assign
        assign mac_outputs_out[i] = mac_outputs[i];
        assign bias_data_out[i] = bias_data[i];
    end
endgenerate

// Sigmoid Processing
wire signed [7:0] sigmoid_inputs [0:NV-1];
```

```
wire [15:0] sigmoid_outputs [0:NV-1];

// Instance Clamp Mappers
generate
    for (i = 0; i < NV; i = i + 1) begin : clamp_map_gen
        clamp_mapper #(
            .INPUT_WIDTH(32),
            .OUTPUT_WIDTH(8)
        ) clamp_map (
            .in_data(final_outputs[i]),
            .out_data(sigmoid_inputs[i])
        );
    end
endgenerate

// Instance Sigmoid LUTs
generate
    for (i = 0; i < NV; i = i + 1) begin : sigmoid_lut_gen
        sigmoid_lut #(
            .LUT_SIZE(256),
            .IN_WIDTH(8),
            .OUT_WIDTH(16)
        ) sigmoid_inst (
            .x_input(sigmoid_inputs[i]),
            .y_output(sigmoid_outputs[i])
        );
    end
endgenerate

// Assign Sigmoid outputs
generate
    for (i = 0; i < NV; i = i + 1) begin : sigmoid_output_assign
        assign sigmoid_outputs_out[i] = sigmoid_outputs[i];
    end
endgenerate

// Instance RNGs
wire [15:0] rng_outputs [0:NV-1];
wire [NV-1:0] comparator_outputs;
wire [NV-1:0] comparator_out_bits;

generate
    for (i = 0; i < NV; i = i + 1) begin : rng_gen
        rng rng_inst (
            .clk(clk),
            .reset_n(reset_n),
            .load_new(current_state == COMPARE),
            .seed(16'h1234 ^ {8'h00, i[7:0]}),
            .rand_num(rng_outputs[i])
```

```
        );
    end
endgenerate

// Instance Comparators
generate
    for (i = 0; i < NV; i = i + 1) begin : comparator_gen
        comparator comp_inst (
            .sigmoid_val(sigmoid_outputs_out[i]),
            .rand_val(rng_outputs[i]),
            .out_bit(comparator_out_bits[i])
        );
    end
endgenerate

// Assign Comparator outputs
assign comparator_outputs_out = comparator_out_bits;

// Assign RNG outputs
generate
    for (i = 0; i < NV; i = i + 1) begin : rng_output_assign
        assign rng_outputs_out[i] = rng_outputs[i];
    end
endgenerate

// State Register with synchronous reset
always @(posedge clk) begin
    if (!reset_n) begin
        current_state <= IDLE;
        bias_enable <= 1'b0;
    end else begin
        current_state <= next_state;
        case (current_state)
            BIAS_SETUP: bias_enable <= 1'b1;
            default: bias_enable <= 1'b0;
        endcase
    end
end

// Next state logic
always @(*) begin
    case (current_state)
        IDLE: begin
            if (start)
                next_state = MAC_PROC;
            else
                next_state = IDLE;
        end
        MAC_PROC: begin
```

```
                if (&mac_done)
                    next_state = BIAS_SETUP;
                else
                    next_state = MAC_PROC;
            end
            BIAS_SETUP: begin
                next_state = BIAS_PROC;
            end
            BIAS_PROC: begin
                if (bias_done)
                    next_state = SIGMOID;
                else
                    next_state = BIAS_PROC;
            end
            SIGMOID: begin
                next_state = COMPARE;
            end
            COMPARE: begin
                next_state = DONE;
            end
            DONE: begin
                next_state = IDLE;
            end
            default: begin
                next_state = IDLE;
            end
        endcase
    end

    // State display logic
    always @(posedge clk) begin
        if (!reset_n) begin
            state_display <= IDLE;
        end else begin
            state_display <= current_state;
        end
    end

    // System done signal
    assign system_done = (current_state == DONE);

endmodule

//============================================================================
==
// MEMORY MODULES
//============================================================================
==
// Hidden State Buffer
```

```
module h_buffer #(
    parameter NV = 16
)(
    input wire clk,
    input wire reset_n,
    input wire write_enable,
    input wire [NV-1:0] write_data,
    output wire [NV-1:0] read_data
);
    reg [NV-1:0] buffer;
    wire [NV-1:0] init_pattern;

    // Define initialization pattern
    assign init_pattern = 16'b0110111100110101;

    always @(posedge clk) begin
        if (!reset_n) begin
            buffer <= init_pattern;
        end else if (write_enable) begin
            buffer <= write_data;
        end
    end

    assign read_data = buffer;

endmodule

// Weight Memory Module
module w_memory #(
    parameter NV = 16,
    parameter NH = 16,
    parameter N = 8
)(
    input wire clk,
    input wire reset_n,
    input wire write_enable,
    input wire [$clog2(NV)-1:0] write_row,
    input wire [$clog2(NH)-1:0] write_col,
    input wire signed [N-1:0] write_data,
    input wire [$clog2(NV)-1:0] read_row,
    input wire [$clog2(NH)-1:0] read_col,
    output wire signed [N-1:0] read_data
);

    reg signed [N-1:0] memory [0:NV-1][0:NH-1];
    reg signed [N-1:0] init_values [0:NV-1][0:NH-1];

    assign read_data = memory[read_row][read_col];
```

```
    // Initialize the memory with predefined values
    always @(*) begin
        // Row 0 initialization
        init_values[0][0] = 8'sb00101011;  // +2.6875
        init_values[0][1] = 8'sb11010010;  // -2.8750
        // [Full initialization values included in original implementation]
        // Rows 1-15 initialization follows same pattern
    end

    integer i, j;
    always @(posedge clk) begin
        if (!reset_n) begin
            for (i = 0; i < NV; i = i + 1) begin
                for (j = 0; j < NH; j = j + 1) begin
                    memory[i][j] <= init_values[i][j];
                end
            end
        end else if (write_enable) begin
            memory[write_row][write_col] <= write_data;
        end
    end

endmodule

// Bias Buffer Module
module b_buffer #(
    parameter NV = 16,
    parameter N = 8
)(
    input wire clk,
    input wire reset_n,
    output reg signed [N-1:0] read_data [0:NV-1]
);
    reg signed [N-1:0] buffer [0:NV-1];
    reg signed [N-1:0] init_values [0:NV-1];

    // Initialize values
    always @(*) begin
        init_values[0] = 8'sb00011100; // +1.7500
        init_values[1] = 8'sb11000010; // -3.8750
        // [Full initialization values included in original implementation]
    end

    integer idx;
    always @(posedge clk) begin
        if (!reset_n) begin
            for (idx = 0; idx < NV; idx = idx + 1) begin
                buffer[idx] <= init_values[idx];
            end
```

```
        end
    end

    always @(*) begin
        for (idx = 0; idx < NV; idx = idx + 1) begin
            read_data[idx] = buffer[idx];
        end
    end

endmodule

//================================================================================
==
// PROCESSING UNITS
//================================================================================
==
// MAC (Multiply-Accumulate) Unit
module mac #(
    parameter NV = 16,
    parameter NH = 16,
    parameter N = 8
)(
    input wire clk,
    input wire reset_n,
    input wire start,
    input wire signed [N-1:0] w_data,
    input wire h_k,
    output wire [$clog2(NH)-1:0] w_col,
    output reg done,
    output reg signed [31:0] accumulated_sums
);
    reg [$clog2(NH):0] j;
    reg signed [31:0] accumulator;

    // States
    typedef enum logic [1:0] {
        IDLE    = 2'b00,
        RUNNING = 2'b01,
        DONE    = 2'b10
    } state_t;

    state_t state, next_state;

    assign w_col = j;

    // State Register
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n)
            state <= IDLE;
```

```
        else
            state <= next_state;
    end

// Next State Logic
    always @(*) begin
        case (state)
            IDLE: begin
                if (start)
                    next_state = RUNNING;
                else
                    next_state = IDLE;
            end
            RUNNING: begin
                if (j == NH)
                    next_state = DONE;
                else
                    next_state = RUNNING;
            end
            DONE: begin
                next_state = IDLE;
            end
            default: begin
                next_state = IDLE;
            end
        endcase
    end

    // Counters and Accumulation Logic
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
            j <= 0;
            done <= 0;
            accumulator <= 0;
        end else begin
            case (state)
                IDLE: begin
                    if (start) begin
                        j <= 0;
                        done <= 0;
                        accumulator <= 0;
                    end
                end
                RUNNING: begin
                    if (j < NH) begin
                        if (h_k) begin
                            accumulator <= accumulator + w_data;
                        end
                        j <= j + 1;
```

```
                    end
                    if (j == NH - 1) begin
                        done <= 1;
                    end
                end
                DONE: begin
                    done <= 1;
                end
            endcase
        end
    end

    // Output assignment
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
            accumulated_sums <= 0;
        end else if (state == DONE) begin
            accumulated_sums <= accumulator;
        end
    end
endmodule

// Bias Adder Module
module bias_adder #(
    parameter NV = 16,
    parameter N_IN = 32,    // Bit-width of MAC accumulator output
    parameter N_BIAS = 8,   // Bit-width of bias values
    parameter N_OUT = 32    // Output bit-width
)(
    input wire clk,
    input wire reset_n,
    input wire enable,
    input wire signed [N_IN-1:0] mac_sums [0:NV-1],
    input wire signed [N_BIAS-1:0] bias [0:NV-1],
    output reg signed [N_OUT-1:0] outputs [0:NV-1],
    output reg done
);
    // State definitions
    typedef enum logic [1:0] {
        IDLE = 2'b00,
        ADD  = 2'b01,
        DONE = 2'b10
    } state_t;

    state_t state, next_state;

    // State Register
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
```

```
            state <= IDLE;
        end else begin
            state <= next_state;
        end
    end

    // Next State Logic
    always @(*) begin
        case (state)
            IDLE: next_state = enable ? ADD : IDLE;
            ADD:  next_state = DONE;
            DONE: next_state = IDLE;
            default: next_state = IDLE;
        endcase
    end

    // Bias Addition Logic
    integer i;
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
            for (i = 0; i < NV; i = i + 1) begin
                outputs[i] <= 0;
            end
            done <= 0;
        end else begin
            case (state)
                IDLE: done <= 0;
                ADD: begin
                    for (i = 0; i < NV; i = i + 1) begin
                        // Sign extend bias to match MAC sum width
                        outputs[i] <= mac_sums[i] +
{{(N_IN-N_BIAS){bias[i][N_BIAS-1]}}, bias[i]};
                    end
                    done <= 1;
                end
                DONE: done <= 0;
            endcase
        end
    end
endmodule

// Sigmoid LUT Module
module sigmoid_lut #(
    parameter LUT_SIZE = 256,
    parameter IN_WIDTH = 8,
    parameter OUT_WIDTH = 16
)(
    input wire signed [IN_WIDTH-1:0] x_input,
    output reg [OUT_WIDTH-1:0] y_output
```

```
);
    wire [7:0] lut_addr = x_input + 8'd128;

    always @(*) begin
        case (lut_addr)
            // Example entries shown - full implementation includes all 256
entries
            8'd0:   y_output = 16'd22;    // sigmoid(-8.0000) = 0.000335
            8'd1:   y_output = 16'd23;    // sigmoid(-7.9375) = 0.000357
            8'd2:   y_output = 16'd25;    // sigmoid(-7.8750) = 0.000380
            // [Additional LUT values would be included here]
            8'd253: y_output = 16'd65508; // sigmoid(7.8125) = 0.999596
            8'd254: y_output = 16'd65510; // sigmoid(7.8750) = 0.999620
            8'd255: y_output = 16'd65512; // sigmoid(7.9375) = 0.999643
            default: y_output = 16'd0;
        endcase
    end
endmodule

// Value Clamping Module
module clamp_mapper #(
    parameter INPUT_WIDTH = 32,
    parameter OUTPUT_WIDTH = 8
)(
    input wire signed [INPUT_WIDTH-1:0] in_data,
    output wire signed [OUTPUT_WIDTH-1:0] out_data
);
    assign out_data = (in_data > 127) ? 8'sb01111111 :
                      (in_data < -128) ? 8'sb10000000 :
                      in_data[7:0];
endmodule

// Random Number Generator
module rng (
    input wire clk,
    input wire reset_n,
    input wire load_new,
    input wire [15:0] seed,
    output reg [15:0] rand_num
);
    reg [15:0] lfsr;
    wire feedback = lfsr[15] ^ lfsr[13] ^ lfsr[12] ^ lfsr[10];
    wire [15:0] init_value = {seed[3:0], seed[7:4], seed[11:8], seed[15:12]};
    wire [15:0] mixed_seed = init_value ^ {init_value[7:0], init_value[15:8]};

    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
            lfsr <= mixed_seed ^ 16'hACE1;
            rand_num <= mixed_seed ^ 16'h1234;
```

```
        end else if (load_new) begin
            lfsr <= {lfsr[14:0], feedback};
            rand_num <= {lfsr[14:0], feedback};
        end
    end
endmodule

// Comparator Module
module comparator (
    input wire [15:0] sigmoid_val,
    input wire [15:0] rand_val,
    output wire out_bit
);
    assign out_bit = (sigmoid_val > rand_val);
endmodule

//------------------------------------------------------------------------------
--
// Implementation Notes:
// 1. All modules use synchronous reset (active low)
// 2. Fixed-point format allows range [-8.0 to +7.9375] with 0.0625 precision
// 3. Clock frequency target of 800MHz requires careful pipelining
// 4. Memory initialization values should be customized for specific
applications
// 5. Sigmoid LUT values should be generated using high-precision calculations
//------------------------------------------------------------------------------
--
```

Python Test Code for Verification

```python
import numpy as np
import math

# Input values from your results
inputs = [
   0.3750,    # Row 0
   -1.3750,   # Row 1
   0.5000,    # Row 2
   -5.6875,   # Row 3
   -4.3125,   # Row 4
   -15.2500,  # Row 5
   0.7500,    # Row 6
   -10.7500,  # Row 7
   0.8750,    # Row 8
   9.7500,    # Row 9
```

```
    -8.8125,    # Row 10
    -12.9375,   # Row 11
    -12.1250,   # Row 12
    -1.5000,    # Row 13
    -6.9375,    # Row 14
    -1.2500     # Row 15
]

def piecewise_sigmoid(x):
    """Implements the piecewise linear approximation of sigmoid"""
    if x <= -4.0:
        return 0.0
    elif x >= 4.0:
        return 1.0
    else:
        # Linear approximation: y = 0.5 + 0.125x
        return 0.5 + 0.125 * x

def true_sigmoid(x):
    """Calculates the true sigmoid value"""
    return 1.0 / (1.0 + math.exp(-x))

def to_fixed_point(x):
    """Converts decimal to 1-3-4 fixed point format"""
    # Multiply by 16 (2^4) to account for 4 fractional bits
    fixed = int(round(x * 16))
    # Ensure it fits in 8 bits (1-3-4 format)
    if fixed > 127:
        fixed = 127
    elif fixed < -128:
        fixed = -128
    return fixed

def generate_lut():
    """Generates a 256-entry LUT for the sigmoid function"""
    lut = []
    for i in range(256):
        # Convert index to signed fixed-point value (-128 to 127)
        fixed = i - 128
        x = fixed / 16.0
```

```
        lut_value = true_sigmoid(x)
        lut.append(lut_value)
    return lut

# Generate the LUT
lut = generate_lut()

print("\nSigmoid Function Expected Values:")
print("-" * 100)
print("Row    Input      Piecewise    True         Fixed Point    Binary
LUT Sigmoid")
print("       Value      Sigmoid      Sigmoid      (1-3-4)          (8-bit)")
print("-" * 100)

for i, x in enumerate(inputs):
    piecewise = piecewise_sigmoid(x)
    true_val = true_sigmoid(x)
    fixed = to_fixed_point(piecewise)

    # Convert to binary, handling negative numbers
    if fixed < 0:
        binary = format(fixed & 0xff, '08b')  # Two's complement for
negative numbers
    else:
        binary = format(fixed, '08b').zfill(8)

    # Retrieve LUT value
    lut_index = fixed + 128  # Map fixed-point value to LUT index (0-255)
    lut_value = lut[lut_index]

    print(f"{i:<7} {x:8.4f}  {piecewise:8.4f}    {true_val:8.4f}
{fixed:4d}          {binary}       {lut_value:.4f}")

print("-" * 100)
```

Test Bench for Verification:

```
`timescale 1ns/1ps

// ----------------------------------------
// Testbench for Complete System with RNG and Comparators
// ----------------------------------------
```

```
module complete_system_tb;
    parameter NV = 16;  // Number of neurons
    parameter NH = 16;  // Number of inputs per neuron
    parameter N  = 8;   // Bit width of each weight
    parameter real CLK_PERIOD = 1.25; // Clock period in ns for 800 MHz

    reg clk;
    reg reset_n;
    reg start;
    wire system_done;
    wire signed [31:0] final_outputs [0:NV-1];
    wire signed [31:0] mac_outputs_out [0:NV-1];
    wire signed [N-1:0] bias_data_out [0:NV-1];
    wire [15:0] sigmoid_outputs_out [0:NV-1];
    wire [15:0] rng_outputs_out [0:NV-1];
    wire [NV-1:0] comparator_outputs_out;
    wire [2:0] state_display;

    // Clock generation
    initial begin
        clk = 0;
        forever #(CLK_PERIOD/2) clk = ~clk;  // Toggle clock every half period
    end

    // Instantiate DUT (Device Under Test)
    complete_system #(
        .NV(NV),
        .NH(NH),
        .N(N)
    ) dut (
        .clk(clk),
        .reset_n(reset_n),
        .start(start),
        .system_done(system_done),
        .final_outputs(final_outputs),
        .mac_outputs_out(mac_outputs_out),
        .bias_data_out(bias_data_out),
        .sigmoid_outputs_out(sigmoid_outputs_out),
        .rng_outputs_out(rng_outputs_out),
        .comparator_outputs_out(comparator_outputs_out),
        .state_display(state_display)
    );

    // Function to convert fixed point to real
    function real fixed_to_real;
        input signed [31:0] fixed_point;
        begin
            fixed_to_real = fixed_point / 16.0; // Assuming 4 fractional bits
        end
    endfunction

    // Function to convert Sigmoid fixed point to real
    function real sigmoid_fixed_to_real;
        input [15:0] fixed_point;
        begin
            sigmoid_fixed_to_real = fixed_point / 65535.0; // Assuming 16 fractional bits
        end
    endfunction

    // Function to convert RNG fixed point to real
    function real rng_fixed_to_real;
        input [15:0] fixed_point;
```

```
        begin
            rng_fixed_to_real = fixed_point / 65535.0; // Assuming 16 fractional bits
        end
    endfunction

    // Test stimulus
    initial begin
        // Initialize control signals
        reset_n = 0;
        start = 0;

        // Apply reset
        #20;
        reset_n = 1;
        #40; // Wait additional time to allow H Buffer initialization

        // Start processing
        $display("\nStarting system processing...");
        start = 1;
        #10;
        start = 0;

        // Wait for completion
        @(posedge system_done);
        #20;

        // Display final results
        $display("\nFinal System Results:");

$display("-------------------------------------------------------------------------------------------
-----------------------------------------------------------");
        $display("Row | Output(int) | Output(decimal) | Sigmoid(int) | Sigmoid(decimal) |
RNG(int) | RNG(decimal) | Comparator | Final Bit");

$display("-------------------------------------------------------------------------------------------
-----------------------------------------------------------");
        for (integer i = 0; i < NV; i = i + 1) begin
            $display("%2d  | %10d | %16.4f | %11d | %17.6f | %8d | %14.6f | %10b | %11b",
                    i,
                    final_outputs[i],
                    fixed_to_real(final_outputs[i]),
                    sigmoid_outputs_out[i],
                    sigmoid_fixed_to_real(sigmoid_outputs_out[i]),
                    rng_outputs_out[i],
                    rng_fixed_to_real(rng_outputs_out[i]),
                    comparator_outputs_out[i],
                    comparator_outputs_out[i]
            );
        end

$display("-------------------------------------------------------------------------------------------
-----------------------------------------------------------\n");

        // Display MAC outputs and bias values
        $display("\nIntermediate Results:");

$display("-------------------------------------------------------------------------------------------
---------------------------------");
        $display("Row | MAC(int) | MAC(decimal) | Bias(int) | Bias(decimal) | Sigmoid(int) |
Sigmoid(decimal) | RNG(int) | Comparator");
```

```
$display("-------------------------------------------------------------------------------------------
--------------------------------");
        for (integer i = 0; i < NV; i = i + 1) begin
            $display("%2d  | %8d | %13.4f | %8d | %13.4f | %11d | %17.6f | %8d | %10b",
                    i,
                    mac_outputs_out[i],
                    fixed_to_real(mac_outputs_out[i]),
                    bias_data_out[i],
                    bias_data_out[i] / 16.0,
                    sigmoid_outputs_out[i],
                    sigmoid_fixed_to_real(sigmoid_outputs_out[i]),
                    rng_outputs_out[i],
                    comparator_outputs_out[i]
            );
        end

$display("-------------------------------------------------------------------------------------------
--------------------------------\n");

        #100;
        $finish;
    end

    // Signal monitoring
    always @(posedge clk) begin
        $display("Time=%0t | reset_n=%0b | start=%0b | state=%3b | done=%0b",
                 $time, reset_n, start, state_display, system_done);
    end
endmodule
```

Additional Test Bench for writing values generated using Python (Not using initialization)

```
# generate_testbench.py

NV = 16
NH = 16
N = 8

# Generate W_memory assignments
w_memory_assignments = ""
for row in range(NV):
   for col in range(NH):
       # Example: Assign row * col as the data
       value = row * col
       # Ensure the value fits in N bits (8 bits)
       if value < 0:
           value = (1 << N) + value  # Two's complement for negative
numbers
       elif value >= (1 << (N - 1)):
```

```
            value = (1 << (N - 1)) - 1  # Saturate to maximum positive
value
        w_memory_assignments += f"                    write_col_w = {col};
write_data_w = 8'd{value};\n"
        w_memory_assignments += "                    @(posedge clk);\n"

# Generate B_buffer assignments
b_buffer_assignments = ""
for addr in range(NV):
    if addr < NV//2:
        bias = 5  # +0.3125 represented as 8'd5
    else:
        bias = -5  # -0.3125 represented as -8'd5
    # Ensure the bias fits in N bits (8 bits)
    if bias < 0:
        bias = (1 << N) + bias  # Two's complement for negative numbers
    elif bias >= (1 << (N - 1)):
        bias = (1 << (N - 1)) - 1  # Saturate to maximum positive value
    b_buffer_assignments += f"                    write_addr_b = {addr};
write_data_b = 8'd{bias};\n"
    b_buffer_assignments += "                    @(posedge clk);\n"

# Combine all parts into the testbench content
testbench_content = f"""`timescale 1ns/1ps
// Auto-generated Test Bench with Manual Assignments
module complete_system_tb;
    parameter NV = 16;
    parameter NH = 16;
    parameter N = 8;
    parameter CLK_PERIOD = 10;

    reg clk;
    reg reset_n;
    reg start;
    // Write interface signals for W_memory
    reg write_enable_w;
    reg [$clog2(NV)-1:0] write_row_w;
    reg [$clog2(NH)-1:0] write_col_w;
    reg signed [N-1:0] write_data_w;
    // Write interface signals for H_buffer
```

```
reg write_enable_h;
reg [NV-1:0] write_data_h;
// Write interface signals for B_buffer
reg write_enable_b;
reg [$clog2(NV)-1:0] write_addr_b;
reg signed [N-1:0] write_data_b;
wire system_done;
wire signed [31:0] final_outputs [0:NV-1];
reg [2:0] state_display;  // For monitoring state

// Clock generation
initial begin
    clk = 0;
    forever #(CLK_PERIOD/2) clk = ~clk;
end

// Instantiate DUT
complete_system #(
    .NV(NV),
    .NH(NH),
    .N(N)
) dut (
    .clk(clk),
    .reset_n(reset_n),
    .start(start),
    // Connect write interface signals for W_memory
    .write_enable_w(write_enable_w),
    .write_row_w(write_row_w),
    .write_col_w(write_col_w),
    .write_data_w(write_data_w),
    // Connect write interface signals for H_buffer
    .write_enable_h(write_enable_h),
    .write_data_h(write_data_h),
    // Connect write interface signals for B_buffer
    .write_enable_b(write_enable_b),
    .write_addr_b(write_addr_b),
    .write_data_b(write_data_b),
    .system_done(system_done),
    .final_outputs(final_outputs)
);
```

```
    // Function to convert fixed point to real
    function real fixed_to_real;
        input signed [31:0] fixed_point;
        begin
            fixed_to_real = fixed_point / 16.0; // Divide by 2^4 since we
have 4 fractional bits
        end
    endfunction

    // State monitoring
    always @(posedge clk) begin
        state_display <= dut.state; // Ensure 'state' is exposed in DUT
    end

    // Test stimulus
    initial begin
        // Initialize signals
        reset_n = 0;
        start = 0;
        write_enable_w = 0;
        write_row_w = 0;
        write_col_w = 0;
        write_data_w = 0;
        write_enable_h = 0;
        write_data_h = 0;
        write_enable_b = 0;
        write_addr_b = 0;
        write_data_b = 0;

        // Apply reset
        #100;
        reset_n = 1;
        #20;

        // Begin writing to W_memory
        write_enable_w = 1;
        for (integer row = 0; row < NV; row = row + 1) begin
            write_row_w = row;
{w_memory_assignments}        end
```

```
        write_enable_w = 0; // Disable writing

        // Write to H_buffer
        #10; // Small delay before writing to H_buffer
        write_enable_h = 1;
        // Assign a 16-bit value to H_buffer
        write_data_h = 16'hAAAA; // 1010101010101010
        @(posedge clk);
        write_enable_h = 0; // Disable writing

        // Write to B_buffer
        #10; // Small delay before writing to B_buffer
        write_enable_b = 1;
{b_buffer_assignments}        write_enable_b = 0; // Disable writing

        // After writing all desired values, start the processing
        #10; // Small delay to ensure all writes are settled
        $display("\\nStarting system processing...");
        start = 1;
        @(posedge clk);
        start = 0;

        // Wait for completion
        @(posedge system_done);
        #20;

        // Display final results
        $display("\\nFinal System Results:");
        $display("----------------------------------------");
        $display("Row    Output(int)    Output(decimal)");
        $display("----------------------------------------");
        for (integer i = 0; i < NV; i = i + 1) begin
            $display("%2d    %10d    %13.4f",
                     i,
                     final_outputs[i],
                     fixed_to_real(final_outputs[i]));
        end
        $display("----------------------------------------\\n");

        // Display MAC outputs and bias values
```

```
        $display("\\nIntermediate Results:");
        $display("----------------------------------------");
        for (integer i = 0; i < NV; i = i + 1) begin
            $display("Row %2d: MAC = %10d (%13.4f), Bias = %4d (%8.4f)",
                     i,
                     dut.accumulated_sums[i], // Assuming 'accumulated_sums'
is exposed
                     fixed_to_real(dut.accumulated_sums[i]),
                     dut.buffer[i], // Assuming 'buffer' is exposed
                     dut.buffer[i] / 16.0);
        end
        $display("----------------------------------------\\n");

        #100;
        $finish;
    end

    // Signal monitoring
    always @(posedge clk) begin
        $display("Time=%0t reset_n=%0b start=%0b state=%3b done=%0b",
                 $time, reset_n, start, state_display, system_done);
    end
endmodule
"""

# Save the generated testbench to a file
with open("testbench_generated.sv", "w") as f:
    f.write(testbench_content)

print("Testbench generation complete. Check 'testbench_generated.sv' for
the output.")
```