8 Bit SRAM Mixed Signal Design using eSim with SKY130 PDK and NgVeri

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Abstract—**Memory cells have become a subject of research to meet the demands for future digital electronics and communication systems. One of the memory component is SRAM (Static Random-Access Memory) and is used in various VLSI chips due to its unique capability to retain data. SRAM is a major data storage device due to its large storage density, less time to access and consumes less power. It does not require refreshing periodically which makes it the most popular memory cell among VLSI designers.**

Here, going to present work on 6T SRAM cell circuit based on MOSFET is designed for 8-Bit storage with the help of decoder. The design is synthesized using the eSim software tool with SKY130 PDK and transient analysis of 8 bit SRAM is performed.

Keyword: 6T RAM cell, Decoder, MOSFET, SRAM

[1] CIRCUIT DETAILS

Here, SRAM cell is designed with two inverters, which are cross-linked like as latch form. This latch is made connection to two bit line along with two transistors M1 and M2 as shown n Fig. 1. Now both transistors are capable to alter their modes (open or close) under control of word line, and this entire process is controlled by address decoder. When word line goes to ground level then both transistors get turned off, and latch starts to retain own state.

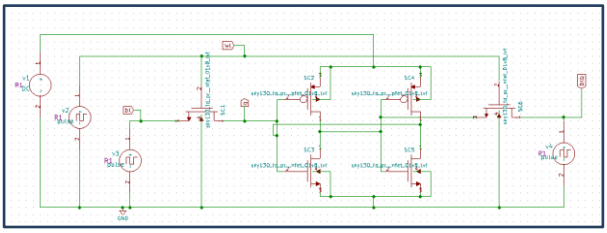

Fig. 1: 6T SRAM

[2] 1 BIT SRAM

The basic block diagram of 1 bit STRAM comprised of 6T RAM cell, writer circuit, pre-charge circuit & sense amplifier as shown in Fig. 2.

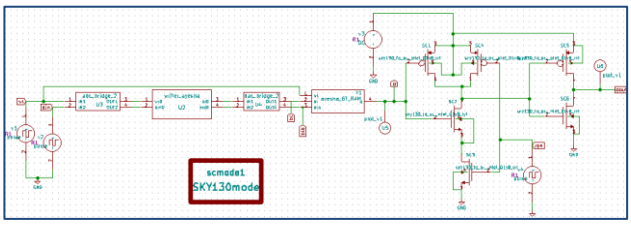

Fig. 2: 1 bit RAM cell

[3] 8 BIT SRAM DESIGN SCHEMATIC

For 8 bit SRAM, we use here 3×8 decoder connected with 8 RAM's for getting 8 bit output as shown in Fig. 3. Output of the decoder specifies address for the SRAM cells, where the data needs to be written or read from.

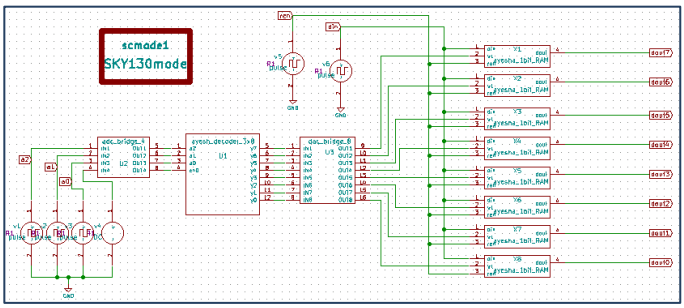

Fig. 3: 8 bit SRAM schematic on eSim

[4] SIMULATION

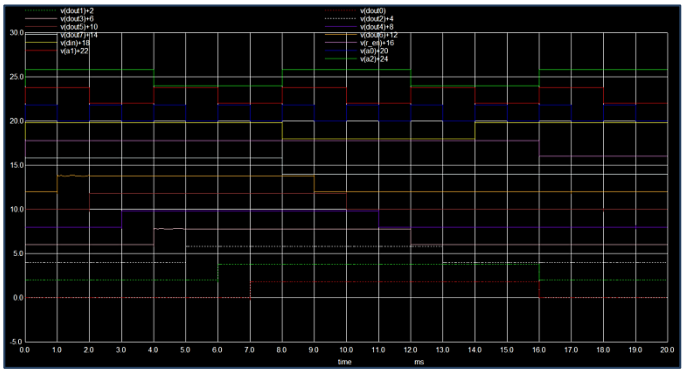

Fig. 4: Transient Analysis of 8 bit SRAM

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