

# Design of Negative edge triggered FF using Master Slave latch using transmission gates

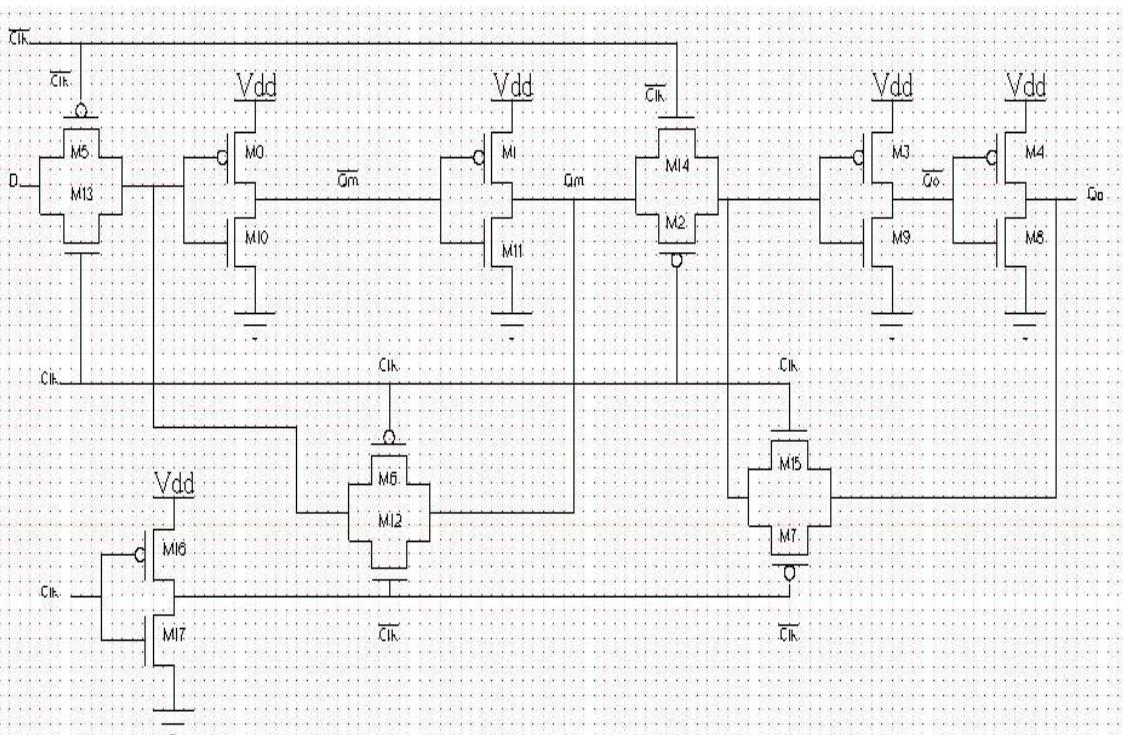
---



INDRAPRASTHA INSTITUTE *of*  
INFORMATION TECHNOLOGY **DELHI**



# Schematic + Sizing



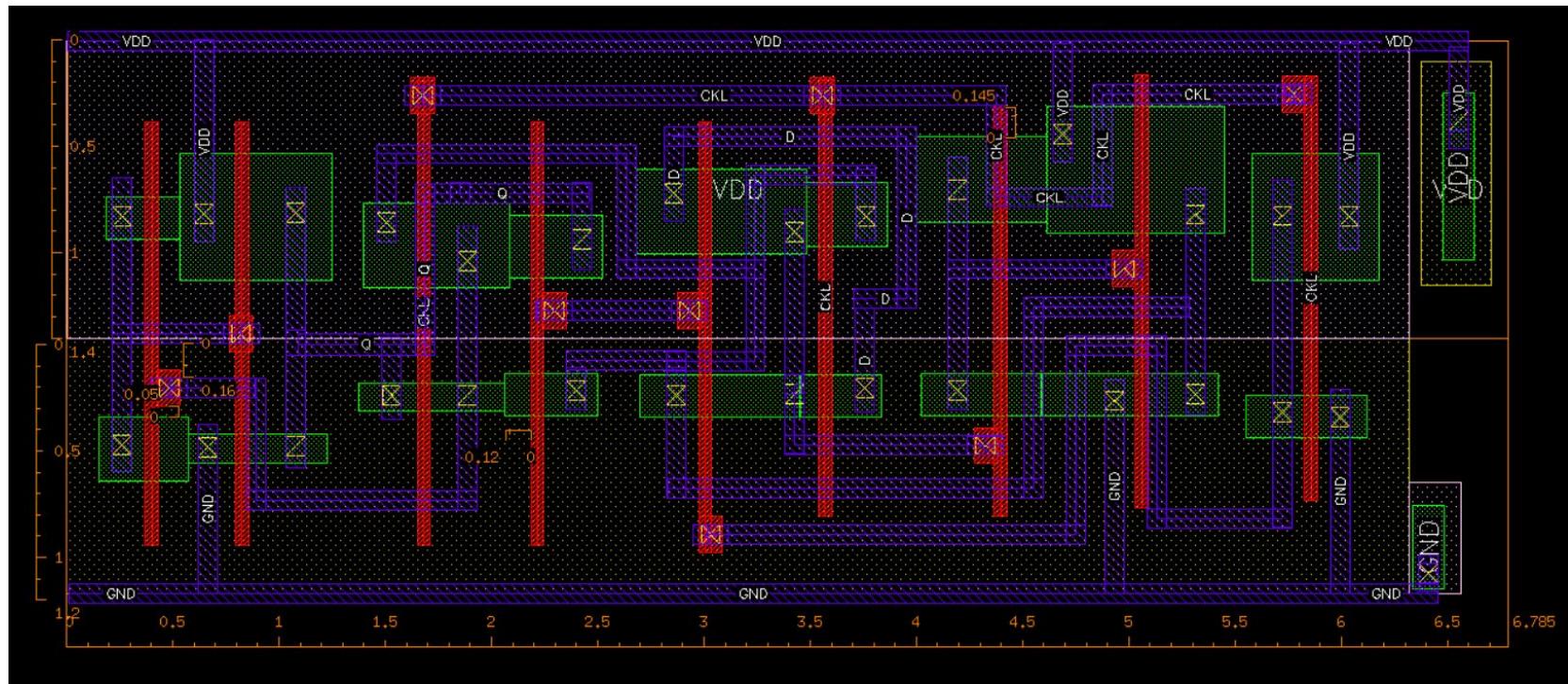
Transistor Type	Width (W)	Transistor Names
PMOS	0.6 $\mu\text{m}$	M4
	0.54 $\mu\text{m}$	XM16, XM3, XM2, XM1
	0.27 $\mu\text{m}$	XMO
	0.135 $\mu\text{m}$	XM7, XM6, XM5
NMOS	0.3 $\mu\text{m}$	M8
	0.27 $\mu\text{m}$	XM14, XM9, XM11, XM17
	0.135 $\mu\text{m}$	XM15, XM13, XM12, XM10

# Stimuli For Verification & Verification Plan



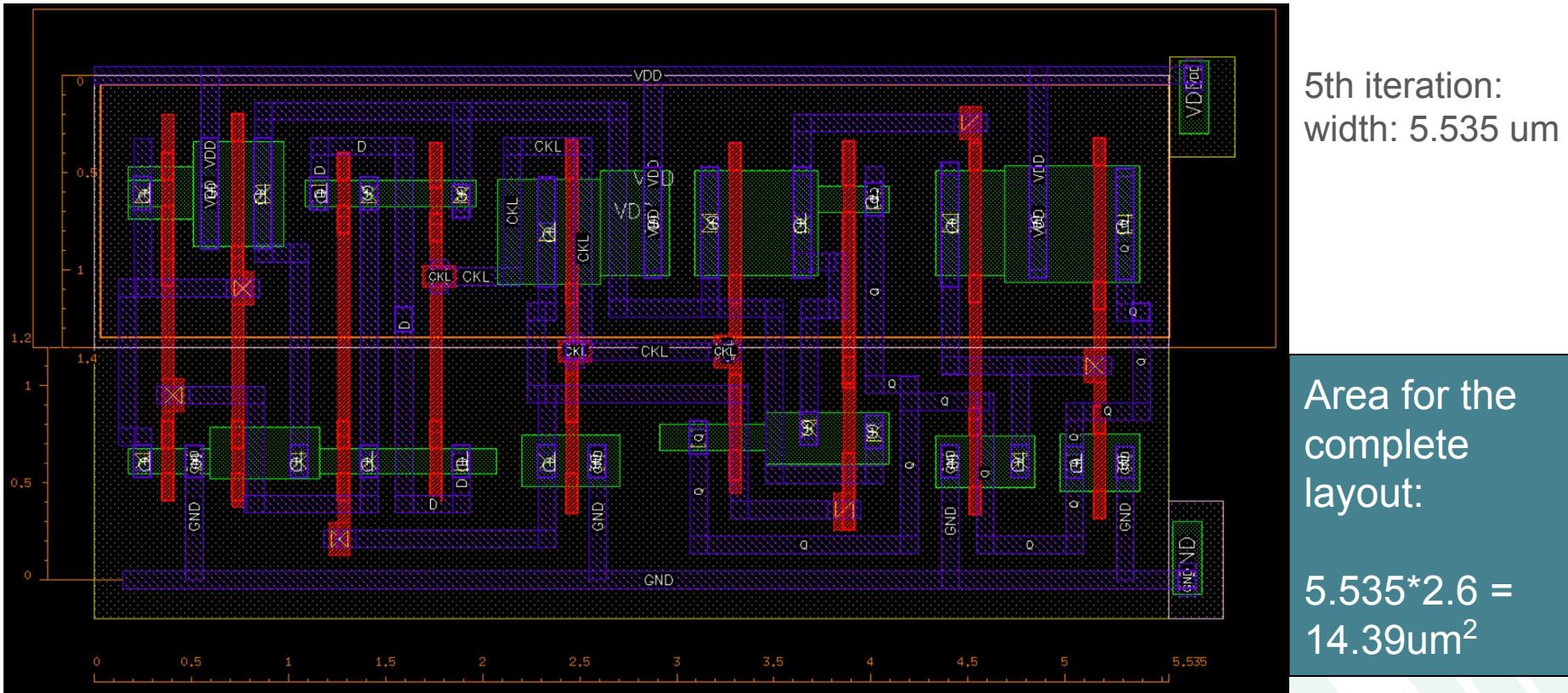
Parameters	Pre-Conditions	Stimuli
Clock to Q delay	Data is stable, D=1, clock is high	Apply Clock=0
Setup Time	Clock is high, about to transition low.	Change the Data input at a time <i>before</i> the clock edge. Time will be measured when Clk-to-Q delay found around 5%
Hold Time	Clock has just transitioned from high to low.	Change the Data input at a time <i>after</i> the clock edge. Time will be measured when Clk-to-Q delay found around 5%

# Layouts



1st iteration: width: 6.75um  
Height: 13 Tracks

# Layouts



# DRC/LVS Reports



Silvaco - RVE v2013.1.3421 : svbh NEFF\_5\_NOV

File View Highlight Tools Window Setup

Show Unresolved NEFF\_5\_NOV, 0 Results (in 0 of 1583 Checks)

Check / Cell / Results

Navigator

Results

- Extraction Results
- Companion Results

ERC

- ERC Results
- ERC Summary

User Files

- LAYOUT\_DSP

Reports

- Extraction Report
- LVS Report
- Separate Properties

Rules

- Rules File

View

- Info
- Finder
- Schematics

Setup

- Options

Calibre - RVE v2013.1.3421 : svbh NEFF\_5\_NOV

File View Highlight Tools Window Setup

Search

Navigator

Companion Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
NEFF_5_NOV	NEFF_5_NOV	11L, 11S	18L, 18S	SL, SS

Cell NEFF\_5\_NOV Summary (Clear)  
CELL COMPARISON RESULTS ( TOP LEVEL )

✓ CORRECT ✓

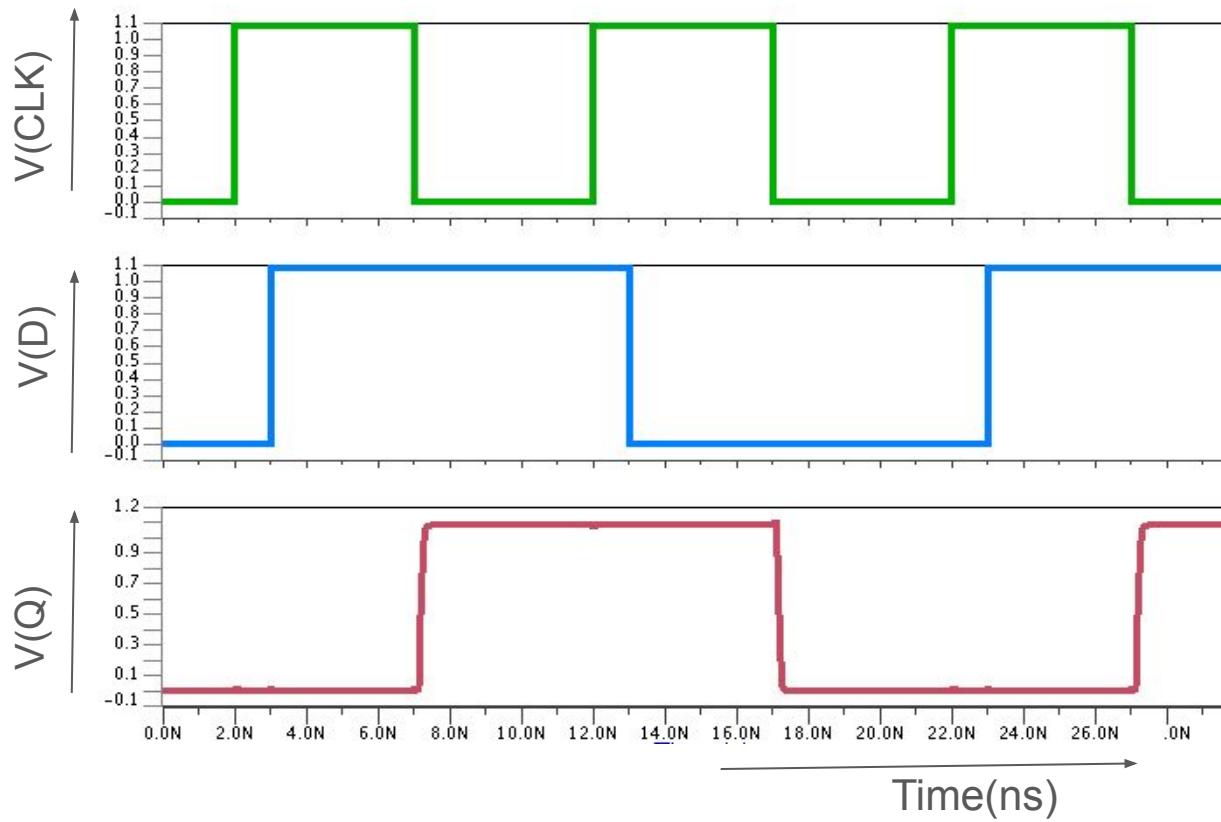
LAYOUT CELL NAME: NEFF\_5\_NOV  
SOURCE CELL NAME: NEFF\_5\_NOV

NUMBERS OF OBJECTS

	Layout	Source	Component	Type
Ports:	5	5		
Nets:	11	11		
Instances:	9	9	MN (4 pins)	
	9	9	MP (4 pins)	
Total Inst:	18	18		

INFORMATION AND WARNINGS

# Verification of Functionality of Design



# Pre and Post Layout Analysis



Parameters	PVT (worst case)	Pre lay	Post lay
Clock to Q delay	SS 1.08V 125°C	178ps	199ps
Setup Time	SS 1.08V 125°C	34ps	59ps
Hold Time	FF 1.32V -40°C	14ps	29ps
Dynamic Power	FF 1.32V -40°C	3.192uW	3.573uW
Leakage Power	FF 1.32V 125°C	0.016uW	0.037 uW

Setup Time and Hold Time estimated when CQ delay changes by 10%

# Monte Carlo Simulations Analysis



Parameters	Mean		Standard deviation	
	Pre	Post	Pre	Post
Clock to Q delay	175ps	189ps	3.85p	6.96p
Setup Time	31ps	49ps	3.23ps	9.56ps
Hold Time	13ps	25ps	1.21ps	4.45ps

# Conclusion



Power (uW)		Performance (ps)			Area(um <sup>2</sup> )
Dynamic P	Leakage P	Tsetup	Thold	Tcq	
3.573	0.037	59	34	199	14.39