# Design of Negative edge triggered FF using Master Slave latch using transmission gates

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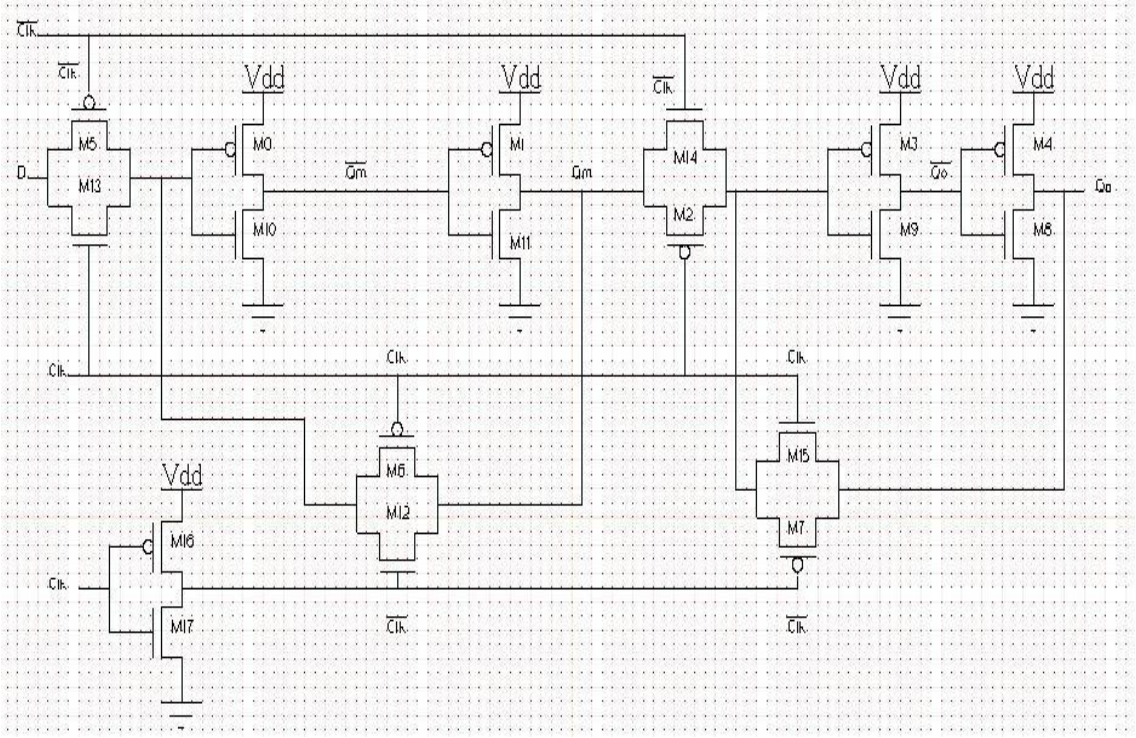
INFORMATION TECHNOLOGY **DELHI**

# Schematic + Sizing

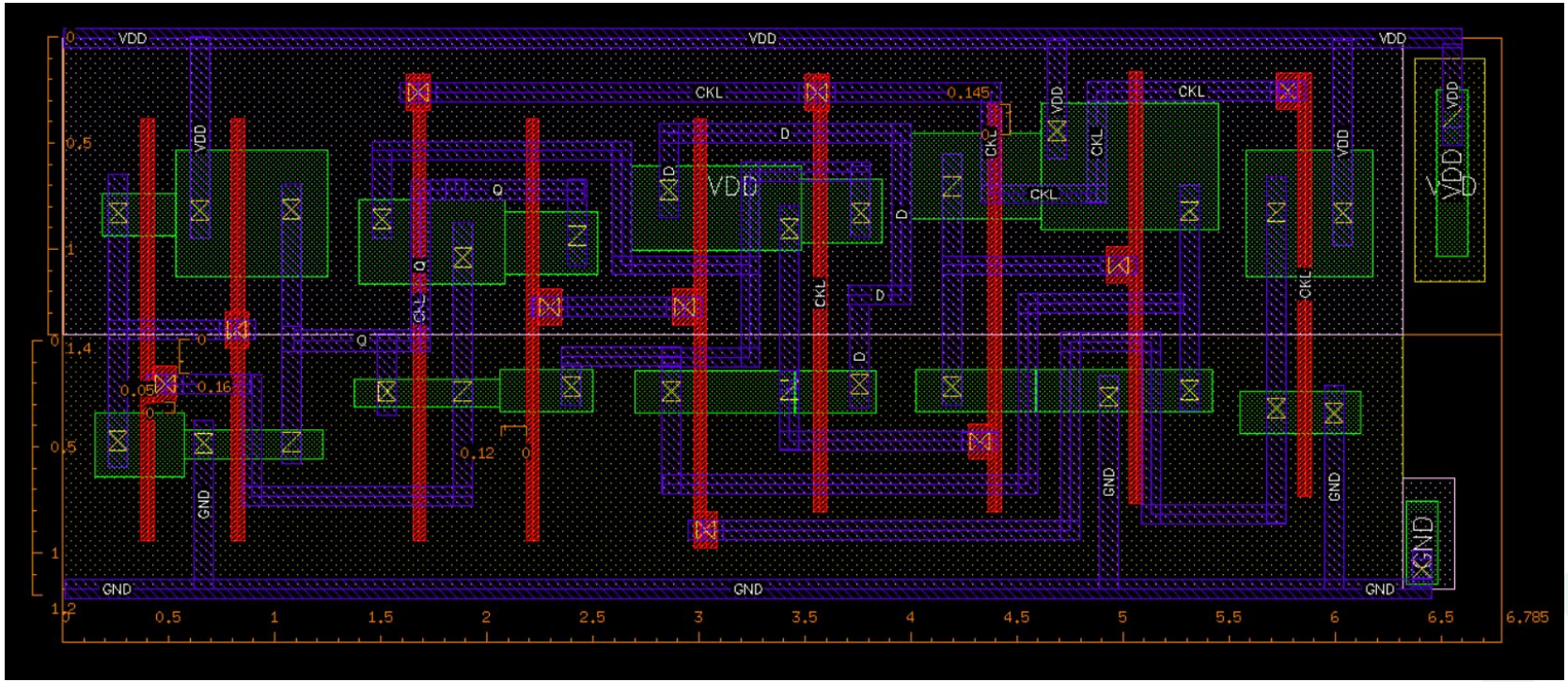



| Transistor Type | Width (W) | Transistor Names |
|---|---|---|
| PMOS | 0.6 µm | M4 |
| | 0.54 µm | XM16, XM3, XM2, XM1 |
| | 0.27 µm | XM0 |
| | 0.135 µm | XM7, XM6, XM5 |
| NMOS | 0.3 µm | M8 |
| | 0.27 µm | XM14, XM9, XM11, XM17 |
| | 0.135 µm | XM15, XM13, XM12, XM10 |

# Stimuli For Verification & Verification Plan

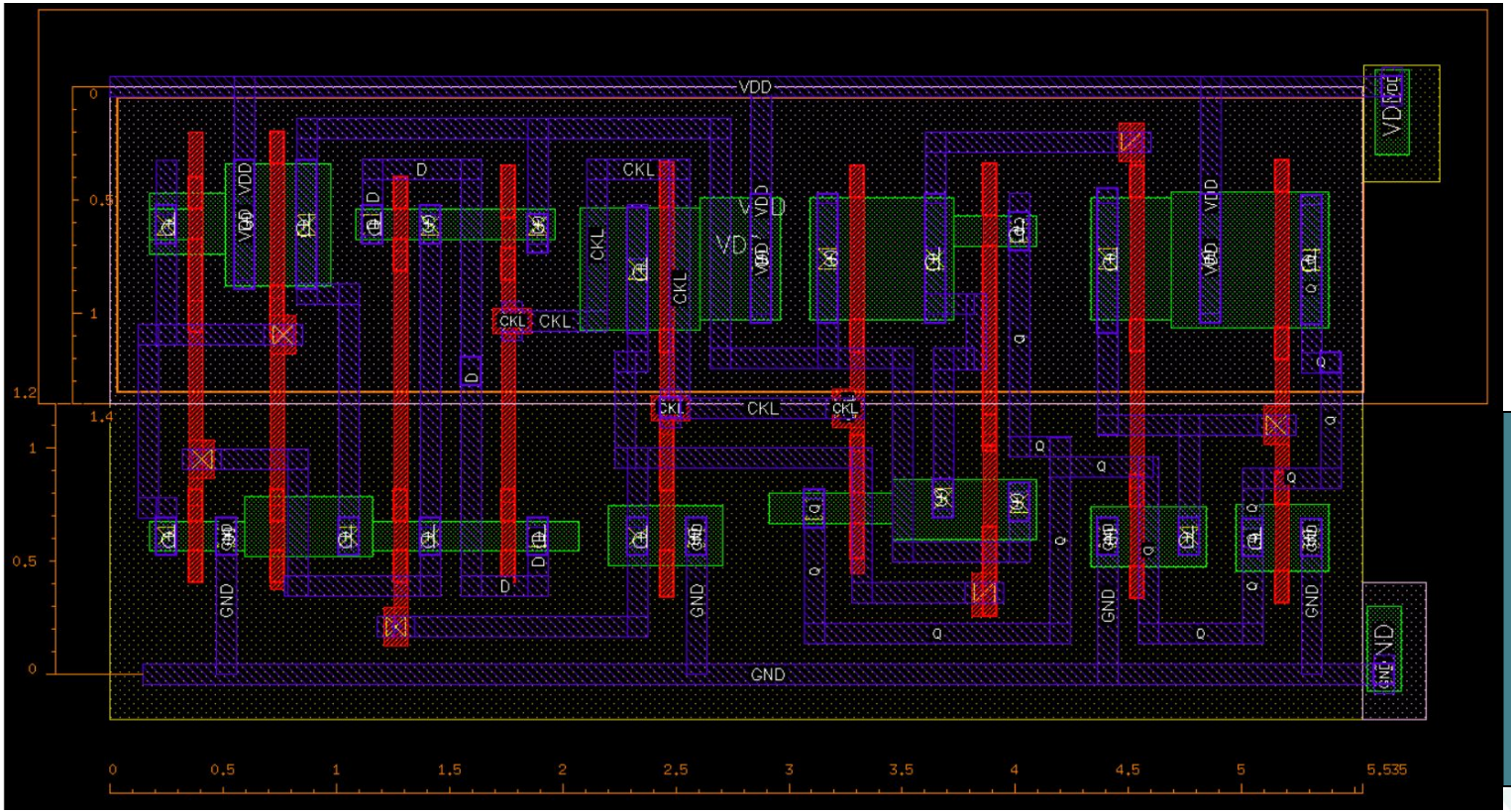
| Parameters | Pre-Conditions | Stimuli |
|---|---|---|
| Clock to Q delay | Data is stable, D=1, clock is high | Apply Clock=0 |
| Setup Time | Clock is high, about to transition low. | Change the Data input at a time *before* the clock edge. Time will be measured when Clk-to-Q delay found around 5% |
| Hold Time | Clock has just transitioned from high to low. | Change the Data input at a time *after* the clock edge. Time will be measured when Clk-to-Q delay found around 5% |

# Layouts




1st iteration: width: 6.75um
Height: 13 Tracks

# Layouts

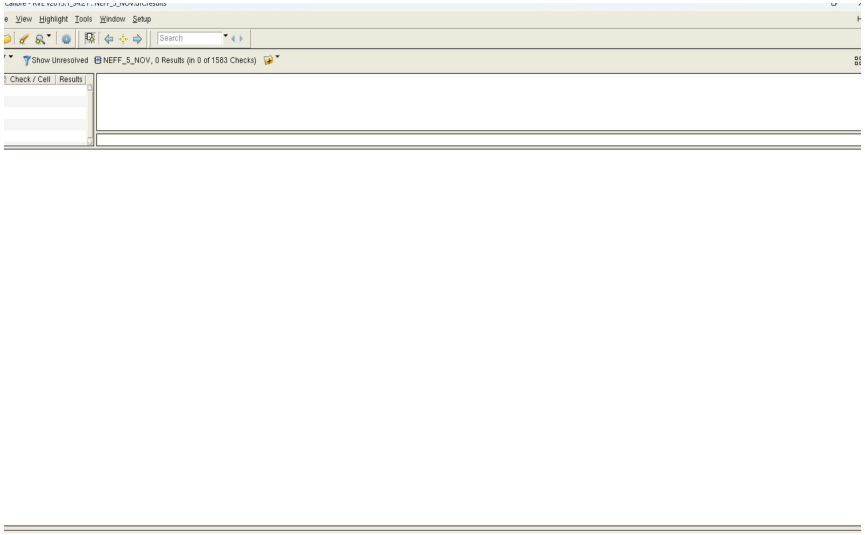


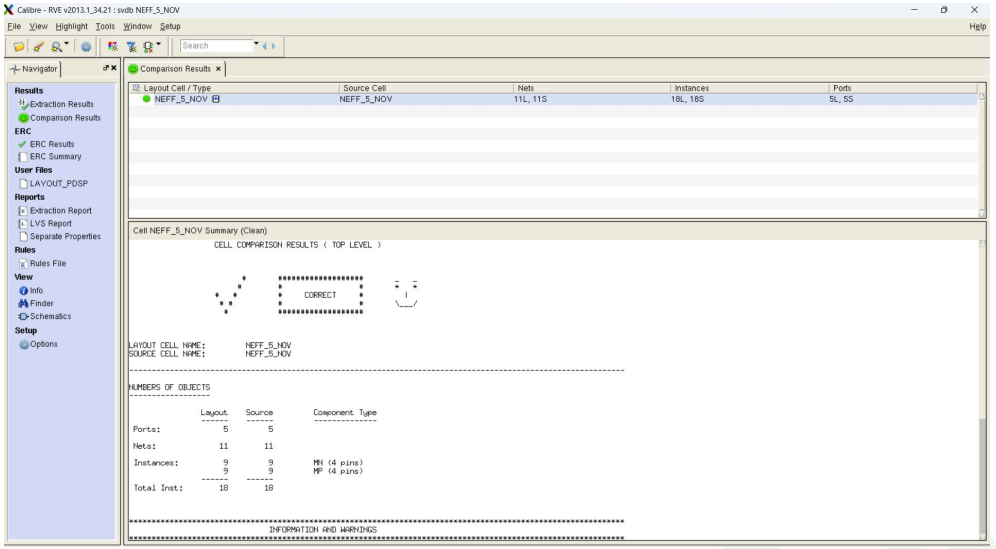

5th iteration:
width: 5.535 um

Area for the complete layout:

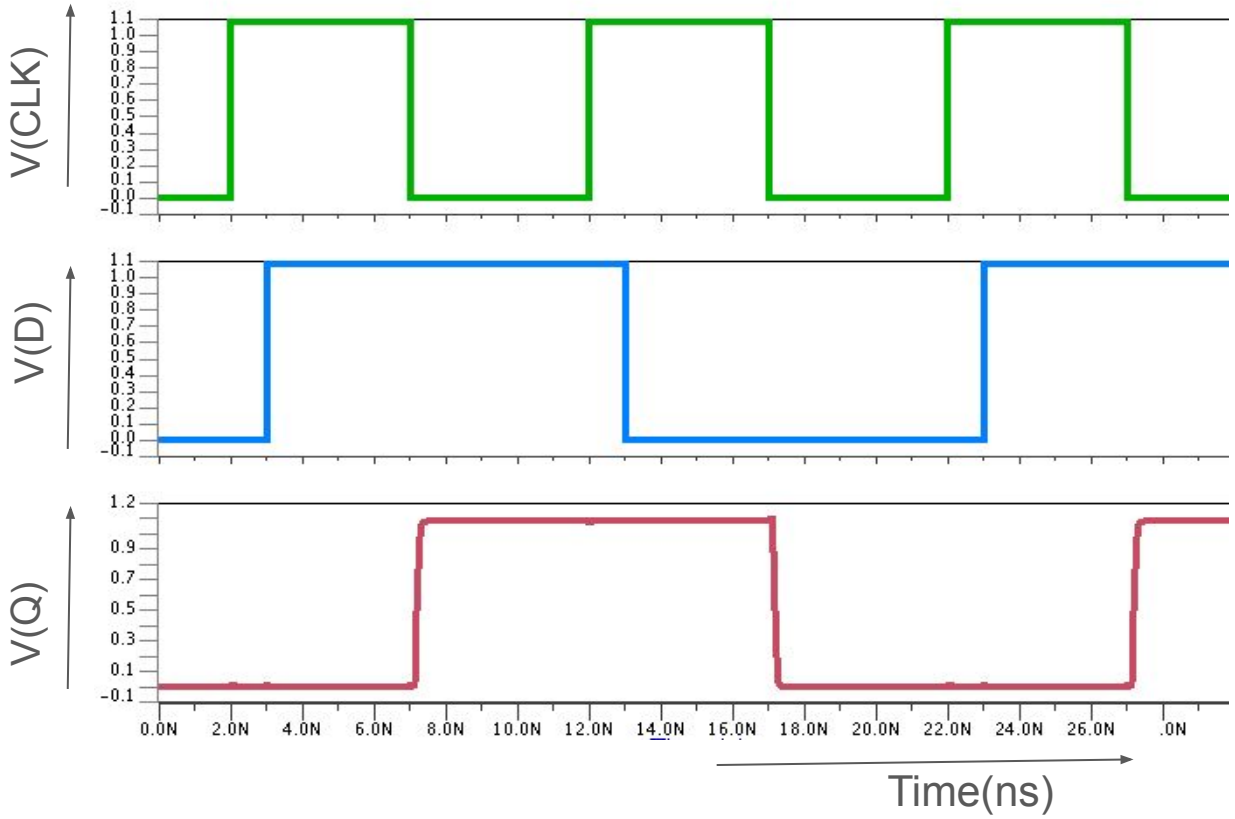
5.535*2.6 = 14.39um$^2$

# DRC/LVS Reports



# Verification of Functionality of Design



# Pre and Post Layout Analysis

| Parameters | PVT (worst case) | Pre lay | Post lay |
|---|---|---|---|
| Clock to Q delay | SS 1.08V 125°C | 178ps | 199ps |
| Setup Time | SS 1.08V 125°C | 34ps | 59ps |
| Hold Time | FF 1.32V -40°C | 14ps | 29ps |
| Dynamic Power | FF 1.32V -40°C | 3.192uW | 3.573uW |
| Leakage Power | FF 1.32V 125°C | 0.016uW | 0.037 uW |

Setup Time and Hold Time estimated when CQ delay changes by 10%

# Monte Carlo Simulations Analysis

| Parameters | Mean | | Standard deviation | |
|---|---|---|---|---|
| | Pre | Post | Pre | Post |
| Clock to Q delay | 175ps | 189ps | 3.85p | 6.96p |
| Setup Time | 31ps | 49ps | 3.23ps | 9.56ps |
| Hold Time | 13ps | 25ps | 1.21ps | 4.45ps |

# Conclusion

| Power (uW) | | Performance (ps) | | | Area($um^2$) |
|---|---|---|---|---|---|
| Dynamic P | Leakage P | Tsetup | Thold | Tcq | |
| 3.573 | 0.037 | 59 | 34 | 199 | 14.39 |