

IMAGE BY DR. E. SANCHEZ-SINENCIO.

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### Abstract

Demand for system-on-chip solutions has increased the interest in low drop-out (LDO) voltage regulators which do not require a bulky off-chip capacitor to achieve stability, also called capacitor-less LDO (CL-LDO) regulators. Several architectures have been proposed; however comparing these reported architectures proves difficult, as each has a distinct process technology and specifications. This paper compares CL-LDOs in a unified manner. We designed, fabricated, and tested five illustrative CL-LDO regulator topologies under common design conditions using  $0.6\mu\text{m}$  CMOS technology. We compare the architectures in terms of (1) line/load regulation, (2) power supply rejection, (3) line/load transient, (4) total on-chip compensation capacitance, (5) noise, and (6) quiescent power consumption. Insights on what optimal topology to choose to meet particular LDO specifications are provided.

# Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison

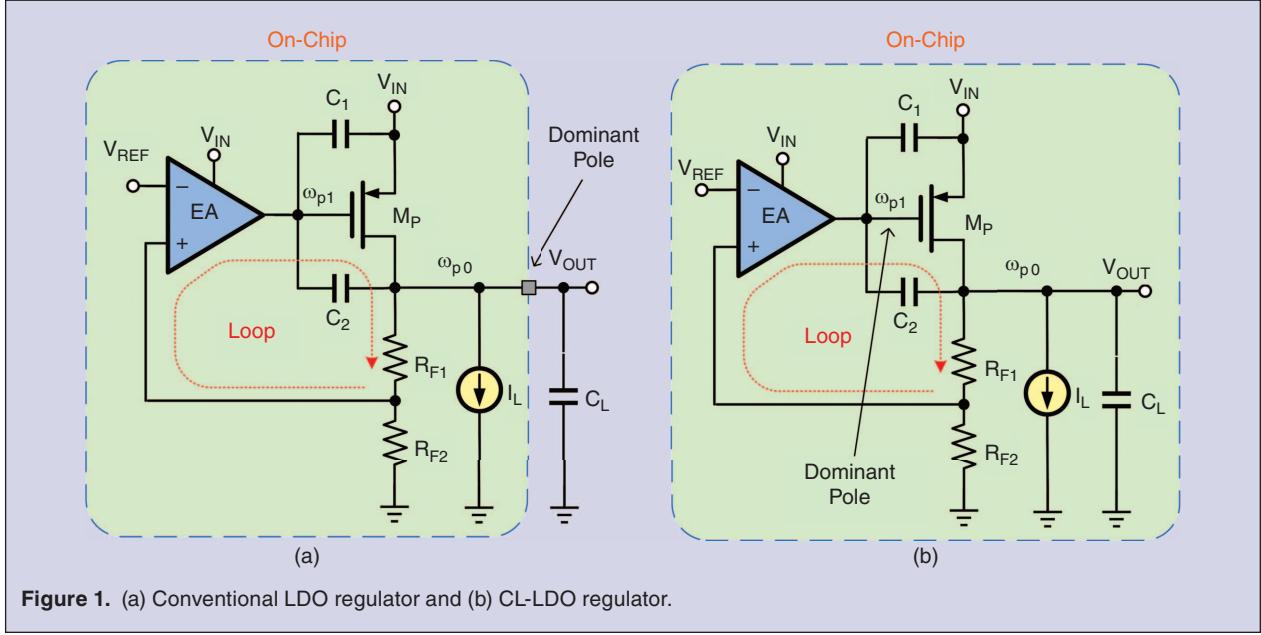
## I. Introduction

Low drop-out (LDO) voltage regulators are essential building blocks in power-management systems. Power-management systems for microprocessors and portable devices often use multiple LDO regulators

to provide a regulated supply voltage with minimal ripple to supply-noise-sensitive blocks. The conventional LDO regulator block diagram is shown in Fig. 1(a) and it consists of a pass transistor  $M_P$ , an error amplifier EA, a feedback network ( $R_{F1}$  and  $R_{F2}$ ), and a bulky off-chip capacitor  $C_L$ . Current source  $I_L$  represents the required current by the load. The off-chip capacitor is used to achieve stability and good transient response,

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**Figure 1.** (a) Conventional LDO regulator and (b) CL-LDO regulator.

and its value is often in the order of several micro-farads. However, this off-chip capacitor increases the total cost of the system and precludes the LDO regulator to be used in system-on-chip solutions. Hence, a LDO regulator that does not require an off-chip capacitor can significantly reduce the number of external components and PCB area, thereby reducing the total cost of the system. This type of LDO regulators are known as capacitor-less LDOs (CL-LDOs) in the literature and its block diagram is shown in Fig. 1(b). In Fig. 1(b),  $C_L$  models the parasitic capacitors and/or any integrated capacitor at the output node.  $C_L$  is typically in the order of pico-farads in CL-LDO regulators.

Previous works have been designed for different system requirements and implemented in different fabrication technologies. As a result, comparing their performance proves difficult. In this work, we designed, fabricated, and measured five different CL-LDO regulators in the same process ( $0.6\mu\text{m}$  CMOS) under common design specifications to facilitate comparison. Our remarks and observations are suitable for the chosen design constraints.

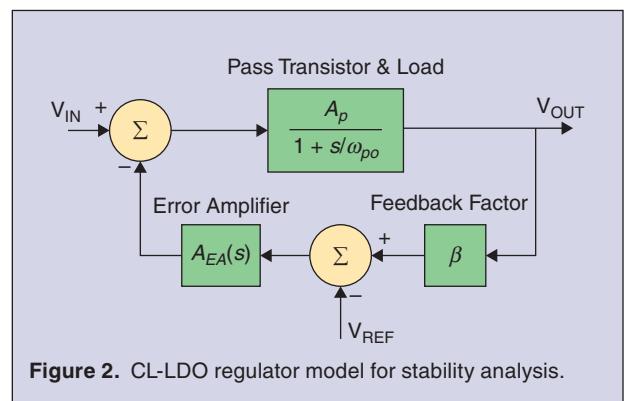
Section II discusses the design issues in CL-LDO regulators. Representative CL-LDO regulator topologies [1]–[5], [15]–[32] are presented in Sections III and IV. Remarks on CL-LDO regulator architectures and experimental results are presented in Section V. Conclusions are drawn in Section VI.

## II. Design Considerations

Key design considerations for CL-LDO regulators include: stability at very light loads (low  $I_L$ ), line/load regulation, line/load transient, and power supply rejection (PSR). Trade-offs between these parameters are often topology dependent. A brief introduction to these design considerations is introduced in this section.

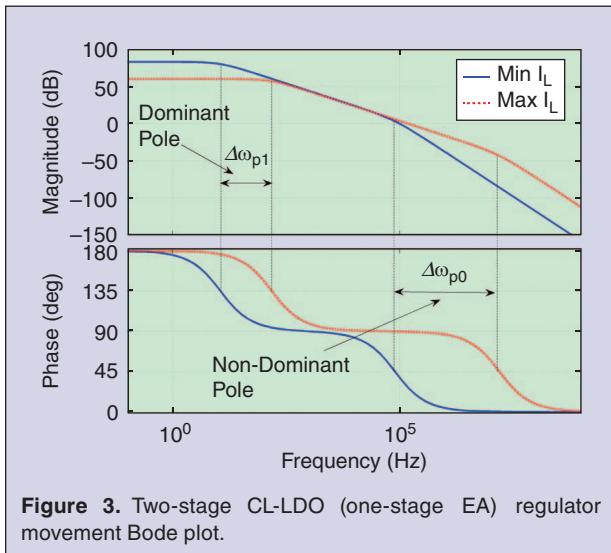
### A. Stability

A CL-LDO regulator model for stability analysis is shown in Fig. 2. This model uses Fig. 1(b) as reference. Signals  $V_{IN}$ ,  $V_{OUT}$ , and  $V_{REF}$  represent the input, output, and reference voltages, respectively.  $\beta$  is the feedback factor set by the  $R_{F2}/(R_{F2} + R_{F1})$ , and  $A_p$  is the pass-transistor



**Figure 2.** CL-LDO regulator model for stability analysis.

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**Figure 3.** Two-stage CL-LDO (one-stage EA) regulator movement Bode plot.

voltage gain. The error amplifier transfer function is represented by  $A_{EA}(s)$  and can be expressed as,

$$A_{EA}(s) = \begin{cases} \frac{A_{EA,o}}{1+s/\omega_{p1}}, & \text{for one-stage EA} \\ \frac{A_{EA,o}}{(1+s/\omega_{p1})(1+s/\omega_{p2})}, & \text{for two-stage EA} \end{cases}, \quad (1)$$

where  $\omega_{po}$  is the output pole of the system and is given by the  $C_L$  and the parallel combination of the output resistance of the pass transistor ( $1/g_{ds}$ ), load resistance ( $1/g_L$ ), and feedback resistors ( $1/g_\beta$ ). The EA DC gain is represented by  $A_{EA,o}$ , and  $\omega_{p1}$  and  $\omega_{p2}$  are the dominant and non-dominant poles of the error amplifier, respectively.

Stability is a critical design criterion since the unity gain frequency (UGF) and location of the poles vary significantly with the load current condition,  $I_L$  [6]. The

poles of a two-stage CL-LDO regulator (one-stage EA) are given by:

$$\omega_{p0} = \frac{g_{out}}{C_L} \propto I_L \quad (2)$$

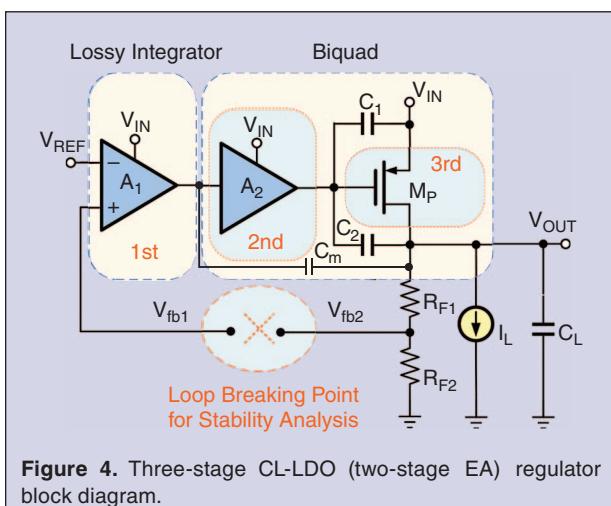
$$\omega_{p1} = \frac{g_{o,EA}}{(C_1 + (1 + A_p)C_2)} \propto \sqrt{I_L}, \quad (3)$$

where

$$\begin{aligned} g_{out} &= g_{ds} + g_L + g_\beta \approx K \cdot I_L \\ g_\beta &= \frac{1}{R_{F1} + R_{F2}}, \quad g_{ds} = \lambda I_L, \quad g_L \propto I_L \\ g_{mp} &= \sqrt{K_p I_L} \\ A_p &= \frac{g_{mp}}{g_{out}} \approx \sqrt{K_p I_L} \cdot \frac{1}{K \cdot I_L} = \frac{\sqrt{K_p}}{K \cdot \sqrt{I_L}} \\ \text{UGF} &\cong \frac{\beta g_{m,EA}}{C_2}, \end{aligned}$$

where  $K_p$  is a process dependent parameter [7],  $\lambda$  is the channel length modulation parameter, and  $K$  is a constant parameter. The pass transistor's transconductance is represented by  $g_{mp}$ , and the error amplifier output conductance and transconductance are represented by  $g_{o,EA}$  and  $g_{m,EA}$ , respectively. Capacitance  $C_1 = C_{gs} + C_{gb}$  and capacitance  $C_2 = C_{gd} + C_m$ , where  $C_{gb}$ ,  $C_{gd}$ ,  $C_{gs}$  are parasitic capacitances of the pass transistor and  $C_m$  is a compensation capacitance. The dominant pole of the conventional LDO regulator is typically placed at  $\omega_{p0}$  whereas the dominant pole of the capacitor-less LDO regulator is usually placed at  $\omega_{p1}$ .

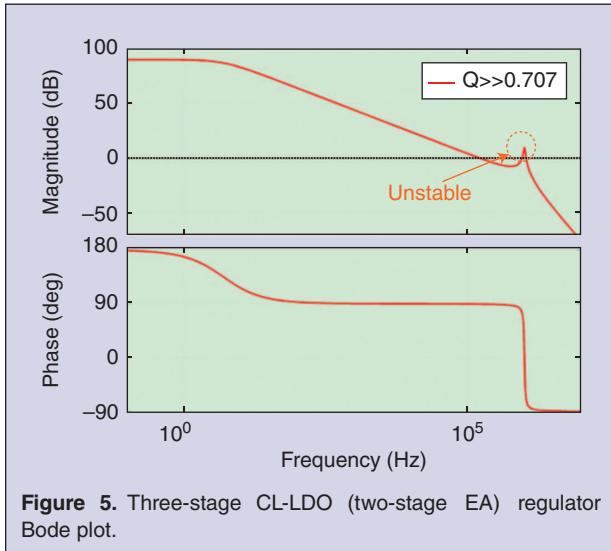
Observe that  $\omega_{p1}$  is a function of  $\sqrt{I_L}$  while  $\omega_{p0}$  is a function of  $I_L$ . Thus,  $\omega_{p0}$  changes at a faster rate than  $\omega_{p1}$  with respect to  $I_L$ . Fig. 3 shows the open loop Bode plot of the two-stage CL-LDO for the minimum load current  $I_{L,\min}$  and the maximum load current  $I_{L,\max}$ . From Fig. 3, it can be observed that the location of  $\omega_{p0}$  and  $\omega_{p1}$  varies as  $I_L$  changes. Note that unlike externally



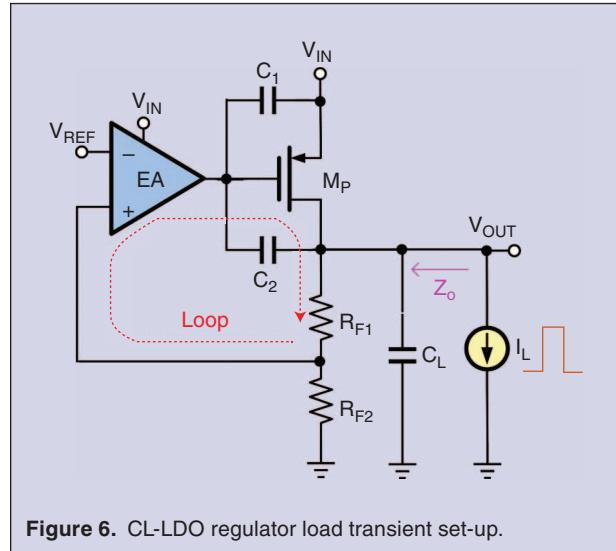
**Figure 4.** Three-stage CL-LDO (two-stage EA) regulator block diagram.

#### HINTS TO ENHANCE STABILITY:

- The worst stability condition typically happens at minimum  $I_L$ , thus it is important to achieve good phase margin at this point. Suggestion:
  - For one-stage EA: place UGF below the non-dominant pole frequency to achieve good phase margin at minimum  $I_L$ .
  - For a multiple-stage EA: distribute the power consumption such that most of the power is spent on the gain stages with non-dominant poles (especially the stage driving the pass transistor). This would place the non-dominant at high frequencies.



**Figure 5.** Three-stage CL-LDO (two-stage EA) regulator Bode plot.



**Figure 6.** CL-LDO regulator load transient set-up.

compensated LDO regulators where the worst-case stability condition occurs at  $i_{L,\max}$ , the worst-case stability condition for CL-LDO regulators occurs at  $i_{L,\min}$ .

Given a three-stage CL-LDO regulator (two-stage EA), we analyze the stability by considering a lossy integrator followed by a biquad, as shown in Fig. 4. Hence, the open loop transfer function can be write as,

$$\frac{V_{fb2}(s)}{V_{fb1}(s)} = -\frac{\beta A_{EA,o} A_p}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(\frac{s^2}{\omega_o^2} + \frac{s}{\omega_o Q} + 1\right)}, \quad (4)$$

where  $\omega_{p1} \cong g_{o1,EA}/(A_2 A_p C_m)$  is the lossy integrator's pole and dominant pole of the loop.  $g_{o1,EA}$  is the output conductance of the EA's first stage. The natural frequency and the quality factor of the biquad are represented by  $\omega_o$  and  $Q$ , respectively.  $Q$  is proportional to  $1/\sqrt{g_{mp}}$  [8] and function of  $1/\sqrt{I_L}$ . Another useful notation is:  $Q = 1/(2\delta)$ , where  $\delta$  is the damping factor.

The biquad poles are generated by the pole at the output of the LDO regulator and the pole at the gate of the pass transistor. These two non-dominant poles must be above UGF  $\cong \beta g_{m1}/C_m$  of the loop to ensure stability. At light loads, these two non-dominant poles become complex and can generate peaking due to the high  $Q$  of the biquad [2], [3] as shown in Fig. 5. If the magnitude of the peaking is large enough to cross the 0 decibels line, then the phase and gain margin will be affected; making the system unstable. Observe that for  $Q \leq 0.707$ , no peaking occurs in the open-loop response.

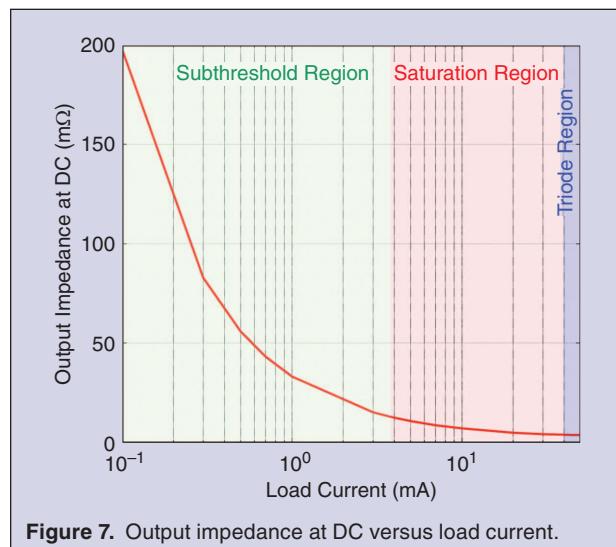
### B. Load Transient

The load transient quantifies the peak output-voltage excursion and signal settling time when the load-current is stepped. An LDO regulator with good load-transient

response must achieve minimal overshoot/undershoot voltage and fast settling time. For small load steps, the undershoot/overshoot of the output voltage is proportional to the output impedance  $Z_o(s)$  (see Fig. 6).

$$Z_o(s) = \frac{R_{out}}{1 + \beta g_{me} R_{o,EA} g_{mp} R_{out}} \cdot \frac{1 + s(C_1 + C_2)R_{o,EA}}{s^2 \frac{C_L(C_2 + C_1) + C_2 C_1}{\beta g_{me} g_{mp}} + s \frac{C_2}{\beta g_{me}} + 1}. \quad (5)$$

The CL-LDO regulator regulator has small-signal output impedance given by (5), where  $g_{me}$  and  $R_{o,EA}$  denote the error-amplifier transconductance and output resistance, respectively, and  $R_{out} = r_{dsp} \parallel (R_{F1} + R_{F2})$ . In (5), it is assumed that  $\beta g_{me} \ll g_{mp}$ . Assuming, for simplicity, that we can apply small-signal perturbation analysis, then



**Figure 7.** Output impedance at DC versus load current.

$$\Delta V_{\text{out}} = Z_o(s) \cdot \Delta I_L, \quad (6)$$

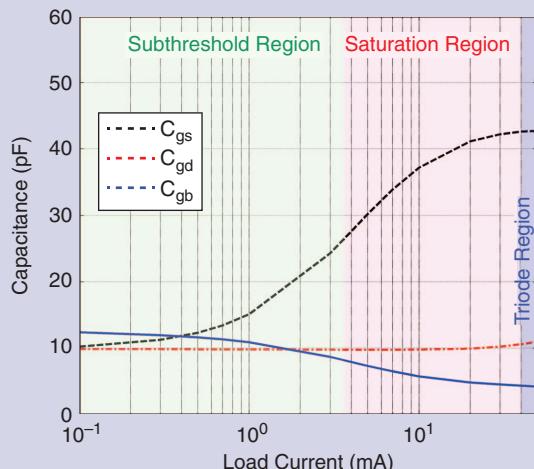
where  $\Delta I_L = I_{\text{step}}/s$  in the Laplace domain. In actuality, small variations in  $I_L$  would cause the parameters of  $Z_o(s)$  to change, adding nonlinearity to the response. However, we note that the load transient is strongly correlated to the output impedance. While externally compensated regulators'  $Z_o(s)$  is dominated by a microfarad-range load capacitor, CL-LDOs  $Z_o(s)$  arises chiefly from the open loop gain and can be improved by increasing the loop bandwidth.

For large load current steps, the analysis is particularly challenging since the pass transistor operates in different operating regions (e.g. subthreshold, saturation, and triode regions) over the entire load current range. Moreover, the transconductance, conductance, and parasitic capacitors of the pass transistor vary dynamically with the load

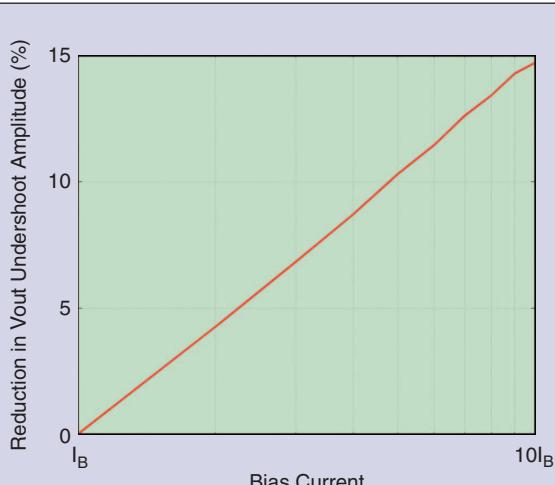
## HINTS FOR GOOD LOAD TRANSIENT AND TRADE-OFFS

- Increase the bias current at the stage driving the gate of the pass transistor to improve slew rate and reduce the EA output impedance. This minimizes the time constant ( $R_{o,EA}(C_1 + C_2)$ ).
- Trade-offs:
  - Increase in power consumption
  - If the EA stage driving the pass transistor is common source, the error amplifier gain is reduced. As a result, a reduction in the line/load regulation and PSR at low frequencies is expected.
- Use techniques to be described in Section III-B

current; hence complicating the analysis even further. Fig. 7 shows an illustrative example of how the CL-LDO output impedance varies as the load current changes and how the pass transistor operates in different regions over the entire load current range. Fig. 8 depicts the parasitic capacitance of the pass transistor variation versus load current. As can be seen, the CL-LDO output impedance and the parasitic capacitances of the pass transistor significantly vary over the entire current range. Fortunately, it has been observed that improving the slew rate (a large signal parameter) helps to minimize the undershoot/overshoots during large load current steps. In CL-LDOs, the slew rate ( $I_{\text{bias}}/C_{\text{gate}}$ ) is highly dependent on total capacitance at the gate of the pass transistor and the bias current of the error amplifier's stage driving it. Fig. 9 shows an example of the  $V_{\text{out}}$  undershoot amplitude variation versus the bias current of the EA's output stage for the CL-LDO regulator in Fig. 4. As can be seen, the undershoot amplitude reduces as the bias current increases. In Section III, several architectures that emphasize on improving the slew rate in CL-LDOs will be discussed. The main idea behind all of them is increasing the charging/discharging current at the gate of the pass transistor during large load transient events.



**Figure 8.**  $M_P$  parasitic capacitance versus load current.



**Figure 9.** Reduction in undershoot amplitude versus bias current.

### C. Load Regulation

The load regulation also quantifies the voltage variation at the output when change in the load-current occurs but it is measured once the output voltage is in steady-state:

$$\text{Load Regulation} \triangleq \left. \frac{\Delta V_{\text{OUT}}}{\Delta I_L} \right|_{t \rightarrow \infty}. \quad (7)$$

Hence, the load regulation is related to the closed loop DC output resistance of the LDO  $R_{\text{out},cl}$ :

$$R_{\text{out},cl} = Z_o(s)|_{s=0} = \frac{R_{\text{out}}}{1 + \beta g_{mp} R_{\text{out}} A_{EA,o}} \cong \frac{1}{\beta g_{mp} A_{EA,o}}. \quad (8)$$

As seen in (8), the higher the error amplifier DC gain, the smaller  $R_{out,cl}$ , and as result, the better the load regulation. High EA DC gain at  $I_{L,max}$  is particularly necessary to achieve good load regulation.

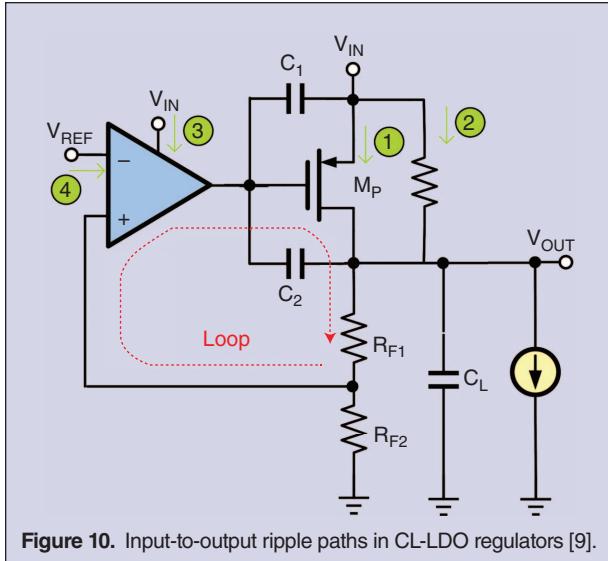


Figure 10. Input-to-output ripple paths in CL-LDO regulators [9].

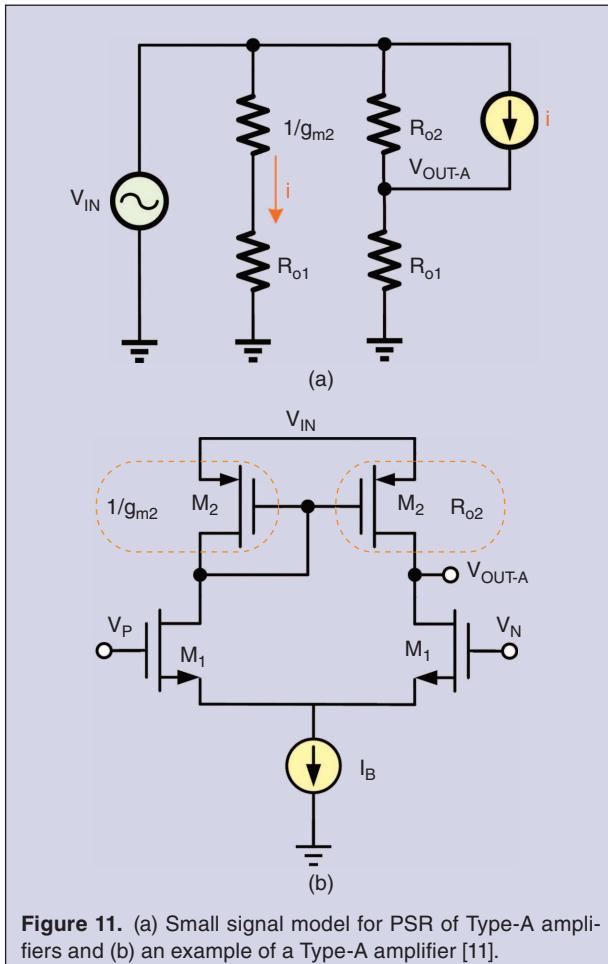


Figure 11. (a) Small signal model for PSR of Type-A amplifiers and (b) an example of a Type-A amplifier [11].

#### D. Power Supply Rejection

PSR refers to the amount of voltage ripple at the output of the LDO coming from the input voltage. The finite PSR in LDO regulators is due to several paths between the input and output. Fig. 10 depicts four paths that could couple input-voltage ripple to the LDO regulator output [9].

The ripple coming from path 4 (voltage reference) is minimum when a high PSR voltage reference is implemented. Otherwise, it can be reduced by adding a low-pass filter to the output of the voltage reference at the

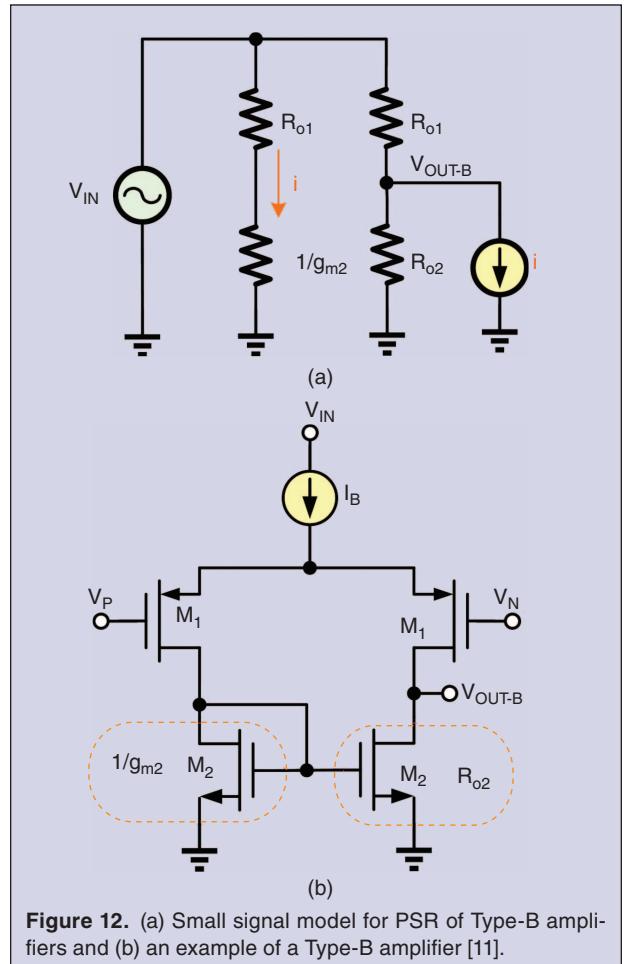


Figure 12. (a) Small signal model for PSR of Type-B amplifiers and (b) an example of a Type-B amplifier [11].

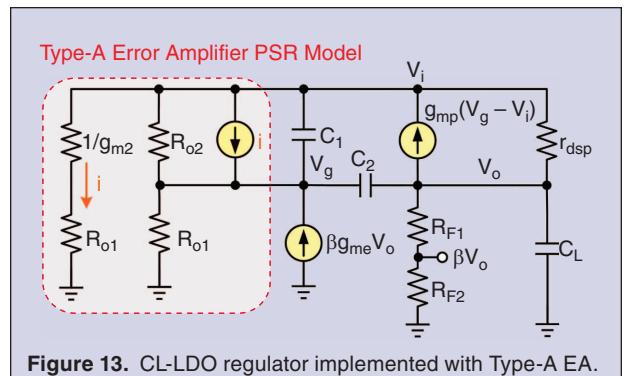
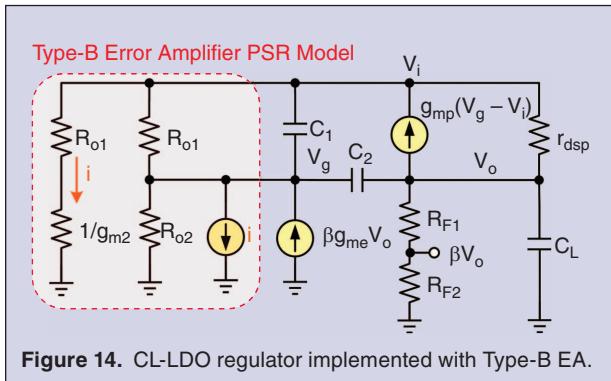


Figure 13. CL-LDO regulator implemented with Type-A EA.

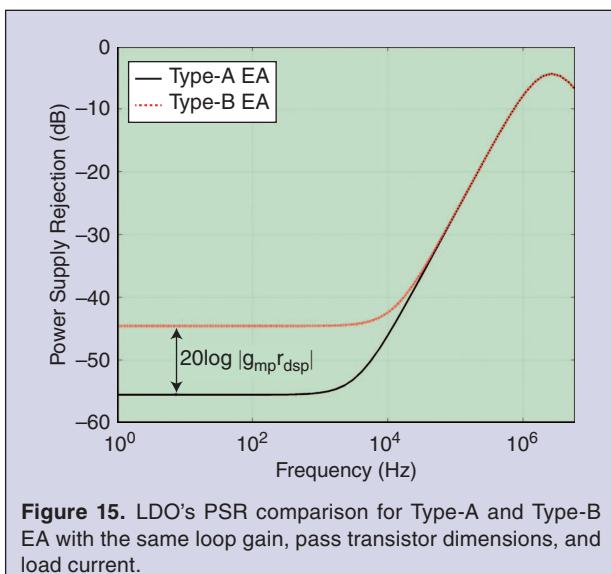


**Figure 14.** CL-LDO regulator implemented with Type-B EA.

expense of increasing area [10]. Therefore, the ripple contribution due to path 4 is neglected. The PSR transfer function of the CL-LDO regulator strongly depends on the type of EA [11]. The concept of the Type-A and Type-B error amplifiers was introduced in [11] to analyze the PSR of CL-LDO regulators. Fig. 11(a) and (b) show the Type-A small-signal model for PSR analysis and an example of a Type-A EA, respectively. Fig. 12(a) and (b) show the Type-B small-signal model for PSR analysis and an example of a Type-B EA, respectively [9]. Current  $i$  is approximately  $V_{IN}/R_{o1}$  for  $R_{o1} \gg 1/g_{m2}$ ,

**Table 1.**  
Analytical expressions for PSR of CL-LDO regulators.

Error amplifier	$A_{PSR}$	$\omega_{z1}$	$ PSR_{DC} $
Type-A	1	$\frac{g_{o,EA}}{g_{mp} r_{ds} C_2}$	$\frac{1}{\beta A_{EA,o} g_{mp} r_{ds}}$
Type-B	0	$\frac{g_{o,EA}}{C_2}$	$\frac{1}{\beta A_{EA,o}}$



**Figure 15.** LDO's PSR comparison for Type-A and Type-B EA with the same loop gain, pass transistor dimensions, and load current.

where  $R_{o1} \cong 1/g_{m,M1} + 2R_B$ . Resistor  $R_B$  represents current source  $I_B$  small signal resistance.

Fig. 13 and Fig. 14 show the PSR small signal model for CL-LDO regulators implemented with Type-A and Type-B EAs, respectively. These small signal models are based on Fig. 10. From Fig. 13 and Fig. 14 and assuming  $R_{o,EA} = R_{o1} \| R_{o2}$ , we obtain the following:

$$PSR = \frac{V_o}{V_i} \cong \frac{1 + A_p(1 - A_{PSR})}{\beta A_p A_{EA,o}} \cdot \frac{(1 + \frac{s}{\omega_{z1}}) \cdot (1 + \frac{s}{\omega_{z2}})}{(1 + \frac{s}{\omega_{p1}}) \cdot (1 + \frac{s}{\omega_{p2}})}, \quad (9)$$

where

$$\omega_{p1} \cong \frac{\beta g_{me}}{C_2}, \quad \omega_{p2} \cong \frac{g_{mp}}{C_L \left( 1 + \frac{C_2}{C_1} \right) + C_1}, \quad \omega_{z2} \cong \frac{g_{mp}}{C_1},$$

$$A_p = g_{mp} r_{dsp}, \quad A_{EA} = g_{me} R_{o,EA}, \quad \beta = \frac{R_{F2}}{R_{F1} + R_{F2}}.$$

$A_{PSR}$  is the error amplifier's open loop PSR; and equals to approximately one or zero for Type-A or B, respectively. In (9), it is assumed that  $\beta g_{me} \ll g_{mp}$ .

Table 1 shows the analytical expressions for  $\omega_{z1}$  and  $|PSR_{DC}|$  in CL-LDO regulators implemented with Type-A and Type-B error amplifiers. As can be seen from Table 1, CL-LDO regulators implemented with Type-A amplifier present higher DC PSR than the ones implemented with Type-B amplifier for the same loop gain.

Fig. 15 compares the PSR performance of LDO implemented with Type-A EA versus Type-B EA for the same loop gain and bandwidth, pass transistor dimensions, and load current. As can be seen from Fig. 15, the CL-LDO implemented with Type-A EA exhibits better PSR performance at low frequencies.

In the case of CL-LDOs implemented with two-stage EAs, it can be proved that the best PSR performance occurs when the first stage is implemented with Type-B amplifier and the second stage is implemented with Type-A amplifier since the overall error amplifier is effectively Type-A.

Table 2 classifies some common amplifier topologies in Type-A and Type-B amplifiers.

#### HINT:

- For the same open loop gain transfer function, Type-A EAs provide better PSR at low-frequencies than Type-B EAs.

#### E. Line Transient and Regulation

Line transient measures the output voltage variation in response to a voltage step at the input of the LDO regulator. Line transient is related to PSR, since both quantify the change in  $V_{OUT}$  due to a variation in  $V_{IN}$ ; however,

**Table 2.**  
**Type-A and Type-B single stage amplifier characteristics.**

Topology	Input Stage	Active Load	Amplifier Type
Simple	NMOS DP	PMOS CM	Type-A
	PMOS DP	NMOS CM	Type-B
Telescopic	NMOS DP	PMOS CM	Type-A
	PMOS DP	NMOS CM	Type-B
Folded cascode	NMOS/PMOS DP	PMOS CM	Type-A
	NMOS/PMOS DP	NMOS CM	Type-B

\* DP = differential pair and CM = current mirror.

they differ in that line transient/PSR are large/small-signal parameters, respectively [10]. Nevertheless, improving PSR at low-frequencies and high frequencies typically improves line regulation and line transient response, respectively. Assuming, for simplicity, that we can apply small-signal perturbation analysis, then

$$\Delta V_{\text{OUT}} = \text{PSR}(s) \cdot \Delta V_{\text{IN}}, \quad (10)$$

where  $\Delta V_{\text{IN}} = V_{\text{step}}/s$  in the Laplace domain and  $\text{PSR}(s)$  is the power supply rejection transfer function of the system. In fact, small changes in  $V_{\text{IN}}$  would cause the parameters of  $\text{PSR}(s)$  to change, adding nonlinearity to the response. However, we note that the line transient is strongly correlated to the power supply rejection transfer function of the system.

The line regulation also quantifies the voltage variation at the output when change in the input voltage happens but it is measured once the output voltage is in steady-state:

$$\text{Line Regulation} \triangleq \left. \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \right|_{t \rightarrow \infty}. \quad (11)$$

Hence, the line regulation is related to the PSR at low-frequencies (DC):

$$\text{Line Regulation} \cong \text{PSR}(s=0). \quad (12)$$

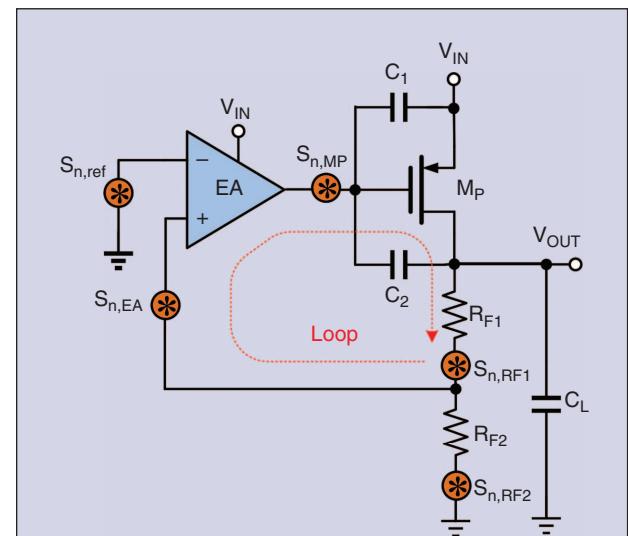
As seen in (12), the better the PSR at low frequencies (DC), the better the line regulation.

#### REMARK:

- Improving PSR, typically improves line regulation/transient.

#### F. Noise

Noise in LDO regulators refers to the thermal and flicker noise in transistors and resistors. It can be specified as output voltage noise spectral density ( $V/\sqrt{\text{Hz}}$ ) or as integrated output noise voltage ( $V_{\text{rms}}$ ) which is essentially the output spectral noise density integrated over



**Figure 16.** LDO regulator major noise contributors.

a bandwidth [12], [13]. For instance, if the LDO provides a regulated voltage to a voltage-control oscillator (VCO) the output spectral noise density curve would prove more useful for phase-noise/jitter computation. If instead the LDO regulates an ADC, then the integrated RMS noise could be more appropriate [13]. Fig. 16 shows the main noise contributors in LDO regulator.  $S_{n,\text{ref}}(f)$ ,  $S_{n,\text{EA}}(f)$ ,  $S_{n,\text{MP}}(f)$ ,  $S_{n,\text{RF1}}(f)$ , and  $S_{n,\text{RF2}}(f)$  represent the noise power spectral density of the voltage reference, error amplifier, pass transistor,  $R_{F1}$ , and  $R_{F2}$ , respectively [14].

The total output noise power spectral density of the LDO regulator is:

$$S_{n,o}(f) = \left( S_{n,\text{ref}}(f) + S_{n,\text{EA}}(f) + \frac{S_{n,\text{MP}}(f)}{A_{\text{EA}}^2} \right) \left( 1 + \frac{R_{F1}}{R_{F2}} \right)^2 + S_{n,\text{RF2}}(f) \left( \frac{R_{F1}}{R_{F2}} \right)^2 + S_{n,\text{RF1}}(f). \quad (13)$$

Notice that the noise contribution of the pass transistor can be neglected since it is divided by the EA gain

which is typically high. Thus, the total output noise power spectral density can be approximated as:

$$S_{n,o}(f) \cong (S_{n,\text{ref}}(f) + S_{n,\text{EA}}(f)) \left(1 + \frac{R_{F1}}{R_{F2}}\right)^2 + S_{n,\text{RF2}}(f) \left(\frac{R_{F1}}{R_{F2}}\right)^2 + S_{n,\text{RF1}}(f). \quad (14)$$

The noise coming from the voltage reference can be significantly reduced by adding a low-pass filter to the output of the voltage reference at the expense of increasing area. The EA and feedback resistors noise are typically the dominant sources of a LDO regulator noise.

#### HINTS:

- The differential pair transistor dimensions need to be large to reduce the flicker noise.
- Reducing feedback-resistors' noise requires smaller resistances, which in turn increases LDO quiescent power consumption.

### III. Comparison of CL-LDO Regulator Topologies

We categorize several illustrative CL-LDO regulator topologies into 3 groups. In this section, it is assumed that the gain stages are powered from  $V_{IN}$  unless otherwise specified.

#### A. Advanced Compensation Topologies

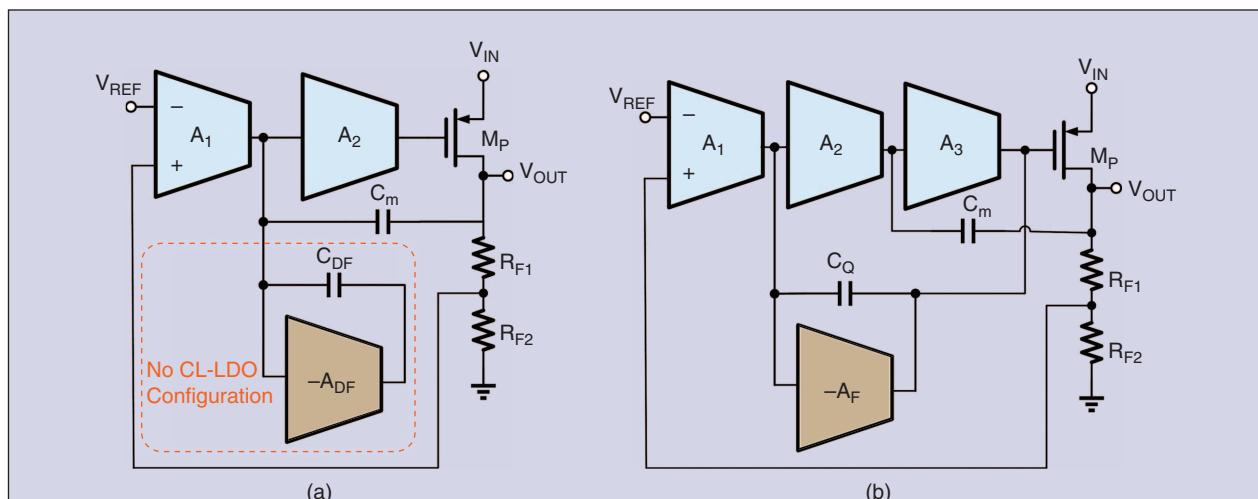
Topologies [1] and [2] are some of the first reported CL-LDO regulators. They are based on Miller pole splitting compensation to achieve small on-chip capacitance when compared with the conventional LDO regulator. In Fig. 17(a) [1], a damping-factor circuit stabilizes the LDO regulator for various capacitive load conditions. The LDO regulator requires the damping factor compensation

(DFC) circuit to be stable with and without an off-chip capacitor. In a capacitor-less configuration, the damping-factor circuitry might not be necessary since the feedback loop is effectively compensated with the Miller-compensation capacitor  $C_m$ . The dominant pole is given by  $A_2 A_p C_m$  and the output resistance of the EA first stage  $A_1$ . In this paper, we will refer to this topology as the Damping Factor architecture. Fig. 17(b) shows the Q-reduction architecture. This architecture was proposed to minimize on-chip capacitance and quiescent current [2]. The Q-reduction circuit is formed by  $C_Q$  and the transconductance  $A_2$ . The Q-reduction technique controls the  $Q$  of the non-dominant complex poles to improve the stability at light loads.

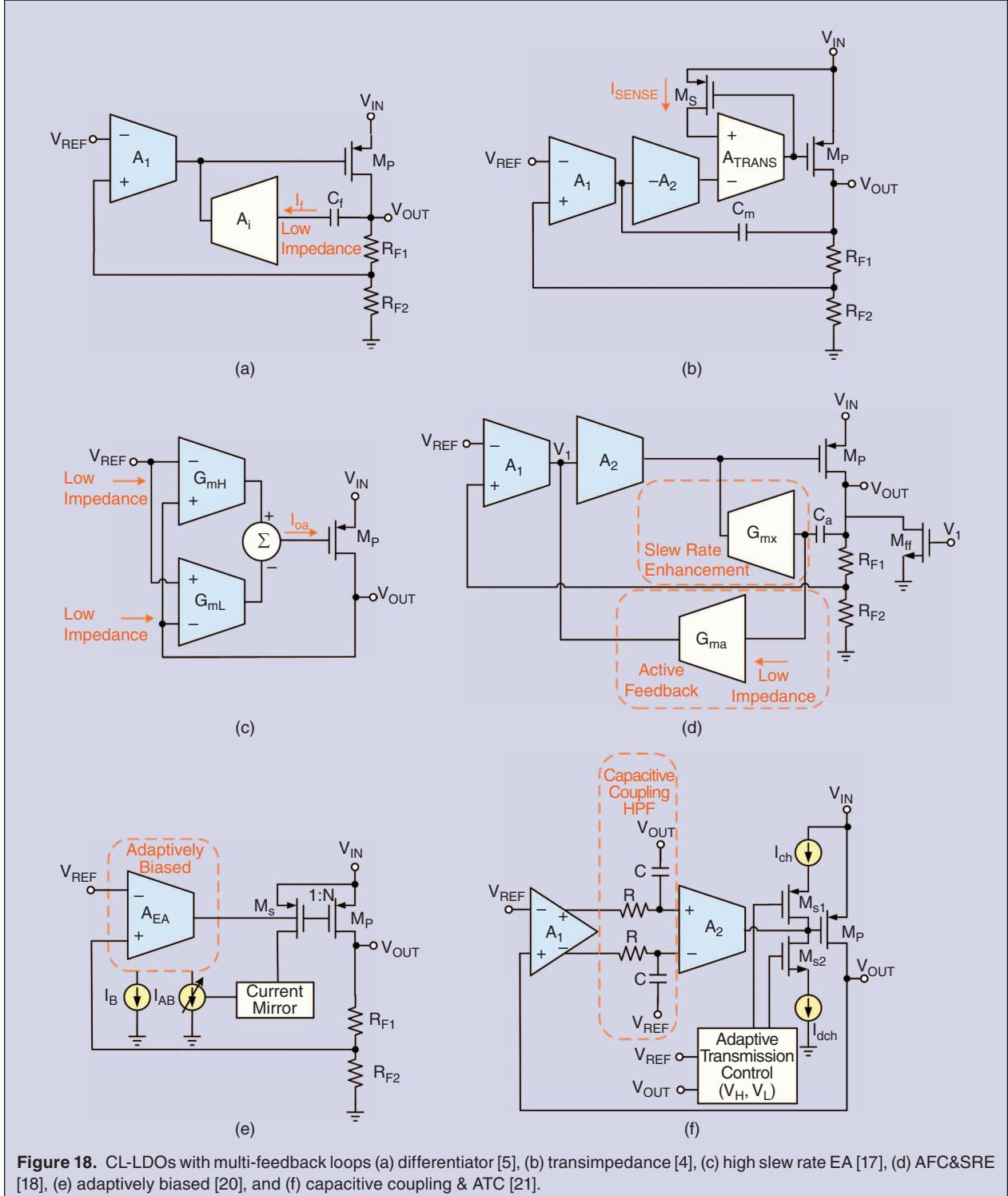
#### B. Load Transient Topologies

Approaches that improve the load transient comprise either pass-transistor-gate-voltage slew-rate enhancement with multiple active loops [4], [5], [15]–[22] and/or output-impedance reduction [23]–[27].

Architectures in [5] and [15] employ a current amplifier  $A_i$  in series with capacitor  $C_f$  that acts as an auxiliary fast loop in addition to the main voltage loop as shown in Fig. 18(a). The capacitance  $C_f$  reacts to sudden changes on  $V_{OUT}$  during load transients by generating an equivalent transient current ( $i_f$ ). Then, current  $i_f$  is amplified by the gain  $A_i$  and injected into the pass transistor's gate capacitance. Thus, this auxiliary loop improves the transient response. Moreover, it helps to achieve internal frequency compensation since the dominant pole of the system is defined by  $\omega_d \cong 1/(A_i A_p C_f R_{oi} \| R_{o1})$  where  $R_{oi}$  and  $R_{o1}$  are the output resistances of  $A_i$  and  $A_1$ , respectively. [16] expands on this technique, employing a bi-directional, asymmetric current amplifier to increase the UGF by cancelling the RHP zero from the pass-transistor  $C_{gd}$ .



**Figure 17.** CL-LDOs with improved frequency compensation techniques (a) damping factor [1] (b) Q-reduction [2].

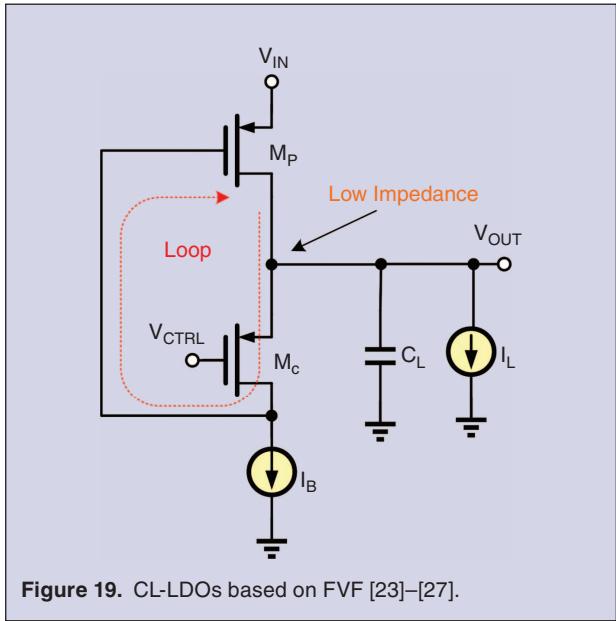


**Figure 18.** CL-LDOs with multi-feedback loops (a) differentiator [5], (b) transimpedance [4], (c) high slew rate EA [17], (d) AFC&SRE [18], (e) adaptively biased [20], and (f) capacitive coupling & ATC [21].

Fig. 18(b) displays a CL-LDO with multiple loops to improve the settling response [4]. This CL-LDO regulator combines a current-sensing transistor  $M_s$  and a transimpedance amplifier  $A_{TRANS}$  to generate an additional fast loop. Load variations are detected by the  $M_s$  to generate a scaled copy of  $I_L$ . During transitions from low

to high load currents, the corresponding increase in the sense current  $I_s$  improves the slew rate at the gate of the pass transistor.

In Fig. 18(c) [17], an EA with push-pull output stage achieves high slew rate at the gate of the pass transistor and reduces the quiescent current consumption. Class

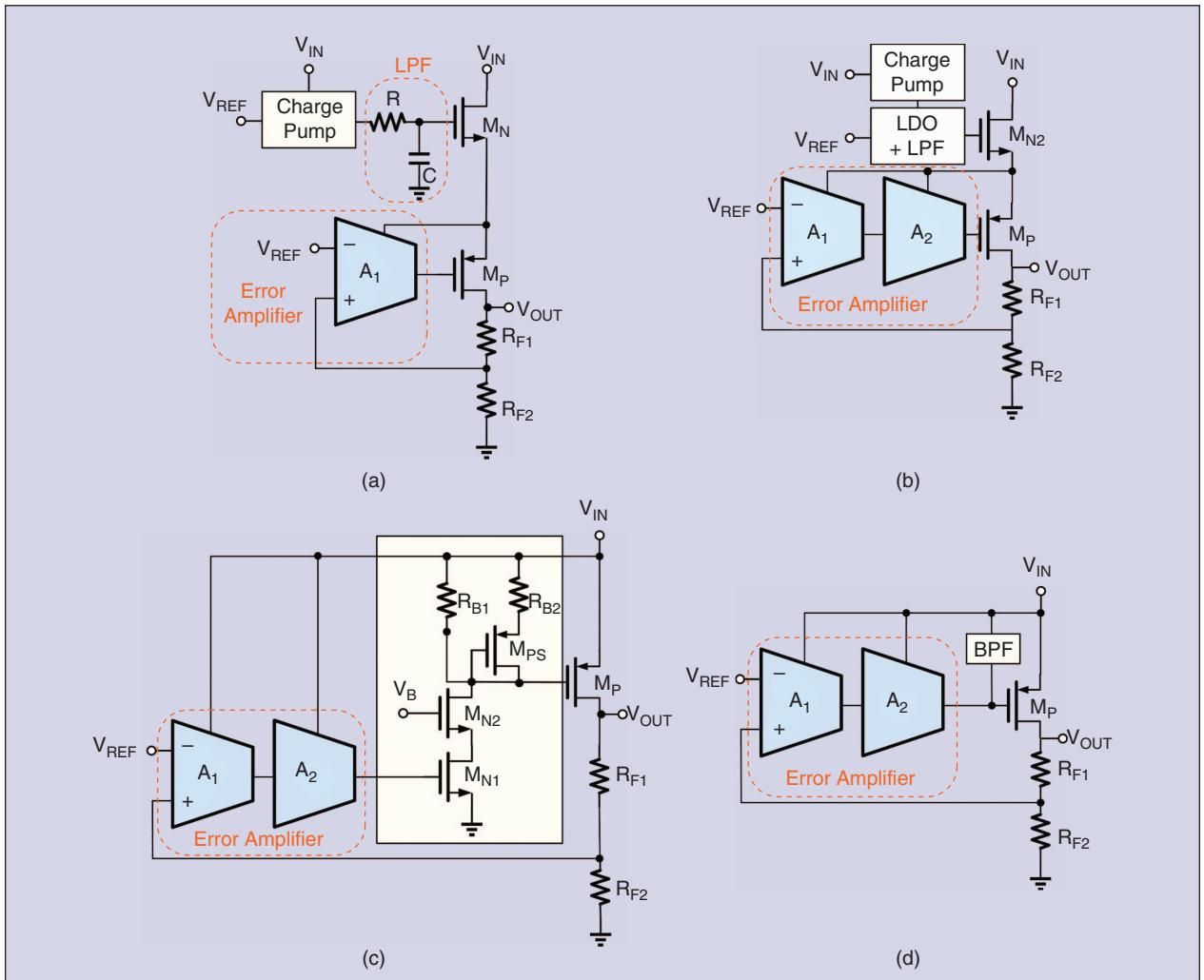


**Figure 19.** CL-LDOs based on FVF [23]–[27].

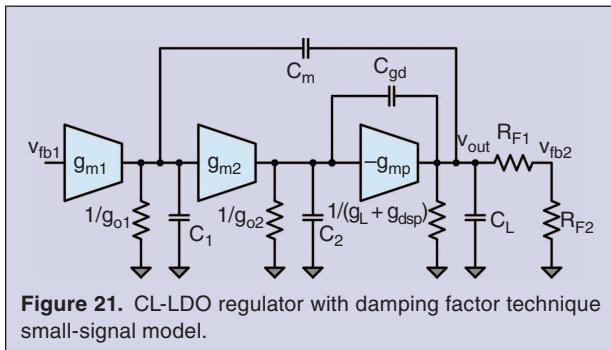
AB operation improves the slew rate since during transient events the peak currents of the transconductors  $G_{mH}$  and  $G_{mL}$  are not limited by the bias current.

The CL-LDO regulator in Fig. 18(d) [18] combines active feedback compensation (AFC)  $G_{ma}$  and slew-rate-enhancement (SRE)  $G_{mx}$  techniques to increase the loop bandwidth, reduce the total on-chip compensation capacitance, and improve the slew rate at the gate of the pass transistor. The slew-rate enhancement block reduces  $V_{OUT}$  variations during load transient events. The combination of  $M_{ff}$  with  $M_P$  creates a weak push-pull at the  $V_{OUT}$  node to reduce the overshoots during load transients. A similar architecture is presented in [19].

In Fig. 18(e) [20], a CL-LDO regulator uses an auxiliary loop to adjust the bias current of the EA's first stage. The EA is biased with a small fixed current  $I_B$  and an adaptive bias current  $I_{AB}$  proportional to  $I_L$ . The auxiliary loop is formed by the current sensing transistor  $M_s$  and a simple current mirror. The adaptive bias current



**Figure 20.** CL-LDOs for PSR enhancement (a) NMOS cascode [28], (b) NMOS cascode with auxiliary LDO [29], [30], (c) voltage subtractor [3], [31], and (d) FF with BPF [32].



**Figure 21.** CL-LDO regulator with damping factor technique small-signal model.

$I_{AB}$  increases the loop bandwidth and, as a result, the load transient performance is improved.

A multi-loop CL-LDO regulator that improves the load/dynamic voltage scaling transient response is shown in Fig. 18(f) [21]. The first loop employs a capacitively coupled high-pass filter that detects voltage variations at  $V_{REF}$  and  $V_{OUT}$  to increase the slew rate at the gate of the pass transistor. This increase in the slew rate improves the transient response. The second loop comprises the adaptive transmission control (ATC) block, two switches  $M_{s1}$  and  $M_{s2}$ , and the current sources  $I_{ch}$  and  $I_{dch}$ . This loop detects large voltage variations of  $V_{OUT}$  and  $V_{REF}$ , compares them with reference voltages  $V_H/V_L$  (not shown), and decides whether to enable  $M_{s1}$  or  $M_{s2}$  to charge or discharge the pass-transistor gate. A multi-loop CL-LDO structure for SRAM bank designed for very fast load step response while maintaining low quiescent current is presented in [22].

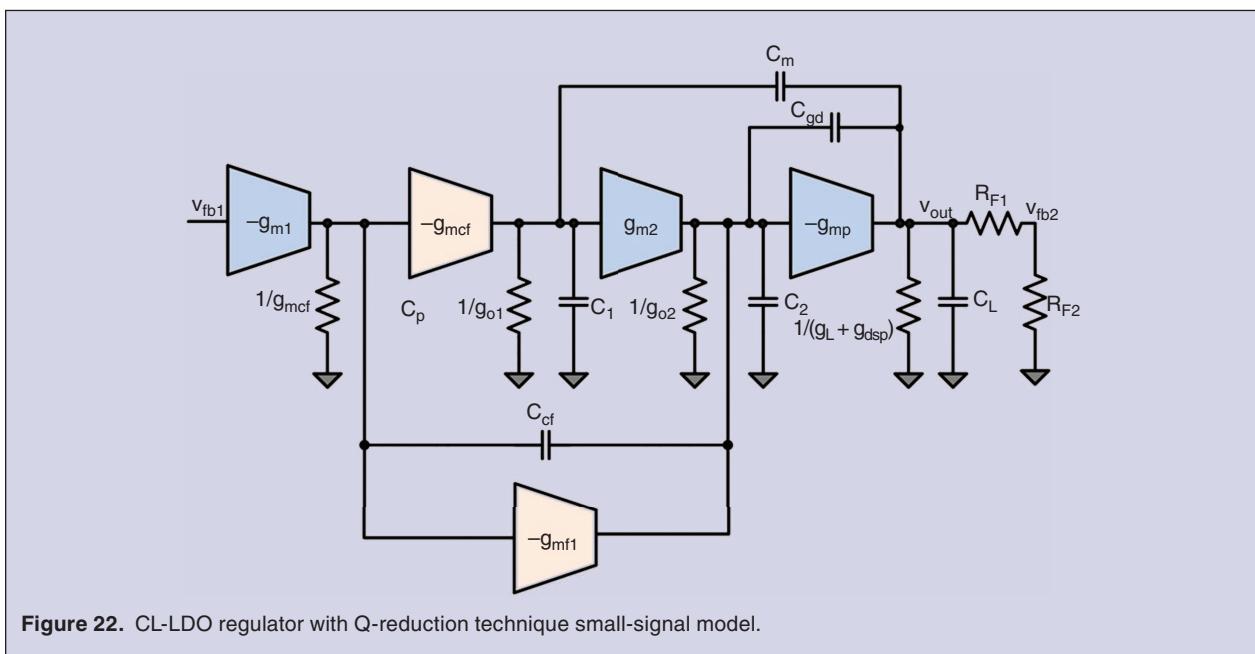
Multiple CL-LDO regulator topologies with a power stage based on the flipped voltage follower (FVF) have

been proposed [23]–[27]. These topologies were not fabricated in this work, but are included in the discussion for the sake of completeness. The FVF exhibits low output impedance due to shunt feedback, thus yielding good load regulation and stability [24]. The basic FVF CL-LDO regulator consists of pass transistor  $M_p$ , control transistor  $M_c$ , and current source  $I_B$  as shown in Fig. 19. Voltage  $V_{CTRL}$  sets  $V_{OUT} = V_{SG,MC} + V_{CTRL}$ . Transistor  $M_c$  source terminal senses variations at  $V_{OUT}$  and then amplifies the error signal to control the gate voltage of  $M_p$ . This mechanism regulates  $V_{OUT}$  and generates the required current by the load. Several architectures [25]–[27] have been proposed to improve the slew rate at the gate of  $M_p$  and increase the loop gain.

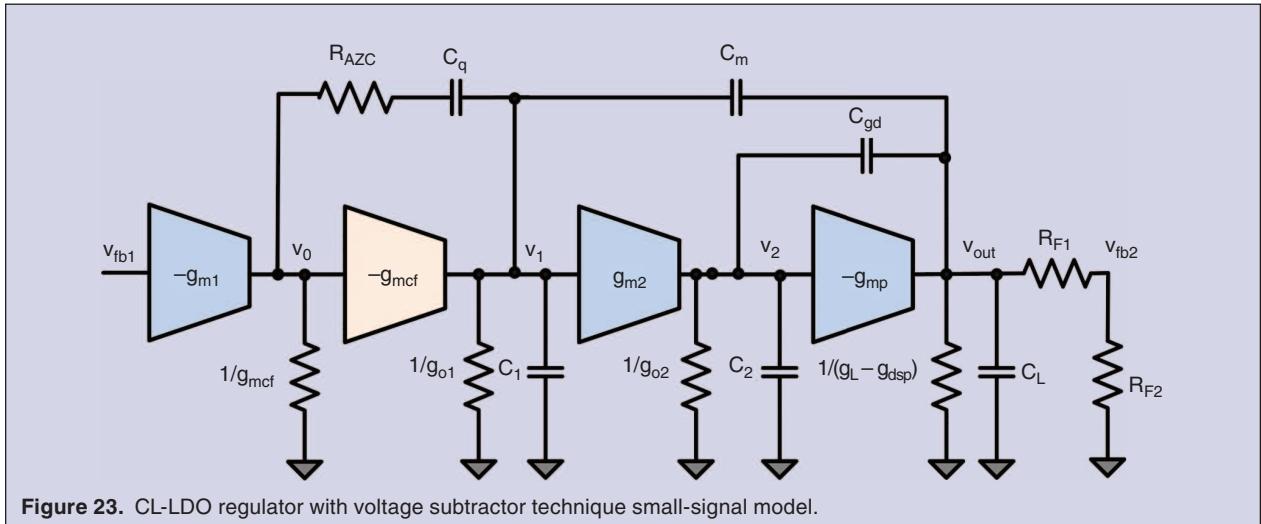
### C. PSR Topologies

Fig. 20 shows several topologies that have been proposed to improve PSR [3], [28]–[32]. The compensation schemes are not included to simplify the diagrams.

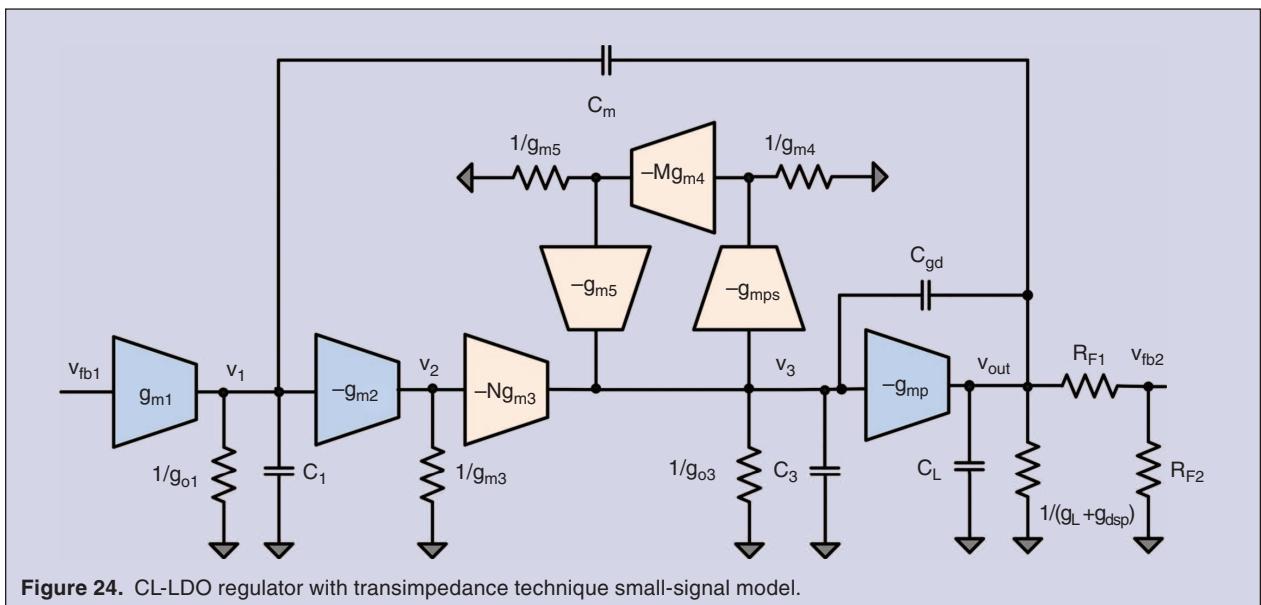
In Fig. 20(a) [28], an NMOS cascaded with the PMOS pass transistor is added to increase the isolation between  $V_{IN}$  and  $V_{OUT}$ . A charge pump generates a large voltage at the gate of the NMOS transistor to reduce its drop out voltage. In addition, a first-order low pass filter (LPF) is placed between the output of the charge pump and the gate of the NMOS device to reduce the charge pump output ripple. In Fig. 20(b) [29], [30] an NMOS cascaded with the PMOS transistor is used as well, but the gate bias of the NMOS is controlled with an auxiliary LDO regulator and first-order LPF. This implementation can potentially reduce the area when compared with [28] since the amplifier consumes low current from the charge pump



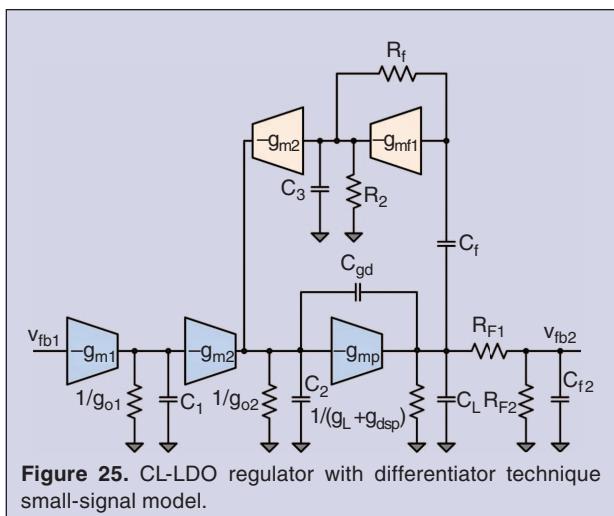
**Figure 22.** CL-LDO regulator with Q-reduction technique small-signal model.



**Figure 23.** CL-LDO regulator with voltage subtractor technique small-signal model.



**Figure 24.** CL-LDO regulator with transimpedance technique small-signal model.



**Figure 25.** CL-LDO regulator with differentiator technique small-signal model.

which reduces the size of its capacitors. In addition, it relaxes the cut-off frequency of the LPF due to smaller ripple at the output of the charge pump, thus potentially saving area. All these works provided very good PSR but they increase the drop-out voltage of the LDO.

In Fig. 20(c) [3] and [31], the main idea is to provide high impedance from the gate of  $M_P$  to ground and low impedance from the gate of  $M_P$  to  $V_{IN}$ . This allows the gate to follow the signal at the source of  $M_P$  such that the EA behaves like a Type-A amplifier ( $A_{PSR} \approx 1$ ); and as a result, PSR at low frequencies is improved. In Fig. 20(c) [3],  $R_{B1}$ ,  $R_{B2}$ , and  $M_{P2}$  form the low impedance from the gate of  $M_P$  to  $V_{IN}$ , and  $M_{N2}$  &  $M_{N1}$  form the high impedance from the gate to ground. A topology with a power-supply-rejection boosting filter circuit is shown in Fig. 20(d) [32]. This topology implements a feed-forward path with bandpass transfer

**TABLE 3.**  
CL-LDO regulator loop small signal transfer functions.

Topologies	$A_{EA,o}$	$\omega_{p1}$	$\omega_o$
Damping factor [1]	$\frac{g_{m1} g_{m2}}{g_{o1} g_{o2}}$	$\frac{g_{o1} g_{o2} g_{out}}{C_m g_{m2} g_{mp}}$	$\sqrt{\frac{g_{m2} g_{mp}}{C_L (C_{gd} + C_2)}}$
Q-reduction [2]	$\frac{g_{m1}}{g_{o1}} \left( \frac{g_{m2}}{g_{o2}} + \frac{g_{m1} g_{o1}}{g_{mcf} g_{o2}} \right)$	$\frac{g_{o1} g_{o2} g_{out}}{C_m g_{m2} g_{mp}}$	$\sqrt{\frac{g_{m2} g_{mp}}{C_L (C_{gd} + C_2)}}$
Voltage subtractor [3]	$\frac{g_{m1} g_{m2}}{g_{o1} g_{o2}}$	$\frac{g_{o1} g_{o2} g_{out}}{C_m g_{m2} g_{mp}}$	$\sqrt{\frac{g_{m2} g_{mp}}{C_L (C_{gd} + C_2)}}$
Transimpedance [4]	$\frac{g_{m1} Ng_{m2}}{g_{o1} g_{o3} \left( 1 + \frac{Mg_{mps}}{g_{o3}} \right)}$	$\frac{g_{o1} g_{o3} g_{out} \left( 1 + M \frac{g_{mps}}{g_{o3}} \right)}{(Ng_{m2} g_{mp} + Mg_{mps} g_{out}) C_m}$	$\sqrt{\frac{Ng_{m2} g_{mp}}{C_L (C_{gd} + C_2)}}$
Differentiator [5]	$\frac{g_{m1} g_{m2}}{g_{o1} g_{o2}}$	$\frac{g_{o2}}{A_{dif} \frac{g_{mp}}{g_{out}} C_f + \left( 1 + \frac{g_{mp}}{g_{out}} \right) C_{gd} + C_2}$	$\sqrt{\frac{g_{o1}}{C_1 C_2 (R_{F1} \  R_{F2})}}$

function to improve the power supply rejection at middle-to-high frequencies over a wide loading range.

#### IV. Selected Topologies

For comparison, we select at least one representative architecture from each of the three groups (Advanced Compensation, Load Transient, and PSR). The selected architectures are: [1]–[5] (Fig. 17(a), Fig. 17(b), Fig. 20(c), Fig. 18(b), and Fig. 18(a)).

The small-signal models for the Damping Factor, Q-reduction, Voltage Subtractor, Transimpedance, and

Differentiator CL-LDO regulators are shown in Fig. 21, Fig. 22, Fig. 23, Fig. 24, and Fig. 25, respectively. Parameters  $g_{mi}$ ,  $g_{oi}$ , and  $C_i$  (for  $i = 1, 2$ ) represent the transconductances, the output conductances, and the parasitic capacitors of each stage, respectively.  $C_{gd}$  and  $g_{mp}$  are the gate to drain capacitance and transconductance of the pass transistor.  $C_L$  and  $g_L$  are the load capacitance and conductance, respectively.  $C_m$  represents a compensation capacitor. In Fig. 21, notice that the damping factor circuit is not included because as mentioned in [1] it has no effect for capacitor-less operation and

**Table 4.**  
CL-LDO regulator loop small signal transfer functions.

Topologies	$Q$	$\omega_{z1}$	$\omega_{p4}$
Damping factor [1]	$\frac{g_{m2} g_{mp}}{\omega_o (g_{mp} - g_{m2}) C_{gd}}$	—	—
Q-reduction [2]	$\frac{g_{m2}/\omega_o}{C_{gd} \left( 1 - \frac{g_{m2}}{g_{mp}} \right) + \frac{C_{cf} C_3 g_{m2}}{C_m g_{mp}} + \frac{C_{cf} g_{m2}}{g_{mcf}}}$	$\frac{g_{m1} g_{m2}}{C_m g_{m1}}$	—
Voltage subtractor [3]	$\frac{g_{mp} g_{m2}/\omega_o}{C_{gd} (g_{mp} - g_{m2}) + \frac{C_2 C_L (1 + 2C_q/C_m)}{C_q (1/g_{mcf} + R_{AZC})}}$	$\frac{1}{R_{AZC} C_q}$	$\frac{g_{mcf}}{C_q}$
Transimpedance [4]	$\frac{Ng_{m2} g_{mp}}{\omega_o ((g_{mp} - Ng_{m2}) C_{gd})}$	—	—
Differentiator [5]	$\frac{1}{\omega_o \left( \frac{C_1}{g_{o1}} + C_{f2} (R_{F1} \  R_{F2}) \right)}$	—	—

**Table 5.**  
CL-LDO regulators PSR analytical expressions.

	Damping Factor [1]	Q-Reduction [2]	Voltage Subtractor [3]	Transimpedance [4]	Differentiator [5]
$\omega_{z1,\text{PSR}}$	$\frac{1 - A_{\text{PSR}}}{R_{o1}C_m}$	$\frac{g_{o1}(1 - A_{\text{PSR}})}{\left(\frac{g_{m2}}{C_{gd}}\right)C_{cf}}$	$\frac{1}{R_{o1}(C_m + 2C_q)}$	$\frac{g_{o1}g_{o3}g_{out}(1 - A_{\text{PSR}})(1 + g_{mp}r_{ds})(1 + M\frac{g_{mps}}{g_{o3}})}{C_m(Ng_{m2}g_{mp} + Mg_{mps}g_{out})}$	$\frac{1 - A_{\text{PSR}}}{R_{o2}C_{gd}}$
$\omega_{z2,\text{PSR}}$	$\frac{1}{R_{o2}C_m}$	—	$\frac{1 - A_{\text{PSR}}}{R_{o2}C_{gd}}$	—	—
$\omega_{p1,\text{PSR}}$	$\frac{\beta g_{m1}}{C_m}$	$\frac{g_{m2}}{C_{gd}}$	$\frac{\beta g_{m1}}{C_m}$	—	$\frac{\beta g_{m1}g_{m2}}{g_{o1}C_m}$
$\omega_{p2,\text{PSR}}$	$\frac{g_{m2}}{C_{gd}}$	—	$\frac{g_{m2}}{C_{gd}}$	—	—
$A_{\text{PSR}}^1$	-0.12/-0.20	1.36/1.43	0.92/0.96	0.68/1.00	1.29/1.36

<sup>1</sup> Results for  $I_L = 100\mu\text{A}/50\text{mA}$

small load currents. In Fig. 22, the Q-reduction circuit is formed by capacitor  $C_{cf}$  and transconductance  $g_{mcf}$ . Also, the feed-forward transconductance stage ( $g_{mf1}$ ) generates a left-half-plane (LHP) zero to improve the stability. In Fig. 23,  $C_q$  and  $R_{AZC}$  generate a pole-zero pair to improve the stability of the CL-LDO regulator. In Fig. 24, the transimpedance circuit is composed of transconductances  $g_{m3}$ ,  $g_{m4}$ , and  $g_{m5}$ .  $g_{mps}$  and  $g_{mp}$  are the transconductance of the current sensing transistor and pass transistor, respectively. In the original implementation, the minimum load current was 10 mA. In this work, the compensation capacitor  $C_m$  was connected at  $V_1$  instead of  $V_2$  to achieve stability at a minimum load current of  $100\mu\text{A}$ . In Fig. 25,  $g_{mf1}$ ,  $g_{mf2}$ ,  $C_f$ , and  $R_f$  form the differentiator circuit.  $C_f$  generates a high-frequency pole for stability purposes.

The loop transfer functions for the selected topologies can be expressed in general as,

$$\frac{V_{fb2}(s)}{V_{fb1}(s)} \approx \frac{-\beta A_{EA,o} \left( \frac{g_{mp}}{g_{out}} \right) \left( 1 + \frac{s}{\omega_{z1}} \right)}{\left( 1 + \frac{s}{\omega_{p1}} \right) \left( 1 + \frac{s}{\omega_{p4}} \right) \left( \frac{s^2}{\omega_o^2} + \frac{s}{\omega_o Q} + 1 \right)}. \quad (15)$$

Tables 3 and 4 show approximated expressions for  $A_{EA,o}$ ,  $\omega_{p1}$ ,  $\omega_o$ ,  $Q$ ,  $\omega_{z1}$ , and  $\omega_{p4}$  for each CL-LDO regulator topology. In Table 3,  $A_{dif} = g_{mf1}g_{mf2}R_fR_2$ .

The PSR transfer function for all the topologies can be approximated as,

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \text{PSR}_{DC} \frac{\left( 1 + \frac{s}{\omega_{z1,\text{psr}}} \right) \left( 1 + \frac{s}{\omega_{z2,\text{psr}}} \right)}{\left( 1 + \frac{s}{\omega_{p1,\text{psr}}} \right) \left( 1 + \frac{s}{\omega_{p2,\text{psr}}} \right)},$$

where

$$\text{PSR}_{DC} \approx \frac{1 + g_{mp}r_{dsp}(1 - A_{\text{PSR}})}{\beta g_{mp}r_{dsp}A_{EA,o}}.$$

Table 5 shows approximate analytical expressions for  $\omega_{z1,\text{psr}}$ ,  $\omega_{z2,\text{psr}}$ ,  $\omega_{p1,\text{psr}}$ ,  $\omega_{p2,\text{psr}}$ , and  $A_{\text{PSR}}$  for each CL-LDO regulator topology. Note that these EA topologies

**Table 6.**  
Targeted design specifications for CL-LDO regulators.

Parameter	Value
$V_{IN}$	3.0 V
$V_{OUT}$	2.8 V
$V_{REF}$	1.4 V
Loop UGF	500 kHz
$R_{F1}, R_{F2}$	100 k $\Omega$ each (on chip)
Pass transistor dimensions	W = 36mm, L = 0.6 $\mu\text{m}$
Technology	0.6 $\mu\text{m}$ CMOS

**Table 7.**  
**Measurement performance summary of the designs in 0.6 $\mu$ m CMOS technology.**

Topologies	Damping Factor [1] Fig. 17(a)	Q-Reduction [2] Fig. 17(b)	Voltage Substractor [3] Fig. 20(c)	Transimpedance [4] Fig. 18(b)	Differentiator [5] Fig. 18(a)
Quiescent current ( $\mu$ A) <sup>1</sup>	63/60	64/60	80/100	<b>46</b> /170	78/80
Total on-chip compensation capacitance (pF)	8	7	2.8	2.7	<b>1.2</b>
Maximum $C_L$ (pF)	180	190	610	450	<b>1500</b>
Load transient $\Delta V_{OUT}$ (V) <sup>2</sup>	1.026/0.650	1.134/0.325	1.207/0.345	<b>0.962</b> /0.289	1.207/ <b>0.281</b>
Load transient settling ( $\mu$ s)	1.20/3.09	4.23/1.54	1.73/1.56	1.04/3.56	<b>0.80</b> / <b>1.34</b>
Load regulation (mV/mA)	0.760	<b>0.721</b>	0.842	0.862	0.902
EA DC gain (dB) <sup>1,3</sup>	79/80	<b>85/87</b>	71/63	80/46	51/53
PSR@50mA (dB) <sup>4</sup>	<b>-52/-50/-27</b>	-63/-45/-20	-48/-47/-26	-46/-26/-7	-53/-36/-16
PSR@100 $\mu$ A (dB) <sup>4</sup>	-54/-52/-38	-66/-48/-26	<b>-82/-62/-39</b>	-50/-31/-11	-49/-42/-22
PSR@100 $\mu$ A at DC (dB) <sup>3</sup> ( $V_{IN} = 3.0V/3.6V$ )	-72/-70	-88/-88	-84/-83	<b>-91/-89</b>	-57/-63
$A_{PSR}$ <sup>3</sup> ( $I_L = 100\mu A/50mA$ )	-0.12/-0.20	1.36/1.43	0.92/0.96	0.68/1.00	1.29/1.36
Line transient (mV)	144/271	264/241	<b>76/93</b>	419/496	428/209
Line regulation (V/V)	0.018	<b>0.001</b>	0.002	<b>0.001</b>	0.003
Output noise spectral density at 100kHz (nV/ $\sqrt{Hz}$ ) <sup>3</sup>	<b>90</b>	100	190	130	140
Integrated output noise from 100Hz to 100kHz ( $\mu V_{rms}$ ) <sup>3</sup>	<b>44</b>	60	106	79	84
FOM <sub>1</sub> (ps)	0.246	0.272	0.386	<b>0.177</b>	0.377
FOM <sub>2</sub>	8.73	17.91	1.59	8.47	<b>0.85</b>

<sup>1</sup> Results for  $I_L = 100\mu A/50mA$

<sup>2</sup> Worst performance dip/surge for a load step from 100 $\mu$ A to 50mA / 50mA to 100 $\mu$ A with rise/fall times of 100ns.

<sup>3</sup> Simulation results

<sup>4</sup> PSR at 1kHz/10kHz/100kHz

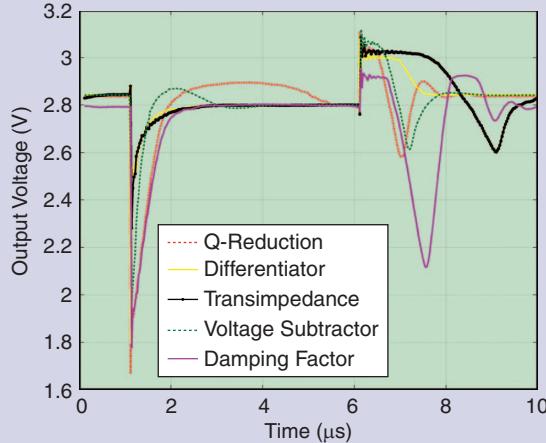
are more complex than the ones discussed in Section II.D and as a result  $-0.2 \leq A_{PSR} \leq 1.43$ .

The voltage subtractor and damping factor topologies have good high frequency PSR since their  $\omega_{z1,psr}$  is located at high frequencies. The voltage subtractor has very good low-frequency PSR at light loads because its  $A_{PSR}$  is approximately 1 and high DC loop gain. The Q-reduction architecture also has excellent low-frequency PSR because of its high DC loop gain. However, its PSR bandwidth is limited due to the effect of the compensation capacitor  $C_Q$  as shown in Table 5 ( $\omega_{z1,psr}$ ). The transimpedance topology has very good low-frequency PSR at light loads due its high DC loop gain. At heavy loads, the low-frequency PSR is significantly reduced due to its

low DC loop gain. This topology has low PSR bandwidth since its  $\omega_{z1,psr}$  is placed at very low-frequencies. The differentiator architecture has poor PSR low-frequency performance due to its low DC loop gain. Moreover, its PSR bandwidth is limited due to the large output impedance of the EA and the gate capacitance of the pass transistor.

## V. Experimental Results

For comparison, we select at least one representative architecture from each of the three groups (Advanced Compensation, Load Transient, and PSR). To compare each topology on the same basis, [1]–[5] (Fig. 17(a), Fig. 17(b), Fig. 20(c), Fig. 18(b), and Fig. 18(a)) architectures were designed in the same technology and with the common



**Figure 26.** Load transient experimental results.

design specifications shown in Table 6. [1] was designed in  $0.6\mu\text{m}$  CMOS process and its UGF was approximately 600 kHz. [2]–[5] were designed in  $0.35\mu\text{m}$  CMOS process and [2], [3], and [5] have UGFs  $< 850\text{kHz}$ . Thus, designing [1]–[3], and [5] for a UGF of approximately 500kHz in  $0.6\mu\text{m}$  CMOS would not significantly degrade their performance. [4] was originally designed for a UGF between 2MHz and 10MHz and hence its transient response might be degraded by reducing its UGF. In terms of the input voltage, all the architectures should be able to operate properly with 3V.

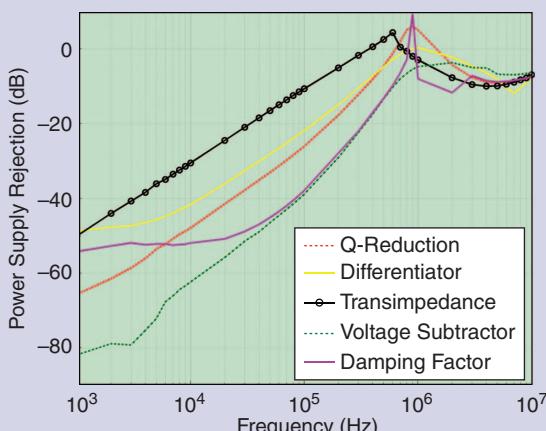
These common design specifications help to reveal the advantages and disadvantages of the five CL-LDO regulator topologies based on their compensation scheme and error amplifier topology. For example, having the same pass transistor dimensions helps to compare stability, transient, and quiescent current since the capacitance at the gate of the pass transistor determines the

location of the pole, the slew rate at that node, and the error amplifier's quiescent current. Moreover, having the same pass transistor dimensions,  $V_{\text{IN}}$ , and  $V_{\text{OUT}}$  helps to evaluate the CL-LDO regulator power supply rejection because all the topologies would have the same  $g_{ds}$ . In addition, having the same  $R_{F1}$ ,  $R_{F2}$ ,  $V_{\text{OUT}}$ ,  $V_{\text{REF}}$ , and loop UGF helps to normalize noise performance, as the difference between all the topologies are given by the error amplifier noise.

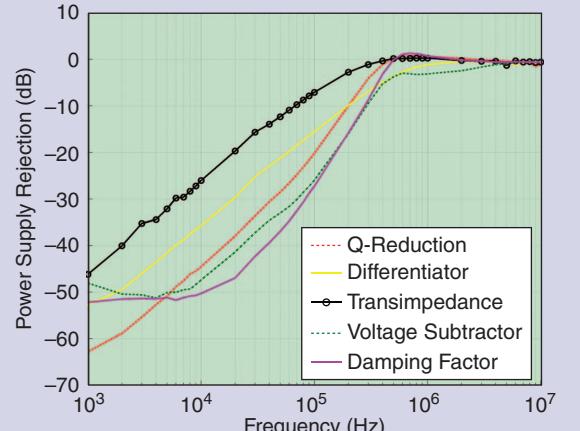
The CL-LDO regulators [1]–[5] were compared in terms of load and line regulation, load and line transient, power supply rejection, quiescent power consumption, maximum tolerable  $C_L$  not causing instability, and total on-chip compensation capacitance. Table 7 summarizes the performance highlights of all topologies.

#### A. Quiescent Current and Stability

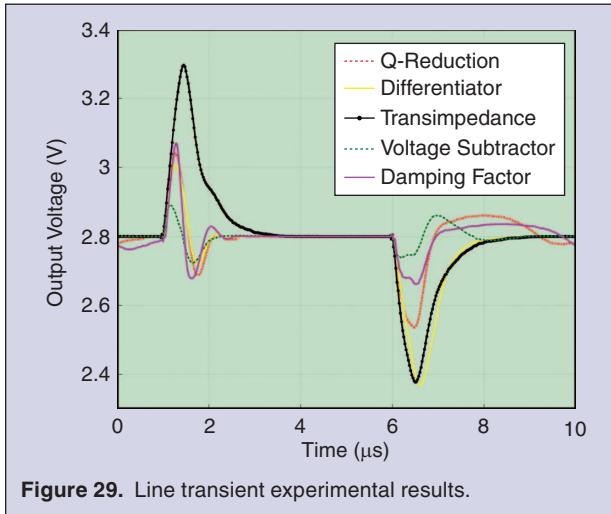
From Table 7, it can be seen that the transimpedance architecture consumes the lowest quiescent current at  $I_L = 100\mu\text{A}$  where it is most critical. This topology uses an adaptive biasing scheme which allows good current efficiency across the entire current range. Also, from Table 7, we observe that the damping factor and Q-reduction topologies require the largest total on-chip compensation capacitance while the differentiator topology requires the smallest amount to have a UGF of 500kHz and be stable. The differentiator architecture has the smallest amount of on-chip compensation capacitance when compared to the other topologies because of the large capacitance multiplication provided by the gain of the differentiator and the pass transistor. In addition, the differentiator architecture can tolerate the maximum  $C_L$  (1500pF) before becoming unstable. This resilience to large capacitive loads stems from capacitive multiplication, which places the internal dominant pole at extremely low frequencies.



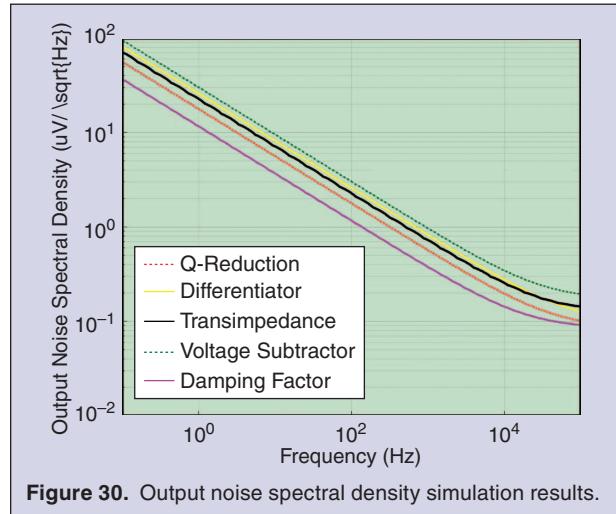
**Figure 27.** PSR versus frequency for  $I_L = 100\mu\text{A}$ .



**Figure 28.** PSR versus frequency for  $I_L = 50\text{mA}$ .



**Figure 29.** Line transient experimental results.



**Figure 30.** Output noise spectral density simulation results.

### B. Load Transient/Regulation

Fig. 26 shows the load-transient response for all architectures. In this test, a load-current step from  $100\mu\text{A}$  to  $50\text{mA}$  and vice versa with rise and fall times of  $100\text{ns}$  was performed. The input voltage  $V_{\text{IN}}$  and load capacitance  $C_L$  were  $3\text{V}$  and  $10\text{pF}$ , respectively. From Fig. 26, the voltage subtractor and differentiator architectures have the largest voltage dips for a current step from  $100\mu\text{A}$  to  $50\text{mA}$ . The transimpedance architecture has the smallest voltage dip, and the differentiator architecture shows the fastest settling time overall due to their additional loops to improve the transient response. From simulations, it can be correlated that architectures with smallest/largest voltage dips are the ones that provides the largest/smallest current to drive the gate of the pass transistor. In all the architectures, with the exception of the differentiator topology, the maximum current to drive the gate of the pass transistor is determined by the bias current of the error amplifier's output stage. For the differentiator topology, the voltage dips can be reduced if the value of  $C_f$  is increased. From Table 7, note that the damping factor and Q-reduction architectures have the best load regulation as well as the highest

EA DC gain. In contrast, the differentiator and transimpedance architectures have the worst load regulation and the lowest EA DC gain at  $I_L = 500\text{mA}$ . These observations confirm the relationship between load regulation and EA DC gain shown in (8), the higher the EA gain, the better the load regulation and vice versa.

### C. PSR

Fig. 27 shows the PSR versus frequency for all the architectures at  $I_L = 100\mu\text{A}$ . The voltage subtractor architecture has the best PSR performance because its  $A_{\text{PSR}}$  is close to 1 and high loop gain from its three gain stages. The Q-reduction architecture has limited PSR bandwidth because of the compensation capacitor  $C_Q$ . Oppositely, the transimpedance and differentiator architectures show the worst PSR performance. The differentiator architecture has low DC loop gain stage and its PSR bandwidth is limited due to the large output impedance of the EA and the gate capacitance of the pass transistor. As a result, PSR is significantly degraded. In this topology, the low-frequency PSR can be improved by increasing the EA DC gain.

**Table 8.**  
CL-LDO qualitative features.

LDO Topology	Best Performance	Second Best Characteristic
Damping factor [1]	Heavy load PSR, low output noise	Light load PSR, load transient $\Delta V_{\text{out}}$ , low $I_a$
Q-reduction [2]	Line regulation, load regulation	Low output noise, low $I_a$
Voltage subtractor [3]	Line transient, light load PSR	Heavy load PSR, maximum $C_L$
Transimpedance [4]	Load transient $\Delta V_{\text{out}}$ , line regulation, low $I_a$	Small compensation capacitance
Differentiator[5]	Load transient settling, maximum $C_L$ , small compensation capacitance	

Fig. 28 shows the PSR versus frequency for all the topologies at  $I_L = 50\text{mA}$ . As can be seen from Fig. 28, the Q-reduction technique shows the best PSR from 1kHz to 4kHz due to its high DC loop gain. The damping factor and voltage subtractor topologies present the best PSR from 5kHz to 300kHz. Observe that the PSR of the voltage subtractor degrades at low frequencies for  $I_L = 50\text{mA}$  compared to the case when  $I_L = 100\mu\text{A}$  because its low-frequency loop gain is lower at  $I_L = 50\text{mA}$ . The transimpedance and differentiator architectures show the worst PSR performance due to its low DC loop gain at  $I_L = 50\text{mA}$ .

#### D. Line Transient/Regulation

Fig. 29 shows the line transient response for all architectures. For this test, a voltage step at  $V_{IN}$  from 3.0V to 3.6V and vice versa with rise and fall times of 600ns was performed. The load current  $I_L$  and a load capacitor  $C_L$  were set to 100 $\mu\text{A}$  and 10pF, respectively. In Fig. 29, the voltage subtractor architecture has the best line transient response. This result should not be surprising since having good high-frequency PSR typically translates into good line transient as shown in (10). For an input voltage step from 3.0V to 3.6V at the input, the transimpedance technique has the largest voltage surge. For an input voltage step from 3.6V to 3.0V, the transimpedance and differentiator architectures have the largest voltage dips. These results make sense because both topologies have poor high-frequency PSR performance, which typically translates to poor line transient performance as shown in (10).

From Table 7, note that the transimpedance and Q-reduction architectures have the best line regulation for  $I_L = 100\mu\text{A}$  as well as the best PSR at DC. The differentiator and damping factor architectures have the worst line regulation performance and the worst PSR at DC. Thus, these results are consistent since often better low-frequency PSR corresponds to better line regulation as shown in (12).

#### E. Noise

Fig. 30 shows the output noise spectral density simulation results for all the topologies. These results were obtained for a load current of 50mA and it can be observed that flicker noise dominates. Table 7 summarizes the integrated output noise from 10Hz to 100kHz and the output noise spectral density at 100kHz results from all the architectures. The best (damping-factor/Q-reduction) and worst (voltage subtractor) noise performances thus correspond to the topologies with the largest and smallest input differential-pairs, respectively. The error amplifier's first stage transistors are the main noise contributors in the Q-reduction, transimpedance, voltage subtractor, and damping factor architectures and the current amplifier's

devices (transistors and resistor) are the main noise contributors of the differentiator topology.

To compare the LDO regulators, we use the following figure of merit (FOM) [22]:

$$\text{FOM}_1 = \frac{C_L V_{out}}{I_{L,max}} \cdot \frac{I_{q,max}}{I_{L,max}} [\text{ps}], \quad (17)$$

where  $C_L = 10\text{pA}$  and  $I_{q,max}$  and  $I_{L,max}$  are the maximum quiescent and load current, respectively. The smallest  $\text{FOM}_1$  indicates the best regulator. To include the contribution of the PSR, maximum  $C_L$ , and total on-chip compensation capacitance  $C_{cm}$ , we propose an alternative figure of merit  $\text{FOM}_2$ :

$$\text{FOM}_2 = \frac{C_{cm}}{C_{L,max}} \cdot \frac{\Delta V_{out}}{V_{out}} \cdot \frac{I_{q,max}}{I_{L,max}} 10^{(\text{PSR(dB)/20})} \cdot 10^7. \quad (18)$$

For the  $\text{FOM}_2$  calculation, we use the PSR at 100kHz for  $I_L = 50\text{mA}$ . The smallest  $\text{FOM}_2$  indicates the best regulator. Table 8 succinctly summarizes the CL-LDOs regulators [1]-[5] key qualitative characteristics.

## VI. Conclusion

A comparative study of illustrative CL-LDO regulator architectures has been presented. All the architectures were designed using 0.6 $\mu\text{m}$  CMOS technology and compared in terms of line and load regulation, PSR, line and load transient, total on-chip compensation capacitance, and quiescent power consumption. There is not a single CL-LDO regulator architecture that outperforms all the other for a set of specifications. Trade-offs between the architecture and performance are very much application-dependent. Key design issues for capacitorless LDO regulators have been addressed.

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