A 0-24mA, 1.2V/1.8V Dual Mode Low Dropout Regulator Design for Efficient Power Management in Battery-Powered Systems

Munazir Reza, Naushad Alam
Dept. of Electronics Engg, Aligarh Muslim University
Aligarh, India
mreza@myamu.ac.in, naushad.el@amu.ac.in

Syed Javed Gaggatur
Intel Foundry
Bengaluru, India
gsjaved@ieee.org

***Abstract*—Low drop-out (LDO) regulators are widely employed in today's electronics industry due to their essential role as subsystems within power management units. The increasing need for mobile battery-operated products and portable devices such as laptops, mobile phones and tablets has led to a rise in the utilization of LDO regulators as integral power management modules within System on Chip (SoC) designs. LDOs are employed to safeguard sensitive analog blocks from unwanted power supply noise, leveraging their high Power Supply Rejection Ratio (PSRR) performance. The LDO is designed in tsmc180nm technology with a dual supply voltage of 1.2V/1.8V and a programmable output voltage of 1.1V/1.5V. The simulations show that the LDO exhibits a transient response with a full load current ranging from 0 to 24mA, coupled with a low dropout voltage of under 100mV/300mV, respectively. The quiescent current of the complete LDO is 225μA and the maximum load regulation of 0.34 μV/mA.**

***Index Terms*—Low drop-out Regulator (LDO), programmable reference voltage, dual supply, error amplifier, battery-operated, low quiescent current**

I. Introduction

Battery-powered devices, including application processors (AP), cameras, laptops, recorders, and memory components, rely on multiple DC supplies to energize different sub-blocks. In the context of portable mobile devices as illustrated in Fig. 1, a Power Management IC (PMIC) is crucial, and it often demands a multitude of DC-DC converters and Low Dropout Regulators (LDOs). For example, an AP PMIC might necessitate over 30 LDOs. Consequently, the total count of LDOs within a PMIC can surpass 80, resulting in a substantial expansion of silicon area requirements.

The proposed Low Dropout Regulator (LDO) operates with a supply voltage of 1.2 V, delivering an output of 1.1V with a low dropout voltage of 100mV. Additionally, for applications requiring multiple supply voltage levels, flexibility is provided by accommodating an input supply of 1.8V and yielding an output voltage of 1.5V.

979-8-3503-8010-1/24/$31.00 © 2024 IEEE

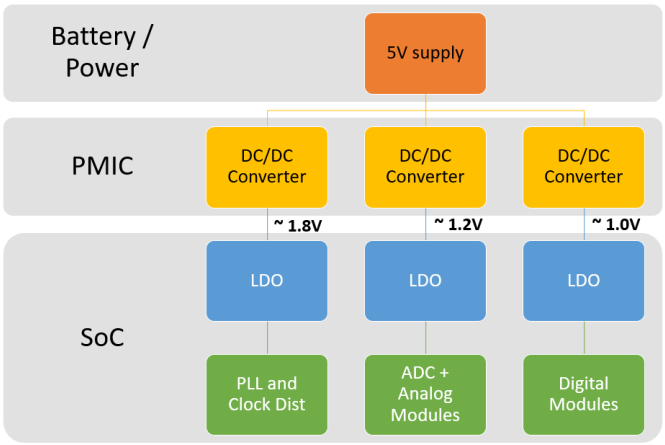

Fig. 1: The planned power delivery from the battery to the System-on-Chip.

The number of blocks within a single chip has grown with advancements in chip fabrication technology. To enhance the performance of these various blocks, individual blocks necessitate distinct supply voltage levels. Moreover, external power sources for the output are susceptible to environmental noise and digital signals within the chip before reaching the blocks. Hence, a voltage regulator is essential to deliver optimal power to the internal loads of the Integrated chip (IC). Moreover, the LDO needs to adapt to changes in the load condition swiftly, ensuring a constant and stable power supply [1]–[4].

The low drop-out nature of the regulator makes it appropriate for use in many applications, namely, automotive, portable [5], industrial [6], and medical applications. A high gain and high output impedance CMOS operational amplifier (op-amp) is used as an error amplifier, with a stable programmable voltage reference given as an input to the amplifier.

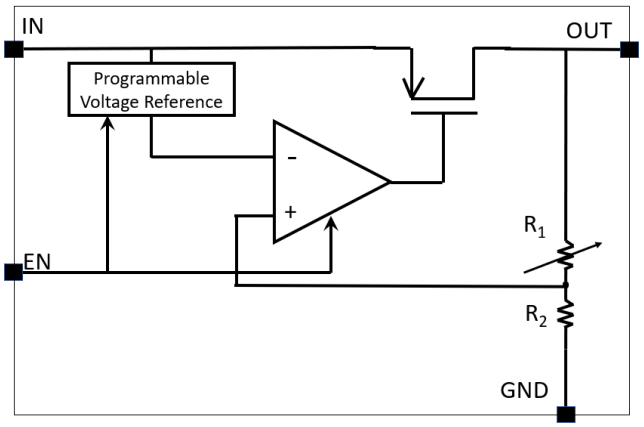

Fig. 2: Block diagram of the proposed capacitorless LDO

TABLE I: Design Parameter of LDO

Parameter	*Design-I*	*Design-II*	*Units*
V_{Supply}	1.8	1.2	V
V_{OUT}	1.5	1.1	V
V_{REF}	1.2	1.0	V
$R1$	10	4	KΩ
$R2$	40	40	KΩ
W_{M1}	2.5	2.5	mm
C_{LOAD}	10	10	pF
I_{LOAD}	0 - 24	0 - 24	mA

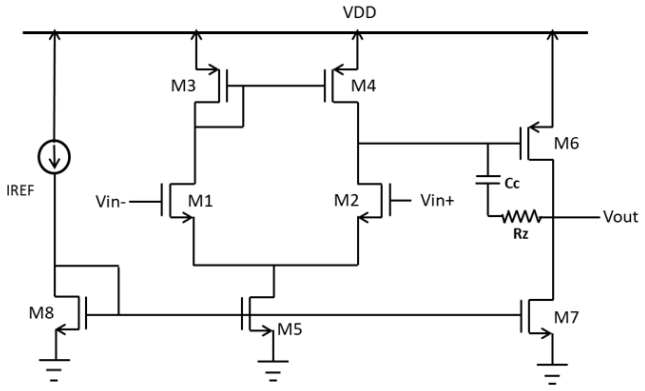

Fig. 3: Schematic of the high gain error amplifier.

TABLE II: Error Amplifier Specification

Parameter	*Value*
Length (L)	360 nm
$Width(W_1)\&W_2$	1.5 μm
$W_3\&W_4$	2.1 μm
W_5	1.5 μm
W_6	31.5 μm
W_7	10.5 μm
Coupling Capacitor (C_c)	0.4 pF
R_z	1 KΩ
C_{L}	1 pF

II. Proposed Capacitorless LDO design

The proposed capacitorless LDO is designed to produce a stable output of 1.5V. It works with an input supply of 1.8V and can handle a current of up to 24mA. The schematic of the LDO is as shown in Fig. 2, featuring an error amplifier (EA) along with a PMOS pass transistor and a negative feedback potential divider. For the desired output voltage, the values of R1 and R2 are 10KΩ and 40 kΩ respectively. The maximum width of the PMOS pass transistor was found to be 2.5mm. Table I summarizes the design parameters of LDO operating in dual-supply voltage mode while providing a constant 0-24mA load current.

III. Error Amplifier Design Consideration

The selection of the topology of the operational amplifier for designing an LDO is based on the specific requirements of the application and the desired performance characteristics to achieve optimal voltage regulation and efficiency. This design employs a two-stage op-amp as an error amplifier (EA). The schematic of the EA is depicted in Fig. 3. The op-amp is designed utilizing the gm-Id methodology within the framework of 180nm CMOS technology. Detailed parameters such as the length, width of the transistor, and load capacitor are tabulated in Table II.

1) High Open-Loop Gain: A high open-loop gain is necessary for stable operation and effective voltage regulation. It ensures that the op-amp can provide sufficient gain to maintain precise control over the output voltage. The open-loop gain of this op-amp is 67.98 dB.

2) Low Input Bias Current: Low input bias current is crucial for minimizing errors in the regulation caused by current flowing into the input terminals. It helps maintain accuracy in the output voltage. The total input bias current of this op-amp is 205.65 μA.

3) High power supply Rejection Ratio (PSRR): High CMRR helps reject common-mode signals, which can be important for maintaining accurate regulation in the presence of noise or interference. The PSRR of this op-amp is -29.8 dB.

4) Low Quiescent Current: Low quiescent current (I_Q) is important for minimizing power consumption when the LDO is in standby or no-load conditions. This contributes to higher overall efficiency. The quiescent current of the designed LDO is is 225μA.

5) Stability and Phase Margin: The op-amp should be stable in the feedback loop and have adequate phase margin to prevent oscillations and ensure reliable performance. Phase Margin of this op-amp is 87.72 degrees.

This design employs a two-stage op-amp as an error amplifier (EA). The schematic of the EA is depicted in figure 3.

IV. Simulation Results and Discussion

The proposed LDO design was simulated using open-source tool *LTSpice* with 180nm CMOS technology parameters.

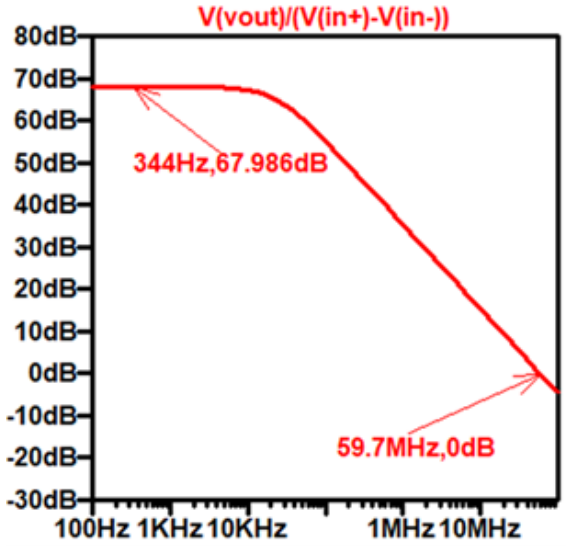

Fig. 4: Frequency response of Error Amplifier

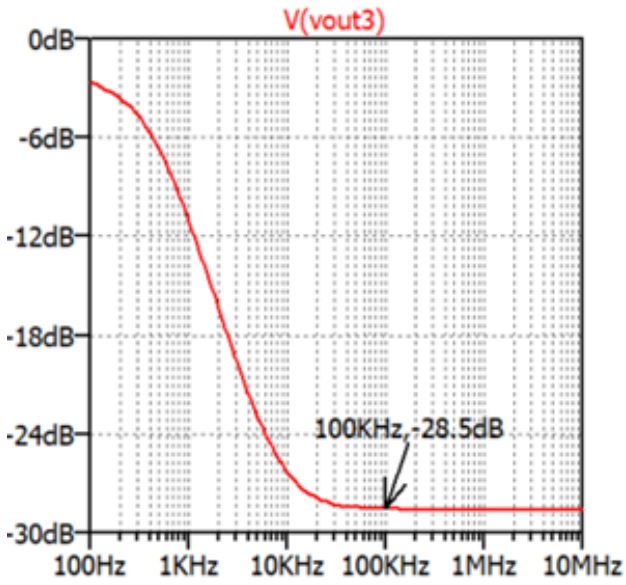

Fig. 5: Power Supply rejection ratio at 100kHz

A. *Error Amplifier*

The optimal performance of the LDO relies significantly on the specifications of the operational amplifier (op-amp) employed. The op-amp exhibits a DC gain of more than 60 dB, a gain bandwidth product of more than 59 MHz, and a bandwidth of more than 23 KHz, as shown in Fig. 4 ensuring efficient signal processing. With a phase margin of 66 degrees, the op-amp maintains stability and fast-settling in the feedback loop. The power dissipation is observed to be 417 μW at 1.8V. The power supply rejection ratio (PSRR) is -29.8 dB @ 100 kHz, as shown in Fig. 5 . The performance summary of the error amplifier is tabulated in Table III.

TABLE III: Performance Summary of the error amplifier

Parameter	***Value***
DC Gain	67.98 dB
Gain Bandwidth Product (GBW)	59.73 MHz
Bandwidth	23.5 KHz
Phase Margin	87.72 deg
Power Dissipation	370 μW
PSRR	-29.8 dB
CMRR	73 dB
$V_{\text{icm,min}}$	0.9 V
$V_{\text{icm,max}}$	1.547 V
Slew Rate	9.63 V/μS

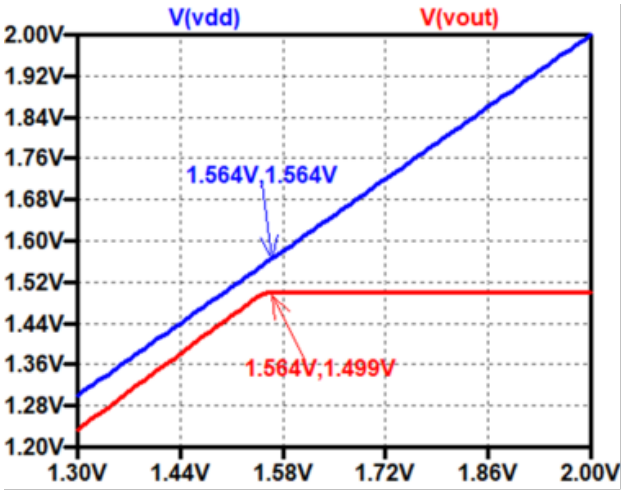

Fig. 6: DC Line regulation of design I

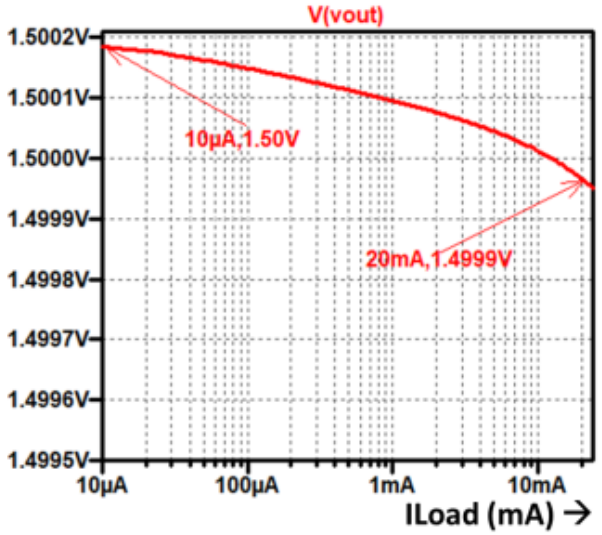

Fig. 7: DC Linear Load Regulation from 0 - 24mA

B. *Proposed LDO*

1) DC Line and Load Regulation: Line regulation measures the LDO's ability to maintain the specified output voltage with varying input voltage [2], [3]. Line regulation is defined as

$$LineRegulation = \Delta V_{OUT}/\Delta V_{IN} \quad (1)$$

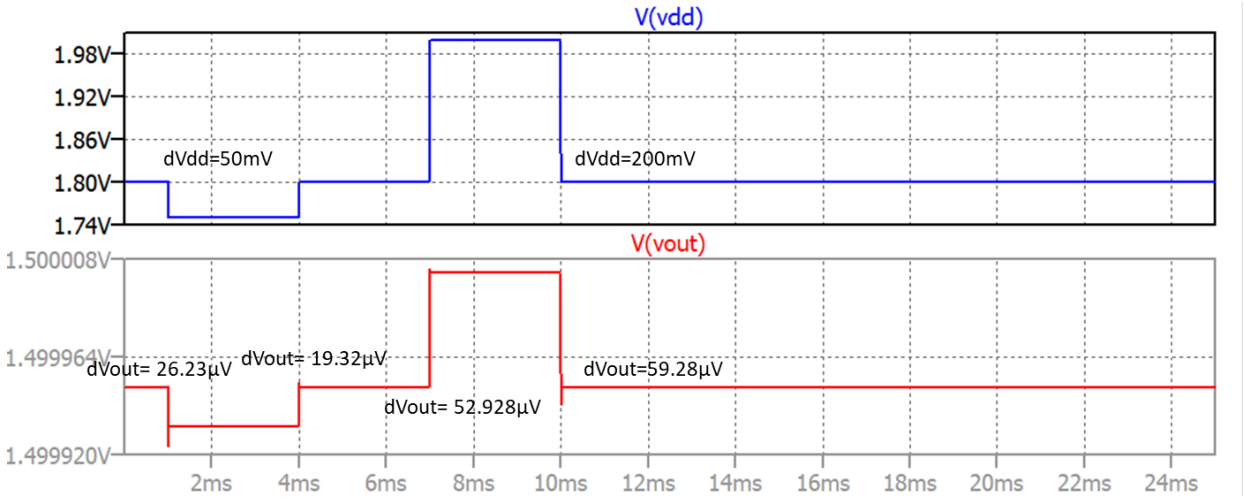

Fig. 8: Line Transient Response of LDO

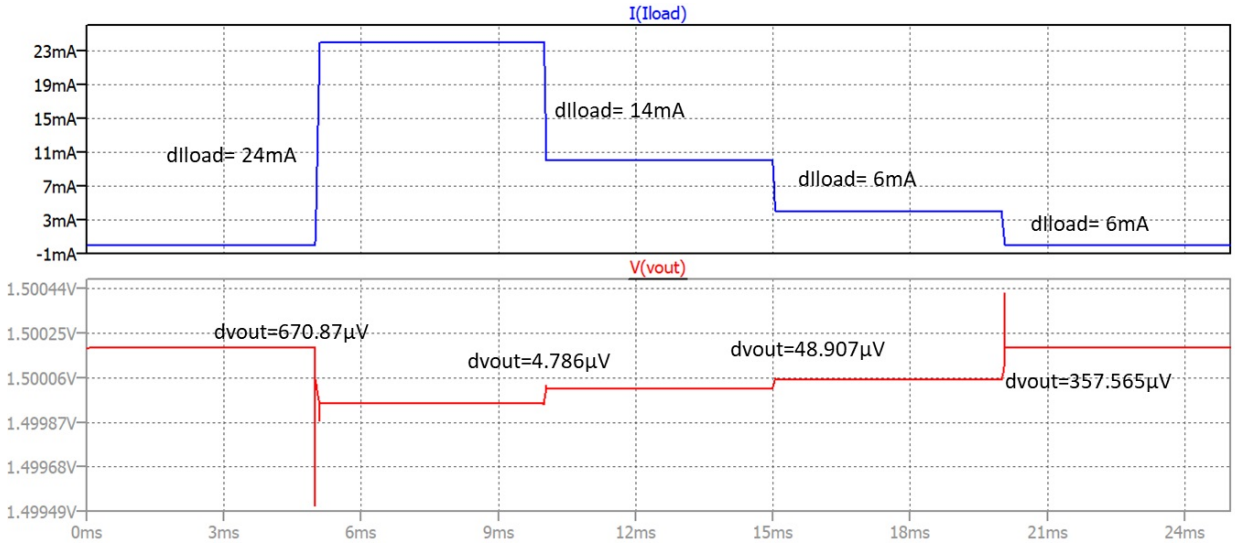

Fig. 9: Load Transient Response of LDO

Load regulation is measured by the LDO's ability to maintain the specified output under varying load conditions [2], [3].

$$LoadRegulation = \Delta V_{OUT}/\Delta I_{OUT} \quad (2)$$

The LDO produces an output voltage of 1.5V when supplied with an input voltage of 1.8V and an output voltage of 1.1V when supplied with an input voltage of 1.2V, exhibiting a dropout voltage of 60.8mV and 70mV respectively, as shown in Fig. 6. The DC load regulation is found to be 9.809 μV/mA, as presented in Fig. 7.

2) Transient Line Regulation : The transient line regulation response evaluates the LDO's ability to handle sudden changes in the input voltage while maintaining a stable and regulated output voltage. This parameter is vital for applications where the input power source may experience fluctuations, and reliable voltage regulation is necessary for proper operation. The line transient regulation of this LDO is 0.3 mV/V, as shown in Fig. 8.

3) Transient Load Regulation : The transient load regulation response of the LDO refers to how quickly and accurately the regulator can adjust its output voltage in response to sudden changes in the load current. Load transient response is a critical parameter in power supply design, especially in applications where the load current can vary rapidly. This is essential for applications where maintaining a constant and precise output voltage is critical for the proper functioning of electronic circuits. The load transient regulation of this LDO is 0.34 μV/mA, as shown in Fig. 9.

Table IV summarises the performance of the LDO and compares with the relevant published works.

4) Power Supply Rejection Ratio: The performance of the LDO is discussed in this subsection. The power supply rejection ratio (PSRR) of the proposed LDO is -29.8dB at

TABLE IV: Performance summary of the proposed LDO and its comparison

	[7]	*[8]*	*[9]*	*[10]*	*[11]*	***Proposed Work-I***	***Proposed Work-II***
	2020	2020	2021	2022	2022		
Technology [nm]	180	180	180	180	180	180	180
V_{in} (V)	1.8	1.4	1.8	1.8	1.8	1.8	1.2
V_{out} (V)	1.6	1.2	1.65	1.6	1.6	1.5	1.1
$I_{\text{L,max}}$ (mA)	50	150	50	200	50	24	24
Minimum I_Q (μA)	1.6	13.5	11	48	2.5	225	225
ΔV_{out} (mV)	26.25	37	-	76	30.75	0.670	1.18
C_L (pF)	1000	4700	4700	1000	1000	10	10
Load Reg (μV/mA)	0.32	0.075	-	0.211	0.41	0.34	0.049
Line Reg. (mV/V)	7.2	7.785	4	2.025	36.8	0.3	0.222
PSRR (dB) (@Hz)	-21 (10k)	-60 (10k)	-37 (100k)	-47 (1k)	-36 (10k)	-29.8 (100K)	-29.8 (100k)

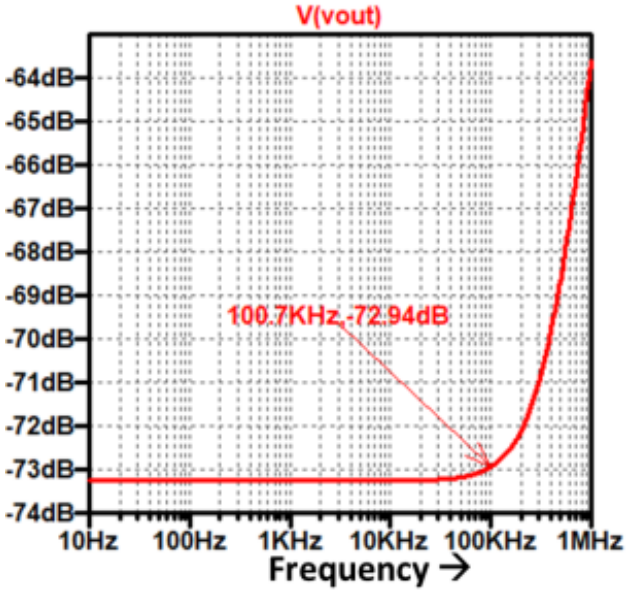

Fig. 10: PSRR of the proposed LDO

100 kHz as shown in Fig. 10.

C. Challenges with Open Source Tools

Open-source software presents a double-edged sword for users. While offering advantages like cost-effectiveness and customization [12], it also comes with inherent challenges compared to its proprietary counterparts. Firstly, open-source tools often lack dedicated customer support, relying instead on the user community for assistance. While online forums can be helpful, troubleshooting issues or finding answers to specific questions can demand significant user effort compared to readily available support channels offered by proprietary software vendors.

Furthermore, while open-source projects are constantly evolving, they may not always offer the same feature set as their commercially developed counterparts. This aspect can be a crucial deciding factor for users depending on their specific needs and the complexity of their tasks. Open-source tools can be valuable resources for circuit design and simulation, offering accurate results for many applications. However, it's important to be aware of their potential limitations in terms of model availability, user expertise requirements, and suitability for complex circuits. Careful selection of tools, models, and thorough verification and validation practices are essential for ensuring reliable simulation results with open-source software.

CONCLUSION

This paper presented a novel low-dropout regulator (LDO) design targeted for dual-supply applications using a cost-effective 180nm CMOS process. The LDO offers two configurations, enabling output voltages of 1.5V (Design I) and 1.1V (Design II) with corresponding input voltages of 1.8V and 1.2V respectively.

The proposed design demonstrates excellent transient response characteristics, achieving a maximum undershoot of only 669μV during load current variations. This combination of low dropout voltage, exceptional transient response, and minimal power consumption makes the LDO well-suited for portable and battery-powered devices where efficient power management is critical. Future work may explore further optimization of the LDO's performance and integration possibilities within System-on-Chip (SoC) designs.

REFERENCES

[1] Heebae Kim, Seung Soo Kwak, and Yong Sin Kim, "Ldo regulator optimized on power efficiency and load transient response with voltage damper and body loop feedback," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022, pp. 3571–3574.

[2] Jung Sik Kim, Khurram Javed, and Jeongjin Roh, "Design of a low-power and area-efficient ldo regulator using a negative-r-assisted technique," *IEEE Trans. Circuits Syst. II*, vol. 70, no. 10, pp. 3892–3896, Oct 2023.

[3] Javed S Gaggatur and et.al, "A 0.009mm^2, 0-230mA Wide-range Load Current Output Capacitor-less Low Dropout Regulator for High Bandwidth Memory parallel IOs," in *2022 35th International Conference on VLSI Design (VLSID)*, 2022, pp. 6–10.

[4] Shaheeda F. S. Vajrala and et. al, "An 860MHz - 1960MHz Multi-band Multi-stage Rectifier for RF Energy Harvesting in 130nm CMOS," in *2020 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)*, July 2020, pp. 1–4.

[5] J. S. Gaggatur and M. Machnoor, "Solar-powered spike-based communication system with analog back scatter," in *2015 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, Nov 2015, pp. 127–132.

[6] GS Javed and Gaurab Banerjee, "Time of arrival measurement for indoor distance monitoring in 130-nm cmos," *Measurement*, vol. 146, pp. 372–379, 2019.

[7] X. Zhao L. Dong and Y. Wang, "Design of an adaptively biased low dropout regulator with a current reusing current-mode OTA using an intuitive analysis method," in *IEEE Trans. Power Electron.*, 2020, vol. 35, p. 10477–10488.

[8] X. Ming and et. al, "A high-efficiency and fast-transient low-dropout regulator with adaptive pole tracking frequency compensation technique," in *IEEE Trans. Power Electron.*, 2020, vol. 35, p. 12401–12415.

[9] M. Radfar A. Nakhlestani, S. V. Kaveri and A. Desai, "Low-power area efficient LDO with loop-gain and bandwidth enhancement using non-dominant pole movement technique for IoT applications," in *IEEE Trans. Circuits Syst. II*, 2021, vol. 68, p. 692–696.

[10] Y. Xin S. Li X. Zhao, Q. Zhang and L. Yu, "A high-efficiency fast-transient LDO with low-impedance transient-current enhanced buffer," in *IEEE Trans. Power Electron.*, 2022, vol. 37, p. 8976–8987.

[11] X. Zhao S. Li L. Dong, Q. Zhang and L. Yu, "Multiple adaptive current feedback technique for small-gain stages in adaptively biased low-dropout regulator," in *IEEE Trans. Power Electron.*, 2022, vol. 37, p. 4039–4049.

[12] G S Javed, *Integrated Interfaces for Sensing Applications*, Ph.D. thesis, Indian Institute of Science, Bangalore, 2016.