Low Dropout Regulator Design for Efficient Power Management in Battery-Powered Systems

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Abstract—**This design presents a dual-mode LDO for battery-powered systems, implemented using SKY130 PDK with the open-source tool eSim. The dual-mode LDO addresses requirements for blocks needing programmable outputs, 1.2V (low-power core logic) and 2.4V (IO interface blocks), providing flexibility in delivering optimized voltage for different functional requirements within the SoC. This adaptability allows for efficient power distribution, minimizes noise in sensitive blocks, and supports stable operation across varying supplies.**

Keyword: low drop-out voltage, battery-powered systems, PSRR, quiescent current, load regulation

I. INTRODUCTION

Low dropout (LDO) regulators are crucial in battery-powered devices for maintaining stable output voltage with minimal supply dependence. In systems with diverse functional requirements, a dual-mode LDO offers significant advantages by providing two programmable output voltages—ideal for powering both low-power core logic and high-power IO interfaces. This dual-mode capability allows optimized power distribution, enhanced efficiency, and effective noise isolation across different blocks, making it essential for reliable performance in complex SoCs.

II. BLOCK DIAGRAM OF LDO

The basic block diagram of proposed Low Dropout Regulator (LDO) comprises the following components, as shown in Figure 1:

1. **Error Amplifier:** Compares output voltage to a reference and generates an error signal for regulation.
2. **Pass Transistor:** Controls current flow from input to output, maintaining the desired output voltage with minimal dropout.
3. **Load Capacitor:** Stabilizes output voltage by smoothing fluctuations from varying loads.
4. **Feedback Loop (Negative):** Feeds back part of the output voltage to the error amplifier, enhancing stability and accuracy in regulation.

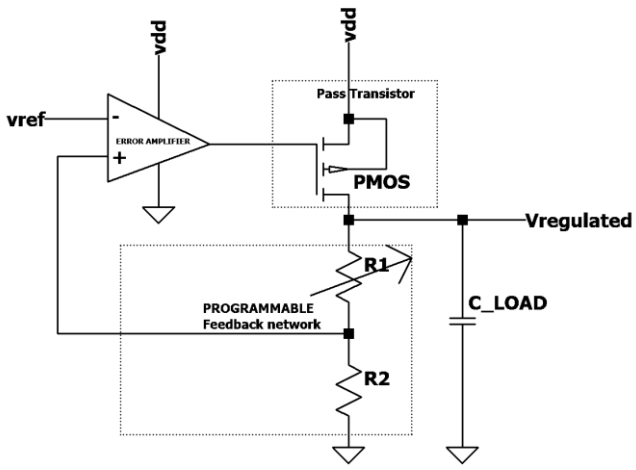

Figure 1: Proposed Block Diagram

III. IMPLEMENTATION (ARCHITECTURE)

The proposed low dropout regulator (LDO) design utilizes the SKY130 PDK to effectively balance power management efficiency and stability for battery-powered systems. The architecture of the LDO comprises several key components, including an error amplifier, a pass transistor, a load capacitor, and a feedback loop.

The error amplifier is configured in a cascode arrangement, to achieve a high open-loop gain, which significantly enhances both regulation accuracy and transient response. A PMOS pass transistor is selected for its low on-resistance, which helps to minimize the dropout voltage. Key performance parameters of LDO mentioned in Table 1.

Table1 : Performance Parameters

Parameter	Design I	Design II
Technology	0.18 µm CMOS	0.18 µm CMOS
Output Voltage	2.4V	1.5V
Line Reg.	3.311mv/v	3.365mv/v
Error Tolerance	±0.75%	±0.8%
VDD Min	2.5V	2.8V
VDD Max	6.2V	6.7541V
VDO	0.9V	1.8V
IQ	160uA	160uA
PSRR @100kHz	30 dB	32.3 dB

IV. ISSUES & IMPROVEMENTS

Transient response is vital in applications with fluctuating load demands, as sudden shifts can cause output fluctuations. Future improvements may involve adaptive quiescent current techniques to optimize power consumption, enhancing efficiency and extending battery life in portable devices.

V. CONCLUSION

In conclusion, this LDO regulator design on the SKY130 PDK platform provides an efficient solution for achieving low dropout voltage, high PSRR, and reduced quiescent current in battery-powered devices. Future work could explore adaptive biasing for better load response, on-chip thermal protection for enhanced reliability, and digital control for dynamic performance adjustments, further optimizing the design for compact, energy-efficient devices.

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