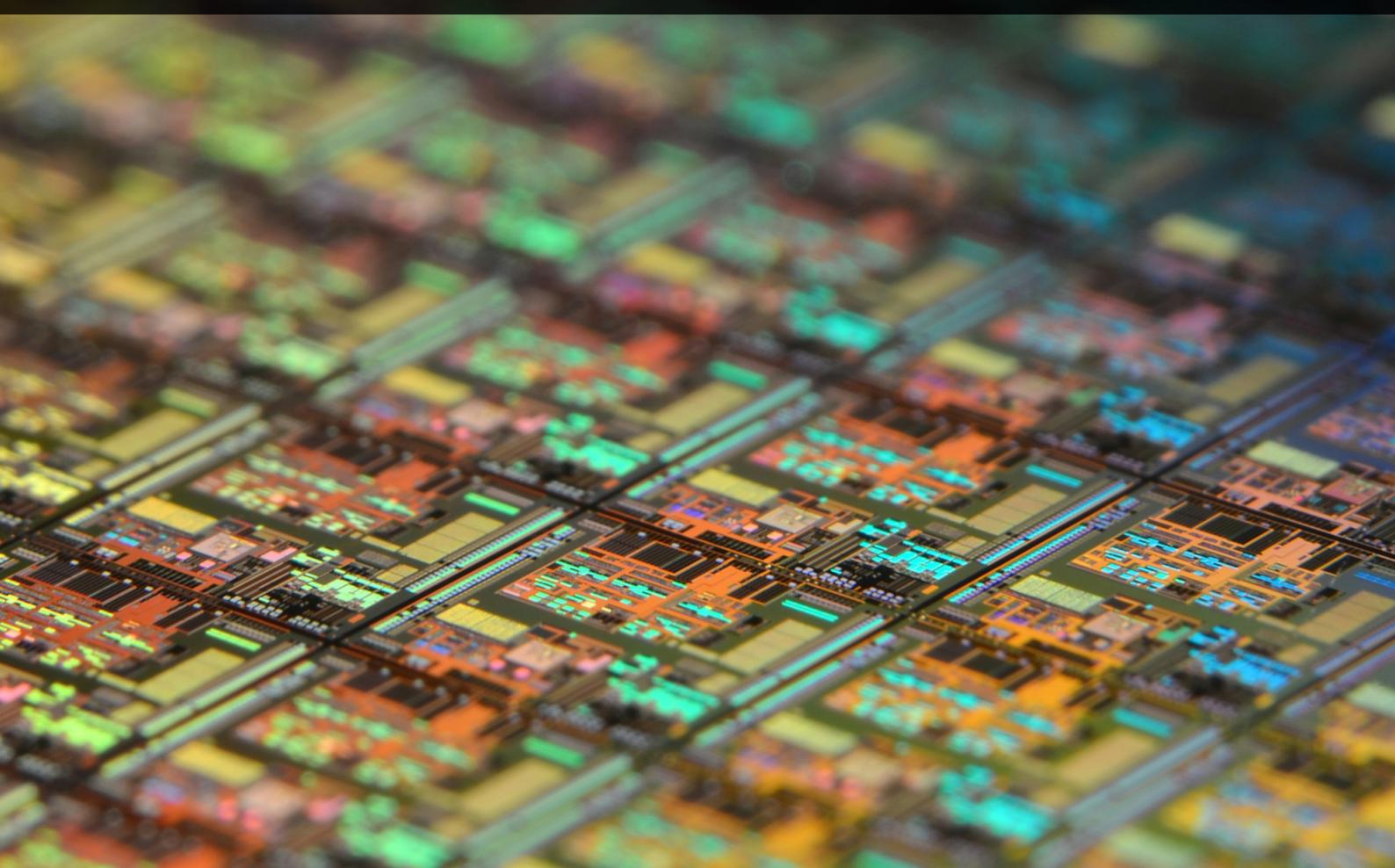


EEG Recording Front-End

Design and Simulation of a Low-Noise, Low-Power, High-Input-Impedance
EEG Front-End in 65nm CMOS Technology



Andreas S. Pedersen

EEG Recording Front-End

Design and Simulation of a Low-Noise, Low-Power, High-Input-Impedance EEG Front-End in 65nm CMOS Technology

Author

Andreas S. Pedersen

Study Number: 202104430

AU-ID: AU666333

Supervisor

Professor Farshad Moradi

Co-Supervisors

Assistant Professor Milad Zamani

Senior Researcher Yasser Rezaeian

A project presented for the degree of
Bachelor of Science
in Electrical Engineering
(15 ECTS)

Department of ECE
Aarhus University
Denmark
June 8, 2024

THIS PAGE LEFT INTENTIONALLY BLANK

1 | Acknowledgements

I would like to thank my dear friend and colleague for this project *Phillip Ferreira Baade-Pedersen*. Together we worked on designing the entire analog front-end. Phillip was responsible for designing the SAR ADC, and without the sparring between us, the project would not have been as successful.

Additionally I would also like to thank [Hossein Esmailbeygi](#) for his technical guidance for Cadence Virtuoso, as well as his expertise regarding analog layout and the TSMC65 technology node.

2 | Abstract

As CMOS technology have evolved, transistor sizes have gotten smaller and smaller. This project focuses on analog design in TSMC 65nm technology. Modern "short-channel" MOS devices differ significantly from the classical models used for analysis. The exact failings of the square-law are examined closely, and the g_m/I_D design method is presented as a modern alternative. Two software tools, developed for quick and easy g_m/I_D design space exploration, are used to size devices. Special techniques for creating resistor equivalents in CMOS technology, such as subthreshold pseudo-resistors and switched-capacitor resistor equivalents, are used for bias networks and setting filter poles.

The project aims to design and implement the analog part of a general purpose analog-to-digital front-end, capable of measuring EEG signals. The front-end consists of a low-noise neural amplifier (NA), a 2nd order programmable gain low-pass filter (LPF) for filtering out higher frequency noise, and a sample-and-hold circuit (S/H) for holding the signal during ADC conversion. Results from three different amplifier structures are presented, a single-stage "three-mirror OTA", a basic two-stage amplifier employing a low-voltage cascode current mirror, and a two-stage rail-to-rail input folded cascode amplifier. Special attention is given to distortion, noise, and power while ensuring sufficient phase margin for stable operation. In total 5 different amplifiers were designed.

Using a three-mirror OTA as neural amplifier, the analog front-end achieves a programmable gain between 60dB and 80dB, a *signal-to-noise ratio* of 56dB for a *effective number of bits* of 8.76. When put together with the ADC, the total power consumption was $14.9\mu\text{W}$, for a ENOB of 8.41.

Contents

| | |
|--|-----------|
| 1 Acknowledgements | I |
| 2 Abstract | II |
| 3 Introduction | 1 |
| 4 MOS Device Design | 2 |
| 4.1 Long-Channel Model | 2 |
| 4.1.1 Limitations | 2 |
| 4.2 Transistor Efficiency | 3 |
| 4.2.1 Transconductance Versus Speed | 3 |
| 4.2.2 Transconductance Versus Noise | 3 |
| 4.3 Inversion Level | 4 |
| 4.3.1 Weak Inversion (Sub-Threshold) | 4 |
| 4.3.2 Strong Inversion | 5 |
| 4.3.3 Moderate Inversion | 5 |
| 4.4 MOS Design Variables | 5 |
| 4.4.1 Source-Body Voltage | 5 |
| 4.4.2 Drain-Source Voltage | 5 |
| 4.4.3 Gate-Source Voltage | 6 |
| 4.4.4 Length | 6 |
| 4.4.5 Width | 6 |
| 4.5 gm/ID Methodology | 7 |
| 4.5.1 Look-Up Tables | 7 |
| 4.6 Tools | 8 |
| 4.6.1 Analog Explorer | 8 |
| 4.6.2 Analog Designer | 8 |
| 5 System Analysis | 9 |
| 5.1 EEG Signals | 9 |
| 5.2 Considerations | 10 |
| 5.2.1 Analog-to-Digital Converter | 10 |
| 5.2.2 Gain | 11 |
| 5.2.3 Gain Bandwidth (GBW) | 11 |
| 5.2.4 Noise | 12 |
| 6 Passive Devices and Equivalents | 13 |
| 6.1 Resistors | 13 |
| 6.1.1 Resistor Variance | 13 |
| 6.2 Pseudo-Resistors | 14 |
| 6.2.1 Results | 14 |
| 6.3 Switched-Capacitor Circuits | 15 |
| 6.3.1 Integrated Circuit Capacitors | 15 |
| 6.3.2 Switches | 15 |

| | | |
|-----------|---|-----------|
| 6.3.3 | Operation and Analysis | 16 |
| 6.3.4 | Parasitic-Insensitive Switched-Capacitor Equivalent Resistors | 16 |
| 6.3.5 | Non-Overlapping Clocks | 16 |
| 7 | Three-Mirror OTA | 17 |
| 7.1 | Analysis | 17 |
| 7.2 | Design | 18 |
| 7.2.1 | Buffer | 19 |
| 7.3 | Results | 20 |
| 7.4 | Results (Buffer) | 22 |
| 8 | Two-Stage Amplifier | 23 |
| 8.1 | Introduction | 23 |
| 8.2 | Analysis | 24 |
| 8.2.1 | Without Compensation | 24 |
| 8.2.2 | Dominant-Pole Compensation | 24 |
| 8.2.3 | Analysis With Compensation | 24 |
| 8.3 | Design | 25 |
| 8.3.1 | Two-Stage LP | 25 |
| 8.3.2 | Two-Stage LN | 26 |
| 8.4 | Low-Power Results | 27 |
| 8.5 | Low-Noise Results | 29 |
| 9 | Folded Cascode Amplifier | 31 |
| 9.1 | Analysis | 31 |
| 9.2 | Design Procedure | 32 |
| 9.3 | Results | 33 |
| 10 | Layout | 35 |
| 10.1 | Basic Layout Considerations | 35 |
| 10.2 | Techniques | 35 |
| 10.2.1 | Multifinger Devices | 35 |
| 10.2.2 | Symmetry | 35 |
| 10.3 | Two-Stage Layout | 36 |
| 10.3.1 | Post-Layout Simulation | 36 |
| 11 | System Design | 38 |
| 11.1 | Neural Amplifier | 38 |
| 11.2 | Low-Pass Filter | 38 |
| 11.2.1 | Programmable Gain Amplifier (PGA) | 39 |
| 11.3 | Sample and Hold | 40 |
| 11.4 | Results | 40 |
| 12 | Results | 41 |
| 13 | Conclusion | 42 |
| 14 | References | 43 |
| A | Github | 48 |
| B | PGA Gain Settings | 48 |

3 | Introduction

In today's world, electronic circuits dominate our everyday lives. They are present in our smartphones, computers, cars, hospitals, and more. Ever since the invention of the first transistor, the need for complex electronic circuits has increased; the future seems to hold even higher demands. As the world focuses more on climate change and sustainability, combined with a higher demand for more compact, portable circuits, energy efficiency has become a key factor. The world is inherently analog; signals, whether electronic or not, are continuous in time and amplitude. While digital devices dominate our everyday lives in the form of computers and smartphones, their increasing use to interface with the 'real' world has heightened the need for high-performing analog circuits.

The invention of the *integrated circuit* (IC) is arguably what led to the microelectronic revolution. Often associated with large-scale digital circuits such as microprocessors, the integrated circuit is also the foundation for modern analog circuits - allowing tightly controlled manufacturing and matching of devices. There is, however, a conflict of interest regarding the evolution of integrated circuit manufacturing. Digital *Very Large Scale Integration* (VLSI) circuits demand transistor density and speed above all else. Due to the switching nature of transistor devices in digital circuits, analog performance is often degraded on newer technologies, challenging analog designers.

Sometimes referred to as *nanometer design*, the design of analog circuits on modern technologies is a challenging task. Classical models of transistors lose their precision; supply voltage is decreased to prevent breakdown, limiting dynamic range; gate threshold is lowered to compensate, muddling the line between operating regions. Why not just use older technologies, then? Scaling decreases parasitic effects and thereby improves speed, allowing high-speed analog blocks such as ADC's and RF circuitry. The answer is therefore: *it depends*. If a design is simple, older technology nodes are often no worse than modern ones.

With this in mind, analog design is an 'art of compromise' - finding the right balance between performance, power and area. Old-school methods is often iterative and time-consuming. While the aid of *electronic computer-aided design* (ECAD/EDA) and SPICE¹ used in conjunction with modern transistor models such as BSIM² help and can accurately predict circuit behavior; it is up to the designer to find the right operating point for each device to achieve maximum performance.

Due to non-linearity, *Metal-Oxide Semiconductor* (MOS) devices are typically analyzed in a two step process. A large-signal model is used to place terminal voltages/currents for desired operation, whereafter a linearized small-signal model is used to analyze device behavior. Classically, a "long-channel" model is used to approximate large-signal behavior, consisting of the triode region quadratic equation and the saturation-region square-law relation. As devices got smaller, their performance differs significantly from the "long-channel" large-signal model.

While the "long-channel" model is still useful for basic intuition, it is simply not accurate enough for modern devices. Models that more accurately describe device behavior have too many parameters to be useful for hand analysis. Instead SPICE simulated performance is introduced during the hand-analysis stage. Using look-up tables (LUT), the g_m/I_D method is used to accurately size and predict device behavior.

¹"Simulation Program with Integrated Circuit Emphasis"

²Berkeley Short-Channel IGFET Model - Currently on its 4th iteration (BSIM4). More than 180 model parameters [12].

4 | MOS Device Design

In this chapter we will explore theory and methods for sizing MOS devices for optimal circuit performance. Starting with the square-law, we will identify its shortcomings, taking in real data from TSMC65 devices, after which we will introduce the more modern g_m/I_D approach.

Starting by defining a critical parameter, *transistor efficiency* ($TE = g_m/I_D$), the ratio between g_m and the bias current needed to achieve it. It is figure of merit representing the trade-off between transconductance and quiescent current. As will be seen later, it also serves as an indicator for other design decisions.

4.1 • Long-Channel Model

Consider a "long-channel" NMOS device. When a sufficiently positive V_{GS} is applied, an *inversion layer* (channel) is formed. This inversion layer appears when $V_{GS} > V_{TH}$, allowing conduction. The V_{GS} is often thought of as V_{TH} plus some *overdrive voltage* V_{OV} . Depending on V_{DS} , there are two scenarios:

- $V_{DS} < V_{OV}$: the device is in the *triode region*, where drain current follows a quadratic relationship.
- $V_{DS} > V_{OV}$: the channel is "pinched-off", operating the device in *saturation*, where the drain current follows a square relationship.

Defining a process parameter $K_p = \mu_n C_{ox}$ and assuming no second-order effects, drain current and transconductance in the long-channel model in triode and saturation:

$$I_{DS} = \frac{1}{2} K_p \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2], \quad g_m = K_p \frac{W}{L} V_{DS} \quad (\text{triode})$$

$$I_{DS} = \frac{1}{2} K_p \frac{W}{L} (V_{GS} - V_{TH})^2, \quad g_m = K_p \frac{W}{L} (V_{GS} - V_{TH}) \quad (\text{saturation})$$

4.1.1 Limitations

The saturation square-law for I_D fits a long-channel device well, but differs from actual device characteristics at higher overdrive [Figure 4.1]. The g_m increases with overdrive for both a short- and long-channel device, but tapers off at some point due to second order effects [Figure 4.2], it is not possible to increase transconductance by simply "overdriving" it. The square-law *fails* at strong inversion.

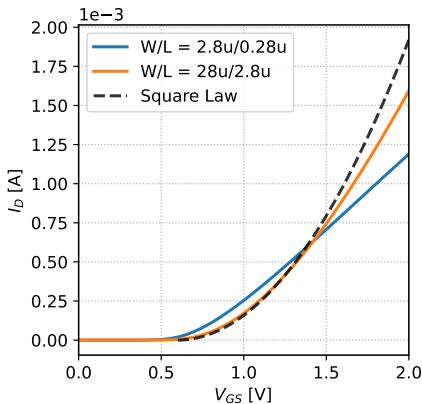


Figure 4.1: Square-law I_D (best-fit) versus short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$

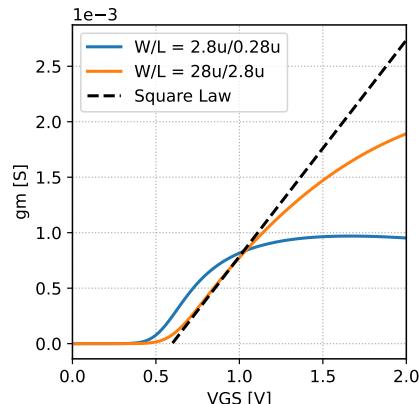


Figure 4.2: Square-law g_m (best-fit) versus short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$

For a short-channel device in strong inversion, the drain current no longer has a square relationship with V_{GS} , more like a linear dependence. Since g_m is simply the slope of I_D , it no longer grows linearly but flattens out and becomes "saturated" at high overdrive. How about transistor efficiency? From (4.1) the square-law predicts a nearly **infinite** $TE = g_m/I_D$ at low overdrive [Figure 4.3] which, unfortunately, is not the case. The square-law fails for both short and long-channel devices at weak inversion.

$$\frac{g_m}{I_D} = \frac{K_p \frac{W}{L} V_{OV}}{\frac{1}{2} K_p \frac{W}{L} V_{OV}^2} = \frac{2}{V_{OV}} = \frac{2}{V_{GS} - V_{TH}} \quad (4.1)$$

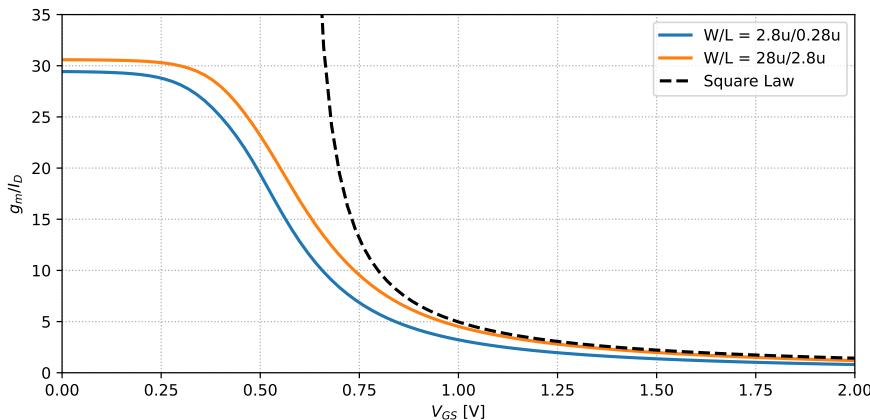


Figure 4.3: g_m/I_D vs V_{GS} for a short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$.

4.2 • Transistor Efficiency

Transconductance is a critical parameter for MOS devices. It is a measure of how well the device converts a gate voltage to a drain current. It is of high importance due to its significance in terms of speed, gain and noise. As will be seen in [Chapter 4.3] it is also an indicator of operation region.

4.2.1 Transconductance Versus Speed

The intrinsic gain of an ideal MOS device is simply $A_V = g_m r_O$. Placing a load capacitor C_L at the output, a low-pass filter is formed by r_O and C_L with a single pole at $\omega_p = 1/r_O C_L$ defining the bandwidth. As seen in (4.2) the gain-bandwidth product, which is a measure of circuit speed, depends only upon g_m .

$$GBW = \frac{g_m r_O}{r_O C_L} = \frac{g_m}{C_L} \quad (4.2)$$

4.2.2 Transconductance Versus Noise

MOS devices exhibit two types of noise: thermal noise and flicker noise. Flicker noise scales inversely with device area WL . Thermal noise on the other hand scales inversely with g_m . Consider the total input-referred noise voltage of a common-source stage with an ideal current source load (4.3) [12]. As g_m increases, the first term (thermal noise) decreases.

$$\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_m} + \frac{K}{C_{ox}WL} \frac{1}{f} \quad (4.3)$$

4.3 • Inversion Level

For a MOS device, the transistor efficiency $\text{TE} = g_m/I_D$ depends on the bias point. The value of g_m/I_D indicates the inversion level and therefore what region the device is operating in. Some rough boundaries are shown in Table 4.1.

| TE | Inversion |
|------------------------|--------------------|
| $g_m/I_D \geq 20$ | Weak inversion |
| $20 > g_m/I_D \geq 10$ | Moderate inversion |
| $10 > g_m/I_D$ | Strong inversion |

Table 4.1: Inversion level depending on g_m/I_D

Each inversion level has its own advantages and disadvantages. Weak inversion corresponds to sub-threshold operation, strong inversion corresponds to saturation. Moderate inversion is a mix of the two and is of particular interest for low-power designs where speed and power both are valued.

4.3.1 Weak Inversion (Sub-Threshold)

When $V_{GS} < V_{TH}$ the device is in weak inversion, classically considered as simply "off". In reality the device will still conduct small currents. The log of the drain current has a linear dependence on V_{GS} , indicating exponential growth [Figure 4.4].

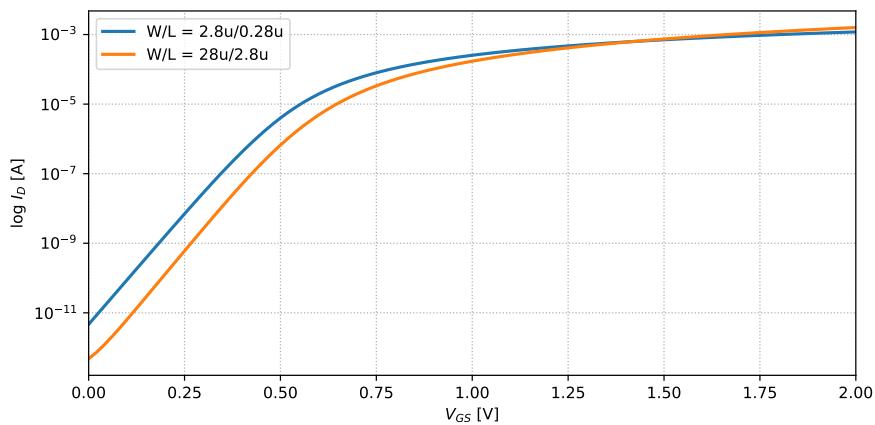


Figure 4.4: $\log I_D$ vs V_{GS} for a short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2\text{V}$.

The exponential behavior is similar to the I_C vs V_{BE} for the BJT. Due to $V_{GS} < V_{TH}$ a channel has not yet formed. The small V_{GS} simply gets rid of the holes in the p-type substrate. A subthreshold MOS device is then simply a NPN junction i.e. a BJT, with the base coupled to the gate and body through the gate oxide capacitor C_{ox} and the body capacitance C_{dep} . The "pseudo"-BJT has base-emitter voltage (4.4)

$$V_{BE} = V_{GS} \frac{C_{ox}}{C_{ox} + C_{dep}} = \frac{V_{GS}}{n}, \quad n > 1 \quad (4.4)$$

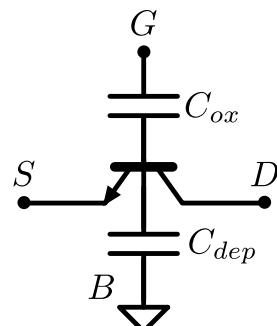


Figure 4.5: MOS device in weak inversion.

The "drain" current of the BJT has an exponential relationship with V_{BE} . Since g_m is the slope of an exponential I_D , g_m is also exponential (4.5).

$$I_D = I_S \exp\left(\frac{V_{GS}}{nV_T}\right), \quad g_m = \frac{I_S \exp\left(\frac{V_{GS}}{nV_T}\right)}{nV_T} = \frac{I_D}{nV_T} \quad (4.5)$$

From (4.5) it becomes apparent that the g_m/I_D in weak inversion is $1/nV_T$ i.e. constant. The weak inversion region offers constant *high* g_m/I_D . To keep the same g_m/I_D with increasing I_D in subthreshold, you need exponentially increasing device width, becoming impractical and slow. Note that the early effect is explicitly ignored in (4.5).

4.3.2 Strong Inversion

In strong inversion the channel is pinched-off, operating the device in what is typically considered saturation. Strong inversion offers high speed due to small device sizes, but at the cost of transistor efficiency. Strong inversion also suffers from significant flicker noise due to small device area.

4.3.3 Moderate Inversion

Weak inversion offers high g_m , but at the cost of increased width and parasitics. Strong inversion offers speed, but at the cost of g_m and therefore power consumption. Moderate inversion offers a compromise between the two. The g_m/I_D is still significantly higher than strong inversion giving high intrinsic gain. Moderate inversion still sacrifices some speed, but modern transistors are fast enough that this is mostly not an issue. Moderate inversion is often a good "sweet spot", and many devices in the following pages are biased in this region. The only problem with moderate inversion is the lack of accurate models *simple enough for hand analysis*.

4.4 • MOS Design Variables

Sizing a MOS device is a function with 5 *Degrees of Freedom* (DOF) [16], three voltages and two dimensions [Table 4.2].

| DOF | | | |
|------------|----------|----------|----------|
| Voltages | V_{DS} | V_{GS} | V_{SB} |
| Dimensions | W | L | |

Table 4.2: Degrees of Freedom for sizing a MOS device

4.4.1 Source-Body Voltage

Arguably the least important *degree of freedom*, the source-body voltage causes *body effect*, giving rise to a non-linearity in V_{TH} . If the body is biased higher than the source, V_{TH} increases, and vice versa. If a transistor is in a dedicated n-well, then the body can simply be tied to source to cancel the body effect. Typically n-type devices are not in a dedicated n-well, and body is then tied to the lowest potential in the circuit. In summary, V_{SB} is not an important DOF. If possible the body is tied to source, if not the designer must live with a small degree of body effect [16].

4.4.2 Drain-Source Voltage

From the ideal square-law in saturation and triode the V_{DS} does not affect the drain current. In reality due to the Early Voltage (V_A) caused by *Channel Length Modulation* and *Drain-Induced Barrier Lowering* (DIBL) [12] the V_{DS} has a significant impact on drain current and overall device characteristics [Figure 4.6]. Modelled by $r_O = V_A/I_D$, an increase in V_A means a larger r_O . To get a large r_O , and therefore high intrinsic gain, the device can not be operating on the edge of saturation.

Early Voltage also scales with device length, keeping in mind that scaling only L in a vacuum moves the device closer to the edge of saturation. In weak inversion, assuming I_S constant for I_C in (4.5), the early-effect is modelled by including the factor $(1 + V_{CE}/V_A)$ [13]. Translating (4.5) with early-effect to an expression relating only to MOS parameters (in subthreshold) (4.6) [12].

$$I_D = \mu C_{dep} \frac{W}{L} V_T^2 \left(\exp \frac{V_{GS} - V_{TH}}{nV_T} \right) \left(1 - \exp \frac{-V_{DS}}{V_T} \right) \quad (4.6)$$

As V_{DS} exceeds only a few V_T the drain current becomes nearly independent of drain-source voltage. It is therefore important to ensure sufficient V_{DS} for subthreshold devices to reduce non-linearity. Overall V_{DS} is an important parameter for device behavior, but is often imposed by the circuit and thereby not a DOF the designer has much control over.

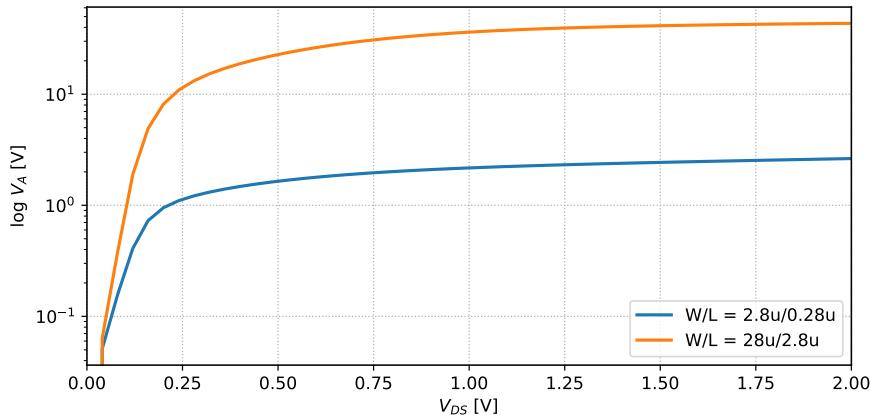


Figure 4.6: V_A versus V_{DS} for short and long channel TSMC65 device (nch_25) @ $V_{GS} = 0.6V$.

4.4.3 Gate-Source Voltage

Gate-source voltage V_{GS} is by far the most important voltage parameter. The drain current is only a "weak" function of V_{DS} and V_{SB} , but is **strongly** dependent on V_{GS} . It is, however, rare to size devices after a specific V_{GS} . Classically a particular I_D is set, and the V_{GS} is then determined from the square-law.

4.4.4 Length

The length L directly affects the trade-off between *speed* and *gain*. A shorter length is chosen for devices where small parasitic capacitances and speed (f_T) is important. A longer length is chosen for devices where $r_O = V_A/I_D$ is important [Figure 4.6]. A larger L also improves flicker noise due to increasing the total device area WL .

4.4.5 Width

Width is the DOF where the designer has the largest freedom. The choice of W depends on nearly all aspects of the design: desired g_m/I_D , speed, noise and length. It can range from submicron levels to several hundreds of μm . Once a width have been chosen, changes to L or I_D affects g_m/I_D and significantly changes device behavior. Improving circuit performance often becomes a dance of "chasing the right W " [16].

Typically to circumvent the difficult choice of W , designers used overdrive as the main DOF instead. Choosing a V_{OV} that results in a desired I_D and TE, and compute W from that using the square-law. However, as seen in [Chapter 4.1], the square-law is simply not accurate enough, resulting in a very iterative process after the initial choice of W . In addition while V_{OV} indicates the operating region, it does not give any indication of speed, gain or noise, leaving the designer in the dark.

4.5 • gm/ID Methodology

To circumvent the limitations of the square-law, the g_m/I_D method is used. Instead of using W or V_{OV} as a main DOF, the transistor efficiency g_m/I_D is used, after which the right W is found from a *look-up table* (LUT). Doing this dramatically reduces the number of DOF to be considered. V_{SB} is often negligible, V_{DS} is imposed by the circuit, and V_{GS} has a direct relationship with g_m/I_D . The only remaining DOF are then g_m/I_D and L .

Almost all MOS parameters are proportional in some way to W . By storing SPICE simulated parameters from a reference device, it is possible to cross-multiply out the dependency on W , resulting in several width-independent *Figure of Merits* (4.7) [14].

$$\text{TE} = \frac{g_m}{I_D}, \quad f_T = \frac{g_m}{2\pi C_{gg}}, \quad g_m r_O = \frac{g_m}{g_{ds}}, \quad V_A = \frac{I_D}{g_{ds}} \quad (4.7)$$

A small g_m/I_D (strong inversion) translates to a low g_m (low gain), low parasitic capacitances (speed), and are often used for devices that do not contribute to gain. A large g_m/I_D (moderate/weak inversion) translates to a high g_m for the given drain current (high gain), low flicker noise (high WL), large input/output range $V_{DS,sat} \approx 2/(g_m/I_D)$, and are often used for devices that contribute to gain.

4.5.1 Look-Up Tables

To accurately size devices using g_m/I_D a LUT is needed. The LUT is created by simulating a reference device with varying L and V_{DS} , and using that to quickly find suitable operating points and the required W for a desired g_m/I_D . A LUT created by *Analog Explorer* [Chapter 4.6] is seen in [Figure 4.7].

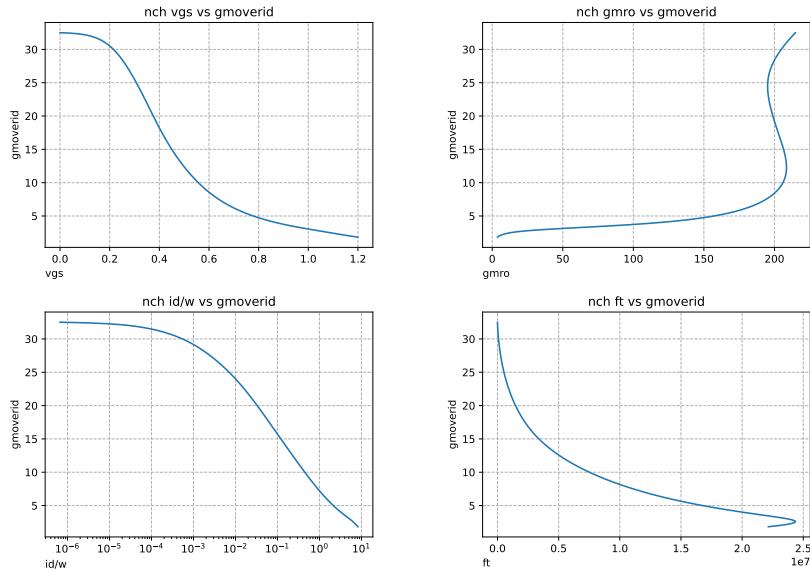


Figure 4.7: Example LUT for TSMC65 nch @ $V_{DS} = 0.6V$, $L = 10\mu m$

Assuming a reference device has width W_{REF} , the width is extracted from the g_m/I_D versus $I_N = I_D/W_{REF}$ plot. To determine the width for a desired g_m/I_D with known drain current (4.8).

$$W = \frac{I_D}{I_N} \quad (4.8)$$

4.6 • Tools

To streamline the g_m/I_D process two software tools were developed in conjunction with the project. The reader is highly encouraged to check out the authors Github page for the latest version of the tools [Appendix A].

4.6.1 Analog Explorer

Choosing the right transistor and its operating point involves cross checking several characteristics for a given g_m/I_D value e.g. V_{GS} , $V_{DS,sat}$, $g_m r_O$, etc.. This is a rather tedious task, especially considering the number of graphs and plots quickly multiplies if accurate values for different gate lengths and V_{DS} is wanted. To help with this *Analog Explorer* was developed alongside the project.

Analog Explorer is Graphical User Interface (GUI) [Figure 4.8] written in Python that parses transistor models generated using SPICE and is capable of plotting parameters of interest. The tool allows quick and easy design space exploration for a given device. It vastly streamlines the g_m/I_D process. After a suitable device and operating point is chosen, the designer can extract width and accurate values for relevant figure of merits (4.7). All circuits in this project were designed using *Analog Explorer*.

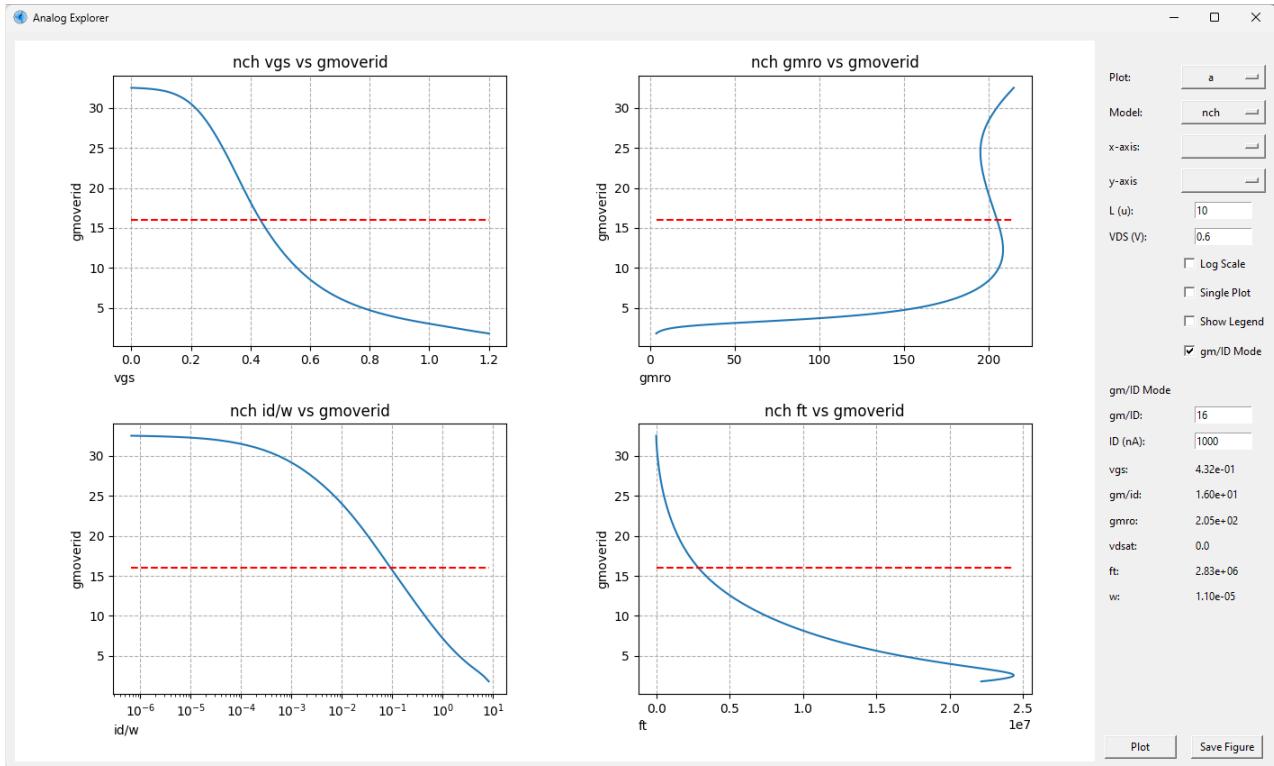


Figure 4.8: Sizing a TSMC65 nch transistor at moderate inversion with $I_D = 1\mu\text{A}$.

4.6.2 Analog Designer

The TSMC65 device look-up tables are further utilized by *Analog Designer*. A collection of Python classes that accurately describe MOS devices and various circuit topologies. *Analog Designer* takes in topology specific parameters such as I_{tail} and C_L , device operating points given in g_m/I_D , and quickly calculates accurate values for circuit parameters such as gain, pole frequencies, power consumption, as well as computing all required device widths. In addition the tool is also capable of generating a fairly accurate AC response in the form of a Bode plot.

5 | System Analysis

The EEG front-end consists of four main stages, of which the first three are purely analog and will be designed in this project.

1. *Neural Amplifier* (NA) which amplifies the raw incoming signal.
2. *Low-Pass Filter* (LPF) which filters out high-frequency noise and amplifies the signal further.
3. *Sample-and-Hold* (S/H) circuit which samples the signal at a fixed frequency.
4. *Analog-To-Digital Converter* (ADC) which converts the analog signal to a digital signal.

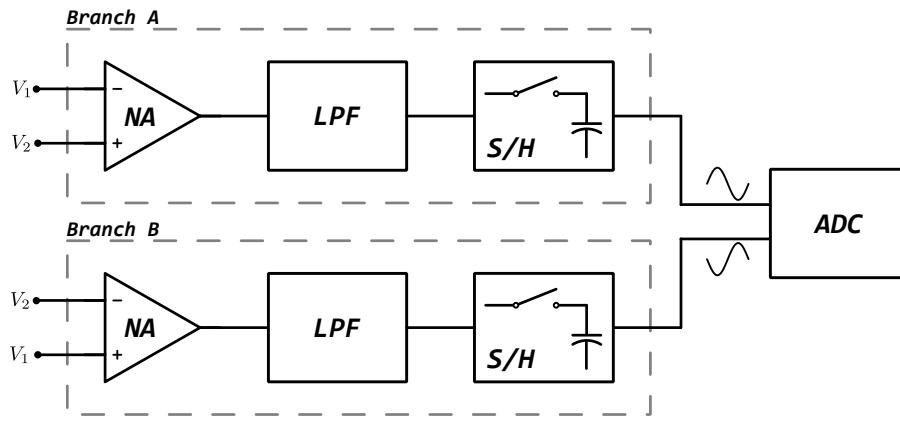


Figure 5.1: System Overview

5.1 • EEG Signals

Neural signals consist of slow *Local Field Potentials* (LFP) ranging from 0.1Hz to 100Hz with amplitudes from $1\mu\text{V}$ to 1mV , and faster *Action Potentials* (AP) ranging from 100Hz to 5kHz [Figure 5.2] [4]. EEG is measured from outside the skull, lowering the bandwidth (Typically $< 100\text{Hz}$). A bandwidth of 1kHz is targeted to make the system more general purpose. An amplitude between $100\mu\text{V}$ to 1mV is assumed.

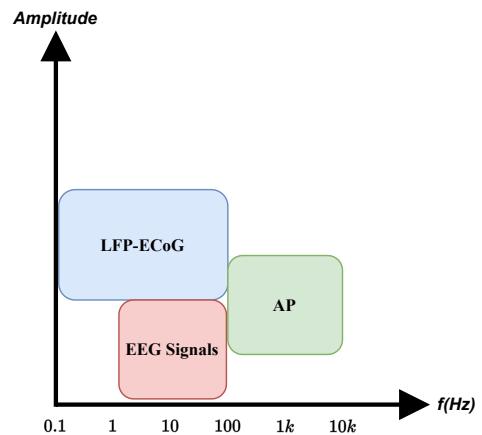


Figure 5.2: Amplitude and frequency characteristics of neural signals. [3] [6]

5.2 • Considerations

The project will be designed for the TSMC65 technology node with a supply voltage of 1.2V. The neural amplifier should ideally amplify the highest amplitude signal to a "full-swing" signal to ensure best possible resolution.

5.2.1 Analog-to-Digital Converter

Analog signals represent the real world and are continuous in time and amplitude. They are, however, also very sensitive to noise and difficult to process. The last part in the front-end is an ADC, which converts the signal to digital. Digital signals are less sensitive to noise, can be reliably stored, and are easier to process (DSP).

The block diagram of an ADC is shown in [Figure 5.3]. V_{in} and V_{ref} are analog input and reference voltages respectively. The ADC outputs a N bit word B_{out} . V_{LSB} is defined to be the analog voltage change corresponding to a single *Least Significant Bit* (LSB). The signals are related by (5.1) [11].

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \dots + b_N 2^{-N}) = V_{in} \pm V_X \quad (5.1)$$

where V_X is given by (5.2). There is a range of input values giving the same output word B_{out} .

$$-\frac{1}{2}V_{LSB} \leq V_X \leq \frac{1}{2}V_{LSB} \quad (5.2)$$

A transfer curve for a 2-bit ADC is shown in [Figure 5.4]. The transitions along the x-axis are shifted by $1/2V_{LSB}$. This way V_{in} has some "wiggle room" before a transition is seen on the output. The task at hand for the analog front-end, is to ensure as best as possible, that noise, non-linearity and gain errors are kept within $1/2V_{LSB}$, as they will then not be seen in B_{out} . The ADC is $N = 10$ bit and takes a differential input. The voltage V_{LSB} is given by (5.3).

$$V_{LSB} = \frac{2V_{REF}}{2^N} = \frac{2.4V}{1024} = 2.34mV \quad (5.3)$$

Analog to Digital converters have a number of specifications for quantifying the noise and distortion performance. In no particular order, these are: SINAD (signal-to-noise-and-distortion ratio), ENOB (effective number of bits), SNR (signal-to-noise ratio), THD (total harmonic distortion), THD + N (total harmonic distortion plus noise) and SFDR (spurious free dynamic range) [9]. All of these specifications can also be translated to the amplifiers presented in this project.

Due to circuit non-linearity, *harmonic distortion* occurs at the output of an amplifier. The power of a single harmonic is usually represented in dBc (dB below carrier). Denoting P_S, V_S and P_N, V_N the power/voltage (rms) of the fundamental and of the N th harmonic respectively. The powers of all harmonics summed together and presented as a ratio to the power of fundamental (THD) (5.4).

$$\text{THD} = 10 \log_{10}(P_S) - 10 \log_{10}(P_2 + P_3 + \dots + P_N) = 20 \log_{10} \frac{\sqrt{V_2^2 + V_3^2 + \dots + V_n^2}}{V_S} \quad (5.4)$$

All elements in a circuit generate some form of noise. The SNR is the ratio of the rms signal voltage to the rms noise voltage in dB (5.5) [10].

$$\text{SNR} = 10 \log_{10} \left(\frac{P_S}{P_N} \right) = 20 \log_{10} \left(\frac{\text{rms Signal voltage}}{\text{rms Noise voltage}} \right) \quad (5.5)$$

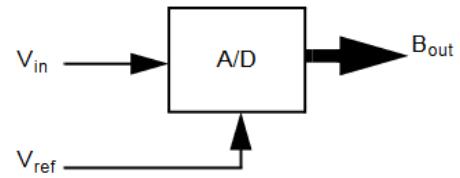


Figure 5.3: ADC block diagram [11].

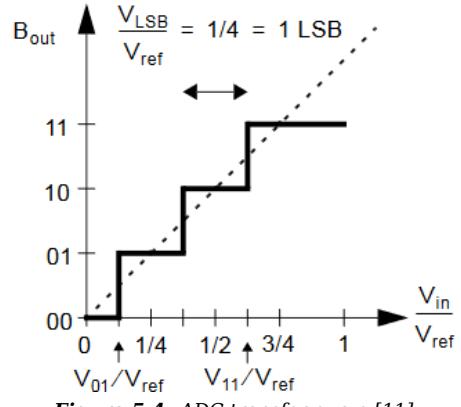


Figure 5.4: ADC transfer curve [11].

THD expresses signal distortion and SNR expresses signal noise. SINAD is a combination of the two and is the ratio of the signal to the sum of all noise and distortion. It is related to THD and SNR by (5.6) [9].

$$\text{SINAD} = -10 \log_{10} \left(10^{-\text{SNR}/10} + 10^{-\text{THD}/10} \right) \quad (5.6)$$

A particular important specification for an ADC is the ENOB. Giving a measure of the effective resolution of the ADC due to noise and distortion. It is derived from SINAD by (5.7).

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (5.7)$$

Due to the definition of ENOB in (5.7), it can also easily be calculated for amplifiers. Ideally the entire analog front-end in this project should have an ENOB of at least 10 bits to make sure the ADC is not limited. Another problem arises regarding the signal swing. The ADC has a maximum differential input voltage of 2.4V, meaning the amplifiers need an actual full-swing output of 1.2V, which is simply not possible at $V_{DD} = 1.2V$ without more exotic structures than those presented in this project. Low V_{DS} for the output devices is a significant source of distortion, and a more modest value for a "full-swing" signal is chosen to be 1V with $V_{CM} = 0.6V$. As the signal level reduces, the SINAD of the ADC decreases, and the ENOB decreases. A correction factor for ENOB can be added to account for this (5.8) [9].

$$\text{ENOB} = \frac{\text{SINAD}_{\text{MEASURED}} - 1.76 \text{dB} + 20 \log_{10} \left(\frac{\text{Fullscale Amplitude}}{\text{Input Amplitude}} \right)}{6.02} \quad (5.8)$$

The theoretical *maximum* SNR of an ADC is directly proportional to the number of bits. The maximum SNR of the 10-bit ADC is given by (5.9) [9].

$$\text{SNR}_{\text{max}} = 6.02N + 1.76 \text{dB} = 6.02 \cdot 10 + 1.76 \text{dB} = 61.96 \text{dB} \quad (5.9)$$

5.2.2 Gain

As shown in [Figure 5.2], the maximum amplitude of a differential neural signal is the LFP at 1mV. Assuming a "full-swing" of 1.0V, leaving a minimum $V_{DS,min} = 100\text{mV}$ for a two transistor output stage, the total gain in the system must be (5.10).

$$A_{sys} = \frac{1\text{V}}{1\text{mV}} = 1000 \approx 60 \text{dB} \quad (5.10)$$

With two-differential "branches", each must then deliver $A_{sys/2} = 500 \approx 54 \text{dB}$.

The higher the closed-loop gain, the easier it is to ensure stability. To reduce power consumption of the NA and the LPF with a guarantee of sufficient phase margin, the total system gain is split between the NA and LPF at 27dB each.

5.2.3 Gain Bandwidth (GBW)

With a bandwidth of 1kHz, sufficient GBW must be ensured to prevent *gain error*. Denoting the gain at some frequency f as A_f and the feedback factor β , the gain error at some frequency f (5.11).

$$(\text{Gain Error})_f = \frac{1}{\beta(1 + \beta A_f)} \quad (5.11)$$

A sufficient GBW must be targeted to ensure the gain error does not get too high at 1kHz. Choosing $A_{1\text{kHz}} = 80 \text{dB}$ and therefore the GBW = 10MHz for the NA and LPF, the maximum gain error (5.12).

$$(\text{Gain Error})_{1\text{kHz}} = \frac{1}{\frac{1}{10^{27/20}}(1 + \frac{1}{10^{27/20}} 10^{80/20})} = 50 \cdot 10^{-3} \quad (5.12)$$

It should be noted that gain error can be partially corrected with two-point calibration at the ADC and is therefore not as critical as distortion and noise.

5.2.4 Noise

MOS devices exhibit two types of noise: *thermal noise* and *flicker noise*. Most of the thermal noise is generated in the channel, and can be modelled as a current source between the drain and source terminals with spectral density (5.13) [12].

$$\overline{I_n^2} = 4kT\gamma g_m \quad (5.13)$$

where k is the Boltzmann constant, T is the temperature in Kelvin, and γ is a process parameter that varies with V_{DS} . The maximum thermal noise occurs if a device sees only its own output impedance as a load, the output noise voltage (5.14) [12].

$$\overline{V_n^2} = \overline{I_n^2}r_O^2 = (4kT\gamma g_m)r_O^2 \quad (5.14)$$

As seen in (5.14) the noise decreases if the g_m decreases. Transconductance must therefore be minimized for current source devices, while it must be maximized for common-source gain devices (4.3). Flicker noise occurs due to the interface between the gate oxide and the silicon substrate and is modelled as a voltage source in series with the gate. In saturation the noise voltage due to flicker noise is (5.15) [12].

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \frac{1}{f} \quad (5.15)$$

where K is a process parameter. Flicker noise is inversely proportional to the frequency, and decreases with device area. The total noise is the sum of the thermal and flicker noise integrated over the bandwidth of interest. Ideally the analog front-end should have a signal-to-noise ratio equal to or better than the ADC (5.9). Assuming a differential configuration, and a maximum differential output amplitude of 1V, the maximum noise rms voltage is shown in (5.16).

$$20 \log_{10} \left(\frac{1V(\sqrt{2})^{-1}}{\overline{V_{n,total}^2} A_{sys}} \right) > 61.96 \text{dB} \quad \Rightarrow \quad \overline{V_{n,total}^2} < 1.13 \mu\text{V}/\sqrt{\text{Hz}} \quad (5.16)$$

Since the noise performance is closely related to the power consumption, a parameter of interest is the *Noise Efficiency Factor* (NEF) (5.17) [7]. Where f_{bw} is the closed-loop 3dB bandwidth.

$$\text{NEF} = \overline{V_{n,rms}} \sqrt{\frac{2I_{tot}}{4V_T k_B T f_{bw} \pi}} \quad (5.17)$$

6 | Passive Devices and Equivalents

Analog circuits often employ passive components such as resistors and capacitors. Unfortunately these components suffer from severe variances and large sizes in most CMOS processes. It is therefore a unique challenge for the designer to compensate for these limitations.

6.1 • Resistors

Modern CMOS technologies often support several different methods for fabricating resistors. The TSMC65 technology node is capable of poly-silicon, diffusion, and metal resistors; with and without *self-aligned silicide* (salicide). An overview of TSMC65 resistors and their resistance per square is shown in Table 6.1.

| Type | Description | Resistance per square (Ω) |
|----------|---------------------------|------------------------------------|
| rnod | N+ diffusion w/ salicide | 15.5 |
| rnodwo | N+ diffusion w/o salicide | 120 |
| rnpoly | N+ poly w/ salicide | 15.1 |
| rnpolywo | N+ poly w/o salicide | 153 |
| rnwod | Nwell under diffusion | 327 |
| rm | Metal | 0.137 |

Table 6.1: Resistor types in TSMC65

The use of salicide creates a lower contact resistance, resulting in a clearer definition of the resistor value. For a low-power design, currents are typically very small, and the required resistance values can typically be in the order of $M\Omega$. This makes it unpractical to use any of the resistor types presented in Table 6.1. For instance, a $100k\Omega$ resistor, where accuracy is non-important, created using a $1\mu M$ wide *rnpolywo*, the length would have to be:

$$L = \frac{RW}{R_{\text{per square}}} = \frac{100k\Omega \cdot 1\mu M}{153\Omega} \approx 654\mu m \quad (6.1)$$

6.1.1 Resistor Variance

Resistors in CMOS processes are subject to high process variances, this is also true for the TSMC65 node. The last column of [Table 6.2] is of particular interest. It shows the maximum \pm percentile (process) variation from the mean which 95% of the resistors fall within.

| Type | Target [Ω] | Min [Ω] | Max [Ω] | Mean [Ω] | Std Dev [Ω] | $\mu \pm 2\sigma$ [$\pm\%$] |
|----------|---------------------|------------------|------------------|-------------------|----------------------|-------------------------------|
| rnod | 10k | 6.816k | 13.25k | 10.05k | 1.117k | 21.8 |
| rnodwo | 10k | 8.208k | 12.63k | 10.05k | 713.1 | 13.9 |
| rnpoly | 10k | 6.344k | 13.62k | 10.04k | 1.264k | 24.7 |
| rnpolywo | 10k | 8.101k | 12.85k | 10.03k | 761.1 | 14.9 |
| rnwod | 10k | 8.331k | 11.91k | 10.07k | 674.4 | 13.1 |

Table 6.2: Monte-carlo (process variance) simulation of TSMC65 resistors ($N = 200$)

6.2 • Pseudo-Resistors

As shown in section 6.1 CMOS technology resistors have a low unit resistance, making them unsuitable when high resistances are needed. An alternative is to use MOS devices as resistors. Technically not a passive device any longer, a transistor can be used in triode or subthreshold as a replacement for a resistor. Various techniques can be used to bias the MOSFET for a certain equivalent resistance.

The main interest lies in replacing the DC feedback resistors for the NA with a super-GOhm *pseudo-resistor*. Six different structures as presented in [2] will be investigated.

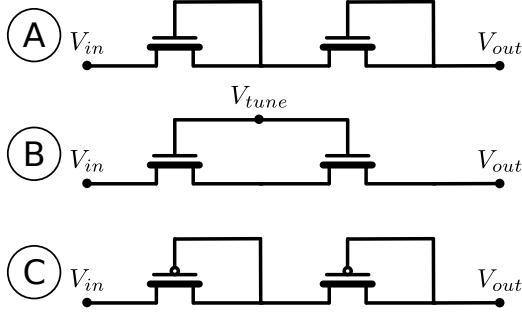


Figure 6.1: Variable V_{GS} pseudo resistor implementations.

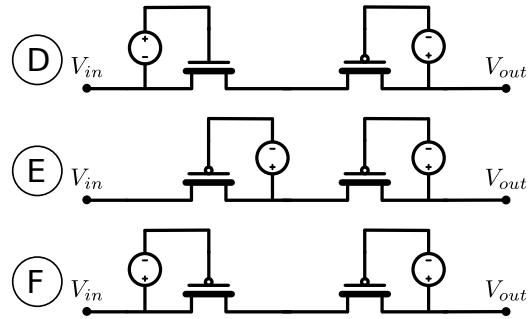


Figure 6.2: Three fixed V_{GS} pseudo resistor implementations.

6.2.1 Results

A 0.6V voltage source is placed at V_{out} , and V_{in} is swept from 0.3V to 0.9V. The variable V_{GS} implementations show considerable resistance variations as the voltage swing changes. Of the fixed V_{GS} implementations, structure F shows the best linearity.

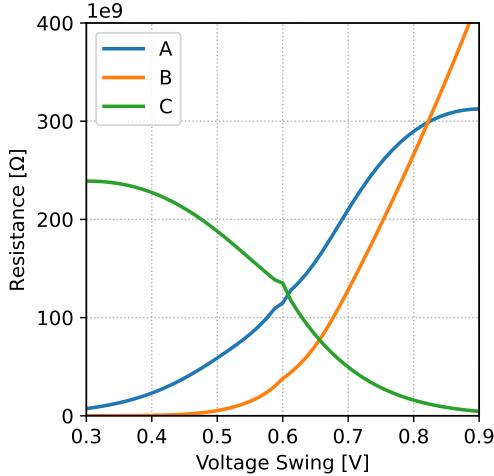


Figure 6.3: Resistance of variable V_{GS} pseudo resistors.

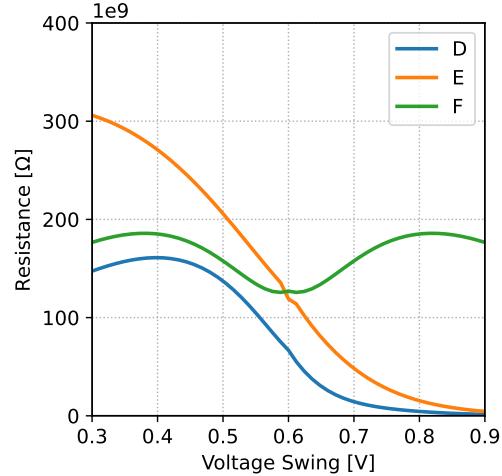
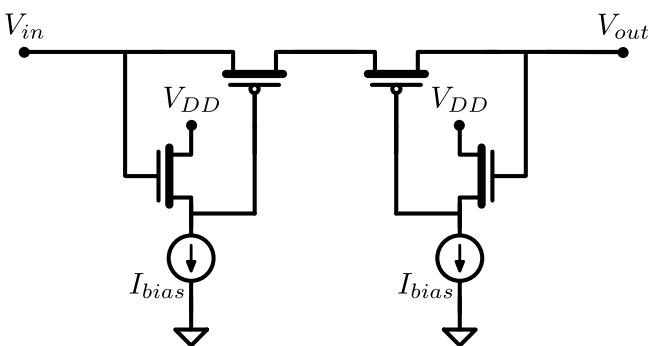
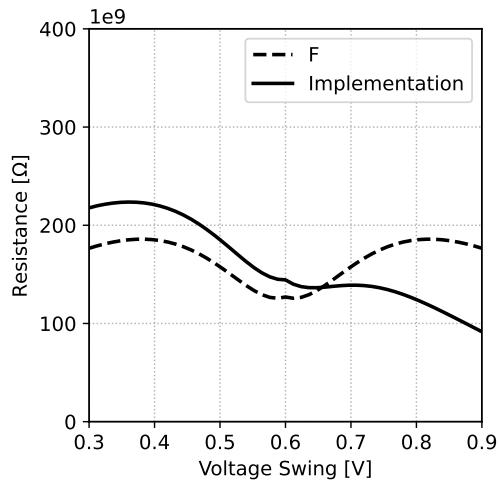


Figure 6.4: Resistance of fixed V_{GS} pseudo resistors.

The fixed V_{GS} pseudo resistor F can be implemented using a single n-type transistor in a source-follower configuration for generating the V_{GS} [Figure 6.5]. Bias current can be adjusted to increase or decrease the resistance. Using $W/L = 0.5\mu/0.5\mu$, $I_{bias} = 15nA$, the simulated resistance of [Figure 6.5] is shown in [Figure 6.6].

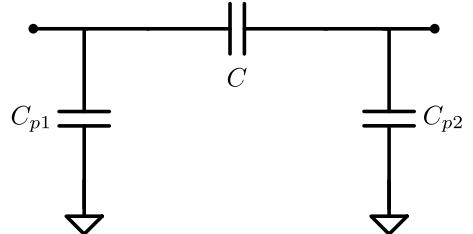
**Figure 6.5:** Active implementation of pseudo resistor F .**Figure 6.6:** Resistance of active pseudo resistor F .

6.3 • Switched-Capacitor Circuits

Switched-capacitor circuits can be used as replacements for resistors. They offer high resistance values and good accuracy.

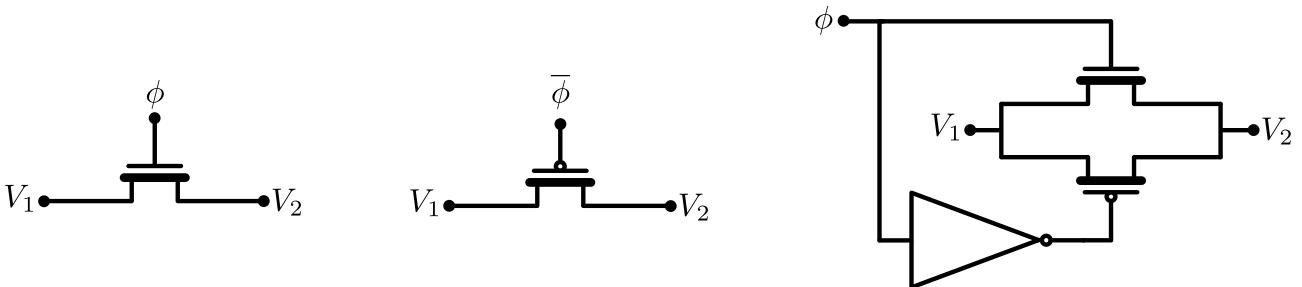
6.3.1 Integrated Circuit Capacitors

There exists several different types of on-chip capacitors. A typical capacitor will be constructed from two closely-spaced conducting layers. The desired capacitance C , is formed by the area of layer 1 and layer 2. This type of capacitor has significant parasitics. The substrate below layer 1 is connected to either one of the power supplies or ground, and is therefore an ac ground. The substrate causes a parasitic *bottom plate capacitance* C_{p1} and the top plate forms a parasitic capacitance C_{p2} . C_{p2} is typically much smaller than C_{p1} [11].

**Figure 6.7:** An integrated circuit capacitor with parasitic capacitances.

6.3.2 Switches

Switches require high off resistance, low on resistance and must not introduce a voltage offset when turned on. MOSFET's satisfy all of these requirements. A switch can be implemented using just a single MOSFET [Figure 6.8 (a), (b)]. Single transistor switches suffer from a limited signal range, and only offer good performance if $V_{DS} > V_{DD} - V_T$. Instead transmission gates will be used to achieve a full signal range [Figure 6.8 (c)].

**Figure 6.8:** Left to right: (a) NMOS switch, (b) PMOS switch, (c) transmission gate.

6.3.3 Operation and Analysis

Two non-overlapping clocks are denoted ϕ_1 and ϕ_2 . A switched-capacitor circuit is shown in [Figure 6.9]. Each cycle a charge $\Delta Q = C(V_1 - V_2)$ is transferred from V_1 to V_2 .

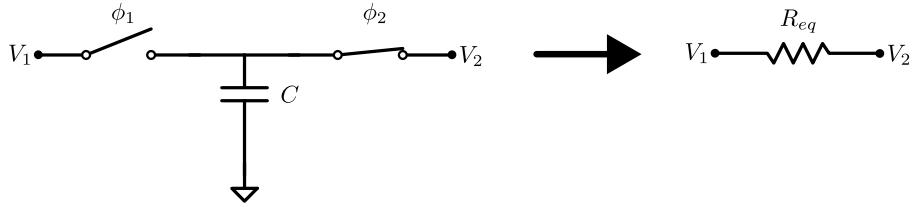


Figure 6.9: Switched-capacitor equivalent resistor circuit.

The equivalent average current due to the charge transfer is found by dividing the charge by the clock period T (6.2). Equation (6.2) closely resembles that of a resistor (6.3).

$$I_{avg} = \frac{C(V_1 - V_2)}{T} \quad (6.2) \qquad I_{eq} = \frac{V_1 - V_2}{R_{eq}} \quad (6.3)$$

We can therefore say that the switched-capacitor circuits acts as an equivalent resistor with value (6.4).

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \quad (6.4)$$

The equivalent resistance can be controlled by either increasing/decreasing the capacitance or the clock frequency.

6.3.4 Parasitic-Insensitive Switched-Capacitor Equivalent Resistors

Using two more switches than in [Figure 6.9], it is possible to reduce the effect of parasitic capacitances C_{p1} and C_{p2} [11]. Shown in [Figure 6.10], when ϕ_1 is on, C and C_{p1} is charged and C_{p2} is shorted to ground. When ϕ_2 is on, C is discharged through the ground node, and C_{p1} is shorted to ground. Even though C_{p1} is charged from the input, the charge never passes through C .

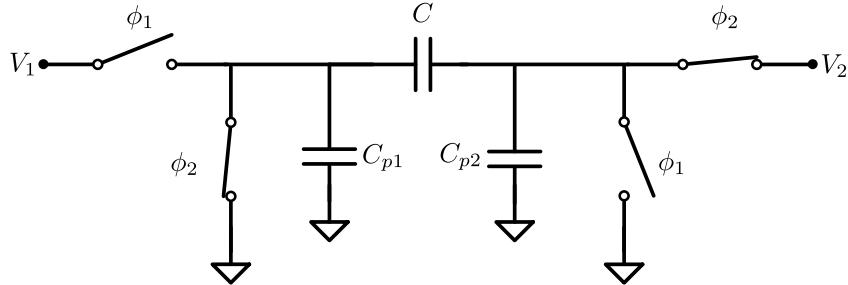


Figure 6.10: Parasitic insensitive switched-capacitor resistor equivalent.

6.3.5 Non-Overlapping Clocks

Non-overlapping clocks is a basic building block for creating switched-capacitor circuits. They are needed to ensure no charge is lost during switching. The structure for generating the clocks is shown in [Figure 6.11] [8].

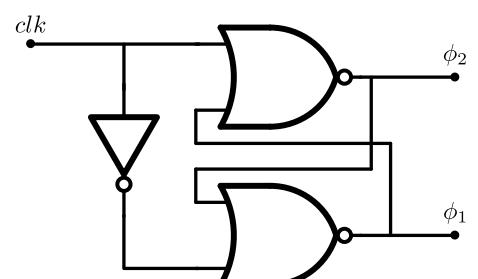


Figure 6.11: Non-overlapping clock generator.

7 | Three-Mirror OTA

The first amplifier structure to be investigated is based on the *Output Transconductance Amplifier* (OTA) structure from [1] [Figure 7.1]. The structure utilizes a p-type long-tailed pair (for lower flicker noise) and three current mirrors, therefore also called the *three-mirror OTA*. It takes a differential input and has a single-ended output. With the use of cascode devices at the output an increased output resistance (and therefore gain) is realized.

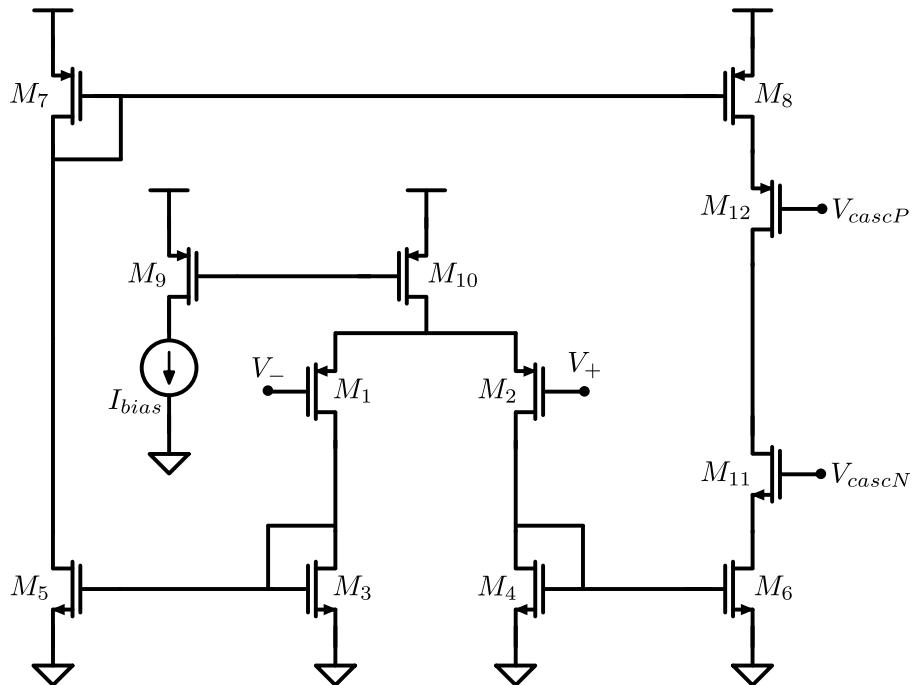


Figure 7.1: Output Transconductance Amplifier Structure

7.1 • Analysis

For easy analysis, symmetry is assumed for ($g_{m1} = g_{m2}$), ($g_{m3} = g_{m4} = g_{m5} = g_{m6}$), ($g_{m7} = g_{m8}$). The input differential pair converts an input voltage to a current by transconductance g_{m1} . This current is then mirrored by a factor B directly to the output by $M_{3,4,5,6,7,8}$. The output resistance is given by the output cascode structures. Amplifier structures where the input device currents flow directly to the output are considered *single stage*, and the gain is given by (7.1).

$$A_V = BG_M R_{out} \quad (7.1)$$

The mirror factor B allows multiplication of output current or output resistance if $B > 1$ or $B < 1$ respectively (assuming constant g_m/I_D). The current requirements of the output stage are low, and increasing the output resistance results in stability problems, so $B = 1$ was chosen. The dominant pole in [Figure 7.1] is at the output and given by (7.2).

$$f_{p1} = \frac{1}{2\pi R_{out} C_L} \quad (7.2)$$

Even though the structure is single-stage, it proves difficult stability wise. Each of the three current mirrors introduce a non-dominant mirror pole (7.3).

$$f_{p2} = \frac{g_{m3}}{2\pi C_3}, \quad f_{p3} = \frac{g_{m3}}{2\pi C_3}, \quad f_{p4} = \frac{g_{m7}}{2\pi C_7} \quad (7.3)$$

where C_3, C_4, C_7 are the total capacitances to ground at the respective nodes, mainly given by C_{GS} of the mirror devices. Each current mirror produces substantial flicker noise propagating to the output. The total thermal noise of the structure is found to be (7.4) [1].

$$\overline{v_{ni,thermal}^2} = \left[\frac{16kT}{3g_{m1}} \left(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}} \right) \right] \quad (7.4)$$

A fairly large output resistance must be targeted to ensure the mirror transistor can operate *at least* in moderate inversion. Operating them in strong inversion results in devices with smaller areas and therefore unacceptable flicker noise. On the other hand, too large mirror devices result in lower frequency mirror poles, sacrificing phase margin.

7.2 • Design

A gain-bandwidth product of $\text{GBW} = 10\text{MHz}$ with $f_{3dB} = 100\text{Hz}$ is targeted, resulting in a DC gain $A_0 = 100\text{dB}$. Starting with the current mirrors, it must be ensured that their poles are sufficiently high enough for a useable phase margin, while also being large enough to provide a low flicker noise. A paradoxical requirement where the solution is either to increase drain current until the speed is high enough, or relax the noise target. Considering the transition frequency f_T as a figure of merit for speed, and the total device area as a figure of merit for noise, a suitable operating point for the mirror transistors is found in *Analog Explorer* at $g_m/I_D = 18$ (moderate inversion). The drain current is increased until the devices are wide enough to provide a low flicker noise. Using SPICE, a tail current of $I_{tail} = 4.4\mu\text{A}$ was found to be suitable.

The input transistors are placed in subthreshold for maximum efficiency at $g_m/I_D \approx 27$. For a DC gain of 100dB , the output resistance must be (7.5).

$$R_{out} = \frac{A_0}{(g_m/I_D)I_{tail}/2} = 1.68\text{G}\Omega \quad (7.5)$$

A maximum load capacitance of $C_L = 500\text{fF}$ is assumed. For the dominant pole to be at 100Hz additional capacitance must be added at the output to compensate the amplifier. The combined C_L is found in (7.6).

$$100\text{Hz} = \frac{1}{2\pi(1.68\text{G}\Omega)C_L} \Rightarrow C_L = 945\text{fF} \quad (7.6)$$

The actual C_L must be found iteratively in SPICE as the parasitic capacitances from the transistors at the output also affect the dominant pole. Finally the cascode devices were sized to reach the output resistance of $1.68\text{G}\Omega$ at $g_m/I_D = 15$ (moderate inversion). *Analog Designer* is used to confirm the expected performance and calculate all device widths. Specifications are summarized in [Table 7.1].

| Designator | Device | g_m/I_D | Inversion | $W/L [\mu\text{m}]$ |
|----------------------|--------|-----------|-----------|---------------------|
| M_1, M_2 | pch_25 | 27 | Weak | 400/1 |
| M_3, M_4, M_5, M_6 | nch_25 | 18 | Moderate | 72/10 |
| M_7, M_8 | pch_25 | 18 | Moderate | 96/10 |
| M_9 | nch_25 | 15 | Moderate | 6/2 |
| M_{10} | pch_25 | 15 | Moderate | 16/2 |

Table 7.1: OTA Device Specifications

7.2.1 Buffer

In addition a unity gain stable variant was designed using the three-mirror OTA structure. The design followed the same procedure as before, but prioritizing unity gain stability and low power consumption. The design is summarized in [Table 7.2].

| Designator | Device | g_m/I_D | Inversion | $W/L [\mu\text{m}]$ |
|----------------------|--------|-----------|-----------|---------------------|
| M_1, M_2 | pch_25 | 26 | Weak | 50/1 |
| M_3, M_4, M_5, M_6 | nch | 20 | Weak | 0.4/1 |
| M_7, M_8 | pch | 20 | Weak | 0.5/1 |
| M_9 | nch_25 | 20 | Weak | 15/20 |
| M_{10} | pch_25 | 20 | Weak | 33/20 |

Table 7.2: OTA buffer device specifications

7.3 • Results

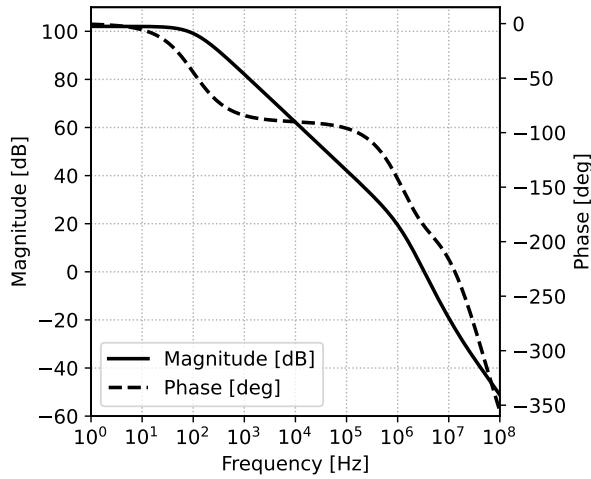


Figure 7.2: OTA closed-loop gain and phase.

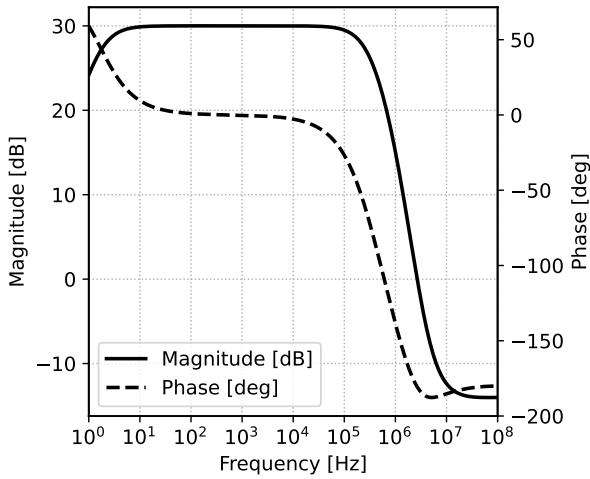


Figure 7.3: OTA closed-loop gain and phase.

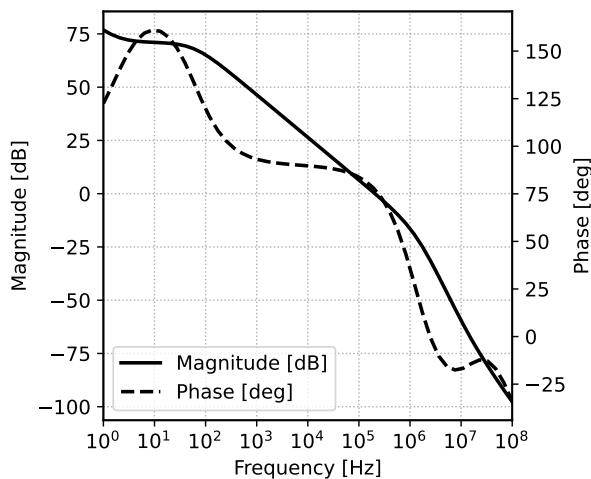


Figure 7.4: OTA loop-gain and phase.

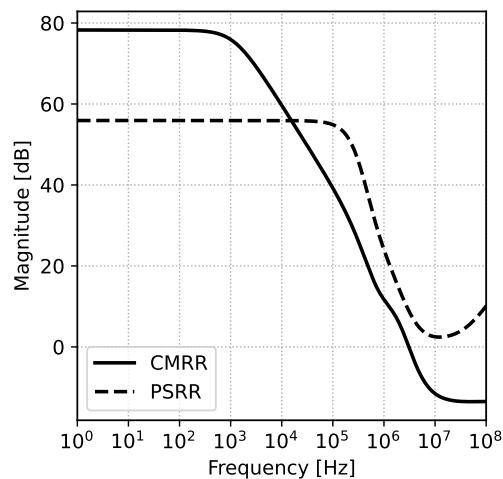


Figure 7.5: OTA CMRR and PSRR.

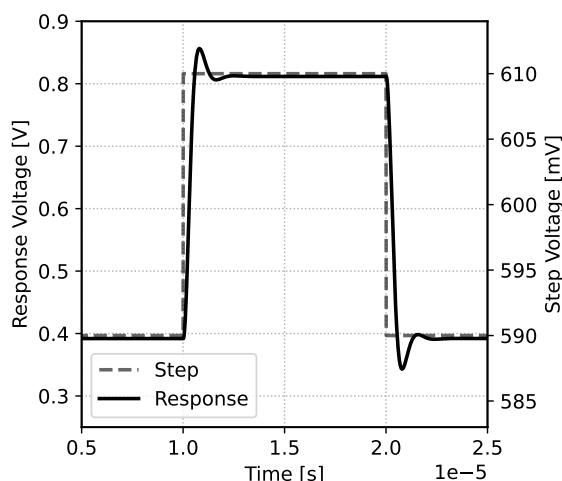


Figure 7.6: OTA closed-loop step response.

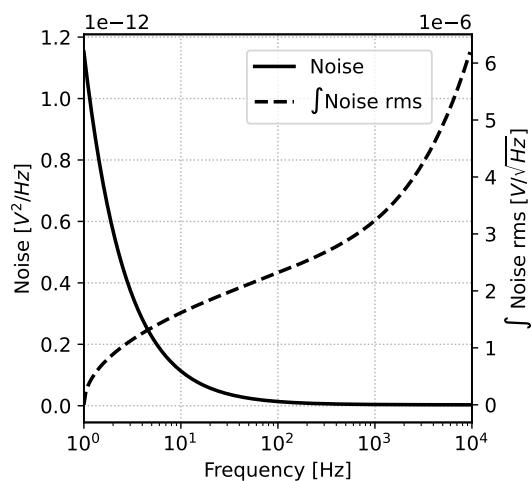
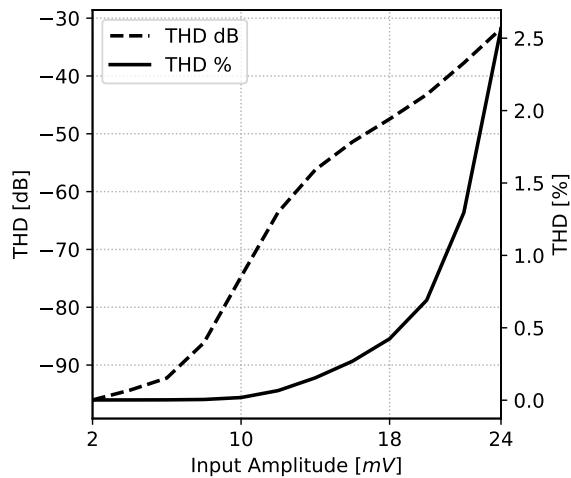
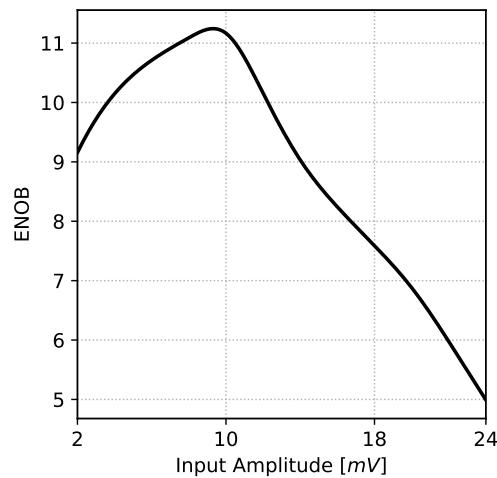


Figure 7.7: OTA input-referred noise.

**Figure 7.8:** OTA closed-loop $A_V = 27\text{dB}$ THD**Figure 7.9:** OTA closed-loop $A_V = 27\text{dB}$ ENOB**Table 7.3: Three-mirror OTA buffer electrical characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|---------------------------------|-------|--------|-------|--------------------------------|------------------------|
| Input offset voltage | V_{IO} | -1495 | -95.49 | 711.1 | μV | $V_O = V_{DD}/2$ |
| Open-loop DC gain | A_0 | 102.0 | 102.1 | 102.1 | dB | |
| Common-mode rejection ratio | CMRR | 70.98 | 79.69 | 105.6 | dB | |
| Power-supply rejection ratio | PSRR | | 55.92 | | dB | |
| Unity-gain bandwidth | B_1 | 3.242 | 3.381 | 3.316 | MHz | |
| Phase margin | $\text{PM}_{30\text{dB}}$ | | 68.2 | | $^\circ$ | $A_{CL} = 30\text{dB}$ |
| Integrated noise 1Hz-200Hz | $\int_1^{200} \overline{V_n^2}$ | 2.368 | 2.374 | 2.379 | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Integrated noise 1Hz-1kHz | $\int_1^{1k} \overline{V_n^2}$ | 2.927 | 2.939 | 2.950 | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Slew rate + | SR+ | 3.255 | 3.393 | 3.552 | $\text{V}/\mu\text{s}$ | Unity gain |
| Slew rate - | SR- | 1.401 | 1.436 | 1.487 | $\text{V}/\mu\text{s}$ | Unity gain |
| Power consumption | P | 9.400 | 9.700 | 10.03 | μW | |
| Noise Efficiency Factor | NEF | | 6.36 | | | |

¹ Monte carlo analysis (process and mismatch) 200 samples, with $C_L = 600\text{fF}$.

7.4 • Results (Buffer)

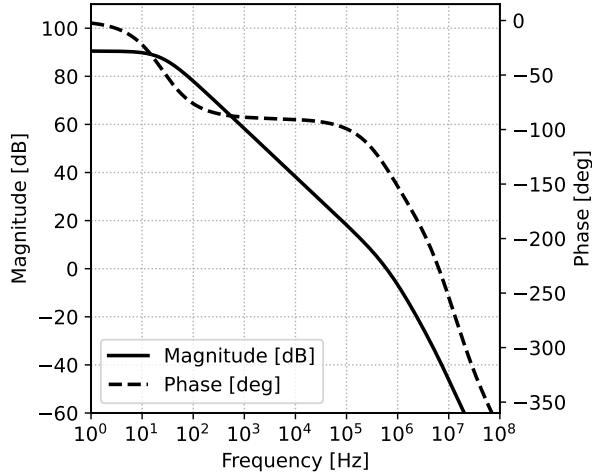


Figure 7.10: OTA buffer open-loop AC response.

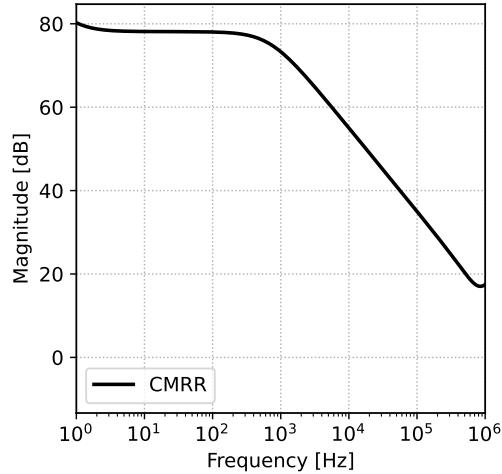


Figure 7.11: OTA buffer CMRR.

Table 7.4: Three-mirror OTA electrical characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------|---------------------------------|------|--------|------|--------------------------------|------------------|
| Input offset voltage | V_{IO} | | -100.3 | | μV | $V_O = V_{DD}/2$ |
| Open-loop DC gain | A_0 | | 90.5 | | dB | |
| Common-mode rejection ratio | CMRR | | 79.02 | | dB | |
| Unity-gain bandwidth | B_1 | | 0.605 | | MHz | |
| Phase margin | $\text{PM}_{30\text{dB}}$ | | 44.5 | | ° | Unity gain |
| Integrated noise 1Hz-200Hz | $\int_1^{200} \overline{V_n^2}$ | | 39.4 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Integrated noise 1Hz-1kHz | $\int_1^{1k} \overline{V_n^2}$ | | 39.6 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Power consumption | P | | 540 | | nW | |

¹ Single analysis, with $C_L = 500\text{fF}$.

8 | Two-Stage Amplifier

8.1 • Introduction

As seen [Chapter 7], single-stage amplifiers have some inherent limits. They only perform voltage-to-current conversion once, limiting the gain to the $g_m R_{out}$ product. Increasing R_{out} directly affects the dominant pole of such amplifiers and therefore limit the bandwidth in low-power applications. The three-mirror OTA was also limited in output-swing due to the cascode structures.

The LPF must deliver high gain and output swing to the sample-and-hold stage. A two-stage structure was chosen. The first stage can deliver high voltage gain while the second can deliver moderate gain and be capable of a high output swing. The structure that will be used is seen in Figure 8.1. A PMOS differential pair is used again for the lower 1/f noise compared to its NMOS counterpart. A *full-swing output stage* is utilized consisting of a single active-loaded NMOS device. Note the use of p-type cascode devices at the input and a low-voltage cascode current mirror. Both of these serve to increase the possible output resistance from the first stage. In addition the input cascode devices significantly improve CMRR.

Two-stage structures are more difficult stability wise and need to be properly compensated. Several techniques exist but the simplest is *Miller compensation*.

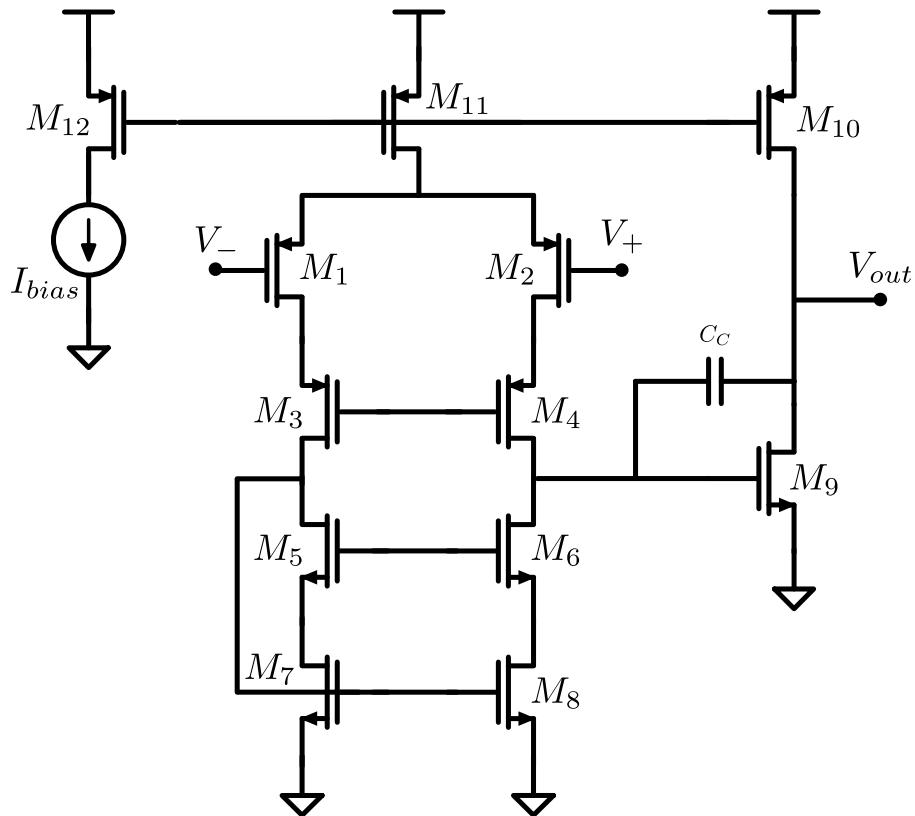


Figure 8.1: Two-stage amplifier schematic.

8.2 • Analysis

8.2.1 Without Compensation

To show the need for compensation, analysis will initially be done without compensation capacitor C_C . For simpler analysis, symmetry is assumed for

$$\begin{aligned} (g_{m1} = g_{m2}) \quad (g_{m3} = g_{m4}) \\ (g_{m5} = g_{m6}) \quad (g_{m7} = g_{m8}) \end{aligned}$$

Considering the circuit stage wise, the gain of the first stage is given by the product of the stage transconductance G_{M1} and the stage output resistance R_{out1} (8.1).

$$A_1 = G_{M1}R_{out1} \quad (8.1)$$

The first stage supplies a mirror pole and a output pole (8.2).

$$f_{p1,mirror} = \frac{g_{m7}}{4\pi C_{gs7}}, \quad f_{p1,out} = \frac{1}{2\pi R_{out1}C_{gs9}} \quad (8.2)$$

Following the same procedure for the second stage, the gain is given by (8.3).

$$A_2 = G_{M2}R_{out2} = g_{m9}(r_{O9}||r_{O10}) \quad (8.3)$$

The second stage supplies a output pole (8.4).

$$f_{p2,out} = \frac{1}{2\pi R_{out2}C_L} \quad (8.4)$$

From equation 8.2 and 8.4 it is clear that the amplifier will have stability issues. Assuming the mirror pole $f_{p1,mirror} \gg f_{p1,out}$, the poles $f_{p1,out}, f_{p2,out}$ will be dominant. Due to both having R_{out} in the denominator, the poles will be close and stability will have to come at the sacrifice of gain for one of the stages. The solution to this issue, compensation, will be discussed in 8.2.2.

8.2.2 Dominant-Pole Compensation

Compensation is the act of not only ensuring closed-loop stability, but also good settling characteristics. The dominant-pole compensation technique is a common method used to increase phase margin. It is performed by decreasing the frequency of the dominant pole, approximating the response as a first-order system up to the loop's unity gain frequency. First-order feedback systems are inherently stable with at least 90° phase margin.

Miller Compensation

A type a dominant-pole compensation utilizing a capacitor bridged between the input and ouptut of the second stage. The second stage multiplies the *Miller capacitor* and lowers the output pole of the first stage.

8.2.3 Analysis With Compensation

Equation 8.1 and 8.3 still hold true with the added Miller capacitor C_C . The output pole of the first stage is now given by

$$f_{p1,out} = \frac{1}{2\pi R_{out1}C_C(1 + A_2)} \quad (8.5)$$

At frequencies higher than $f_{p1,out}$ the compensation capacitor C_C can be approximated as a short circuit, diode connecting the gain device M_9 creating a pole at

$$f_{p2,out} = \frac{g_{m9}}{2\pi C_L} \quad (8.6)$$

From equation 8.5 and 8.6 it can be seen that as g_{m9} is increased $f_{p1,out}$ will be decreased and $f_{p2,out}$ will be increased. Called pole splitting, this separation can be used to make the amplifier more stable. It is also seen that as C_C is increased, $f_{p1,out}$ will be decreased without affecting $f_{p2,out}$.

8.3 • Design

Two designs using the two-stage structure will be shown. One prioritizing a good compromise between power, noise and gain (hereinafter referred to as the two-stage LP), and one prioritizing only low noise (hereinafter referred to as the two-stage LN).

8.3.1 Two-Stage LP

A GBW = 10MHz will be targeted with a DC gain of $A_0 = 120$ dB with $f_{3dB} = 10$ Hz. Assuming $C_L = 500$ fF the output device transconductance is chosen for placing the pole at 10MHz, $g_{m9} = (10\text{MHz})2\pi(500\text{fF}) = 31.4\mu\text{S}$. The device is placed in moderate inversion at $(g_m/I_D)_9 = 17$ for a $V_{GS9} \approx 0.6$ V. The required output stage drain current $I_{out} = 1.85\mu\text{A}$. The second stage PMOS is placed in strong inversion at $(g_m/I_D)_{10} = 20$. Using *Analog Designer* the second stage gain is found to be $A_{V,2} = 44$ dB. Using compensation capacitor $C_C = 150$ fF, the first stage output resistance is determined from the dominant pole (8.7).

$$f_{p1,out} = 10\text{Hz} = \frac{1}{2\pi R_{out1}C_C(1 + A_{V,2})} \Rightarrow R_{out1} = 650\text{M}\Omega \quad (8.7)$$

For the first stage to deliver $120\text{dB} - 44\text{dB} = 76\text{dB}$, the input transconductance is set at $g_{m1} = 12\mu\text{S}$. Operating the input devices M_1, M_2 in weak inversion at $(g_m/I_D)_1 \approx 27$, the tail current $I_{tail} \approx 0.9\mu\text{A}$. The n-type current mirror transistors are put in moderate inversion as a compromise between flicker noise and speed. Cascode devices in the first stage are sized to reach the required output resistance. The design is summarized in [Table 8.1].

| Designator | Device | $g_m I_D$ | Inversion | $W/L [\mu\text{m}]$ |
|------------|--------|-----------|-----------|---------------------|
| M_1, M_2 | pch_25 | 27 | Weak | 400/1 |
| M_3, M_4 | pch_25 | 17 | Moderate | 5/2 |
| M_5, M_6 | nch | 17 | Moderate | 1/1 |
| M_7, M_8 | nch | 23 | Weak | 12/5 |
| M_9 | nch_25 | 17 | Moderate | 4/1 |
| M_{10} | pch_25 | 20 | Weak | 38/2 |
| M_{11} | pch_25 | 20 | Weak | 19/2 |

Table 8.1: Two-stage LP Transistor Specifications

8.3.2 Two-Stage LN

A similar process as described for the low-power amplifier [Chapter 8.3.1] is used to design the higher power low-noise variant. Due to the difficulty of predicting noise, the design was done iteratively; increasing the power until sufficiently low noise was achieved. To eliminate flicker noise transistors were made extremely large. The largest contributor to noise is then thermal noise. At $I_{tail} = 8\mu A$ and $I_{out} = 18\mu A$ the noise was low enough. The design is summarized in [Table 8.2].

| Designator | Device | $g_m I_D$ | Inversion | $W/L [\mu m]$ |
|------------|--------|-----------|-----------|---------------|
| M_1, M_2 | pch_25 | 25 | Weak | 1600/2 |
| M_3, M_4 | pch_25 | 19 | Moderate | 80/2 |
| M_5, M_6 | nch | 11 | Moderate | 10/10 |
| M_7, M_8 | nch | 16 | Moderate | 70/20 |
| M_9 | nch_25 | 14 | Moderate | 80/5 |
| M_{10} | pch_25 | 20 | Weak | 380/2 |
| M_{11} | pch_25 | 18 | Moderate | 190/2 |

Table 8.2: Two-stage LN Transistor Specifications

8.4 • Low-Power Results

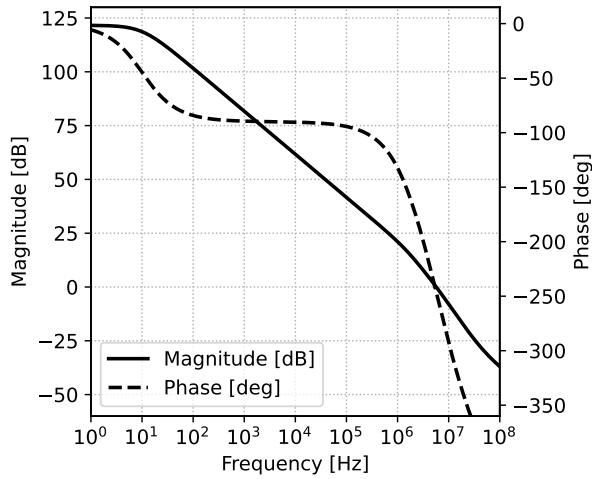


Figure 8.2: Two-stage LP closed-loop gain and phase.

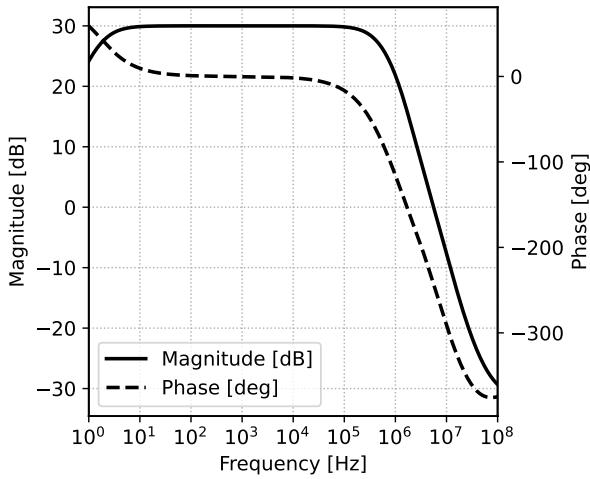


Figure 8.3: Two-stage LP closed-loop gain and phase.

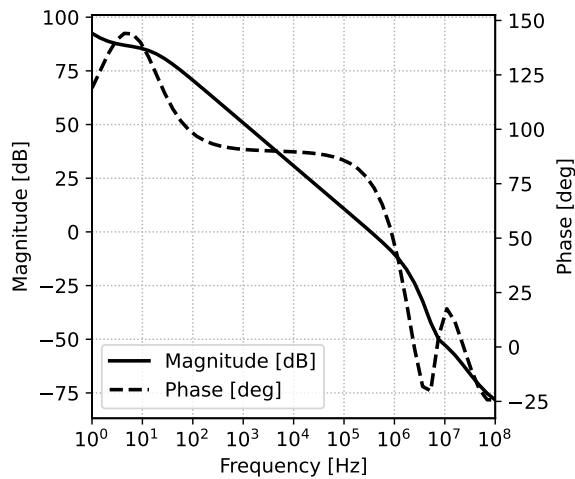


Figure 8.4: Two-stage LP loop-gain and phase.

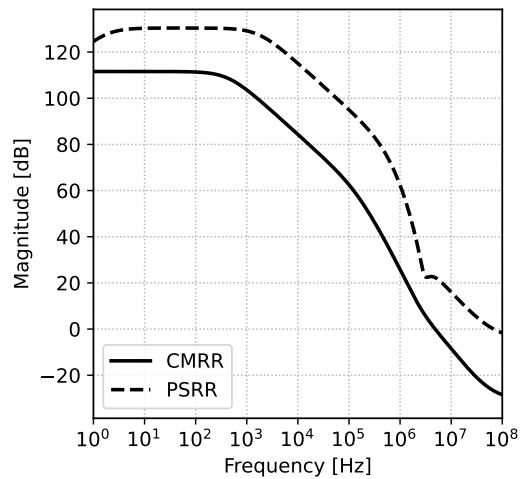


Figure 8.5: Two-stage LP CMRR and PSRR.

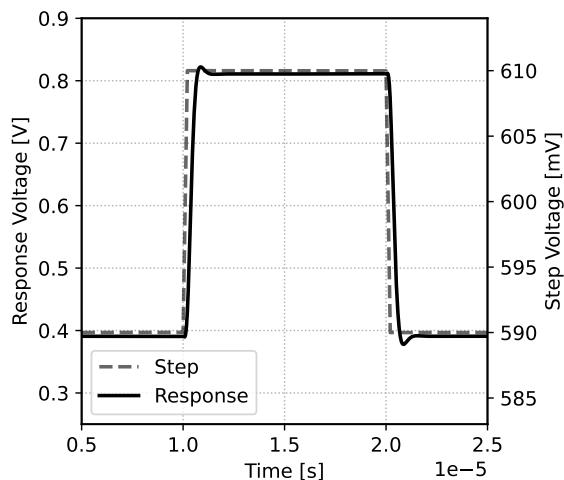


Figure 8.6: Two-stage LP closed-loop step response.

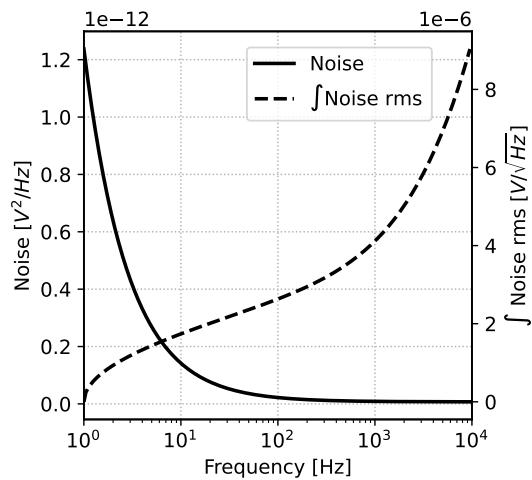
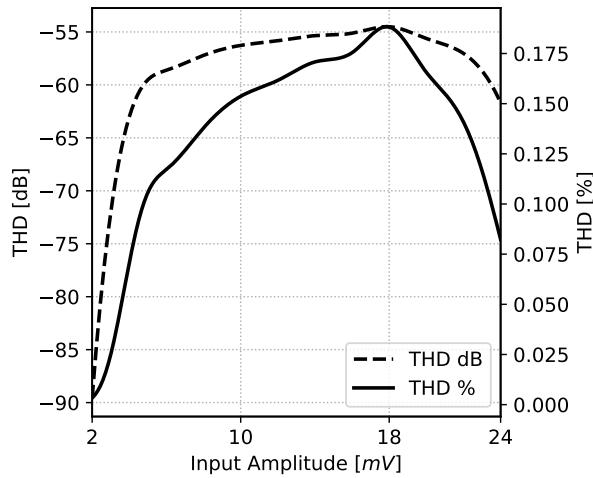
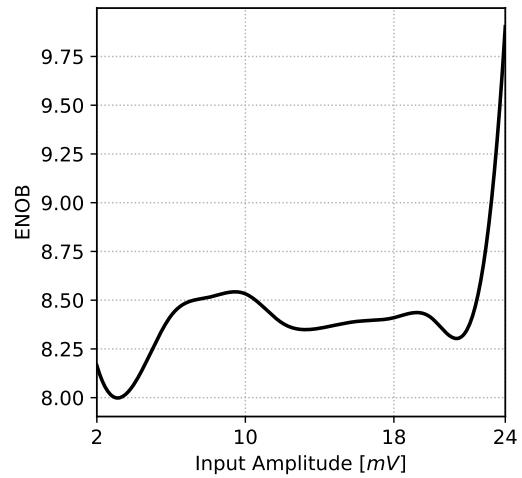


Figure 8.7: Two-stage LP input-referred noise.

**Figure 8.8:** Two-stage LP closed-loop $A_V = 27\text{dB}$ THD**Figure 8.9:** Two-stage LP closed-loop $A_V = 27\text{dB}$ ENOB**Table 8.3: Two-stage LP Electrical Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|---------------------------------|-------|--------|-------|--------------------------------|------------------------|
| Input offset voltage | V_{IO} | -1702 | -41.20 | 1899 | μV | $V_O = V_{DD}/2$ |
| Open-loop DC gain | A_0 | 121.3 | 121.6 | 121.8 | dB | |
| Common-mode rejection ratio | CMRR | 84.73 | 99.55 | 138.1 | dB | |
| Power-supply rejection ratio | PSRR | | 125.0 | | dB | |
| Unity-gain bandwidth | B_1 | 5.514 | 5.723 | 5.934 | MHz | |
| Phase margin | $\text{PM}_{30\text{dB}}$ | | 73.5 | | ° | $A_{CL} = 30\text{dB}$ |
| Integrated noise 1Hz-200Hz | $\int_1^{200} \overline{V_n^2}$ | 2.791 | 2.802 | 2.812 | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Integrated noise 1Hz-1kHz | $\int_1^{1k} \overline{V_n^2}$ | 3.544 | 3.570 | 3.594 | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Slew rate + | SR+ | 1.306 | 1.363 | 1.415 | $\text{V}/\mu\text{s}$ | Unity gain |
| Slew rate - | SR- | 0.797 | 0.833 | 0.876 | $\text{V}/\mu\text{s}$ | Unity gain |
| Power consumption | P | | 3.207 | | μW | |
| Noise Efficiency Factor | NEF | | 7.68 | | | |

¹ Monte carlo analysis (process and mismatch) 200 samples, with $C_L = 500\text{fF}$.

8.5 • Low-Noise Results

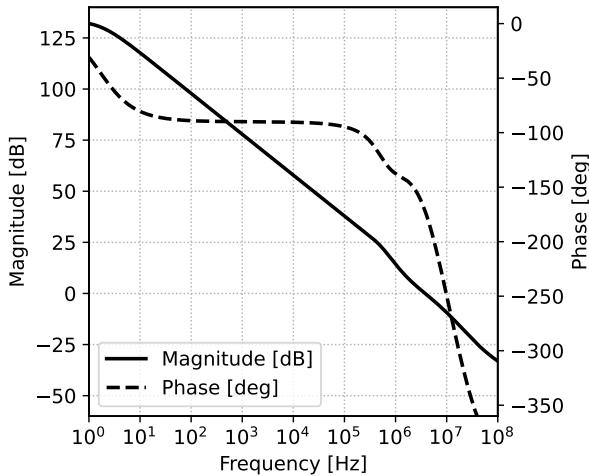


Figure 8.10: Two-stage LN closed-loop gain and phase.

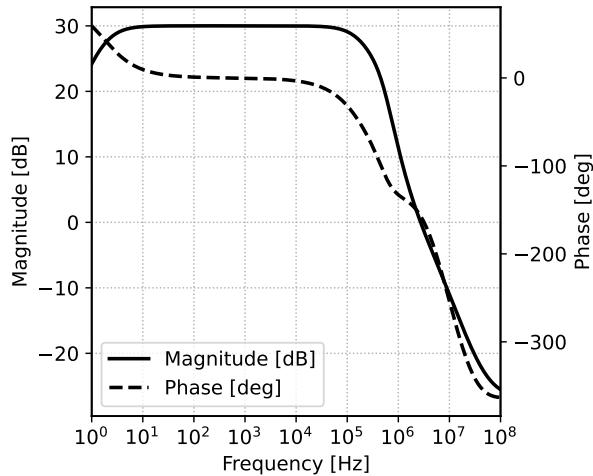


Figure 8.11: Two-stage LN closed-loop gain and phase.

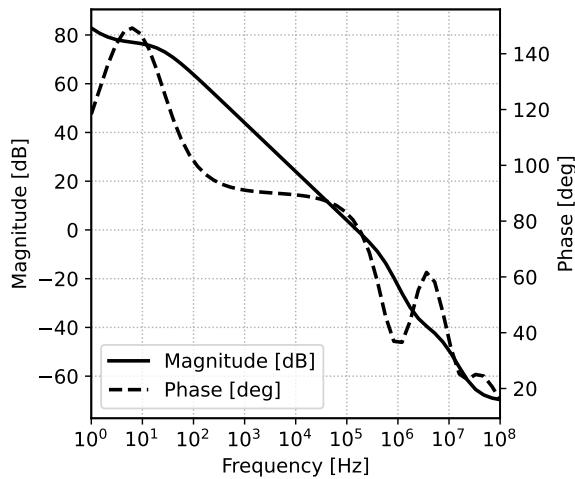


Figure 8.12: Two-stage LN loop-gain and phase.

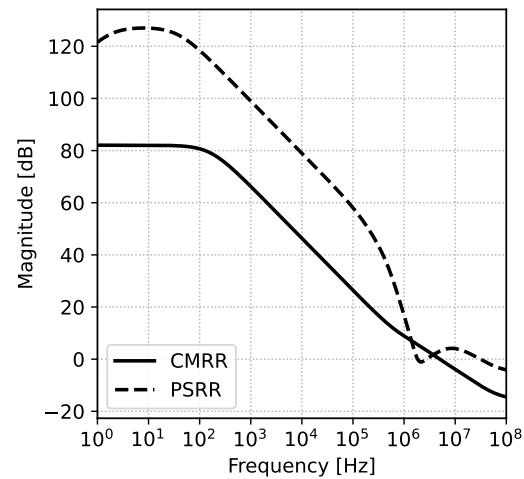


Figure 8.13: Two-stage LN CMRR and PSRR.

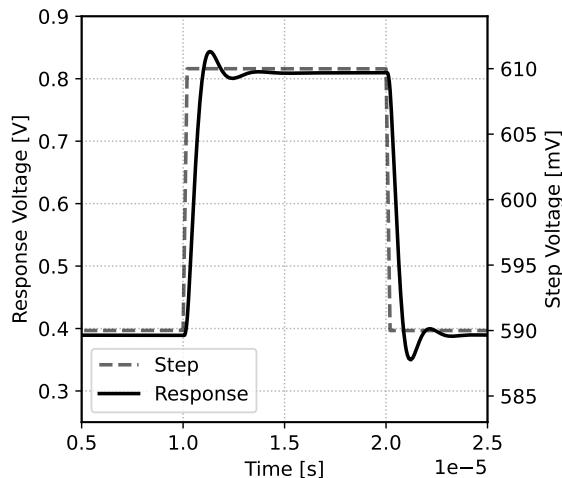


Figure 8.14: Two-stage LN closed-loop step response.

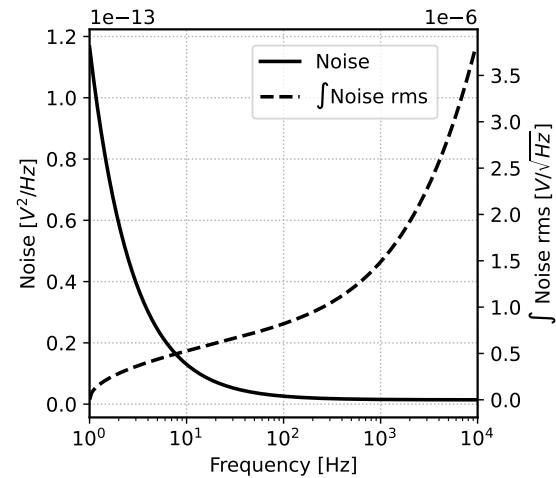
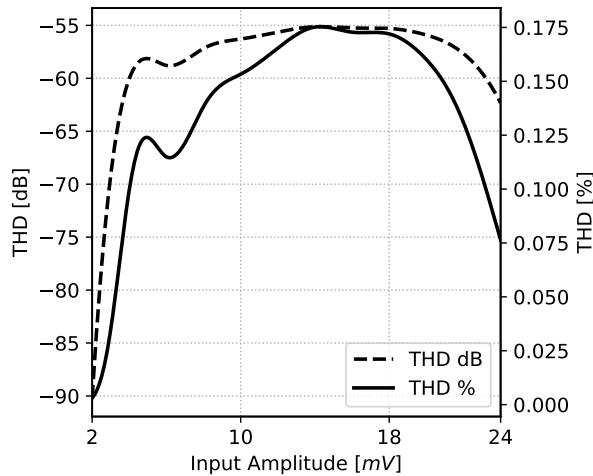
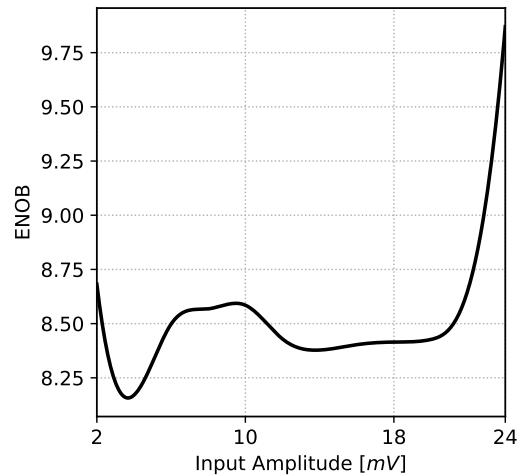


Figure 8.15: Two-stage LN input-referred noise.

**Figure 8.16:** Two-stage LN closed-loop $A_V = 27\text{dB}$ THD**Figure 8.17:** Two-stage LN closed-loop $A_V = 27\text{dB}$ ENOB**Table 8.4: Two-stage LN Electrical Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|---------------------------------|--------|-------|-------|--------------------------------|------------------------|
| Input offset voltage | V_{IO} | -302.1 | 38.62 | 298.3 | μV | $V_O = V_{DD}/2$ |
| Open-loop DC gain | A_0 | 131.7 | 132.1 | 132.4 | dB | |
| Common-mode rejection ratio | CMRR | 67.69 | 82.13 | 104.8 | dB | |
| Power-supply rejection ratio | PSRR | | 130.0 | | dB | |
| Unity-gain bandwidth | B_1 | 3.678 | 3.783 | 3.910 | MHz | |
| Phase margin | $\text{PM}_{30\text{dB}}$ | | 76.2 | | $^\circ$ | $A_{CL} = 30\text{dB}$ |
| Integrated noise 1Hz-200Hz | $\int_1^{200} \overline{V_n^2}$ | 0.852 | 0.856 | 0.860 | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Integrated noise 1Hz-1kHz | $\int_1^{1k} \overline{V_n^2}$ | 1.172 | 1.181 | 1.191 | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Slew rate + | SR+ | 1.913 | 1.970 | 2.030 | $\text{V}/\mu\text{s}$ | Unity gain |
| Slew rate - | SR- | 1.170 | 1.237 | 1.294 | $\text{V}/\mu\text{s}$ | Unity gain |
| Power consumption | P | | 30.0 | | μW | |
| Noise Efficiency Factor | NEF | | 5.55 | | | |

¹ Monte carlo analysis (process and mismatch) 200 samples, with $C_L = 500\text{fF}$.

9 | Folded Cascode Amplifier

After the filter the signal can have amplitudes up to 1V. To buffer such a signal without introducing non-linearity from the input devices, the buffer structure seen in Figure 9.1 is used. When the signal is at its maximum the PMOS input pair M_{1p}, M_{2p} will be off, but NMOS input devices M_1, M_2 will still keep the amplifier "alive" and vice versa when the signal is at its minimum.

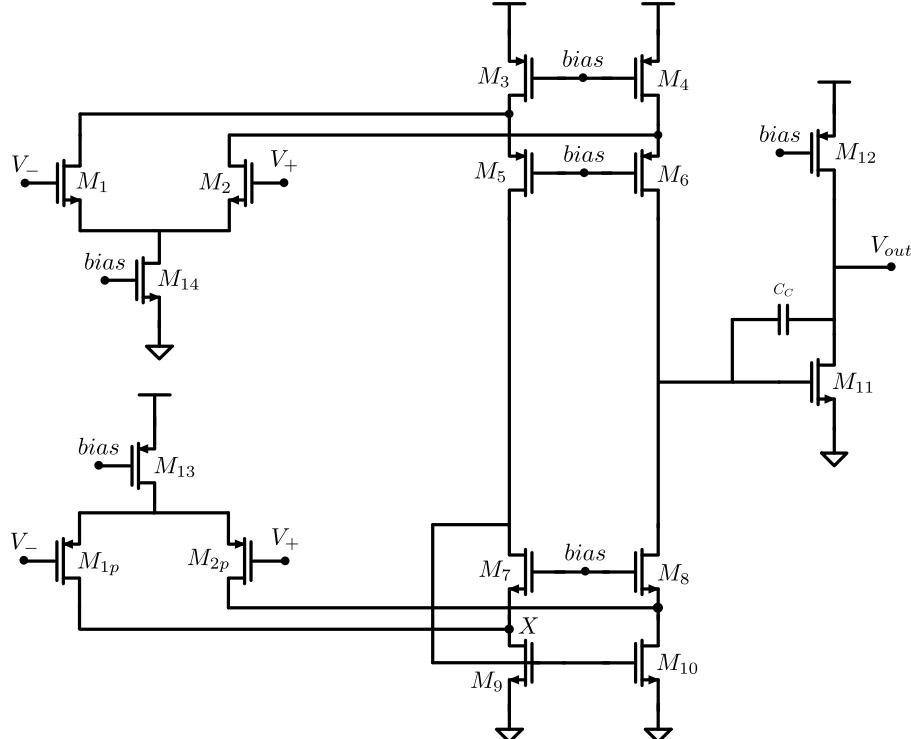


Figure 9.1: Two-stage folded cascode with rail-to-rail input.

9.1 • Analysis

For easy analysis symmetry is assumed for the following devices:

$$\begin{aligned} (g_{m1} = g_{m2}) \quad (g_{m1p} = g_{m2p}) \quad (g_{m3} = g_{m4}) \\ (g_{m5} = g_{m6}) \quad (g_{m7} = g_{m8}) \quad (g_{m9} = g_{m10}) \end{aligned}$$

The tail currents for the NMOS and PMOS input pairs are the same $I_{tail,N} = I_{tail,P} = I_{tail}$. If the bias current in the folded-cascode structure is denoted I_{SS1}, I_{SS2} , then $I_{B1} = I_{B2} = I_{tail}$. Assuming the worst case scenario, the transconductance of the first stage $G_{M,1} = \min(g_{m1}, g_{m1p})$. The input current flows directly to the output of the first stage, the gain and output resistance of the first stage is shown in (9.1).

$$A_1 = G_{M1}R_{out1}, \quad R_{out1} \approx \left(\frac{1}{r_{O10}r_{O8}g_{m8}} + \frac{1}{r_{O4}r_{O6}g_{m6}} \right)^{-1} \quad (9.1)$$

The gain of the second stage is simply $A_{V2} = g_{m11}(r_{O11}||r_{O12})$. Just like the earlier two-stage design the dominant pole will be at the output of the first stage and is caused by Miller capacitor C_C . The pole frequencies are

$$f_{p1,out} = \frac{1}{2\pi R_{out1} C_C (1 + A_{V2})}, \quad f_{p2,out} = \frac{g_{m11}}{2\pi C_L}, \quad f_{p,mirror} = \frac{g_{m9}}{2C_{gs7}}$$

In addition there is another pole present at cascode node X . The pole frequency is given by

$$f_{p4} = \frac{1}{2\pi C_{GS9} + C_{DB1p} + C_{DB2p}}$$

The input PMOS devices can contribute significant capacitance to this. Operation in deep weak inversion, for the input devices, is therefore not used in this design to decrease the size of M_{1p}, M_{2p} .

9.2 • Design Procedure

The amplifier will be used as a buffer so unity gain stability is therefore absolutely critical. As will be seen - this translates to a fairly high power consumption. The design procedure will be close to the one used for the two-stage amplifier, with the addition of concern for the pole at X . As explained, the structure inherently suffers from g_m variance as the input voltage changes. The maximum transconductance will be seen at an approximate input voltage of 0.6V, when both input pairs are conducting. Assuming a maximum open-loop gain of 80dB at 1kHz at $V_+ = V_- = 0.6V$ and a first-order response, the unity-gain bandwidth will be at 10MHz. The output pole is placed at 50MHz to ensure sufficient phase margin. Sizing for a maximum output capacitance of $C_L = 500fF$, the required transconductance of the second stage

$$50\text{MHz} = \frac{g_{m11}}{2\pi 500\text{fF}} \quad \Rightarrow \quad g_{m11} = 157\mu\text{S}$$

Placing device M_{11} at $(g_m/I_D)_{11} = 17$ for operation in moderate inversion, the required output current is (9.2).

$$I_{out} = \frac{g_{m11}}{(g_m/I_D)_{11}} = 9.24\mu\text{A} \quad (9.2)$$

Using Analog Explorer and Analog Designer, the output resistance of the second stage is found to be (9.3), and the 2nd stage gain (9.4).

$$R_{out,2} = (r_{O11} \parallel r_{O12}) \approx 843\text{k}\Omega \quad (9.3) \quad A_{V2} = g_{m11} R_{out,2} = 42.2\text{dB} \quad (9.4)$$

Several iterations of the first stage was done. The limiting pole proved to be f_{p4} from node X . To move the pole to a higher frequency, the input devices were shrunk and placed at $(g_m/I_D)_{1,2,1p,2p} = 20$. In addition the current was set to $I_{tail} = I_{B1} = I_{B2} = 3.14\mu\text{A}$. The output resistance were sized with gain and the dominant pole in mind. The resulting design is summarized in Table 9.1.

| Designator | Device | $g_m I_D$ | Inversion | $W/L [\mu\text{m}]$ |
|------------------|--------|-----------|-----------|---------------------|
| M_1, M_2 | nch_25 | 20 | Weak | 8/1 |
| M_{1p}, M_{2p} | pch_25 | 20 | Weak | 14/1 |
| M_3, M_4 | pch | 17 | Moderate | 4/1 |
| M_5, M_6 | nch | 17 | Moderate | 2/1 |
| M_7, M_8 | nch_25 | 17 | Moderate | 7/1 |
| M_9, M_{10} | pch | 17 | Moderate | 7/1 |
| M_{11} | nch_25 | 17 | Moderate | 19/1 |
| M_{12} | pch_25 | 20 | Weak | 80/1 |

Table 9.1: Folded Cascode Transistor Specifications

9.3 • Results

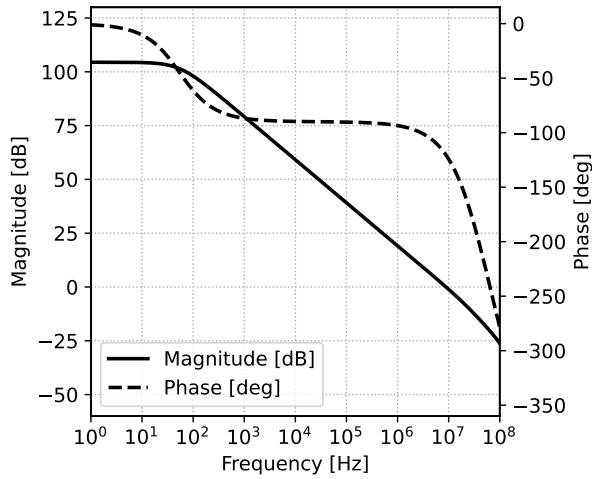


Figure 9.2: Folded cascode closed-loop gain and phase.

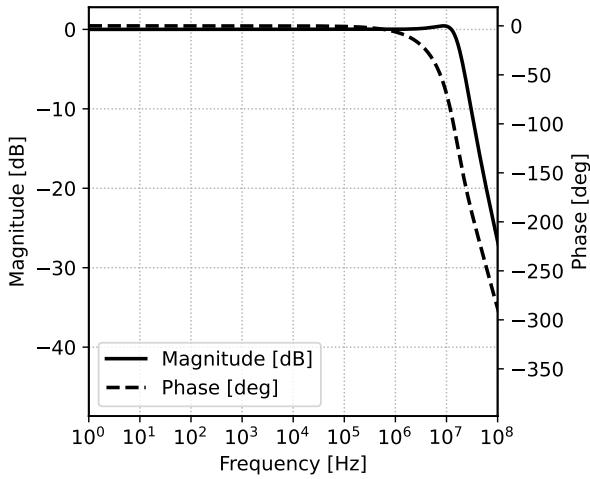


Figure 9.3: Folded cascode closed-loop gain and phase.

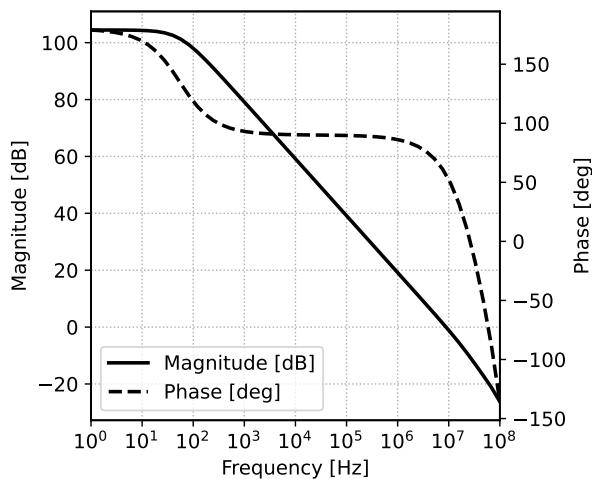


Figure 9.4: Folded cascode loop-gain and phase.

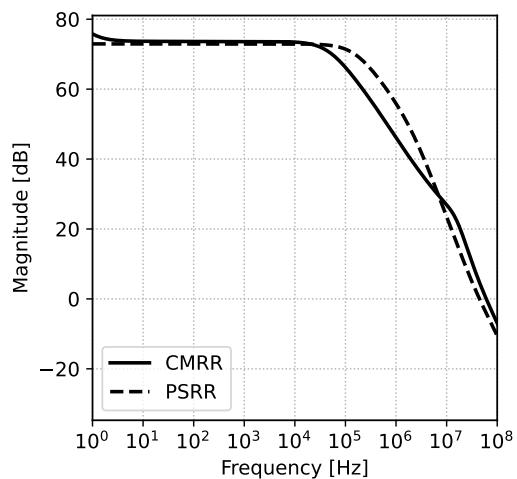


Figure 9.5: Folded cascode CMRR and PSRR.

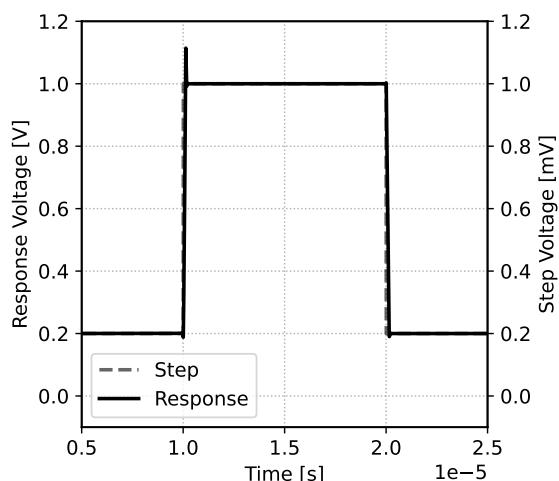


Figure 9.6: Folded cascode closed-loop step response.

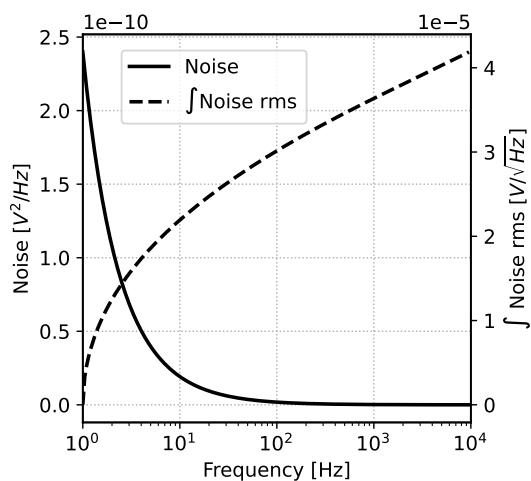
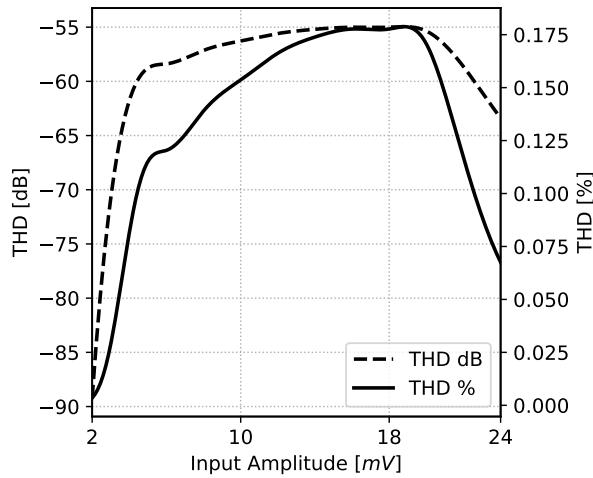
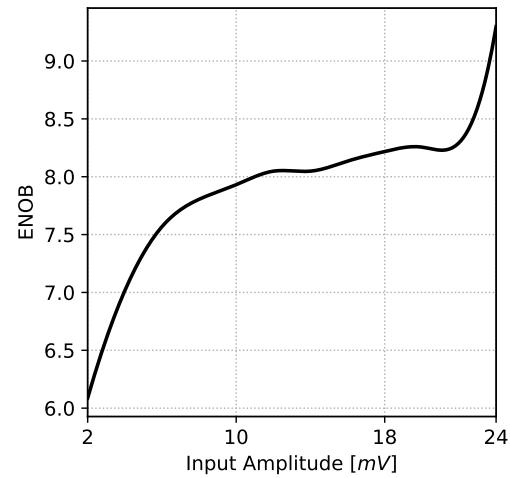
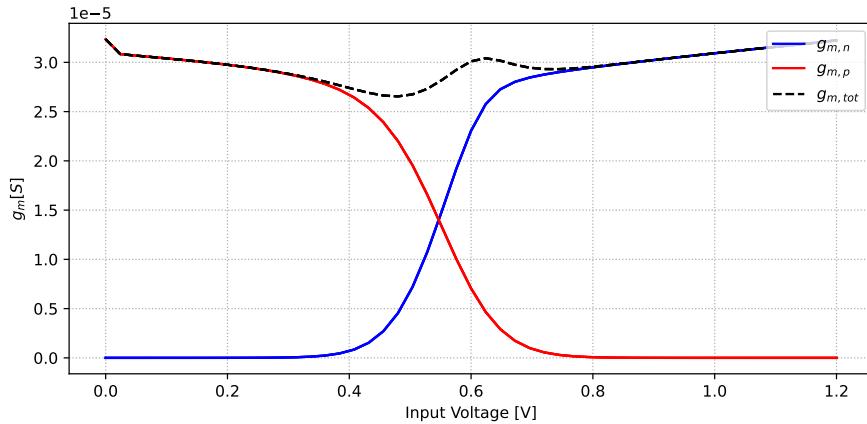


Figure 9.7: Folded cascode input-referred noise.

**Figure 9.8:** Folded-cascode closed-loop $A_V = 27\text{dB}$ THD**Figure 9.9:** Folded-cascode closed-loop $A_V = 27\text{dB}$ ENOB**Figure 9.10:** Folded-cascode g_m variance with input common-mode.**Table 9.2: Two-Stage Folded Cascode Electrical Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|---------------------------------|------|--------|------|--------------------------------|------------------|
| Input offset voltage | V_{IO} | | -97.66 | | μV | $V_O = V_{DD}/2$ |
| Open-loop DC gain | A_0 | | 104.5 | | dB | |
| Common-mode rejection ratio | CMRR | | 74.98 | | dB | |
| Power-supply rejection ratio | PSRR | | 72.94 | | dB | |
| Unity-gain bandwidth | B_1 | | 8.88 | | MHz | |
| Phase margin | $\text{PM}_{30\text{dB}}$ | | 59.5 | | $^\circ$ | |
| Integrated noise 1Hz-200Hz | $\int_1^{200} \overline{V_n^2}$ | | 32.15 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Integrated noise 1Hz-1kHz | $\int_1^{1k} \overline{V_n^2}$ | | 36.36 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Power consumption | P | | 30.0 | | μW | |

¹ Single analysis, with $C_L = 1\text{pF}$.

10 | Layout

With today's high speed analog systems, layout and packaging is increasingly important and sometimes the limiting factor. In this chapter we will review basic layout considerations, discuss techniques for optimal performance, and showcase a layout made for the two-stage amplifier presented in Chapter (8).

10.1 • Basic Layout Considerations

Integrated circuits are made in layers. Usually the "stack-up" consists of the p-type substrate, into which MOS devices are created by etching and diffusion¹. An oxide layer followed by polysilicon creates the gate of the devices. On top of the devices metal layers are deposited, creating the interconnects. The TSMC65 node supports up to 9 metal layers.

Layout is the process of defining the physical geometry of the devices and interconnects. These geometries are what appear on the masks used in the photolithography process. During the layout process it is crucial to keep within the design rules of the technology, done by a *design rule check* (DRC). The DRC ensures that the final design is manufacturable. Examples of design rules include minimum geometry widths, spacing between n-wells of different potentials, etc.

10.2 • Techniques

Analog circuits require careful layout to reduce mismatches, parasitics, noise, etc.

10.2.1 Multifinger Devices

So far only the effective width of transistors have been considered. For wide transistors it is common to use multiple *fingers*, reducing source/drain junction area and improving gate resistance. In addition multipliers are often used to split a single wide transistor into multiple narrower devices.

10.2.2 Symmetry

Circuits dealing with fully differential circuits require symmetry. Mismatch between devices introduce offsets, even-order nonlinearity, and reduce common-mode rejection, worsening noise performance. The layout of structures such as differential pairs and current mirrors require careful attention. Many steps during the fabrication process behave differently along different axes [12].

Transistor operation is dependent on the surrounding environment. Maintaining the same environment on two sides of a axis of symmetry is important. A common technique is to place "dummy" devices on each side of a device, ensuring the same environment.

To reduce the mismatches for large transistors along the axes, a *common-centroid* layout can be used, cancelling the axes "gradients". Consider two devices *A* and *B*, each with a multiplier of four, placed on a common-centroid layout in Table 10.1. Summing across the either axis results in zero for both devices.

| -2 | -1 | +1 | +2 | |
|----|----|----|----|----|
| A | B | B | A | +1 |
| B | A | A | B | -1 |

Table 10.1: Common-centroid layout of devices *A* and *B*

¹Or an equivalent process such as ion implantation.

10.3 • Two-Stage Layout

For the two-stage amplifier the input PMOS and current mirror NMOS devices are placed in a common-centroid configuration. Variations in the cascode devices due to the surrounding environment have little effect due to heavy source generation. Reference voltages/currents were out of scope for this project, and were not included in the layout. The total area of the layout is $120\mu\text{m} \cdot 70\mu\text{m} = 8400\mu\text{m}^2$.

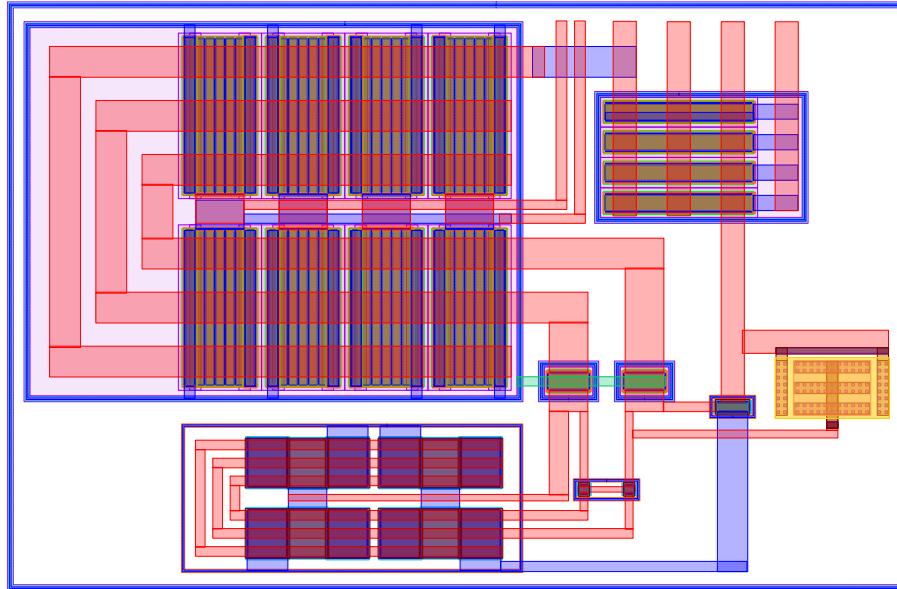


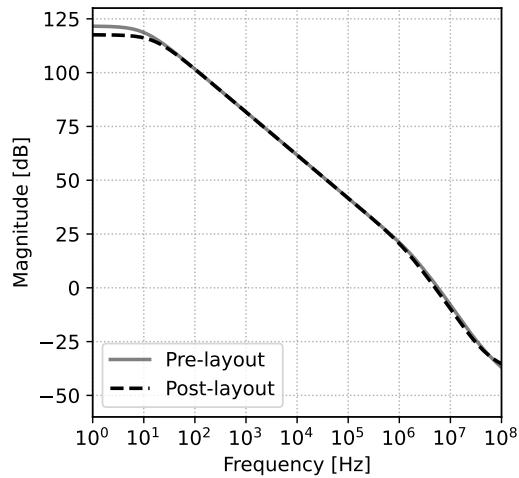
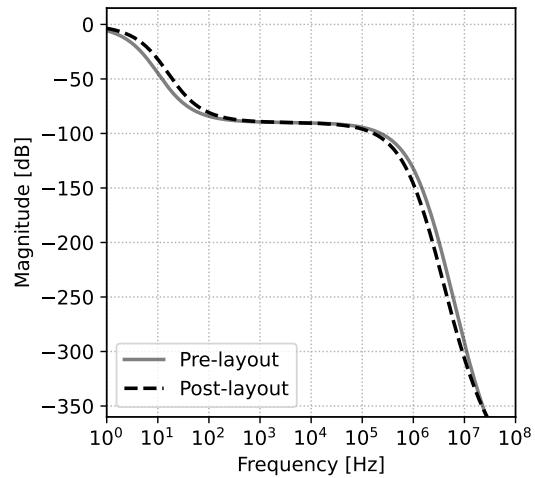
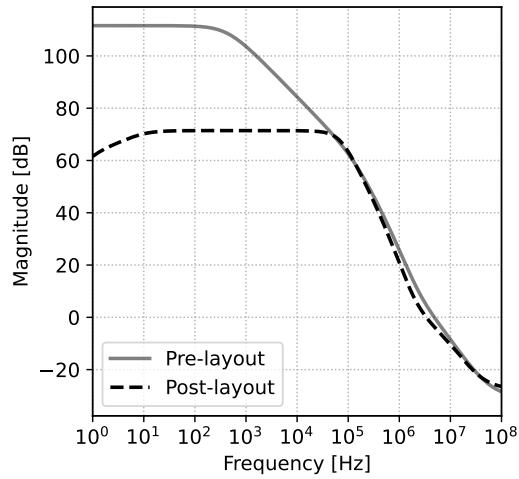
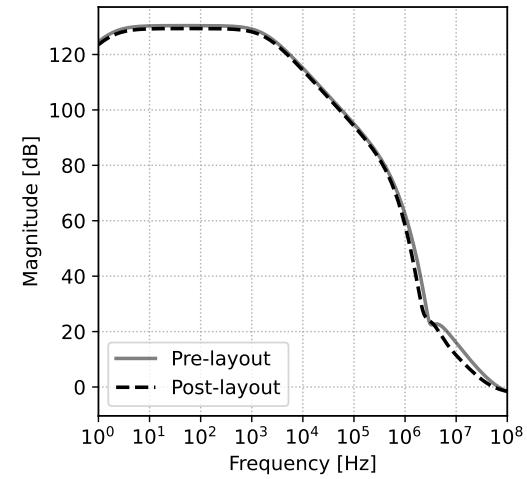
Figure 10.1: Layout of the two-stage amplifier.

10.3.1 Post-Layout Simulation

Table 10.2: Two-Stage Post-Layout Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|---------------------------------|------|--------|------|--------------------------------|------------------------|
| Input offset voltage | V_{IO} | | -101.4 | | μV | |
| Open-loop DC gain | A_0 | | 117.6 | | dB | |
| Common-mode rejection ratio | CMRR | | 70.21 | | dB | |
| Power-supply rejection ratio | PSRR | | 125 | | dB | |
| Unity-gain bandwidth | B_1 | | 5.021 | | MHz | |
| Phase margin | $\text{PM}_{30\text{dB}}$ | | 68 | | ° | $A_{CL} = 30\text{dB}$ |
| Integrated noise 1Hz-200Hz | $\int_1^{200} \overline{V_n^2}$ | | 2.969 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | |
| Integrated noise 1Hz-1kHz | $\int_1^{1k} \overline{V_n^2}$ | | 4.138 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | |

¹ Single analysis, with $C_L = 500\text{fF}$.

**Figure 10.2:** Two-stage post-layout open-loop gain.**Figure 10.3:** Two-stage post-layout open-loop phase.**Figure 10.4:** Two-stage post-layout open-loop CMRR.**Figure 10.5:** Two-stage post-layout open-loop PSRR

11 | System Design

With the amplifiers and pseudo-resistors designed, and a solid understanding of switched-capacitor equivalent resistors, we are now ready to design the system to the specifications presented in Chapter [5].

11.1 • Neural Amplifier

The neural amplifier must provide low noise and a closed-loop gain of 30dB. The closed loop configuration is shown in [Figure 11.2]. There are three candidates to choose for the amplifier [Table 11.1]. There is a significant compromise between power and noise. Capacitors C_1 and C_2 set the gain $A_{CL} = C_1/C_2$. The pseudo-resistor from Chapter [6.2] is used for common-mode feedback.

| Amplifier | A_0 [dB] | Power [μW] | \int Noise [$\text{nV}/\sqrt{\text{Hz}}$] |
|------------------|------------|-------------------------|---|
| Two-Stage LP | 121.6 | 3.2 | 3.570 |
| Three-Mirror OTA | 102.1 | 9.7 | 2.939 |
| Two-Stage LN | 132.1 | 31 | 1.181 |

Figure 11.1: Amplifier comparison for NA.

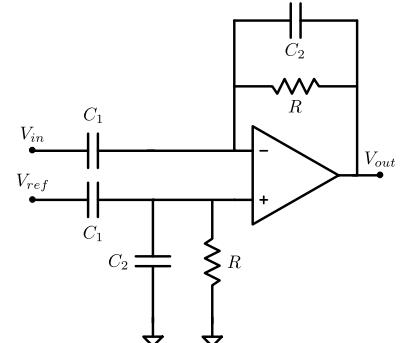


Figure 11.2: Neural amplifier closed loop configuration.

11.2 • Low-Pass Filter

For the 2nd order butterworth filter, a salien-key topology is chosen. Shown in [Figure 11.4], resistors are replaced with switched-capacitor equivalents. A switching frequency of 100kHz is chosen as it is well above the bandwidth of interest (it is also the clock frequency for the ADC).

The pole frequency is given by (11.1). If the filter gain is denoted A_f , $R_{eq1} = R_{eq2}$, and $C_1 = C_2$, the quality factor is given by (11.2). Denoting the switched capacitors $C_{eq1}, C_{eq2}, C_{eq3}, C_{eq4}$, the chosen values are shown in [Table 11.1], giving a cut-off frequency of $f_0 = 1\text{kHz}$ and $A_f = 6\text{dB}$ for a quality factor of $Q = 1$. The filter response is shown in [Figure 11.3].

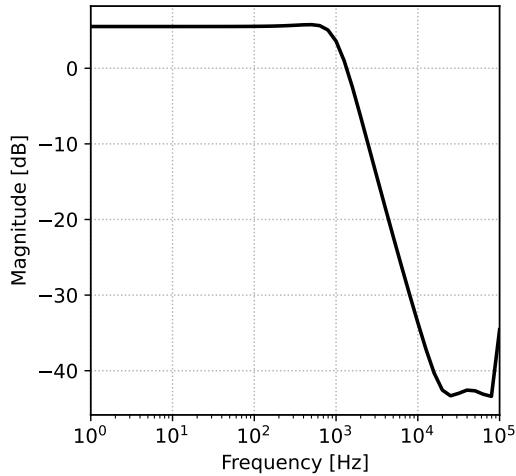
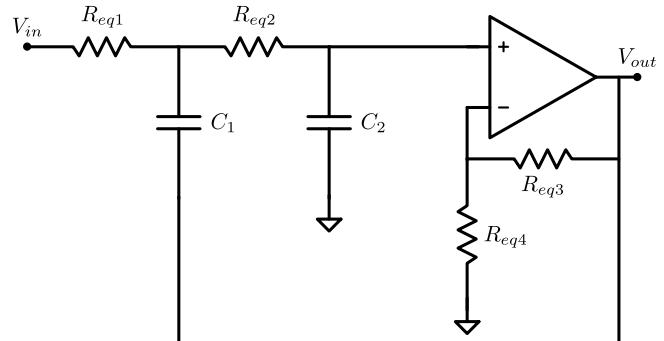
The unity-gain stable three-mirror OTA was used in the filter.

$$f_0 = \frac{1}{2\pi\sqrt{R_{eq1}R_{eq2}C_1C_2}} \quad (11.1)$$

$$Q = \frac{1}{3 - A_f} \quad (11.2)$$

| Designator | C_{eq1} | C_{eq2} | C_{eq3} | C_{eq4} | C_1 | C_2 | f_s |
|------------|-----------|-----------|-----------|-----------|-------|-------|--------|
| Value | 100fF | 100fF | 200fF | 200fF | 1.6pF | 1.6pF | 100kHz |

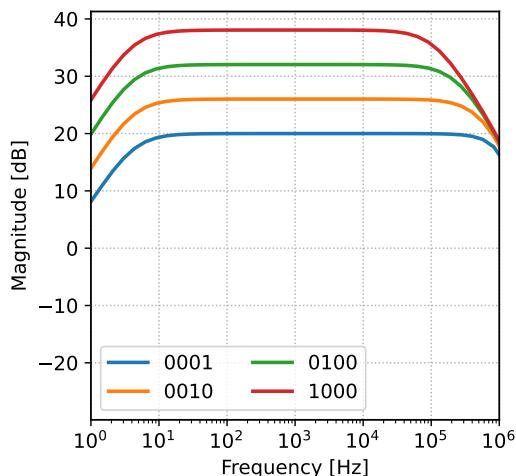
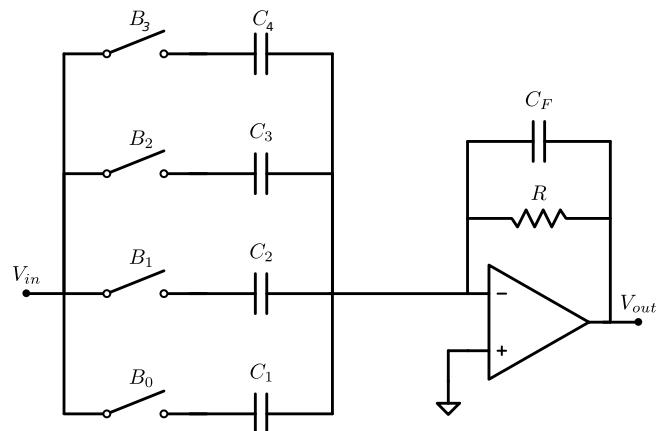
Table 11.1: Sallen-key capacitor values.

**Figure 11.3:** Sallen-key filter AC response.**Figure 11.4:** Sallen-key low-pass filter.

11.2.1 Programmable Gain Amplifier (PGA)

Considered as a part of the filter at the system level, the salen-key structure seen in [Figure 11.4] will be followed by a programmable gain amplifier. A separate amplifier is needed since the salen-key becomes unstable at higher gain. The PGA takes a 4-bit digital word, and switches the input capacitor to adjust the gain, shown in [Figure 11.6]. A pseudo-resistor is chosen for the common-mode feedback resistor R . By choosing capacitors as shown in [Table 11.2], the gain can be adjusted from approximately 20dB to 40dB. This way signals from $100\mu\text{V}$ to 1mV can be amplified to 1V . Note that while it is possible to switch the feedback capacitor for the same effect, it also changes the low frequency cut-off, which is not desired. The two-stage LP amplifier is used for the PGA. Fairly large capacitors were needed since the feedback capacitor sets the pole frequency, which ideally should be at least under 10Hz . All possible gain settings are shown in [Appendix B].

| Designator | C_F | C_1 | C_2 | C_3 | C_4 |
|------------|----------------|--------------|--------------|--------------|--------------|
| Value | 100fF | 1pF | 2pF | 4pF | 8pF |

Table 11.2: PGA capacitor values.**Figure 11.5:** PGA AC Response**Figure 11.6:** Programmable gain amplifier.

11.3 • Sample and Hold

A simple sample-and-hold circuit is created with a single sampling capacitor [Figure 11.8]. The unity-gain stable rail-to-rail input amplifier is used to buffer and sample the signal, and the clock splitter [Figure 6.11] is used to provide two non-overlapping clocks ϕ_1 and ϕ_2 . When ϕ_1 is high, the circuit is in sampling mode, and the voltage across the capacitor tracks the V_{in} . When ϕ_2 is high, the circuit is in amplification mode, and V_{out} rises to the sampled voltage. The clock frequency is chosen to be 100kHz to match the ADC. The response of the sample-and-hold is shown in [Figure 11.7].

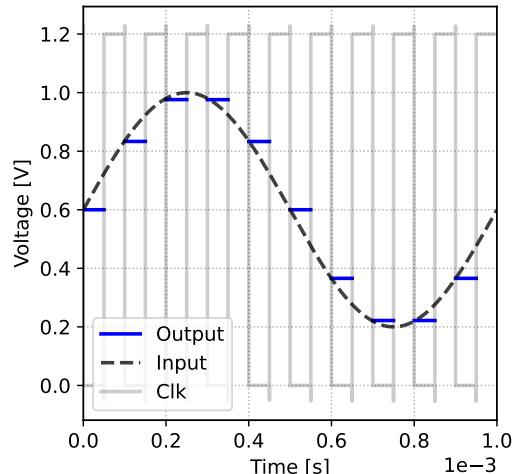


Figure 11.7: Sample-and-hold input, output, and clock.

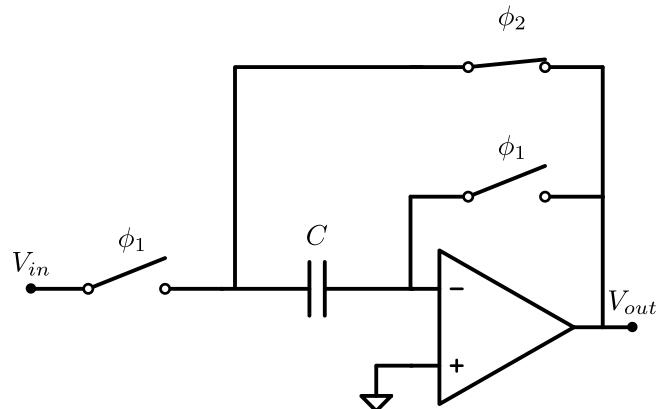


Figure 11.8: Sample-and-hold unity gain buffer.

11.4 • Results

The entire analog front-end is simulated, excluding the sample-and-hold. The bootstrap circuit in the ADC turned out to be performing well, so the S/H is not needed. Results are shown in [Table 11.3] (differential operation) with a 1mV input at 200Hz.

| NA | THD [dB] | SNR [dB] | ENOB | Total Power Consumption [μW] |
|------------------|----------|----------|------|---|
| Two-stage LN | -62.49 | 57.71 | 9.12 | 33.7 |
| Two-stage LP | -57.35 | 50.33 | 7.97 | 11.2 |
| Three-mirror OTA | -59.27 | 55.96 | 8.76 | 14.40 |

Table 11.3: Analog front-end performance.

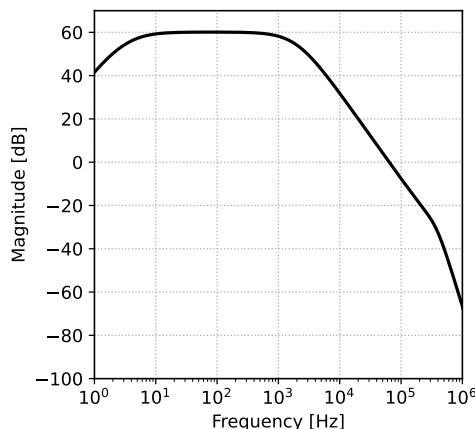


Figure 11.9: Analog front-end AC response (NA = three-mirror OTA)

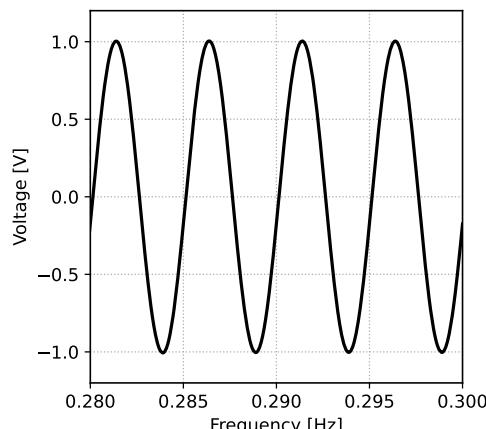


Figure 11.10: Analog front-end transient response @ 200Hz (NA = three-mirror OTA)

12 | Results

The analog-frontend was put together with the ADC. All three amplifier candidates for the NA were tested. ENOB, SNR, and SINAD were measured at the ADC output for each, and the results are shown in [Table 12.1]. Overall the three-mirror OTA is the best compromise between power and noise. It offers a sufficient ENOB more than 8.

The transient response of the entire system is shown in [Figure 12.1]. The delay between the input and output is due to the 10 clock cycles for the ADC to do a binary search for the correct digital output word. Performance is summarized in [Table 12.1] with a 1mV input at 225Hz. The ADC uses approximately $0.5\mu\text{W}$.

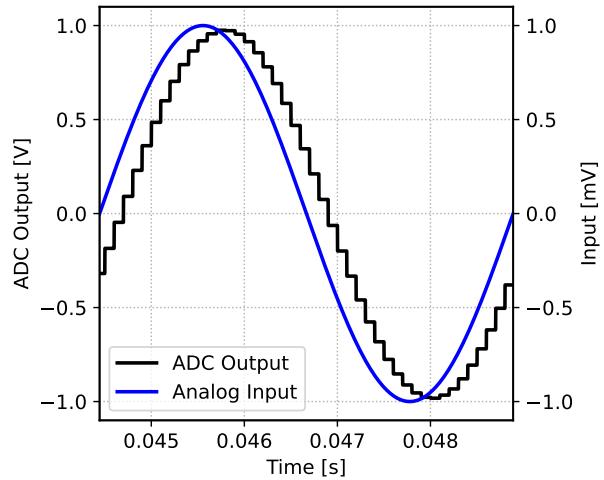


Figure 12.1: Input signal and ADC output with two-stage LP NA.

| NA | THD [dB] | SNR [dB] | ENOB | Total Power Consumption [μW] |
|------------------|----------|----------|------|---|
| Two-stage LP | -62.34 | 49.77 | 7.98 | 11.7 |
| Two-stage LP | -67.83 | 58.14 | 9.33 | 34.2 |
| Three-mirror OTA | -61.87 | 52.68 | 8.41 | 14.9 |

Table 12.1: System performance.

13 | Conclusion

For this project a general purpose analog front-end capable of measuring EEG signals was designed for the TSMC65 technology node. The front-end was designed with a 10-bit SAR ADC in mind, and was capable of 8.41 ENOB with a total power consumption of $11.7\mu\text{W}$ when using the three-mirror OTA as the neural amplifier. The g_m/I_D method was used in conjunction with custom built applications (*Analog Explorer*, *Analog Designer*) to accurately size devices. Operation in moderate inversion, which is a region not easily described by equations, was used heavily as a compromise between power and speed. Three common amplifier topologies were studied; a three-mirror OTA, a two-stage amplifier, and a two-stage folded cascode amplifier.

In addition techniques for designing resistor equivalents were investigated thoroughly, and a subthreshold pseudo resistor was used for common-mode feedback, and parasitic agnostic switched-capacitors were used in the low-pass filter for accurately setting the cut-off frequency. With the PGA, the system is capable of gain from 57dB to 77dB.

A layout was done for the two-stage low-noise amplifier, employing various techniques for reducing transistor variance, e.g. common centroid. The combined area for the amplifier was $8400\mu\text{m}^2$. A post-layout simulation was done to show the effects that parasitics have on the amplifier.

In summary, this project proved a good exploration of modern techniques for sizing analog CMOS circuits, and the impact that layout has on performance. The project demonstrated clearly the challenges and compromises in analog design, and sought solutions for them. There is however many things that could be improved in future works. With more time and experience, the layout could certainly be more optimized, perhaps improving the lackluster CMRR. The noise performance was also unsatisfactory considering the power consumption needed to achieve it. For future work it would be worth exploring chopper stabilization, a technique that allows filtering of flicker noise. This system was made general purpose, but if a future system was targeting *only* EEG, it would be worth designing the amplifiers with a lower GBW target, improving the power consumption.

14 | References

Articles

- [1] R. Harrison, "A Low-Power, Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003. DOI: [10.1109/JSSC.2003.811979](https://doi.org/10.1109/JSSC.2003.811979).
- [2] H. Kassiri, K. Abdelhalim, and R. Genov, "Low-Distortion super-GOhm subthreshold-MOS resistors for CMOS neural amplifiers," *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2013. DOI: [10.1109/BioCAS.2013.6679691](https://doi.org/10.1109/BioCAS.2013.6679691).
- [3] D. Markovic, "An 80-mV_{pp} Linear-Input Range, 1.6-GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That is Tolerant to 650-mV_{pp} Common-Mode Interference," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, 2017. DOI: [10.1109/JSSC.2017.2753824](https://doi.org/10.1109/JSSC.2017.2753824).
- [4] H. Chandrakumar and D. Markovic, "A High Dynamic-Range Neural Recording Chopper Amplifier for Simultaneous Neural Recording and Stimulation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, 2017. DOI: [10.1109/JSSC.2016.2645611](https://doi.org/10.1109/JSSC.2016.2645611).
- [5] S. L. Pinjare, G. Nithya, V. S. Nagaraja, and A. Sthuthi, "A gm/id based methodology for designing common source amplifier," 2018. DOI: [10.1109/icmete.2018.00073](https://doi.org/10.1109/icmete.2018.00073).
- [6] S. Tiwari, S. Goel, and A. Bhardwaj, "Midnn- a classification approach for the eeg based motor imagery tasks using deep neural network," *Applied Intelligence*, vol. 52, Mar. 2022. DOI: [10.1007/s10489-021-02622-w](https://doi.org/10.1007/s10489-021-02622-w).
- [7] D. A. Hall, K. A. Makinwa, and T. Jang, "Quantifying biomedical amplifier efficiency: The noise efficiency factor," *IEEE Solid-State Circuits Magazine*, vol. 15, no. 2, pp. 28–33, 2023. DOI: [10.1109/MSSC.2023.3256353](https://doi.org/10.1109/MSSC.2023.3256353).
- [8] K. Martin and A. Sedra, "Switched-capacitor building blocks for adaptive systems," *IEEE Transactions on Circuits and Systems*, vol. 28, no. 6, pp. 576–584, 1981. DOI: [10.1109/TCS.1981.1085017](https://doi.org/10.1109/TCS.1981.1085017).

Application Notes

- [9] W. Kester, *Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor*, MT-003, Analog Devices.
- [10] *Noise Calculations of Op-Amp Circuits*, R13AN0010, Rev.1.00, Renesas, Aug. 2020.

Books

- [11] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed. John Wiley and Sons, 2012, ISBN: 978-0-470-77010-8.
- [12] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. McGraw-Hill, 2017, ISBN: 978-0-07-252493-2.
- [13] A. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. Oxford University Press, 2014, ISBN: 978-0-19-933913-6.
- [14] P. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press, 2017. DOI: [10.1017/9781108125840](https://doi.org/10.1017/9781108125840).
- [15] M. J. M. Pelgrom, *Analog-to-Digital Conversion*, 4th ed. Springer, 2021, ISBN: 978-3-030-90807-2.

Videos

- [16] D. H. Omran, *the gm/ID Design Methodology Demystified (English)*, Master Micro, 2021. [Online]. Available: <https://www.youtube.com/watch?v=dzz4z3ijVts>.

Websites

- [17] "How to calculate enob for adc dynamic performance measurement," Analog Devices. (Jun. 2019), [Online]. Available: <https://www.analog.com/en/resources/technical-articles/how-to-calculate-enob-for-adc-dynamic-performance-measurement.html>.

List of Figures

| | | |
|------|--|----|
| 4.1 | Square-law I_D (best-fit) versus short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$ | 2 |
| 4.2 | Square-law g_m (best-fit) versus short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$ | 2 |
| 4.3 | g_m/I_D vs V_{GS} for a short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$ | 3 |
| 4.4 | $\log I_D$ vs V_{GS} for a short and long channel TSMC65 device (nch_25) @ $V_{DS} = 2V$ | 4 |
| 4.5 | MOS device in weak inversion. | 4 |
| 4.6 | V_A versus V_{DS} for short and long channel TSMC65 device (nch_25) @ $V_{GS} = 0.6V$ | 6 |
| 4.7 | Example LUT for TSMC65 nch @ $V_{DS} = 0.6V$, $L = 10\mu m$ | 7 |
| 4.8 | Sizing a TSMC65 nch transistor at moderate inversion with $I_D = 1\mu A$. | 8 |
| 5.1 | System Overview | 9 |
| 5.2 | Amplitude and frequency characteristics of neural signals. [3] [6] | 9 |
| 5.3 | ADC block diagram [11]. | 10 |
| 5.4 | ADC transfer curve [11]. | 10 |
| 6.1 | Variable V_{GS} pseudo resistor implementations. | 14 |
| 6.2 | Three fixed V_{GS} pseudo resistor implementations. | 14 |
| 6.3 | Resistance of variable V_{GS} pseudo resistors. | 14 |
| 6.4 | Resistance of fixed V_{GS} pseudo resistors. | 14 |
| 6.5 | Active implementation of pseudo resistor F. | 15 |
| 6.6 | Resistance of active pseudo resistor F. | 15 |
| 6.7 | An integrated circuit capacitor with parasitic capacitances. | 15 |
| 6.8 | CMOS switches. | 15 |
| 6.9 | Switched-capacitor equivalent resistor circuit. | 16 |
| 6.10 | Parasitic insensitive switched-capacitor resistor equivalent. | 16 |
| 6.11 | Non-overlapping clock generator. | 16 |
| 7.1 | Output Transconductance Amplifier Structure | 17 |
| 7.2 | OTA closed-loop gain and phase. | 20 |
| 7.3 | OTA closed-loop gain and phase. | 20 |
| 7.4 | OTA loop-gain and phase. | 20 |
| 7.5 | OTA CMRR and PSRR. | 20 |
| 7.6 | OTA closed-loop step response. | 20 |
| 7.7 | OTA input-referred noise. | 20 |
| 7.8 | OTA closed-loop $A_V = 27dB$ THD | 21 |
| 7.9 | OTA closed-loop $A_V = 27dB$ ENOB | 21 |
| 7.10 | OTA buffer open-loop AC response. | 22 |
| 7.11 | OTA buffer CMRR. | 22 |
| 8.1 | Two-stage amplifier schematic. | 23 |
| 8.2 | Two-stage LP closed-loop gain and phase. | 27 |
| 8.3 | Two-stage LP closed-loop gain and phase. | 27 |
| 8.4 | Two-stage LP loop-gain and phase. | 27 |
| 8.5 | Two-stage LP CMRR and PSRR. | 27 |
| 8.6 | Two-stage LP closed-loop step response. | 27 |

| | | |
|-------|---|----|
| 8.7 | Two-stage LP input-referred noise. | 27 |
| 8.8 | Two-stage LP closed-loop $A_V = 27\text{dB}$ THD | 28 |
| 8.9 | Two-stage LP closed-loop $A_V = 27\text{dB}$ ENOB | 28 |
| 8.10 | Two-stage LN closed-loop gain and phase. | 29 |
| 8.11 | Two-stage LN closed-loop gain and phase. | 29 |
| 8.12 | Two-stage LN loop-gain and phase. | 29 |
| 8.13 | Two-stage LN CMRR and PSRR. | 29 |
| 8.14 | Two-stage LN closed-loop step response. | 29 |
| 8.15 | Two-stage LN input-referred noise. | 29 |
| 8.16 | Two-stage LN closed-loop $A_V = 27\text{dB}$ THD | 30 |
| 8.17 | Two-stage LN closed-loop $A_V = 27\text{dB}$ ENOB | 30 |
| 9.1 | Two-stage folded cascode with rail-to-rail input. | 31 |
| 9.2 | Folded cascode closed-loop gain and phase. | 33 |
| 9.3 | Folded cascode closed-loop gain and phase. | 33 |
| 9.4 | Folded cascode loop-gain and phase. | 33 |
| 9.5 | Folded cascode CMRR and PSRR. | 33 |
| 9.6 | Folded cascode closed-loop step response. | 33 |
| 9.7 | Folded cascode input-referred noise. | 33 |
| 9.8 | Folded-cascode closed-loop $A_V = 27\text{dB}$ THD | 34 |
| 9.9 | Folded-cascode closed-loop $A_V = 27\text{dB}$ ENOB | 34 |
| 9.10 | Folded-cascode g_m variance with input common-mode. | 34 |
| 10.1 | Layout of the two-stage amplifier. | 36 |
| 10.2 | Two-stage post-layout open-loop gain. | 37 |
| 10.3 | Two-stage post-layout open-loop phase. | 37 |
| 10.4 | Two-stage post-layout open-loop CMRR. | 37 |
| 10.5 | Two-stage post-layout open-loop PSRR | 37 |
| 11.1 | Amplifier comparison for NA. | 38 |
| 11.2 | Neural amplifier closed loop configuration. | 38 |
| 11.3 | Sallen-key filter AC response. | 39 |
| 11.4 | Sallen-key low-pass filter. | 39 |
| 11.5 | PGA AC Response | 39 |
| 11.6 | Programmable gain amplifier. | 39 |
| 11.7 | Sample-and-hold input, output, and clock. | 40 |
| 11.8 | Sample-and-hold unity gain buffer. | 40 |
| 11.9 | Analog front-end AC response (NA = three-mirror OTA) | 40 |
| 11.10 | Analog front-end transient response @ 200Hz (NA = three-mirror OTA) | 40 |
| 12.1 | Input signal and ADC output with two-stage LP NA. | 41 |

List of Tables

| | | |
|-----|--|----|
| 4.1 | Inversion level depending on g_m/I_D | 4 |
| 4.2 | Degrees of Freedom for sizing a MOS device | 5 |
| 6.1 | Resistor types in TSMC65 | 13 |

| | |
|---|----|
| 6.2 Monte-carlo (process variance) simulation of TSMC65 resistors (N = 200) | 13 |
| 7.1 OTA Device Specifications | 18 |
| 7.2 OTA buffer device specifications | 19 |
| 7.3 Three-mirror OTA buffer electrical characteristics | 21 |
| 7.4 Three-mirror OTA electrical characteristics | 22 |
| 8.1 Two-stage LP Transistor Specifications | 25 |
| 8.2 Two-stage LN Transistor Specifications | 26 |
| 8.3 Two-stage LP Electrical Characteristics | 28 |
| 8.4 Two-stage LN Electrical Characteristics | 30 |
| 9.1 Folded Cascode Transistor Specifications | 32 |
| 9.2 Two-Stage Folded Cascode Electrical Characteristics | 34 |
| 10.1 Common-centroid layout of devices <i>A</i> and <i>B</i> | 35 |
| 10.2 Two-Stage Post-Layout Electrical Characteristics | 36 |
| 11.1 Sallen-key capacitor values. | 38 |
| 11.2 PGA capacitor values. | 39 |
| 11.3 Analog front-end performance. | 40 |
| 12.1 System performance. | 41 |
| B.1 PGA gain settings. | 48 |

A | ***Github***

All software developed for this project is available on the author's Github page.

The repository can be found at <https://github.com/Ponti17/bsc-eeg-frontend>.

B | ***PGA Gain Settings***

| Binary | Gain [dB] |
|--------|-----------|
| 0001 | 19.95 |
| 0010 | 25.97 |
| 0011 | 29.49 |
| 0100 | 31.99 |
| 0101 | 33.93 |
| 0110 | 35.51 |
| 0111 | 36.85 |
| 1000 | 38.01 |
| 1001 | 39.04 |
| 1010 | 39.95 |
| 1011 | 40.78 |
| 1100 | 41.53 |
| 1101 | 42.23 |
| 1110 | 42.87 |
| 1111 | 43.47 |

Table B.1: PGA gain settings.