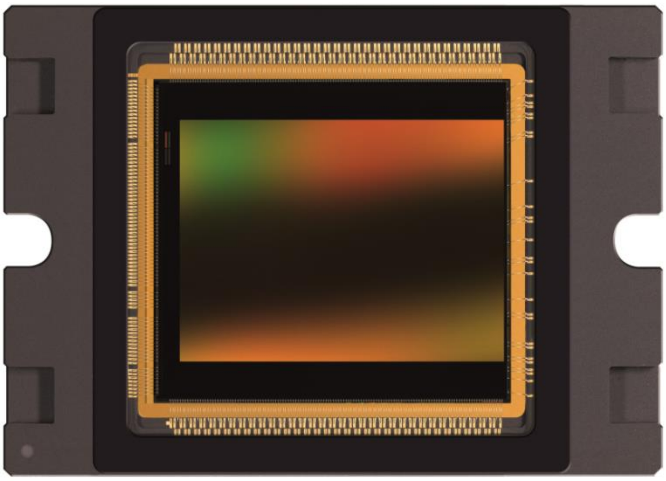
image sensors

12 Megapixel machine vision CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
1	27/10/10	Origination
2	4/5/11	Update to version 2
3	24/11/11	Update to version 3
4	25/4/12	Update to version 4, output rate from 600Mbps to 300Mbps
5	24/10/2012	Added frame rate formulas Added subsampling in Y output remapping Updated required register settings Updated one side and two side read-out modes Updated image flipping Updated color binning remapping
6	30/10/2012	Updated subsampling in Y examples Updated color binning pixel remapping Updated recommended value for register 107
7	19/04/2013	Added high grade variant to ordering info
8	19/06/2013	Removed Draft watermark and confidential footer
9	02/07/2013	Added: - Spectral response - Exposure timings - Tdig pins functionality Updated: - Frame rate and calculations - CLK_IN and SPI_CLK: 60MHz → 30MHz - Input clock speed restrictions - Frame request timings - Pixel timing figures for 2 sided read-out - Multiple windows details - PLR register functionality - Required register settings of chapter 5.16 - Register 107 setting: 9814 → 10326
10	01/08/2013	Updated: - Required register settings of chapter 5.16 Removed preliminary text in header
11	02/08/2013	Added High Grade definition
v1.12	18/10/2013	Splitting up the datasheets for v1 (300MHz) and v2 (600MHz) devices. Updated: - Pixel (0,0) location - Assembly drawing - Row order for 1 sided read out - Training pattern 1 & 2 location Added: - Test pattern

Issue	Date	Modification
v1.13	20/01/2014	Removed: - High grade variant from ordering info as all devices are now high grade. Updated: - Supply settings - Figures 21, 23 - Title of chapter 4.3 - References Added: - Power saving per disabled output in ch 5.13
V1.14	14/02/2014	Updated: - Frame rate formula (ch3.6) of XY-subsampling (frame rate x2)
V1.15	13/03/2014	Updated: - Figure 54: Color binning, pixel to output remapping - Exposure time calculation and FOT overlap Added: - ADC vs. clock speed plot
V1.16	04/07/2014	Updated: - VDD18 from 1.9V → 1.98V - Temperature sensor description - Power consumption 2W → 3W Added: - Typical LVDS output skew (Figure 35) - Self-heating
V1.17	18/12/2014	Updated: - Figures for multiple slopes. The figures are also correct when using only 1 knee point. - Temperature sensor offset in DN instead of °C/DN - Digital gain details Added: - Tilt and rotation of die in assembly drawing - SPI I/O's pulled low when not used/enabled.
V1.18	10/02/2015	Updated: - Binning sums the pixels in the analog domain - In binning mode, only PGA /3 is useable

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1 INTRODUCTION

1.1 OVERVIEW

The CMV12000 is a high speed CMOS image sensor with 4096 by 3072 pixels (22.5mm x 16.9mm) developed for machine vision and other applications. The image array consists of 5.5µm x 5.5µm pipelined global shutter pixels which allow exposure during read-out. The image sensor has 64 8-, 10- or 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 300 Mbps which results in 74 fps frame rate at full resolution and 12-bit. When 10-bit per pixel is used, the frame rate increases to 150 fps. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read-out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- 4096 * 3072 active pixels on a 5.5um pitch
- Frame rate 74 frames/sec in 12-bit mode
- Frame rate 150 frames/sec in 10-bit mode
- Frame rate 168 frames/sec in 8-bit mode
- Row windowing capability (up to 32 separate windows)
- X-Y mirroring function
- Master clock max 300 MHz
- 64 LVDS-outputs @ 300 Mbps multiplexable to 32, 16, 8 ,4 ,2 and 1 output(s) at reduced frame rate
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- High Dynamic Range modes supported (multiple slope and dual exposure)
- On chip temperature sensor
- On chip timing generation
- SPI-control
- Ceramic µPGA package (237 pins)
- 3.3V signaling

1.3 SPECIFICATIONS

- Full well charge: 13.5 Ke$^-$
- Sensitivity: 4.64 V/lux.s (with microlenses)
- Dark noise: 13 e$^-$
- Conversion factor: 0.075 bit/e$^-$
- Dynamic range: 60 dB
- Parasitic light sensitivity: 1/50 000
- Dark current: 22 LSB/s
- Fixed pattern noise: <1 LSB (<0.1% of full swing in 10-bit mode)
- Power consumption: 3 W

1.4 CONNECTION DIAGRAM

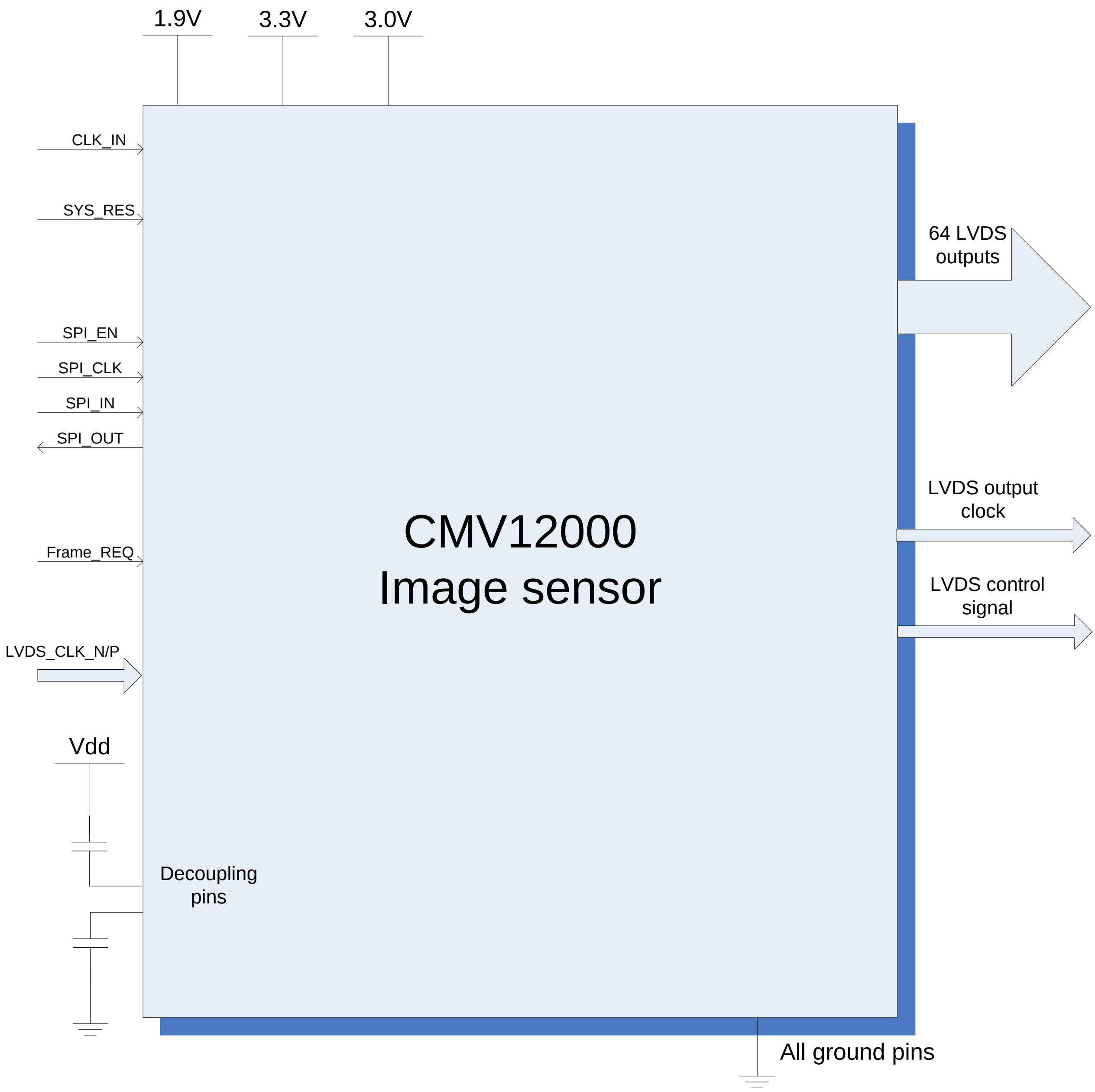


FIGURE 1: CONNECTION DIAGRAM FOR THE CMV12000 IMAGE SENSOR

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

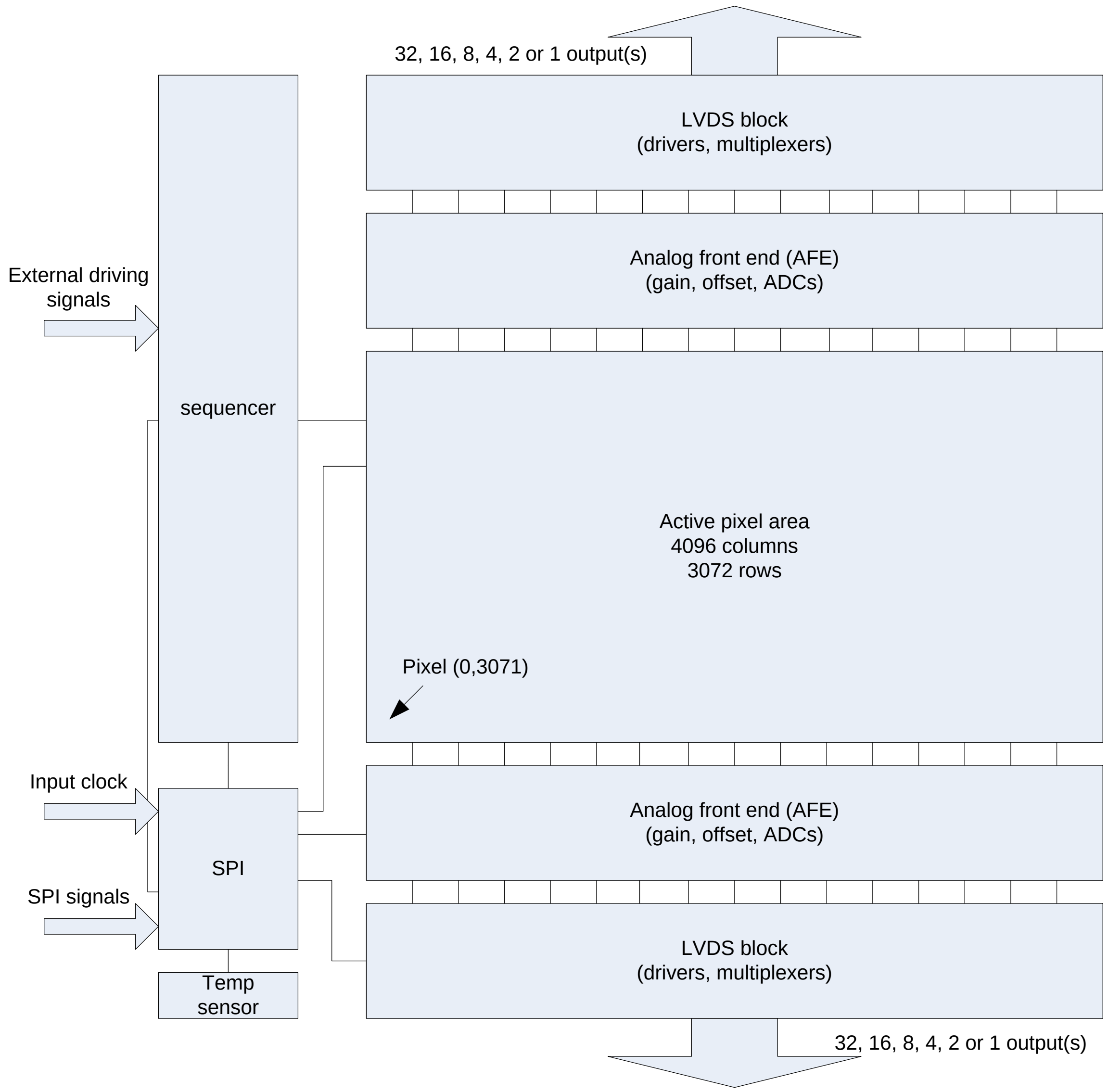


FIGURE 2: SENSOR BLOCK DIAGRAM

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and they are read out sequentially, row-by-row. On the pixel output, an analog gain is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 128 adjacent columns of the array. The read-out of the pixel array is performed on both sides (top and bottom) of the pixel array to speed up the read-out process and achieve the frame rate of 150 fps at full resolution and 10-bit. In each line read-out cycle, two lines are selected for read-out. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 4096 x 3072 square global shutter pixels with a pitch of 5.5um (5.5µm x 5.5µm). This results in an optical area of 22.5mm x 16.9mm (28.1mm diameter).

The pixels are designed to achieve maximum sensitivity with low noise (using CDS) and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%).

There are 16 dark reference columns available on the sensor (columns 0 to 7 and 4088 to 4095) which can be enabled/disabled by programming the appropriate sensor register. See chapter 5 for more information.

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to an 8-, 10- or 12-bit value and can apply a gain. A digital offset can also be applied to the output of the column ADCs. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 300 Mbps. The sensor has 66 LVDS output pairs:

- 64 Data channels
- 1 Control channel
- 1 Clock channel

The 64 data channels are used to transfer 8-bit, 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock (max 150 MHz), synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 0 of this document.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.5 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the register with address 127.

A calibration of the temperature sensor (read-out the value at specific temperatures to get a calibration factor) is needed by the surrounding system, because the offset can differ per device. The slope is very similar for all devices. A typical temperature sensor output vs. temperature curve can be found below together with a typical offset and slope formula.

$Slope = 3.5 * \frac{LVDS\_CLK\_IN}{300}\ [°C/DN]$	$Offset\ at\ 0°C = 825 * \frac{LVDS\_CLK\_IN}{300}\ [DN]$

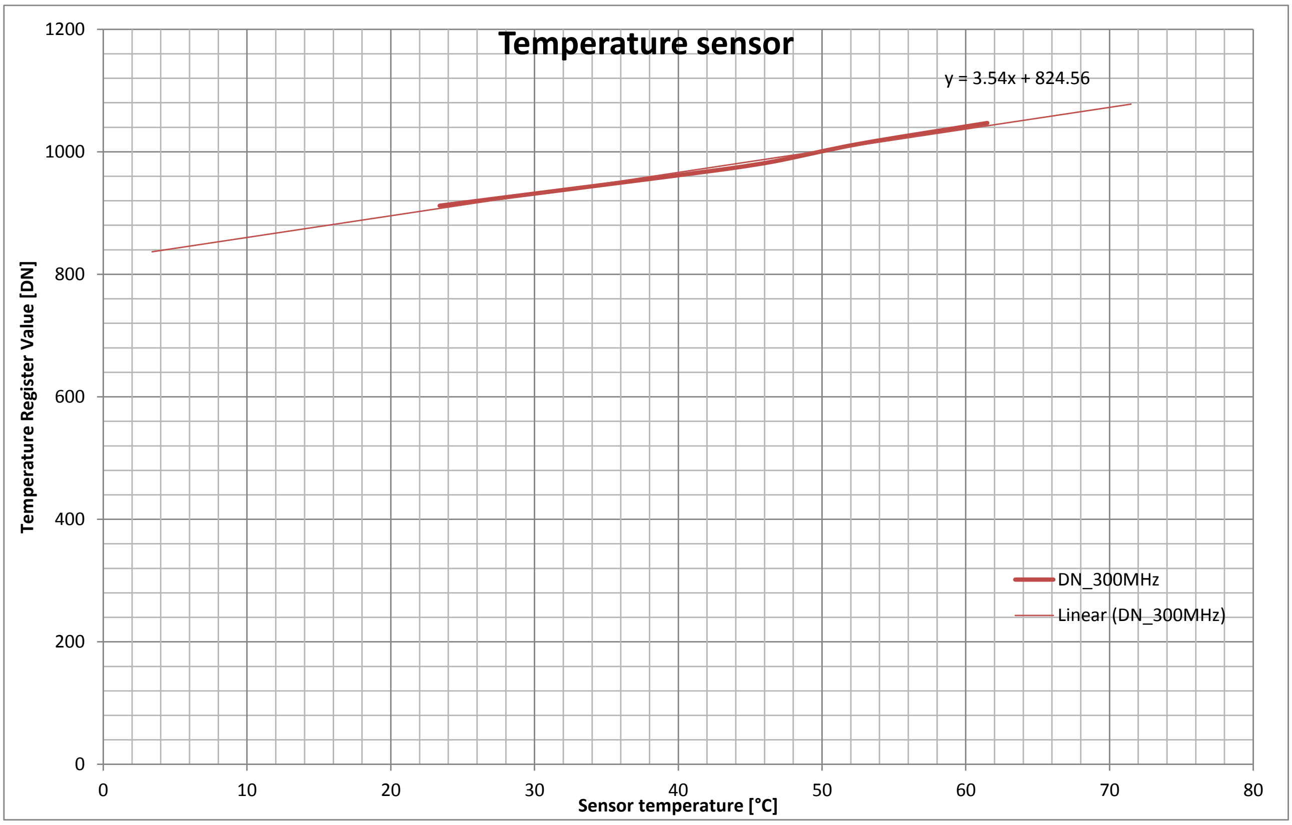


FIGURE 3: TYPICAL OUTPUT OF THE TEMPERATURE SENSOR OF THE CMV12000

3 DRIVING THE CMV12000

3.1 SUPPLY SETTINGS

The CMV12000 image sensor has the following supply settings:

Supply name	Required value	Max. Range	Current nominal	DC Power nom.	Current peak
VDD18	1.98V	1.80V-1.98V	700mA	1260mW	1.1A
VDD33	3.3V	3V-3.6V	180mA	600mW	250mA
VDD_PIX	3.0V	2.3V-3.6V	15mA	15mW	1A
VDD_RES	3.3V	3.0V-3.6V	25mA	17mW	100mA

See pin list for exact pin numbers for every supply.

VDD18 will draw the peak current during read out. The VDD18 peak current scales with the clock speed. The VDD33 has peak currents during read out, although they can be partially caught by decoupling. The VDD_PIX peak happens during FOT (when all pixels will reset). This peak is composed of spikes (1A) and a general DC current increase (~110mA). VDD_RES has its peaks during FOT.

VDD18 and VDD_PIX need the most decoupling to prevent the supplies to dip. For more details on the power figures and peak plots, an application note is available. This supply needs therefor decent decoupling to dampen the 1A peak.

The sensor will heat up above ambient. Below you can see some figures. Decent system heat management is needed to keep the sensors temperature below the specifications limit of 70°C.

LVDS input clock	IDLE	Readout at max. fps
100MHz	+20°C	+24°C
300MHz	+21°C	+30°C

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor

Pin name	Description
CLK_IN	Input clock, frequency range between 5 and 30 MHz. Usually set to the LVDS input clock divided by the bitmode.
LVDS_CLK_P/N	Input clock, frequency range between 100 and 300MHz, depending on the bit mode. See details in chapter 3.5.
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
FRAME_REQ	Frame request pin. When a high state is detected on this pin the programmed number of frames is captured and sent by the sensor. The pulse should be at least 8, 10 or 12 * LVDS input clock periods wide to be detected, depending on the used bitmode.

Pin name	Description
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 30 MHz)
T_EXP1	Input pin which can be used to program the exposure time externally. The pulse should be at least 8, 10 or 12 * LVDS input clock periods wide to be detected, depending on the used bitmode. Optional
T_EXP2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. The pulse should be at least 8, 10 or 12 * LVDS input clock periods wide to be detected, depending on the used bitmode. Optional

3.4 ELECTRICAL IO SPECIFICATIONS

3.4.1 DIGITAL IO CMOS/TTL DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 LVDS RECEIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

3.4.3 LVDS DRIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV

Parameter	Description	Conditions	min	typ	max	Units
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.125	1.25	1.375	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.5 Input clock

The LVDS input clock defines the output data rate of the CMV12000. The maximum data rate of the output is 300 Mbps which results in an input LVDS_CLK_P/N clock of 300MHz. The minimum LVDS_CLK_P/N frequency is 300MHz for 12 bit, 150MHz for 10 bit and 100MHz for 8 bit. If set lower, full swing may not be achieved. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate.

3.6 Frame rate

The frame rate of the CMV12000 is defined by 2 main factors.

1. Exposure time
2. Read-out time

For ease of use we will assume that the exposure time is equal to or shorter than the read-out time. By assuming this the frame rate is completely defined by the read-out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 300 MHz
2. ADC mode: 8-, 10- or 12-bit
3. Number of lines read-out (also subsampling or binning)
4. Number of LVDS outputs used: max 64 outputs

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV12000.

The total read-out time is composed of the FOT (frame overhead time) and the image read-out time.

$$FOT = (reg82[15:8] + 2) * Line\ time$$

$$Line\ time = (reg85 + 1) * \mathrm{LVDS\_CLK\_P/N\_period} * \#\mathrm{bits}$$

When running at 300MHz in 10 bit mode with 64 output channels, register 82[15:8] is 14 and register 85 is 128. This will result in a FOT = 68.8µs and a line time of 4.3µs

The image read-out time is dependent of the total number of read out lines (#read out lines) and the line time.

$$Readout\ time = Line\ time * \frac{\#read\ out\ lines}{\#\ sides\ used}$$

The number of read out lines will depend on the mode you are using:

$$
\begin{array}{ll}
Normal: & \#read\ out\ lines =\ Number\_lines\_tot \\
Subsampling\ in\ X/Y: & \#read\ out\ lines = Number\_lines\_tot/2 \\
Binning: & \#read\ out\ lines = Number\_lines\_tot/4
\end{array}
$$

Number_lines_tot is the value of register 1. So with the above conditions and reading the full pixel array we have an image read-out time of 6.6048ms.

The total frame time will be 6.6048ms + 0.0688ms = 6.6736ms which results in a frame rate of 149.8fps.

If the exposure time is longer than the read-out time the frame rate will depend on the exposure time.

Below you can see an overview of the frame rate in fps for a full resolution image and 64 outputs with a 300MHz LVDS input clock.

Full resolution 64 outputs	Normal	X/Y Subsampling	Binning
Frame rate 8 bit	168	250.7	249.7
Frame rate 10 bit	149.8	266.4	265.7
Frame rate 12 bit	74.5	147.4	166.5

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV12000 is started up.

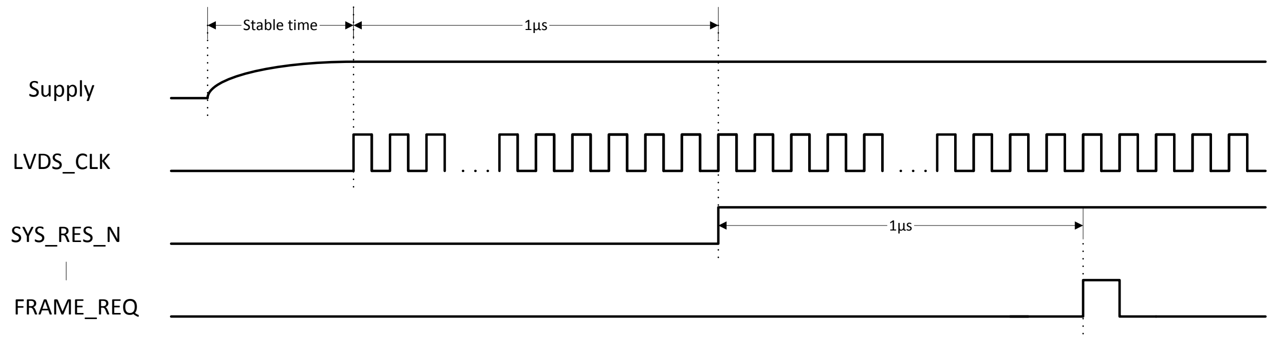


FIGURE 4: START-UP SEQUENCE

The master clock (300 MHz in for 300 Mbps) should only start after the rise time of the supplies. The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the FRAME_REQ pulse must be postponed until after the SPI upload has been completed.

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

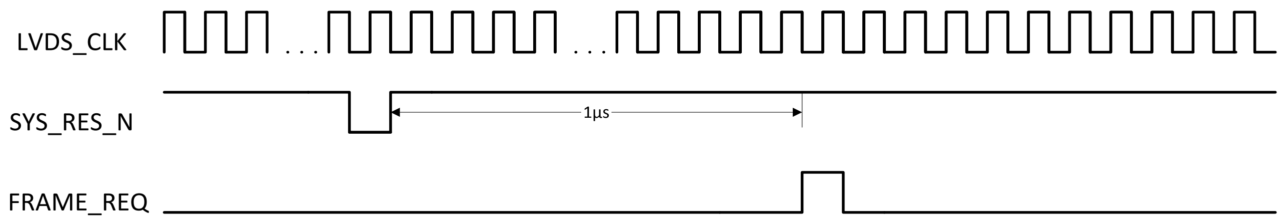


FIGURE 5: RESET SEQUENCE

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent.

When a switch from 12-bit to 10-bit or 8-bit mode (or vice versa) is necessary, the following sequence should be followed.

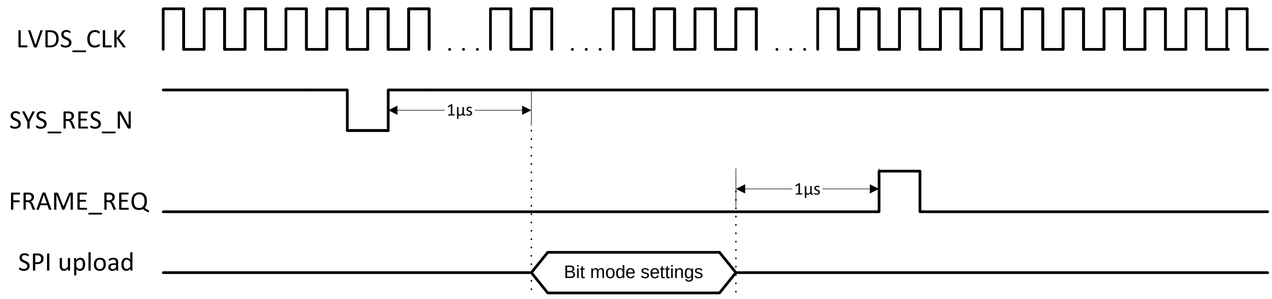


FIGURE 6: RESET SEQUENCE WHEN CHANGING BIT MODE

The following SPI register should be uploaded in this mode: Bit_mode (address 118): set to desired bit resolution mode

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

SPI I/O's are pulled low when not used/enabled.

3.9.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

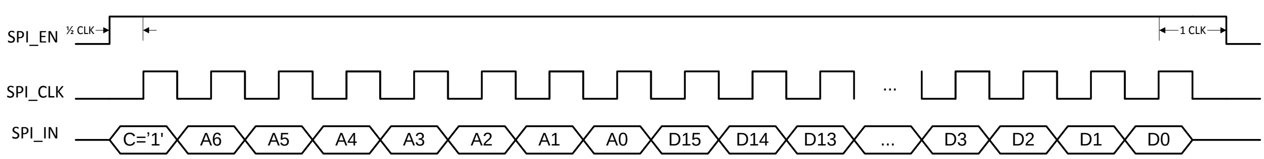


FIGURE 7: SPI WRITE TIMING

The data is sampled by the CMV12000 on the rising edge of the SPI_CLK and read-in at the last falling SPI_CLK edge. The SPI_CLK has a maximum frequency of 30 MHz. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled. SPI_EN has to remain high for 1 clock period after the last data bit is sampled.

One write action contains 24 data bits:

- One control bit: First bit to be sent, indicates whether a read ('0') or write ('1') will occur on the SPI interface.

- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 16 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written.

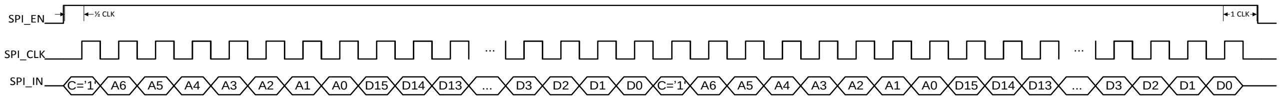


FIGURE 8: SPI WRITE TIMING FOR 2 REGISTERS

3.9.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

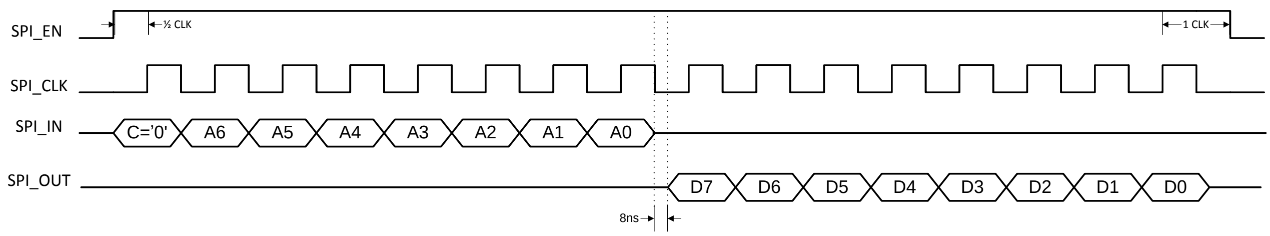


FIGURE 9: SPI READ TIMING

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK with an 8ns delay (independent of SPI or sensor clock speeds). This means that the data can be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first.

3.10 REQUESTING A FRAME

After starting up the sensor (see section 3.7), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (address 80). The default number of frames to be grabbed is 1.

In internal-exposure-time mode the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode the exposure time is set by programming the appropriate register (addresses 71-72) of the CMV12000.

After the high state of the FRAME_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

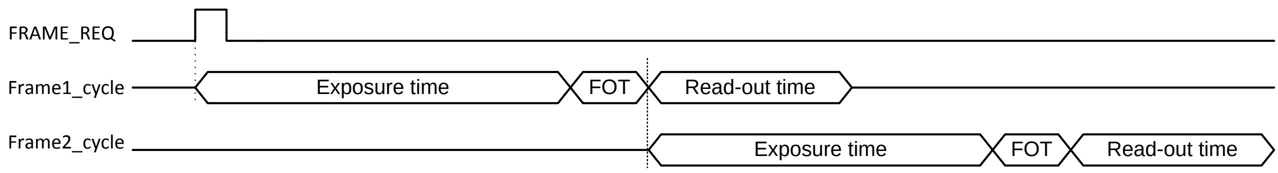


FIGURE 10: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

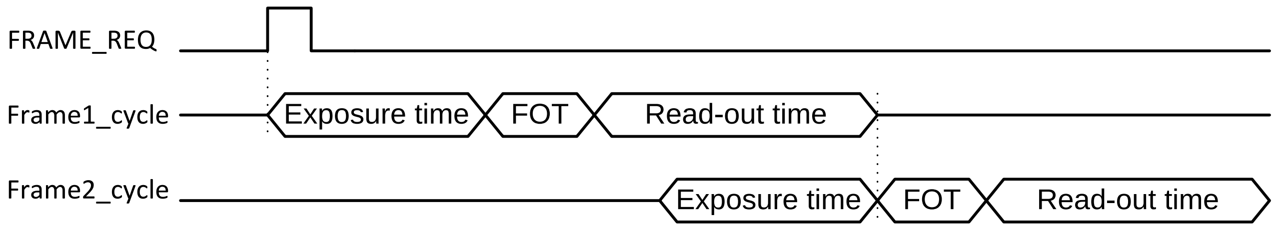


FIGURE 11: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE WITH EXPOSURE TIME < READ-OUT TIME

When you request a second frame during the read-out of the current frame, the current read-out will always be finished before the FOT of the new requested frame starts. When the new Frame_REQ pulse is too early, it will be delayed internally so that the FOT starts immediately after the readout.

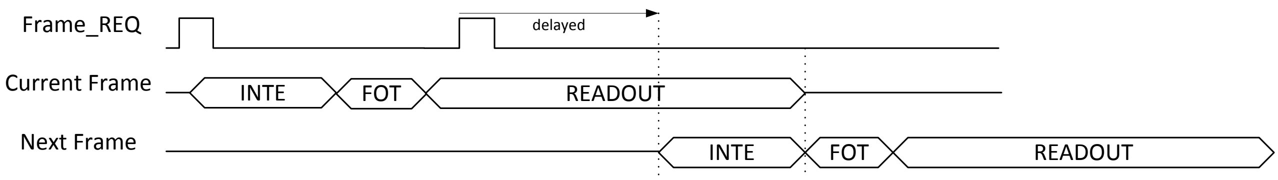


FIGURE 12: DELAY OF FRAME REQUEST

If a 2nd frame request is given during the integration of the current frame, the sensor will remember this and delay the request as described above. This only works for 2 Frame_req pulses during integration.

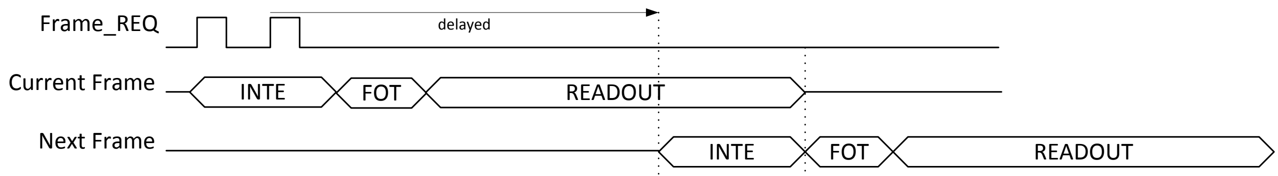


FIGURE 13: 2 FRAME REQUESTS DURING INTEGRATION

When keeping the Frame_REQ pin continuously high, the sensor will continuously read out frames at the maximum achievable frame rate.

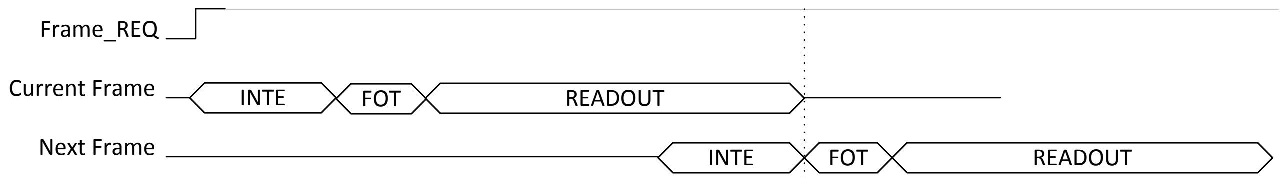


FIGURE 14: CONTINUOUS FRAME_REQ

3.10.2 External exposure control

The exposure time can also be programmed externally by using the T_EXP1 (and T_EXP2) input pin. This mode needs to be enabled by setting the appropriate register (address 70[0]). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high value is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

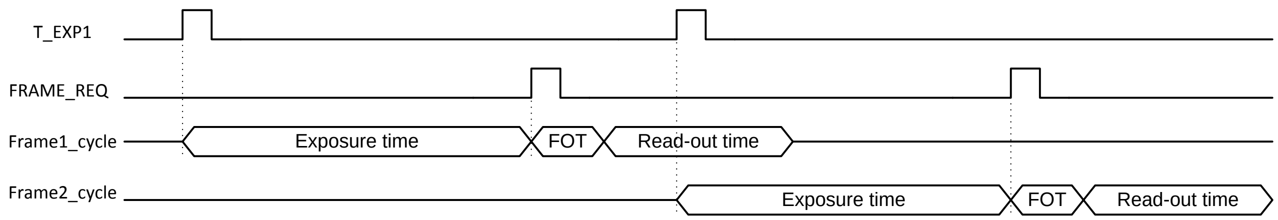


FIGURE 15: REQUEST FOR 2 FRAMES USING EXTERNAL-EXPOSURE-TIME MODE

When the exposures stops too soon (by giving a Frame_REQ pulse during read-out), the current read-out will be finished normally and the exposure time will be extended so that the FOT starts immediately after the read-out.

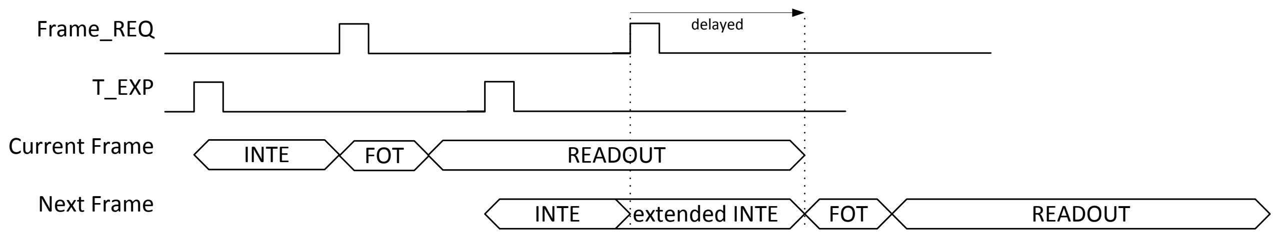


FIGURE 16: EXTENDED INTEGRATION TIME IN EXTERNAL MODE

4 READING OUT THE SENSOR

4.1 LVDS DATA OUTPUTS

The CMV12000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 64 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 66 LVDS output pairs (2 pins for each LVDS channel):

- 64 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 132 pins of the CMV12000 are used for the LVDS outputs (128 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 64 data channels are used to transfer the 12-bit, 10-bit or 8-bit pixel data from the sensor to the receiver in the surrounding system. The 32 bottom channels use pins OUT1_N/P to OUT32_N/P and the top channels use pins OUT33_P/N to OUT64_P/N.

The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 300Mbps output data rate is used, the LVDS output clock will be 150 MHz (half of input clock).

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 8-bit, 10-bit or 12-bit words that are transferred synchronous to the 64 data channels.

4.2 LOW-LEVEL READ OUT TIMING

The figures below show the timing for transfer of 8-bit, 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

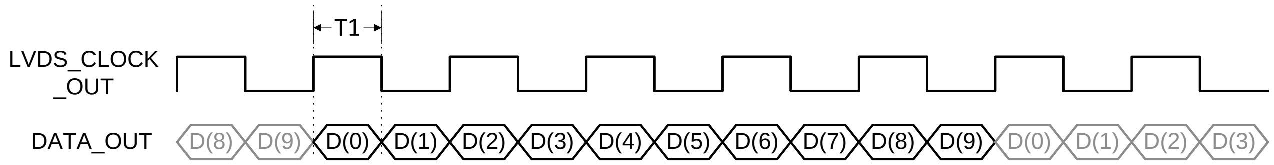


FIGURE 17: 10-BIT PIXEL DATA ON AN LVDS CHANNEL

The time ‘T1’ in the diagram above is equal to the period of the input clock (LVDS_CLK_P/N) of the CMV12000.

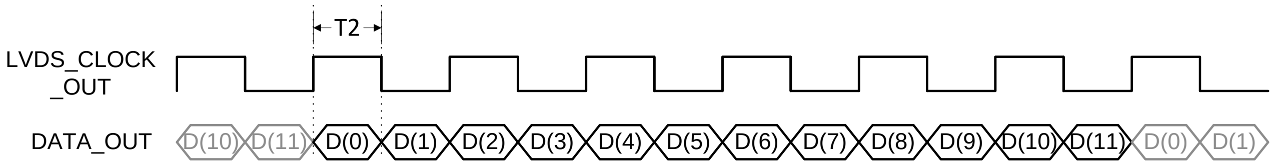


FIGURE 18: 12-BIT PIXEL DATA ON AN LVDS CHANNEL

The time ‘T2’ in Figure 18 is equal to the period of the input clock (LVDS_CLK_P/N) of the CMV12000.

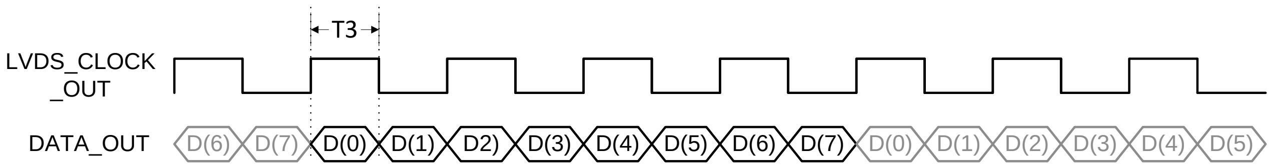


FIGURE 19: 8-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T3' in Figure 19 is equal to the period of the input clock (LVDS_CLK_P/N) of the CMV12000.

4.3 PIXEL READ-OUT

The read-out of image data is grouped in bursts of 128 pixels per channel (2 rows at the same time via top and bottom outputs). Each pixel is 8, 10 or 12 bits of data (see section 4.2). For details on pixel remapping and pixel vs. channel location please see section 4.4 of this document. An overhead time exists between two bursts of 128 pixels. This overhead time has the length of one pixel read-out (i.e. the length of 8, 10 or 12 bits at the selected data rate).

Please note that depending on the bit mode (8-bit, 10-bit or 12-bit) and read-out mode (subsampling, binning…), the actual timing of the image data may differ from one mode to another. The sections below show the relative location of the pixel data only.

The sensor is designed to be used with both sides (bottom and top) simultaneously. There is a "one side mode" where only one side (bottom) can be used to read out data, but binning and subsampling in X and Y direction are not supported in this mode.

4.3.1 64 OUTPUT CHANNELS

By default, all 64 data output channels are used to transmit the image data. This means that two entire rows of image data are transferred (one using the top outputs and one using the bottom outputs) in one slot of 128 pixel periods (64 x 128 = 8192). Next figure shows the timing for the top and bottom LVDS channels.

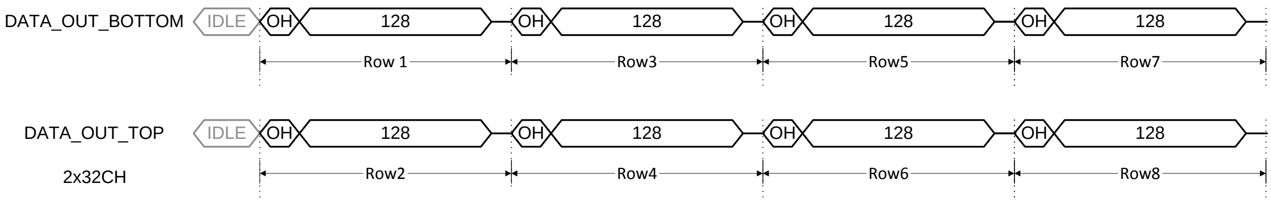


FIGURE 20: OUTPUT TIMING IN DEFAULT 64 CHANNEL MODE

Only when 64 data outputs, running at 300 Mbps and, are used, the frame rate of 150 fps can be achieved in 10 bit (default).

4.3.2 32 OUTPUT CHANNELS

The CMV12000 has possibility to use less than 64 outputs. Also if using 32 or less outputs you can use two sided read-out (using top and bottom outputs) or one sided read-out (using only bottom outputs). In this multiplexed mode the frame rate will be reduced by a factor of 2 compared to the 64 channel output.

4.3.2.1 TWO SIDED READ-OUT

This setting can be programmed with register 81 (see section 5.9). Now you will have 16 channels at each side. In this multiplexed mode the read-out of one row takes 2*128 periods but two rows will be sent out at the same time. Next figure shows the timing, the odd rows are read out by the bottom outputs, the even rows by the top outputs.

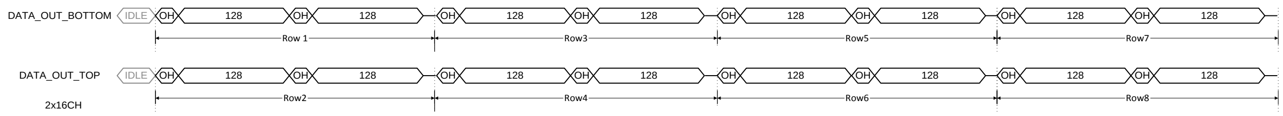


FIGURE 21: OUTPUT TIMING IN TWO SIDED 32 CHANNEL MODE

4.3.2.2 ONE SIDED READ-OUT

This setting can be programmed with register 81 and 66 (see section 5.9). Now you will have 32 channels at the bottom side. In this multiplexed mode the read-out of one row takes 1*128 periods. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … Next figure shows the timing for the bottom LVDS channels.

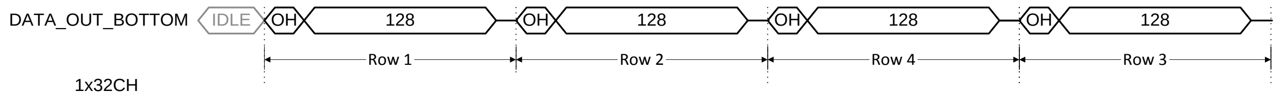


FIGURE 22: OUTPUT TIMING IN ONE SIDED 32 CHANNEL MODE

4.3.3 16 OUTPUT CHANNELS

In this multiplexed mode the frame rate will be reduced by a factor of 4 compared to the 64 channel output.

4.3.3.1 TWO SIDED READ-OUT

This setting can be programmed with register 81 (see section 5.9). Now you will have 8 channels at each side. In this multiplexed mode the read-out of one row takes 4*128 periods but two rows will be sent out at the same time. Next figure shows the timing.

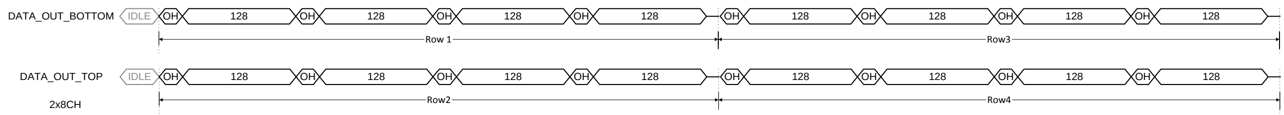


FIGURE 23: OUTPUT TIMING IN TWO SIDED 16 CHANNEL MODE

4.3.3.2 ONE SIDED READ-OUT

This setting can be programmed in the register with address 81 and 66 (see section 5.9). In such multiplexed output mode, only 16 of the bottom 32 LVDS channels are used and the read-out of one row takes 2*128 periods. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … Next figure shows the timing for the bottom LVDS channels.

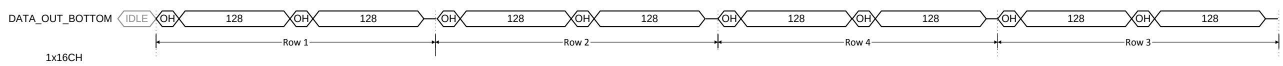


FIGURE 24: OUTPUT TIMING IN ONE SIDED 16 CHANNEL MODE

4.3.4 8 OUTPUT CHANNELS

In this 8 channel mode, the frame rate is reduced with a factor of 8 compared to 64 channel mode.

4.3.4.1 TWO SIDED READ-OUT

This setting can be programmed in the register with address 81 (see section 5.9). In such multiplexed output mode, 4 outputs of each side are used and the read-out of one row takes 8*128 periods but two rows will be sent out at the same time. The timing follows the pattern of the other multiplex modes.

4.3.4.2 ONE SIDED READ-OUT

This setting can be programmed in the register with address 81 and 66 (see section 5.9). In such multiplexed output mode, only 8 of the bottom 32 LVDS channels are used and the read-out of one row takes 4*128 periods. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … Next figure shows the timing for the bottom LVDS channels.

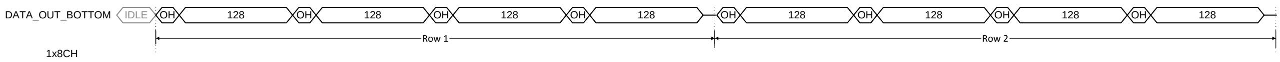


FIGURE 25: OUTPUT TIMING IN ONE SIDED 8 CHANNEL MODE

4.3.5 4 OUTPUT CHANNELS

The CMV12000 has also the possibility to use only 4 LVDS output channels.

4.3.5.1 TWO SIDED READ-OUT

This setting can be programmed in the register with address 81 (see section 5.9). In such multiplexed output mode, 2 outputs of each side are used and the read-out of one row takes 16*128 periods but two rows will be sent out at the same time. In this 4 channel mode, the frame rate is reduced with a factor of 16 compared to 64 channel mode. The timing follows the pattern of the other multiplex modes.

4.3.5.2 ONE SIDED READ-OUT

This setting can be programmed in the register with address 81 and 66 (see section 5.9). In such multiplexed output mode, only 4 of the bottom 32 LVDS channels are used and the read-out of one row takes 8*128 periods. In this 4 channel mode, the frame rate is reduced with a factor of 16 compared to 64 channel mode. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … The timing follows the pattern of the other multiplex modes.

4.3.6 2 OUTPUT CHANNELS

The CMV12000 has also the possibility to use only 2 LVDS output channels.

4.3.6.1 TWO SIDED READ-OUT

This setting can be programmed in the register with address 81 (see section 5.9). In such multiplexed output mode, 2 outputs of each side are used and the read-out of one row takes 32*128 periods but two rows will be sent out at the same time. In this 2 channel mode, the frame rate is reduced with a factor of 32 compared to 64 channel mode. The timing follows the pattern of the other multiplex modes.

4.3.6.2 ONE SIDED READ-OUT

This setting can be programmed in the register with address 81 and 66 (see section 5.9). In such multiplexed output mode, only 2 of the bottom 32 LVDS channels are used and the read-out of one row takes 16*128 periods. In this 2 channel mode, the frame rate is reduced with a factor of 32 compared to 64 channel mode. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … The timing follows the pattern of the other multiplex modes.

4.3.7 1 OUTPUT CHANNEL

The CMV12000 has also the possibility to use only 1 LVDS output channel.

4.3.7.1 ONE SIDED READ-OUT

This setting can be programmed in the register with address 81 and 66 (see section 5.9). In such multiplexed output mode, only 1 of the bottom 32 LVDS channels is used and the read-out of one row takes 32*128 periods. In this 1 channel mode, the frame rate is reduced with a factor of 64 compared to 64 channel mode. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … The timing follows the pattern of the other multiplex modes.

4.4 PIXEL REMAPPING

Depending on the number of output channels, the pixels are located at different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixels on the outputs to their correct image array location.

4.4.1 64 OUTPUTS

The figure below shows the location of the image pixels versus the output channel of the image sensor.

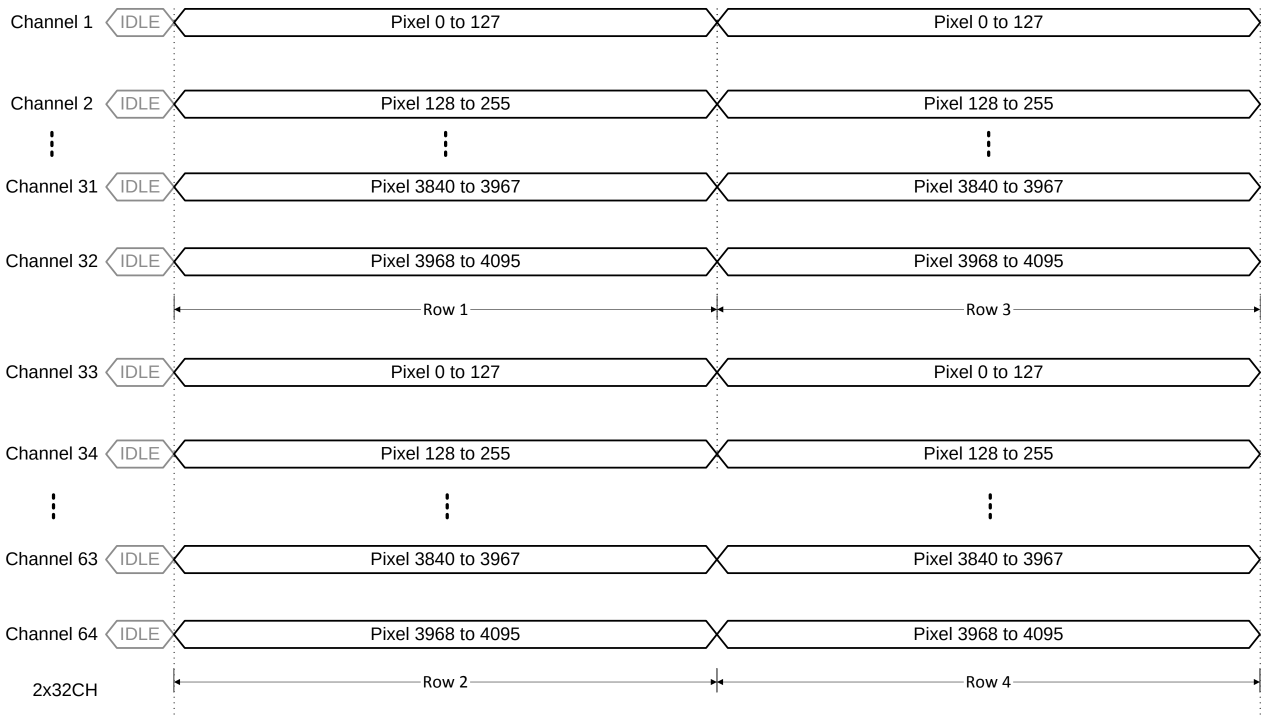


FIGURE 26: PIXEL REMAPPING FOR 64 OUTPUT CHANNELS

64 bursts (2 x 32) of 128 pixels happen in parallel on the data outputs. This means that two complete rows are read out in one burst; the odd rows via the bottom channels, the even rows via the top channels. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.2 32 OUTPUTS

4.4.2.1 ONE SIDED READ-OUT

When 32 outputs of one side are used, the pixel data is placed on the outputs as detailed in the figure below. 32 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The rows will be read out following the pattern: row 1, row 2, row 4, row 3, row 5, row 6, row 8, row 7 … So every 3th and 4th row are switched.

The time needed to read out two rows is doubled compared to when 64 outputs are used. The top LVDS channels are not being used in this mode, so they can be turned off by setting the correct bits in the register with addresses 92-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

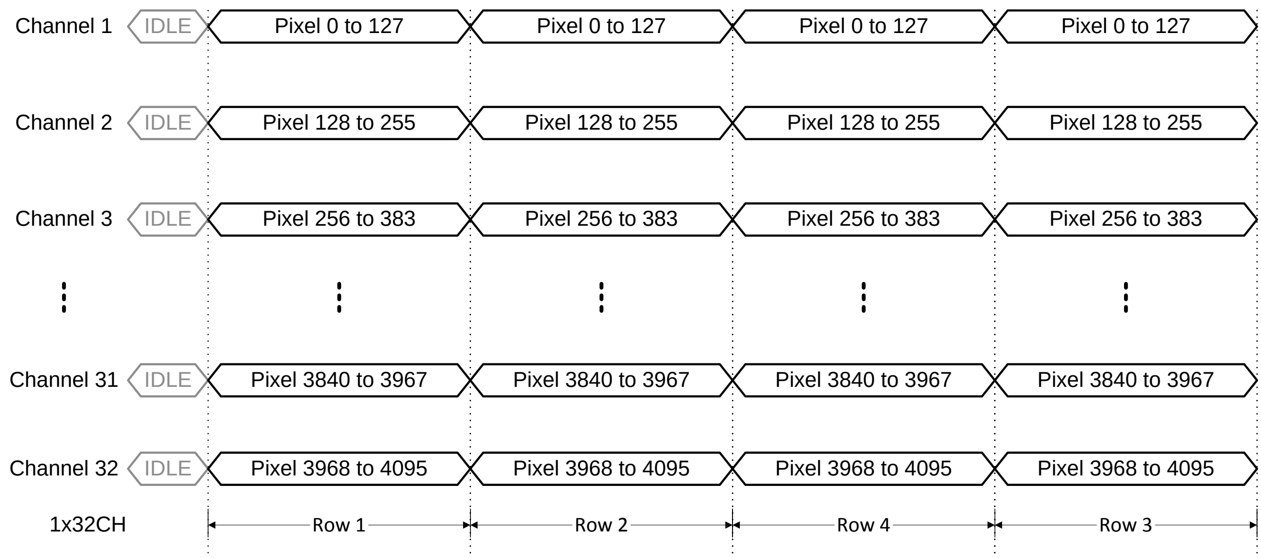


FIGURE 27: PIXEL REMAPPING FOR ONE SIDED 32 OUTPUT CHANNELS

4.4.2.2 TWO SIDED READ-OUT

When two sided 32 output mode is used, the pixel data is placed on the outputs as detailed in the figure below. 16 bursts of 128 pixels happen in parallel on the data outputs on both sides simultaneous (16 on the top and 16 on the bottom outputs); the odd rows via the bottom channels, the even rows via the top channels. This means that one complete row one each side is read out in two burst (so effectively two rows are read-out in two bursts).

The time needed to read out two rows is doubled compared to when 64 outputs are used. The even LVDS channels are not being used in this mode, so they can be turned off by setting the correct bits in the register with addresses 92-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

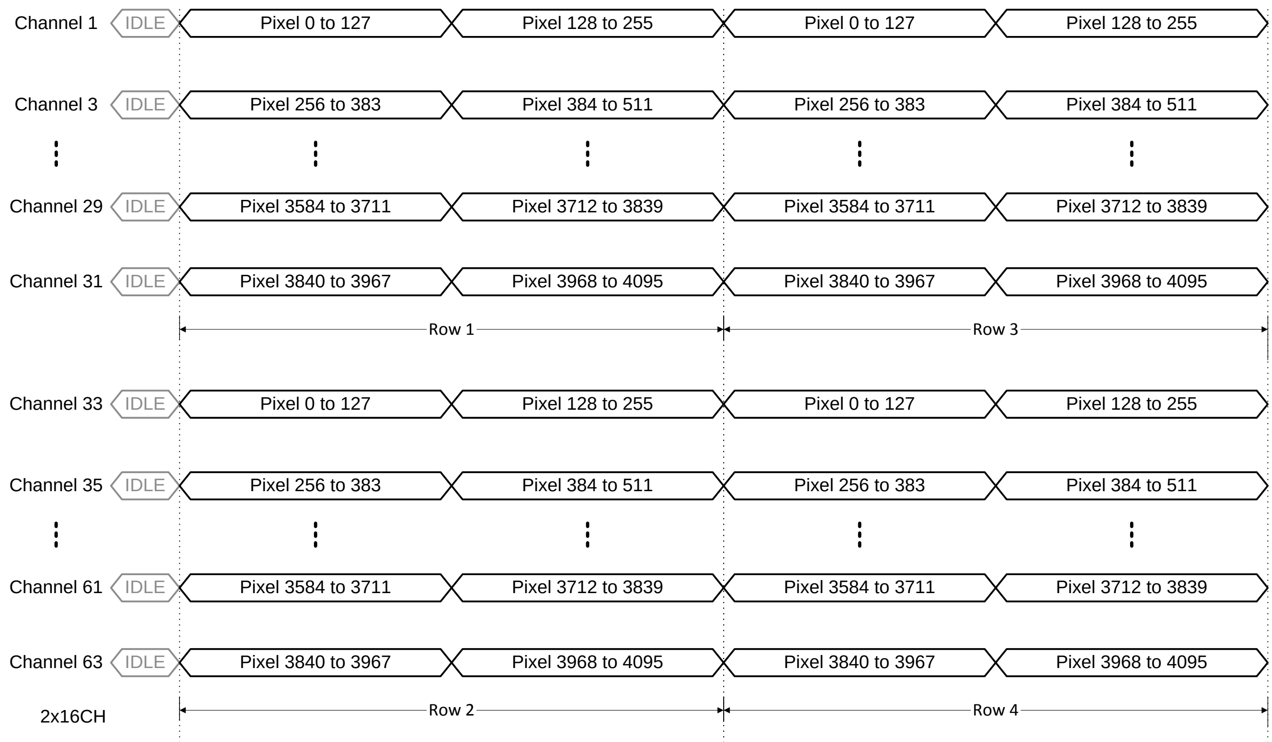


FIGURE 28: PIXEL REMAPPING FOR TWO SIDED 32 CHANNELS

4.4.3 16 OUTPUTS

4.4.3.1 ONE SIDED READ-OUT

When only 16 outputs on one side are used, the pixel data is placed on the outputs as detailed in the figure below. 16 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in two bursts. The rows will be read out following the pattern: row 1, row 2, row 4, row 3, row 5, row 6, row 8, row 7 … So every 3th and 4th row are switched.

The time needed to read out one row is 2x longer compared to when 32 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining even 16 bottom channels can be turned off by setting the correct bits in the registers with addresses 90-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

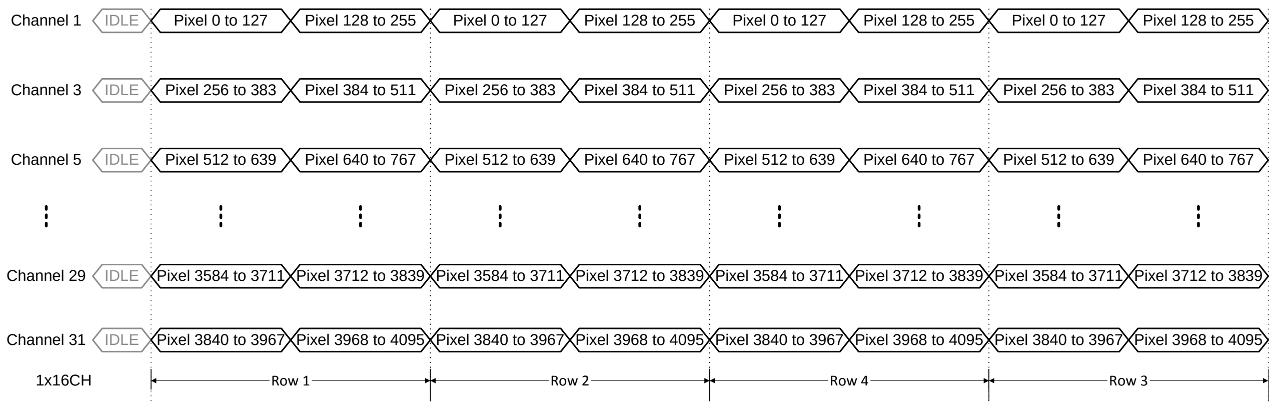


FIGURE 29: PIXEL REMAPPING FOR ONE SIDED 16 OUTPUT CHANNELS

4.4.3.2 TWO SIDED READ-OUT

When two sided 16 output mode is used, the pixel data is placed on the outputs as detailed in the figure below. 8 bursts of 128 pixels happen in parallel on the data outputs on both sides simultaneous (8 on the top and 8 on the bottom outputs); the odd rows via the bottom channels, the even rows via the top channels. This means that one complete row one each side is read out in 4 burst (so effectively two rows are read-out in 4 bursts).

The time needed to read out two rows is doubled compared to when 32 outputs are used. The LVDS channels not used can be turned off by setting the correct bits in the register with addresses 92-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

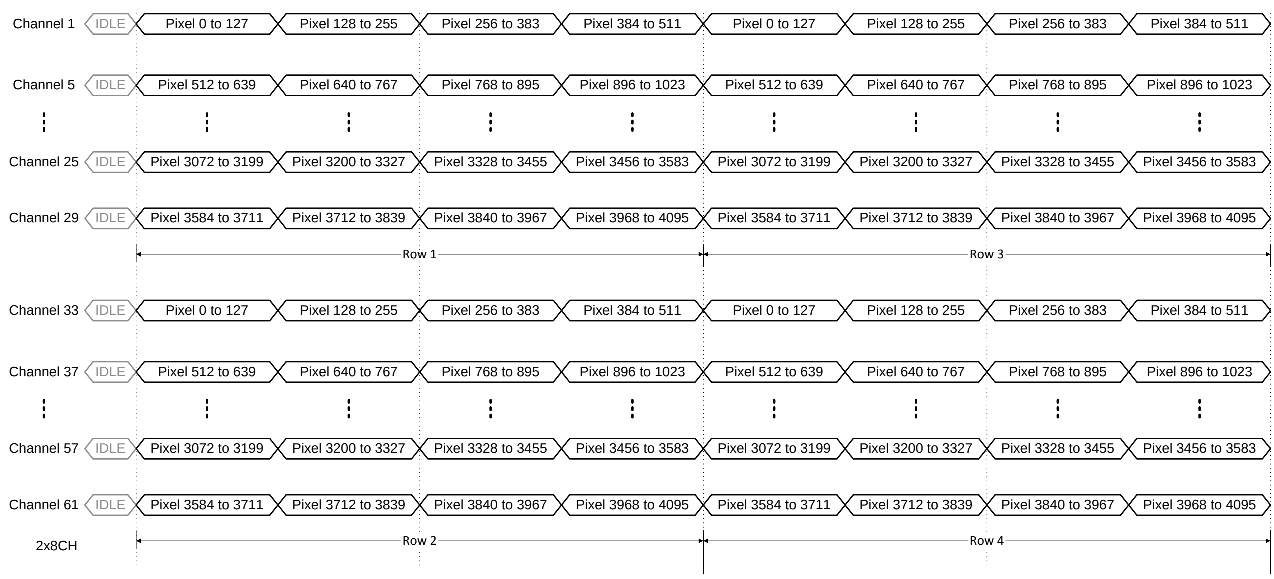


FIGURE 30: PIXEL REMAPPING FOR TWO SIDED 16 OUTPUT CHANNELS

4.4.4 8 OUTPUTS

The remapping schemes follow the pattern used in the previous multiplexing modes.

4.4.4.1 ONE SIDED READ-OUT

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 8 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 4 bursts. The rows will be read out following the pattern: row 1, row 2, row 4, row 3, row 5, row 6, row 8, row 7 … So every 3th and 4^{th} row are switched.

The time needed to read out one row is 2x longer compared to when 16 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining 24 bottom channels can be turned off by setting the correct bits in the registers with addresses 90-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

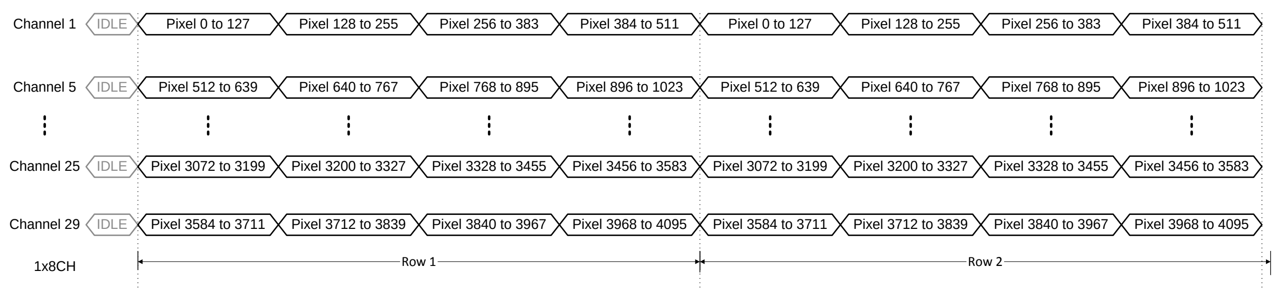


FIGURE 31: PIXEL REMAPPING FOR ONE SIDED 8 OUTPUT CHANNELS

4.4.4.2 TWO SIDED READ-OUT

When two sided 8 output mode is used, 4 bursts of 128 pixels happen in parallel on the data outputs on both sides simultaneous (4 on the top and 4 on the bottom outputs); the odd rows via the bottom channels, the even rows via the top channels. This means that one complete row one each side is read out in 8 bursts (so effectively two rows are read-out in 8 bursts)

The time needed to read out two rows is doubled compared to when 16 outputs are used. The LVDS channels not used can be turned off by setting the correct bits in the register with addresses 92-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.5 4 OUTPUTS

The remapping schemes follow the pattern used in the previous multiplexing modes.

4.4.5.1 ONE SIDED READ-OUT

When only 4 outputs are used, 4 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 8 bursts. The rows will be read out following the pattern: row 1, row 2, row 4, row 3, row 5, row 6, row 8, row 7 … So every 3th and 4th row are switched.

The time needed to read out one row is 8x longer compared to when 32 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining 28 bottom channels can be turned off by setting the correct bits in the registers with addresses 90-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.5.2 TWO SIDED READ-OUT

When two sided 4 output mode is used, 2 bursts of 128 pixels happen in parallel on the data outputs on both sides simultaneous (2 on the top and 2 on the bottom outputs); the odd rows via the bottom channels, the even rows via the top channels.. This means that one complete row one each side is read out in 16 burst (so effectively two rows are read-out in 16 bursts).

The time needed to read out two rows is doubled compared to when 8 outputs are used. The LVDS channels not used can be turned off by setting the correct bits in the register with addresses 92-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.6 2 OUTPUTS

The remapping schemes follow the pattern used in the previous multiplexing modes.

4.4.6.1 ONE SIDED MODE

When only 2 outputs are used, 2 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 16 bursts. The rows will be read out following the pattern: row 1, row 2, row 4, row 3, row 5, row 6, row 8, row 7 … So every 3th and 4th row are switched.

The time needed to read out one row is 16x longer compared to when 32 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining 30 bottom channels can be turned off by setting the correct bits in the registers with addresses 90-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.6.2 TWO SIDED READ-OUT

When two sided 2 output mode is used, 1 burst of 128 pixels happen in parallel on the data outputs on both sides simultaneous (1 on the top and 1 on the bottom outputs); the odd rows via the bottom channels, the even rows via the top channels.. This means that one complete row one each side is read out in 32 burst (so effectively two rows are read-out in 32 bursts).

The time needed to read out two rows is doubled compared to when 4 outputs are used. The LVDS channels not used can be turned off by setting the correct bits in the register with addresses 92-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.7 1 OUTPUT

The remapping scheme follows the pattern used in the previous multiplexing modes.

4.4.7.1 ONE SIDED READ-OUT

When only 1 output is used, 1 burst of 128 pixels happens on the data outputs. This means that one complete row is read out in 32 bursts. The rows will be read out following the pattern: row 1, row 2, row 4, row 3, row 5, row 6, row 8, row 7 … So every 3th and 4th row are switched.

The time needed to read out one row is 32x longer compared to when 32 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining 31 bottom channels can be turned off by setting the correct bits in the registers with addresses 90-93. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3072 rows being read out.

4.4.8 OVERVIEW

Below you can find an overview of which outputs are used when multiplexing to 32, 16, 8 … channels per side.

	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	OUT 6	OUT 7	OUT 8	OUT 9	OUT 10	OUT 11	OUT 12	OUT 13	OUT 14	OUT 15	OUT 16	OUT 17	OUT 18	OUT 19	OUT 20	OUT 21	OUT 22	OUT 23	OUT 24	OUT 25	OUT 26	OUT 27	OUT 28	OUT 29	OUT 30	OUT 31	OUT 32
32	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
16	x		x		x		x		x		x		x		x		x		x		x		x		x		x		x		x	
8	x				x				x				x				x				x				x				x			
4	x								x								x								x							
2	x																x															
1	x																															

	OUT 33	OUT 34	OUT 35	OUT 36	OUT 37	OUT 38	OUT 39	OUT 40	OUT 41	OUT 42	OUT 43	OUT 44	OUT 45	OUT 46	OUT 47	OUT 48	OUT 49	OUT 50	OUT 51	OUT 52	OUT 53	OUT 54	OUT 55	OUT 56	OUT 57	OUT 58	OUT 59	OUT 60	OUT 61	OUT 62	OUT 63	OUT 64
32	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
16	x		x		x		x		x		x		x		x		x		x		x		x		x		x		x		x	
8	x				x				x				x				x				x				x				x			
4	x								x								x								x							
2	x																x															
1	x																															

4.5 CONTROL CHANNEL

The CMV12000 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 8-bit, 10-bit or 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates the validity of the read-out of a row
[2]	FVAL	Indicates the validity of the read-out of a frame
[3]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[4]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[5]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[6]	‘0’	Constant zero
[7]	‘1’	Constant one
[8]	‘0’	Constant zero
[9]	‘0’	Constant zero
[10]	‘0’	Constant zero
[11]	‘0’	Constant zero

(*)Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

The bits of the control channel can be put on the Tdig1/2 pins (G26/G27) to easily see the state of the sensor. Use register 123[7:0] to program the Tdig pins output functionality:

Reg123[3:0]	Tdig1
0	LVAL
2	FOT
3	INTE_2
Reg123[7:4]	**Tdig2**
0	DVAL
3	INTE_1
15	FVAL

4.5.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the read-out status. The next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the read-out of a frame of 4 rows (default is 3072 rows). This example uses the default mode of 64 outputs (identical for one-side 32 outputs).

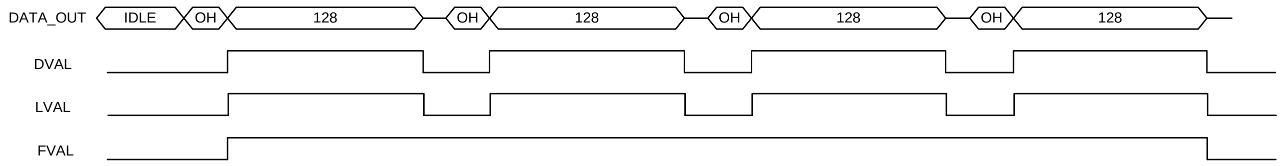


FIGURE 32: DVAL, LVAL AND FVAL TIMING IN 64CH OR 1X32CH OUTPUT MODE

When only 16 outputs are used per side, the line read-out time is 2x longer. The control channel takes this into account and the timing in this mode looks like the diagram below. The timing extrapolates identically for 8, 4 2 and 1 output(s). Below is an example of a frame of 2 rows when only using 16 channels per side.

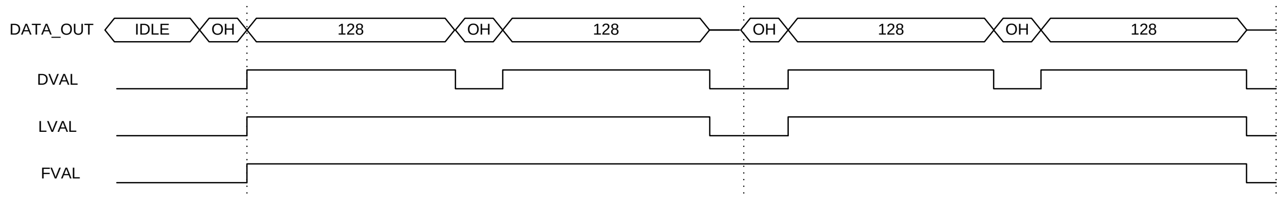


FIGURE 33: DVAL, LVAL AND FVAL TIMING WHEN USING 16CH PER SIDE

4.6 TRAINING DATA

To synchronize the receiving side with the LVDS outputs of the CMV12000, a known data pattern can be put on the output channels. This pattern can be used to "train" the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. Such a training pattern is put on all 64 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 128 pixels). The training pattern is an 8-bit, 10-bit or 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 89) that can be loaded via SPI to change the contents of the 12-bit training pattern TP1 for training during idle mode. TP2 equals TP1 with the 8 LSBs inverted and the 4 MSBs set to '0' and can be used for word alignment during overhead time (OH). TP2 will be put on the data channels for 1 (lvds_per/bitmode) clock period and only before every LVAL. When there is more than 1 clock cycle of idle time between two LVAL's TP1 will be set on the outputs for the remaining time. When DVAL is low but LVAL is high, only TP1 will be set on the data outputs.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [7] (TPC).

The figure below shows the location of the training pattern on the data channels and control channel when the sensor is in idle mode and when a frame of 2 rows is read out. The mode of 16 outputs is selected.

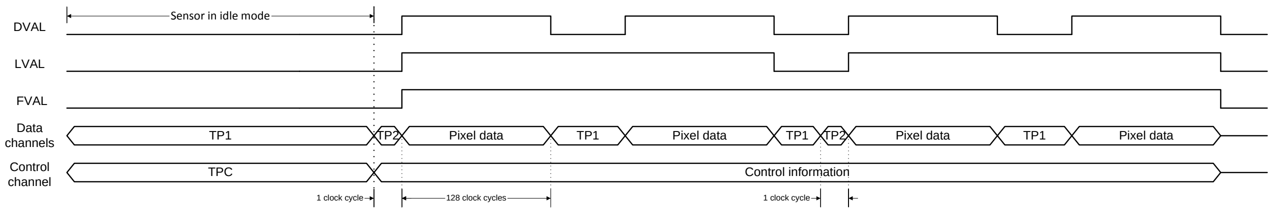


FIGURE 34: TRAINING PATTERN LOCATION IN THE DATA CHANNELS AND CONTROL CHANNEL

The typical output skew of the CMV12000 can be seen in Figure 35. Per channel per side there is about a 150ps skew, which leads to a total skew of 4800ps between the first and lasts channels. TP1 and TP2 can be used to correct for this during operation. The skew is independent of the clock speed, but shifts with temperature. Therefor realignment is needed when (large) temperature changes occur. The skew can differ a bit between devices.

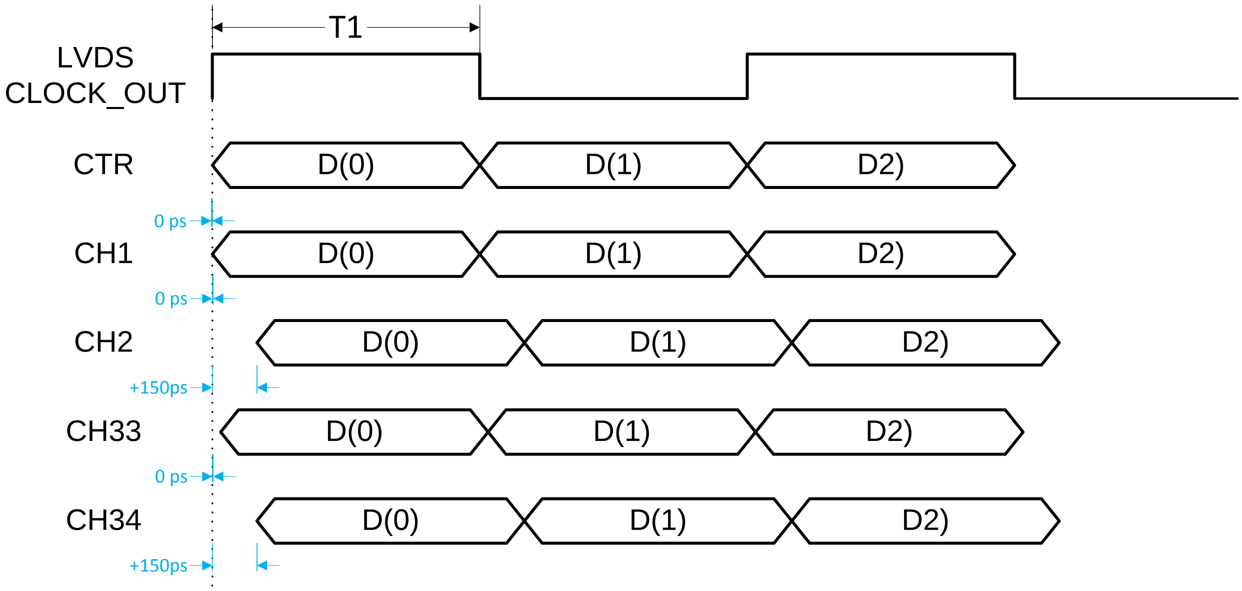


FIGURE 35: TYPICAL LVDS OUTPUT SKEW

5 IMAGE SENSOR PROGRAMMING

This section explains how the CMV12000 can be programmed using the on-board sequencer registers.

5.1 EXPOSURE MODES

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see section 3.10.2 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

The table below gives an overview of the registers involved in the exposure mode.

Exposure time settings			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_ext	70[0]	0	0: Exposure time is defined by the value uploaded in the sequencer register (71-72) 1: Exposure time is defined by the pulses applied to the T_EXP1 and FRAME_REQ pins
Exp_time	71-72[7:0]	1536	When the Exp_ext register is set to '0', the value in this register defines the exposure time according to the formula in section 5.2

5.2 EXPOSURE TIME CALCULATION

The formula to calculate the actual exposure time in internal-exposure mode from the programmed registers is given by the following formula:

$$Exposure\ time = \big((Exp\_time - 1) * (reg85 + 1) + 1 + (34 * reg82[7:0])\big) * LVDS\_CLK\_P/N\_period * \#bits$$

The minimal exposures when running at 300MHz in internal mode will be:

Bit mode	Min. Exposure Time
8b	27.23µs
10b	34.03µs
12b	40.84µs

When using external exposure mode, the actual exposure time will be given by:

$$Exposure\ time = \text{"time between T\_EXP and Frame\_REQ"} + (34 * reg82[7:0]) * LVDS\_CLK\_P/N\_period * \#bits)$$

The time between the T_EXP and Frame_REQ pulses will be clocked to a multiple of (LVDS_CLK_P/N_period * #bits).

For both modes there is an overlap of the exposure during the FOT (the "34 * reg82[7:0]" part).

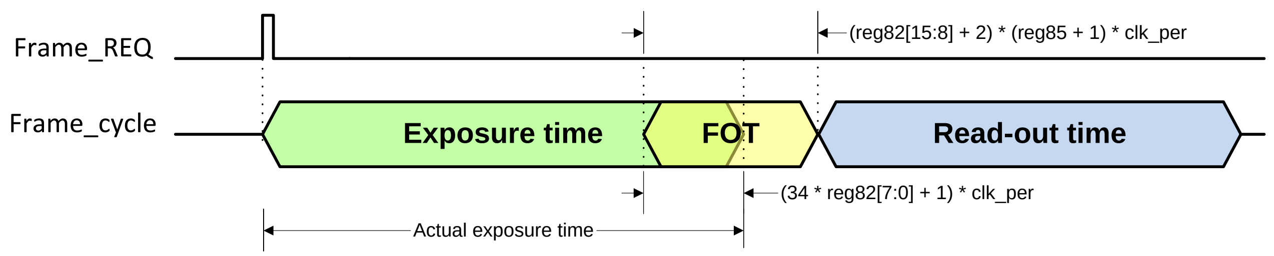


FIGURE 36: EXPOSURE OVERLAP DURING FOT

5.3 HIGH DYNAMIC RANGE MODES

The sensor has different ways to achieve high optical dynamic range in the grabbed image.

- Interleaved read-out: the odd and even columns have a different exposure time
- Multiple slope: partial reset of the photodiode, within an exposure time, to reset the saturated pixels

All the HDR modes mentioned above can be used in both the internal- and external-exposure-time mode.

5.3.1 INTERLEAVED READ-OUT

In this HDR mode, the odd and even columns of the image sensor will have a different exposure time. This mode can be enabled by setting the register in the table below.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_dual	70[1]	0	0: interleaved exposure mode disabled 1: interleaved exposure mode enabled

The surrounding system can combine the image of the odd columns with the image of the even columns which can result in a high dynamic range image. In such an image very bright and very dark objects are made visible without clipping. The table below gives an overview of the registers involved in the interleaved read-out when the internal exposure mode is selected.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	71-72[7:0]	1536	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the even columns according to the formula in section 5.2
Exp_time2	73-74[7:0]	1536	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the odd columns according to the formula in section 5.2

When the external exposure mode and interleaved read-out are selected, the different exposure times are achieved by using the T_EXP1 and T_EXP2 input pins. T_EXP1 defines the exposure time for the even columns, while T_EXP2 defines the exposure time for the odd columns. See the figure below for more details.

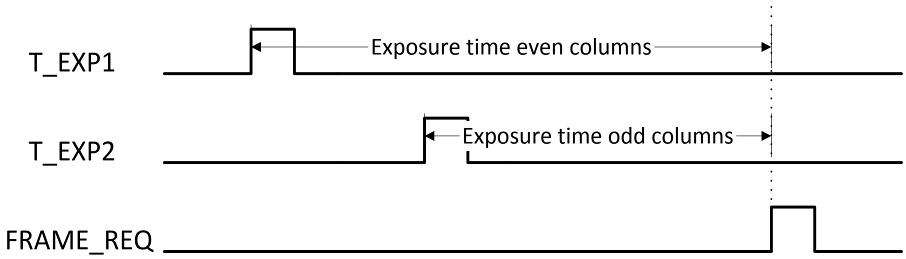


FIGURE 37: INTERLEAVED READ-OUT IN EXTERNAL EXPOSURE MODE

When a color sensor is used, the sequencer should be programmed to make sure it takes the Bayer pattern into account when doing interleaved read-out. This can be done by setting the appropriate registers to '0'.

Color/mono			
Register name	**Register address**	**Default value**	**Description of the value**
Color	68[0]	1	0: color sensor is used 1: monochrome sensor is used

Color/mono			
Register name	**Register address**	**Default value**	**Description of the value**
Color_exp	68[3]	1	0: color sensor is used 1: monochrome sensor is used

5.3.2 MULTIPLE SLOPE

The CMV12000 has the possibility to achieve a high optical dynamic range by using a multiple slope feature. This feature will partially reset those pixels which reach a programmable voltage, while leaving the other pixels untouched. This can be done 2 times within one exposure time to achieve a maximum of 3 exposure slopes. More details can be found in the figure below.

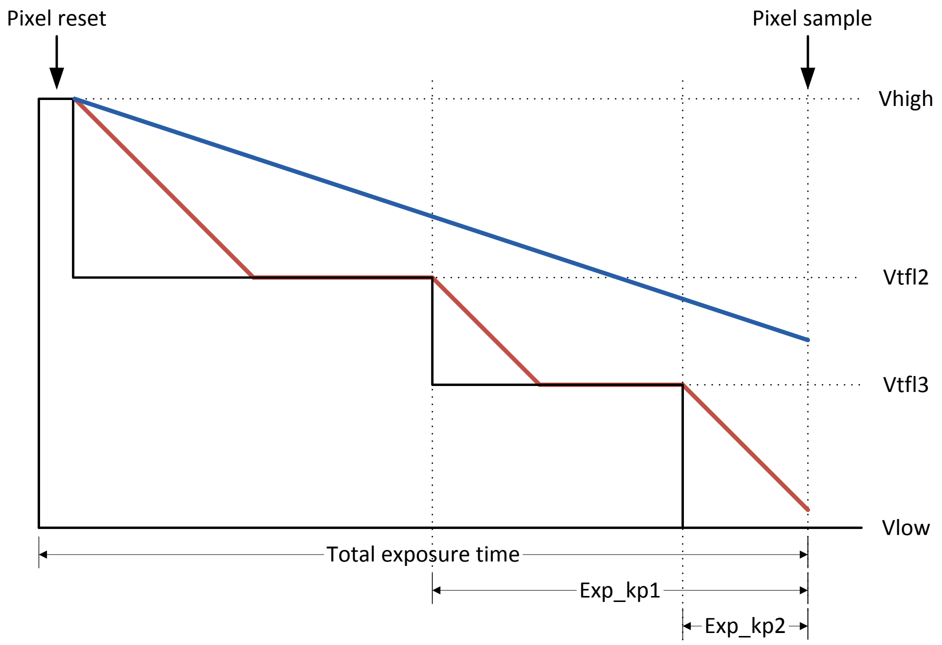


FIGURE 38: MULTIPLE SLOPE DETAILS

In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced by this multiple slope and will have a normal response. The Vtfl voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in the figure below can be achieved. The placement of the kneepoints in X is controlled by the Vtfl programming (64 = Vlow; 127 = Vhigh), while the slope of the segments is controlled by the programmed exposure times.

A good starting point is to set Exp_kp1 to 1% of the total exposure time and Exp_kp2 to 10% and setting Vtfl2 to 84 and Vtfl3 to 104.

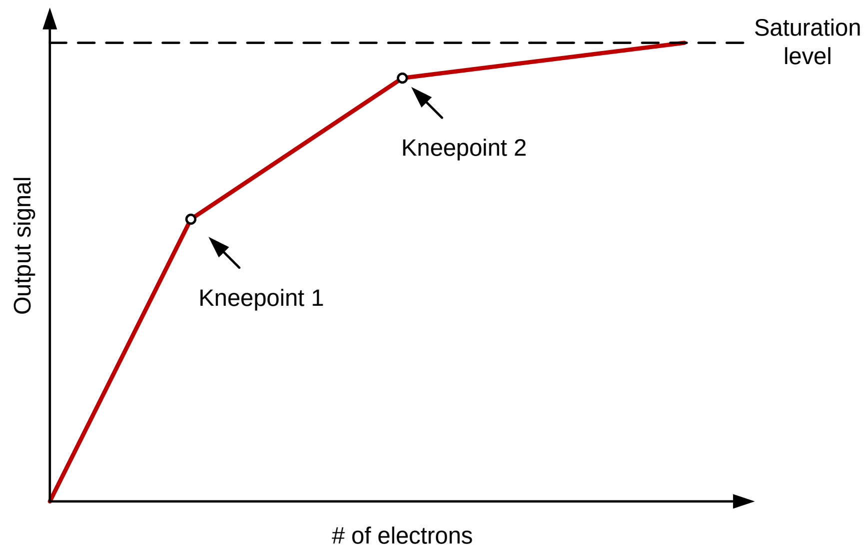


FIGURE 39: MULTIPLE SLOPE RESPONSE

5.3.2.1 Multiple slope with internal exposure mode

The following registers need to be programmed when multiple slopes in internal exposure mode are desired.

HDR settings – multiple slope			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	71-72[7:0]	1536	The value in this register defines the total exposure time according to the formula in section 5.2
Number_slopes	79[1:0]	1	The value in this register defines the number of slopes (min=1, max=3)
Exp_kp1	75-76[7:0]	0	The value in this register defines the exposure time from kneepoint 1 to the end of total exposure time. See the formula in section 5.2
Exp_kp2	77-78[7:0]	0	The value in this register defines the exposure time from kneepoint 2 to the end of total exposure time. See the formula in section 5.2
Vtfl2	106[6:0]	64	The value in this register defines the Vtfl2 voltage (DAC setting). Bit [6]: Enable/Disable Bits [5:0]: Vtfl2 voltage level
Vtfl3	106[13:7]	64	The value in this register defines the Vtfl3 voltage (DAC setting). Bit [13]: Enable/Disable Bits [12:7]: Vtfl3 voltage level

5.3.2.2 Multiple slope with external exposure mode

When external exposure is used and multiple slopes are desired, the following registers should be programmed.

HDR settings – multiple slope			
Register name	**Register address**	**Default value**	**Description of the value**
Number_slopes	79[1:0]	1	The value in this register defines the number of slopes (min=1, max=3)
Vtfl2	106[6:0]	64	The value in this register defines the Vtfl2 voltage (DAC setting). Bit [6]: Enable/Disable Bits [5:0]: Vtfl2 voltage level

HDR settings – multiple slope			
Register name	**Register address**	**Default value**	**Description of the value**
Vtfl3	106[13:7]	64	The value in this register defines the Vtfl3 voltage (DAC setting). Bit [13]: Enable/Disable Bits [12:7]: Vtfl3 voltage level

The timing that needs to be applied in this external exposure mode looks like the one below.

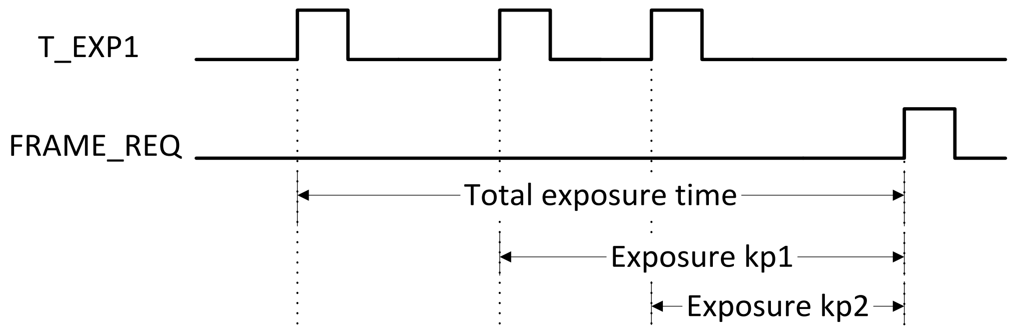


FIGURE 40: MULTIPLE SLOPE IN EXTERNAL EXPOSURE MODE

Please note, that a combination of the multiple slope and interleaved read-out is not supported.

5.4 Windowing

To limit the amount of data or to increase the frame rate of the sensor, windowing in Y direction is possible. The number of lines and start address can be set by programming the appropriate registers. The start address and the number of lines per window should be a multiple of 4. The CMV12000 has the possibility to read out multiple (max=32) predefined sub-windows in one read-out cycle. The default mode is to read out one window with the full frame size (4096x3072).

5.4.1 Single window

When a single window is read out, the start address and size can be uploaded in the corresponding registers. The default start address is 0 and the default size is 3072 (full frame).

Windowing – single window			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the number of lines read out by the sensor (min=1, max=3072)
Y_start_1	2	0	The value in this register defines the start address of the window in Y (min=0, max=3071)

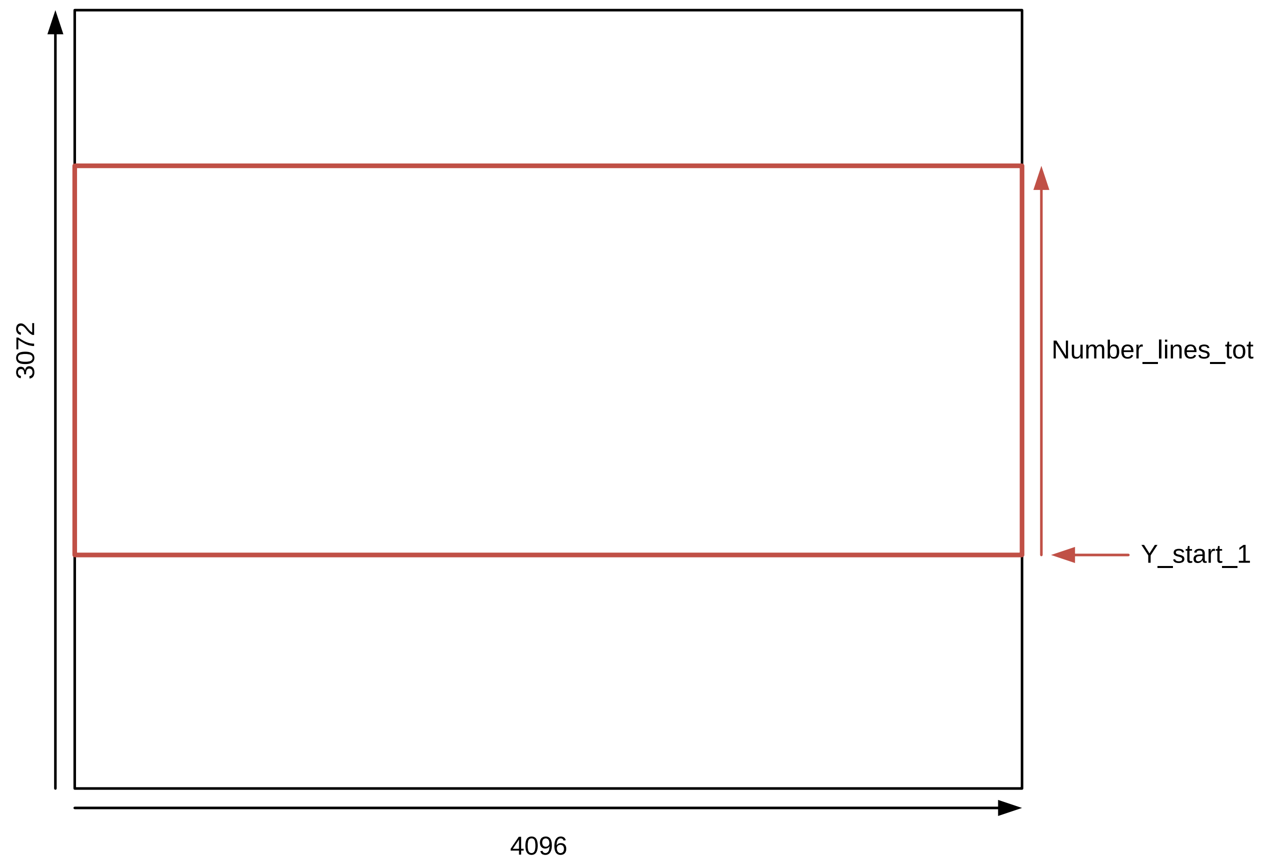


FIGURE 41: SINGLE WINDOW SETTINGS

5.4.2 MULTIPLE WINDOWS

The CMV12000 can read out a maximum of 32 different sub-windows in one read-out cycle. The location and length of these sub-windows must be programmed in the correct registers. The location of multiple windows can be random bu the windows should not overlap. The total number of lines to be read out (sum of all windows) needs to be specified in the Number_lines_tot register. The registers which need to be programmed for the multiple windows can be found in the table below.

Windowing – multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines read out by the sensor (min=1, max=3072)
Y_start_1	2	0	The value in this register defines the start address of the first window in Y (min=0, max=3071)
Y_size_1	34	0	The value in this register defines the number of lines of the first window (min=1, max=3072)
Y_start_2	3	0	The value in this register defines the start address of the second window in Y (min=0, max=3071)
Y_size_2	35	0	The value in this register defines the number of lines of the second window (min=1, max=3072)
Y_start_3	4	0	The value in this register defines the start address of the third window in Y (min=0, max=3071)
Y_size_3	36	0	The value in this register defines the number of lines of the third window (min=1, max=3072)
Y_start_4	5	0	The value in this register defines the start address of the fourth window in Y (min=0, max=3071)

Windowing – multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
Y_size_4	37	0	The value in this register defines the number of lines of the fourth window (min=1, max=3072)
Y_start_5	6	0	The value in this register defines the start address of the fifth window in Y (min=0, max=3071)
Y_size_5	38	0	The value in this register defines the number of lines of the fifth window (min=1, max=3072)
Y_start_6	7	0	The value in this register defines the start address of the sixth window in Y (min=0, max=3071)
Y_size_6	39	0	The value in this register defines the number of lines of the sixth window (min=1, max=3072)
Y_start_7	8	0	The value in this register defines the start address of the seventh window in Y (min=0, max=3071)
Y_size_7	40	0	The value in this register defines the number of lines of the seventh window (min=1, max=3072)
Y_start_8	9	0	The value in this register defines the start address of the eighth window in Y (min=0, max=3071)
Y_size_8	41	0	The value in this register defines the number of lines of the eighth window (min=1, max=3072)
Y_start_9	10	0	The value in this register defines the start address of the 9th window in Y (min=0, max=3071)
Y_size_9	42	0	The value in this register defines the number of lines of the 9th window (min=1, max=3072)
Y_start_10	11	0	The value in this register defines the start address of the 10th window in Y (min=0, max=3071)
Y_size_10	43	0	The value in this register defines the number of lines of the 10th window (min=1, max=3072)
Y_start_11	12	0	The value in this register defines the start address of the 11th window in Y (min=0, max=3071)
Y_size_11	44	0	The value in this register defines the number of lines of the 11th window (min=1, max=3072)
Y_start_12	13	0	The value in this register defines the start address of the 12th window in Y (min=0, max=3071)
Y_size_12	45	0	The value in this register defines the number of lines of the 12th window (min=1, max=3072)
Y_start_13	14	0	The value in this register defines the start address of the 13th window in Y (min=0, max=3071)
Y_size_13	46	0	The value in this register defines the number of lines of the 13th window (min=1, max=3072)
Y_start_14	15	0	The value in this register defines the start address of the 14th window in Y (min=0, max=3071)
Y_size_14	47	0	The value in this register defines the number of lines of the 14th window (min=1, max=3072)
Y_start_15	16	0	The value in this register defines the start address of the 15th window in Y (min=0, max=3071)
Y_size_15	48	0	The value in this register defines the number of lines of the 15th window (min=1, max=3072)
Y_start_16	17	0	The value in this register defines the start address of the 16th window in Y (min=0, max=3071)
Y_size_16	49	0	The value in this register defines the number of lines of the 16th window (min=1, max=3072)
Y_start_17	18	0	The value in this register defines the start address of the 17th window in Y (min=0, max=3071)
Y_size_17	50	0	The value in this register defines the number of lines of the 17th window (min=1, max=3072)

Windowing – multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
Y_start_18	19	0	The value in this register defines the start address of the 18th window in Y (min=0, max=3071)
Y_size_18	51	0	The value in this register defines the number of lines of the 18th window (min=1, max=3072)
Y_start_19	20	0	The value in this register defines the start address of the 19th window in Y (min=0, max=3071)
Y_size_19	52	0	The value in this register defines the number of lines of the 19th window (min=1, max=3072)
Y_start_20	21	0	The value in this register defines the start address of the 20th window in Y (min=0, max=3071)
Y_size_20	53	0	The value in this register defines the number of lines of the 20th window (min=1, max=3072)
Y_start_21	22	0	The value in this register defines the start address of the 21st window in Y (min=0, max=3071)
Y_size_21	54	0	The value in this register defines the number of lines of the 21st window (min=1, max=3072)
Y_start_22	23	0	The value in this register defines the start address of the 22nd window in Y (min=0, max=3071)
Y_size_22	55	0	The value in this register defines the number of lines of the 22nd window (min=1, max=3072)
Y_start_23	24	0	The value in this register defines the start address of the 23rd window in Y (min=0, max=3071)
Y_size_23	56	0	The value in this register defines the number of lines of the 23rd window (min=1, max=3072)
Y_start_24	25	0	The value in this register defines the start address of the 24th window in Y (min=0, max=3071)
Y_size_24	57	0	The value in this register defines the number of lines of the 24th window (min=1, max=3072)
Y_start_25	26	0	The value in this register defines the start address of the 25th window in Y (min=0, max=3071)
Y_size_25	58	0	The value in this register defines the number of lines of the 25th window (min=1, max=3072)
Y_start_26	27	0	The value in this register defines the start address of the 26th window in Y (min=0, max=3071)
Y_size_26	59	0	The value in this register defines the number of lines of the 26th window (min=1, max=3072)
Y_start_27	28	0	The value in this register defines the start address of the 27th window in Y (min=0, max=3071)
Y_size_27	60	0	The value in this register defines the number of lines of the 27th window (min=1, max=3072)
Y_start_28	29	0	The value in this register defines the start address of the 28th window in Y (min=0, max=3071)
Y_size_28	61	0	The value in this register defines the number of lines of the 28th window (min=1, max=3072)
Y_start_29	30	0	The value in this register defines the start address of the 29th window in Y (min=0, max=3071)
Y_size_29	62	0	The value in this register defines the number of lines of the 29th window (min=1, max=3072)
Y_start_30	31	0	The value in this register defines the start address of the 30th window in Y (min=0, max=3071)
Y_size_30	63	0	The value in this register defines the number of lines of the 30th window (min=1, max=3072)
Y_start_31	32	0	The value in this register defines the start address of the 31st window in Y (min=0, max=3071)

Windowing – multiple windows			
Register name	Register address	Default value	Description of the value
Y_size_31	64	0	The value in this register defines the number of lines of the 31st window (min=1, max=3072)
Y_start_32	33	0	The value in this register defines the start address of the 32nd window in Y (min=0, max=3071)
Y_size_32	65	0	The value in this register defines the number of lines of the 32nd window (min=1, max=3072)

Note: The default values will result in one window with 3072 lines to be read out

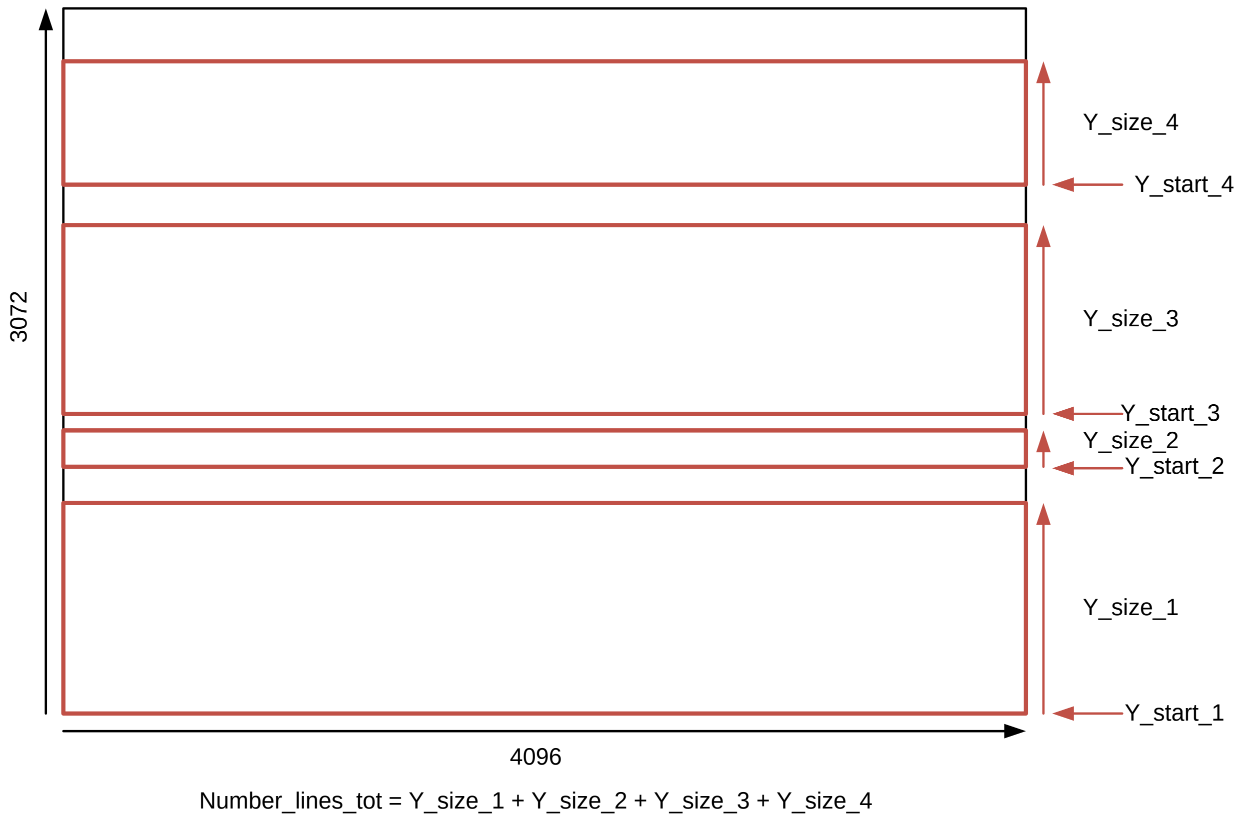


FIGURE 42: EXAMPLE OF 4 SUBWINDOWS READ-OUT

5.5 IMAGE FLIPPING

The image coming out of the image sensor, can be flipped in X and/or Y direction. When flipping in Y is enable, the bottom left pixel (0, 3071) is read out first instead of the top left one (0, 0). When flipping in X is enabled only the pixels within a channel are flipped on the X-axis, not the channels themselves. Flipping in X is only supported when using 32 channels per side. The following registers are involved in image flipping.

Image flipping			
Register name	Register address	Default value	Description of the value
Image_flipping	69[1:0]	0	0: No image flipping 1: Image flipping in X 2: Image flipping in Y (recommended) 3: Image flipping in X and Y

5.6 IMAGE SUBSAMPLING

This mode is only supported in two sided read-out. To maintain the same field of view but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers. These subsampling schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. The registers involved in subsampling are detailed below. A distinction is made between a monochrome and color mode. Subsampling can be enabled in every windowing mode.

5.6.1 MONOCHROME SUBSAMPLING

5.6.1.1 MONOCHROME SUBSAMPLING IN Y DIRECTION

When monochrome subsampling in Y direction is used, the CMV12000 can subsample according to the following scheme:

- read 1 line and skip 1 line
- read 1 line and skip 5 lines
- read 1 line and skip 9 lines
- read 1 line and skip 13 lines
- …

To enable this subsampling, the following registers need to be changed. See section 0 for additional required register settings.

Image subsampling – mono Y			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines read out by the sensor (min=1, max=1536)
Sub_offset	66	0	Value should be (number_of_lines_to_skip +1) /2
Sub_step	67	1	Value should be (number_of_lines_to_skip +1)
Sub_en	68[1]	0	Set to 0
Color	68[0]	1	Set to 1
Color_exp	68[3]	1	Set to 1

The figures below give a monochrome subsampling in Y example (skip 5x and skip 1x).

FIGURE 43: MONOCHROME SUBSAMPLING IN Y EXAMPLES (SKIP 5X AND SKIP 1X)

When monochrome subsampling in Y is enabled, the pixel to output remapping is different from section 4.4. The correct remapping of the subsampled image when this mode is enabled using 64 outputs can be found in the figure below.

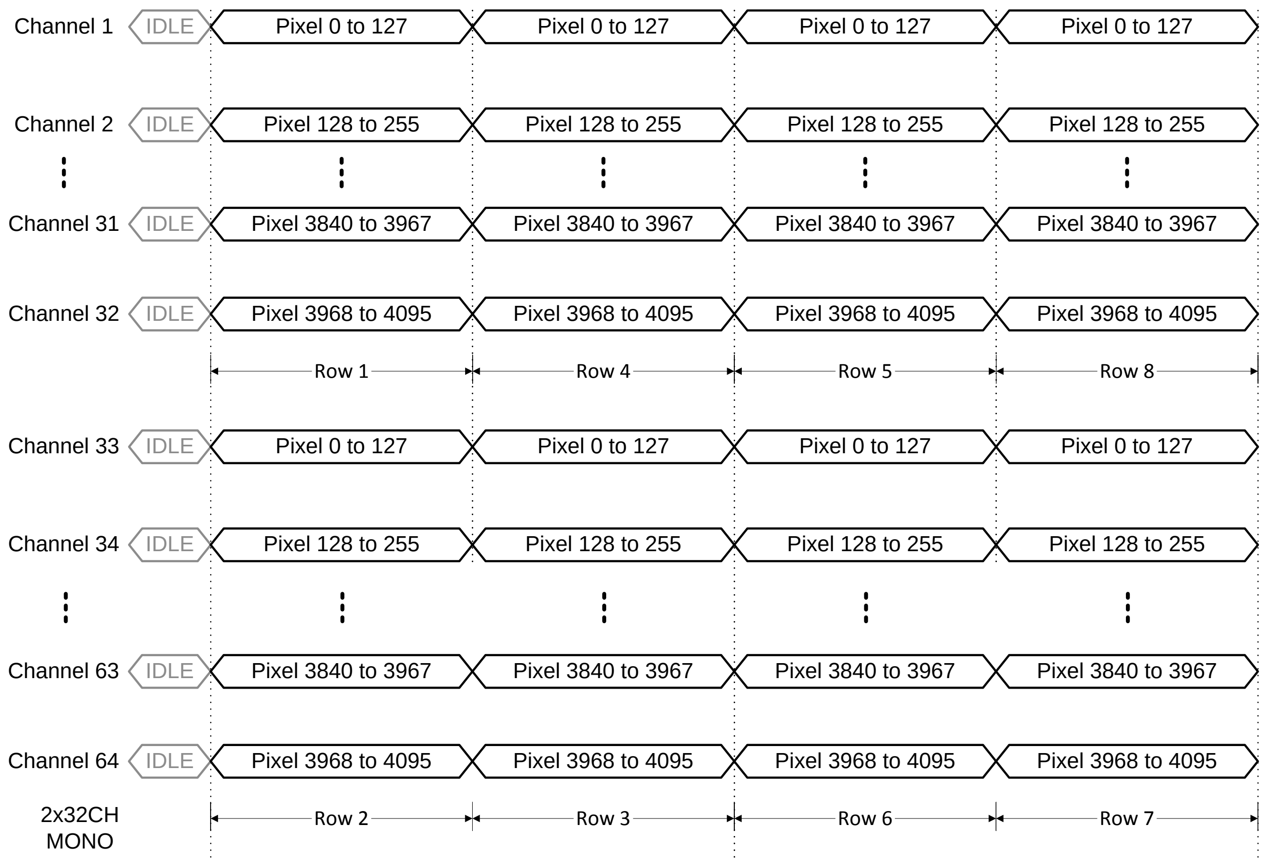


FIGURE 44: MONOCHROME SUBSAMPLING IN Y, PIXEL TO OUTPUT REMAPPING

So the bottom channels will read out rows 1, 4, 5, 8, 9, 12 … and the top channels will read out rows 2, 3, 6, 7, 10, 11 … 64 bursts (2 x 32) of 128 (2 x 64) pixels happen in parallel on the data outputs. This means that four complete subsampled rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 1536 rows being read out (3072/2).

5.6.1.2 Monochrome subsampling in X and Y direction

When monochrome subsampling in X and Y is used, the CMV12000 will only subsample according to the following scheme:

- In X: skip 1
- In Y: skip 1

To enable this subsampling, the following registers need to be changed. See section 0 for additional required register settings.

Image subsampling – mono X/Y			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines read out by the sensor (min=1, max=1536)
Sub_offset	66	0	Value should be 1
Sub_step	67	1	Value should be 2
Sub_en	68[1]	0	Set to 1
Color	68[0]	1	Set to 1
Color_exp	68[3]	1	Set to 1

The figure below gives the monochrome subsampling example (skip 1x).

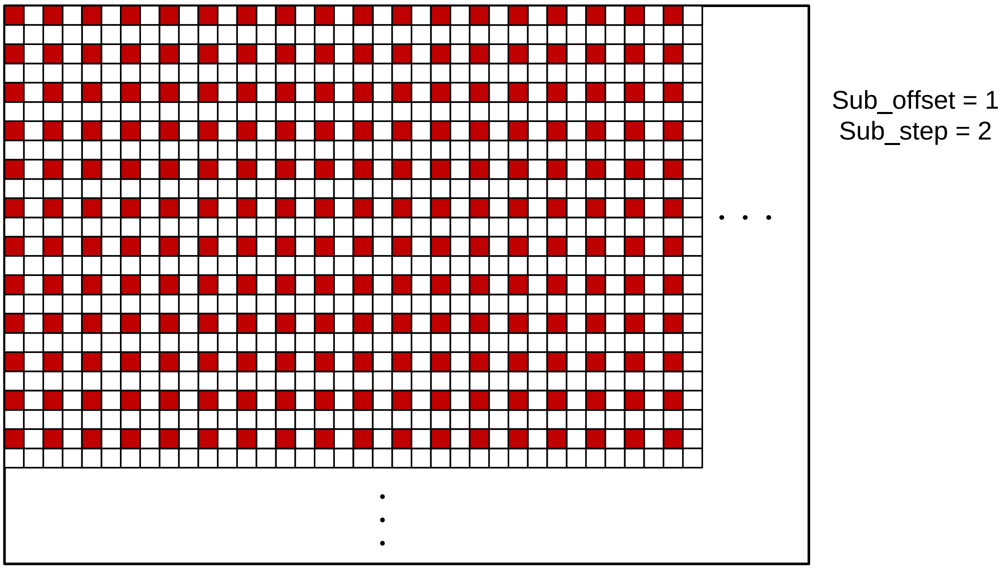


FIGURE 45: MONOCHROME SUBSAMPLING IN X AND Y (SKIP 1X)

When this monochrome subsampling in X and Y mode is enabled, the pixel to output remapping is different from section 4.4. The correct remapping of the subsampled image when this mode is enabled using 64 outputs can be found in Figure 45 below.

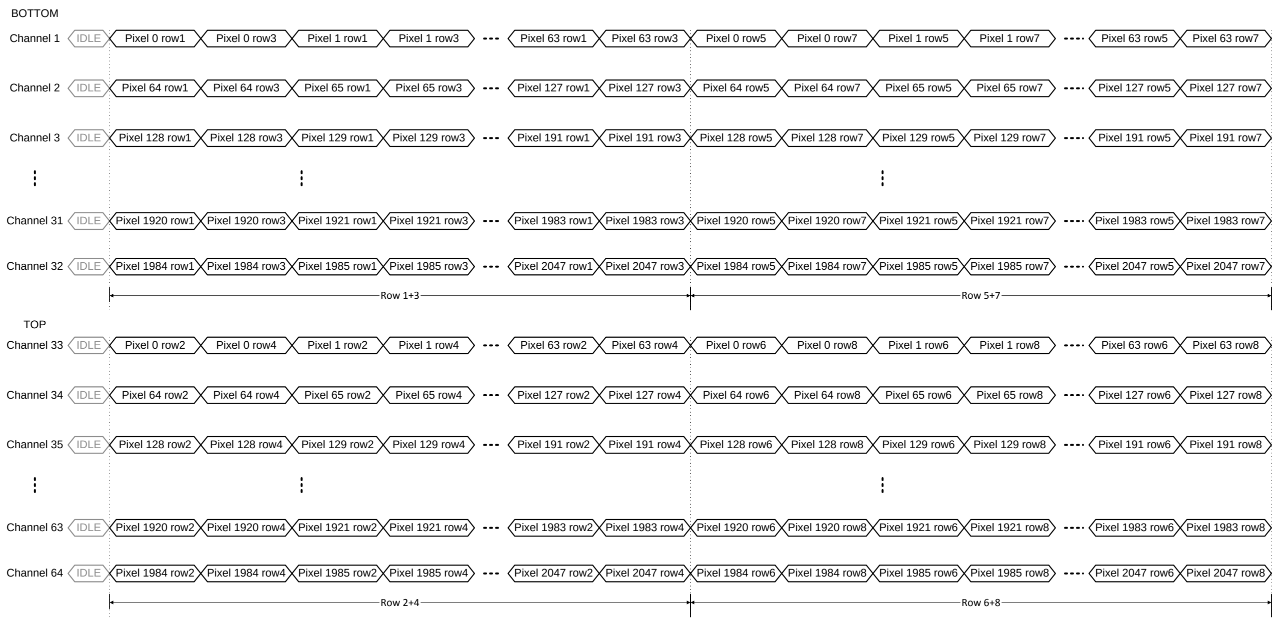


FIGURE 46: MONOCHROME SUBSAMPLING IN X AND Y, PIXEL TO OUTPUT REMAPPING

64 bursts (2 x 32) of 128 (2 x 64) pixels happen in parallel on the data outputs. This means that four complete subsampled rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 1536 rows being read out (3072/2).

5.6.2 COLOR SUBSAMPLING

When a color sensor is used, the subsampling scheme should take into account that a Bayer color filter is applied on the sensor. This Bayer pattern should be preserved when subsampling is used. This means that the number of rows and columns to be skipped should always be a multiple of two. A color subsampling scheme can be programmed to achieve these requirements. Of course, this color subsampling scheme can also be programmed in a monochrome sensor.

5.6.2.1 Color subsampling in Y direction

When color subsampling in Y direction is used, the CMV12000 can subsample according to the following scheme:

- read 2 lines and skip 2 lines
- read 2 lines and skip 6 lines
- read 2 lines and skip 10 lines
- read 2 lines and skip 14 lines
- …

See the table of registers below for more details. See section 0 for additional required register settings.

Image subsampling – color Y			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines read out by the sensor (min=1, max=1536)
Sub_offset	66	0	Value should be 0
Sub_step	67	1	Value should be (number_of_lines_to_skip/2)+1
Sub_en	68[1]	0	Set to 0
Color	68[0]	1	Set to 0
Color_exp	68[3]	1	Set to 0

The figures below give two subsampling in Y examples (skip 6x and skip 2x) in color mode.

FIGURE 47: SUBSAMPLING IN Y EXAMPLES IN COLOR MODE (SKIP 6X AND SKIP2X)

When color subsampling in Y is enabled, the pixel to output remapping is different from section 4.4. The correct remapping of the subsampled image when this mode is enabled using 64 outputs can be found in the figure below.

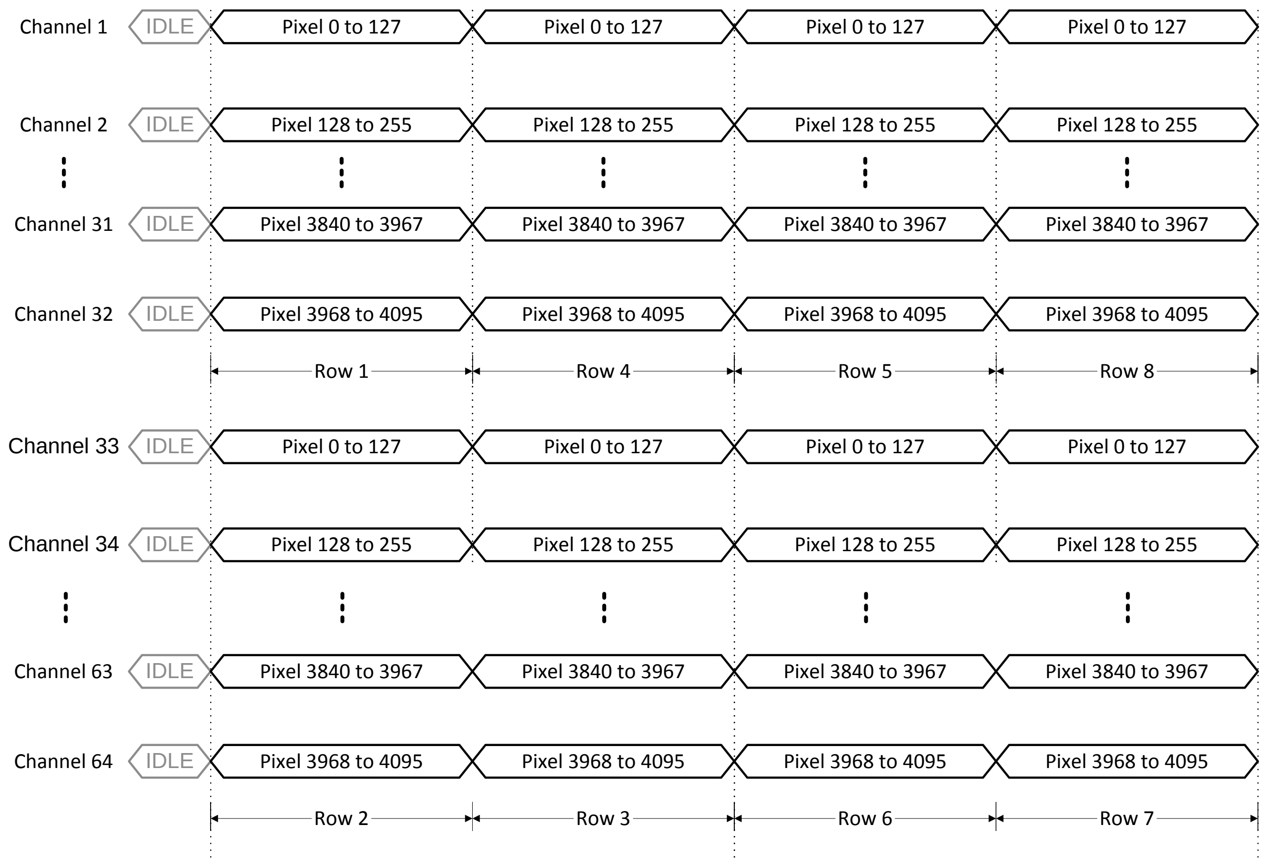


FIGURE 48: COLOR SUBSAMPLING IN Y, PIXEL TO OUTPUT REMAPPING

So the bottom channels will read out rows 1, 4, 5, 8, 9, 12 … and the top channels will read out rows 2, 3, 6, 7, 10, 11 … 64 bursts (2 x 32) of 128 (2 x 64) pixels happen in parallel on the data outputs. This means that four complete subsampled rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 1536 rows being read out (3072/2).

5.6.2.2 COLOR SUBSAMPLING IN X AND Y DIRECTION

When color subsampling in X and Y is used, the CMV12000 will only subsample according to the following scheme

- In X: skip 2
- In Y: skip 2

To enable this subsampling mode, the following registers need to be changed. See section 0 for additional required register settings.

Image subsampling – color X/Y			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines read out by the sensor (min=1, max=1536)
Sub_offset	66	0	Value should be 0
Sub_step	67	1	Value should be 2
Sub_en	68[1]	0	Set to 1
Color	68[0]	1	Set to 0
Color_exp	68[3]	1	Set to 0

The figure below gives the color subsampling example (skip 2x).

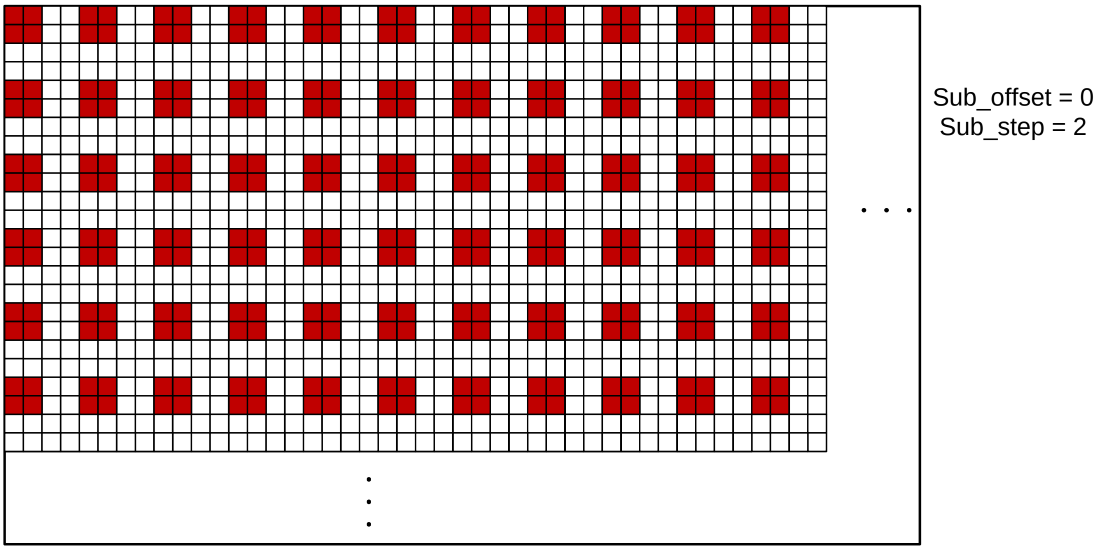


FIGURE 49: COLOR SUBSAMPLING IN X AND Y (SKIP 2X)

When this color subsampling in X and Y mode is enabled, the pixel to output remapping is different from section 4.4. The correct remapping of the subsampled image when this mode is enabled using 64 outputs can be found in Figure 49 below.

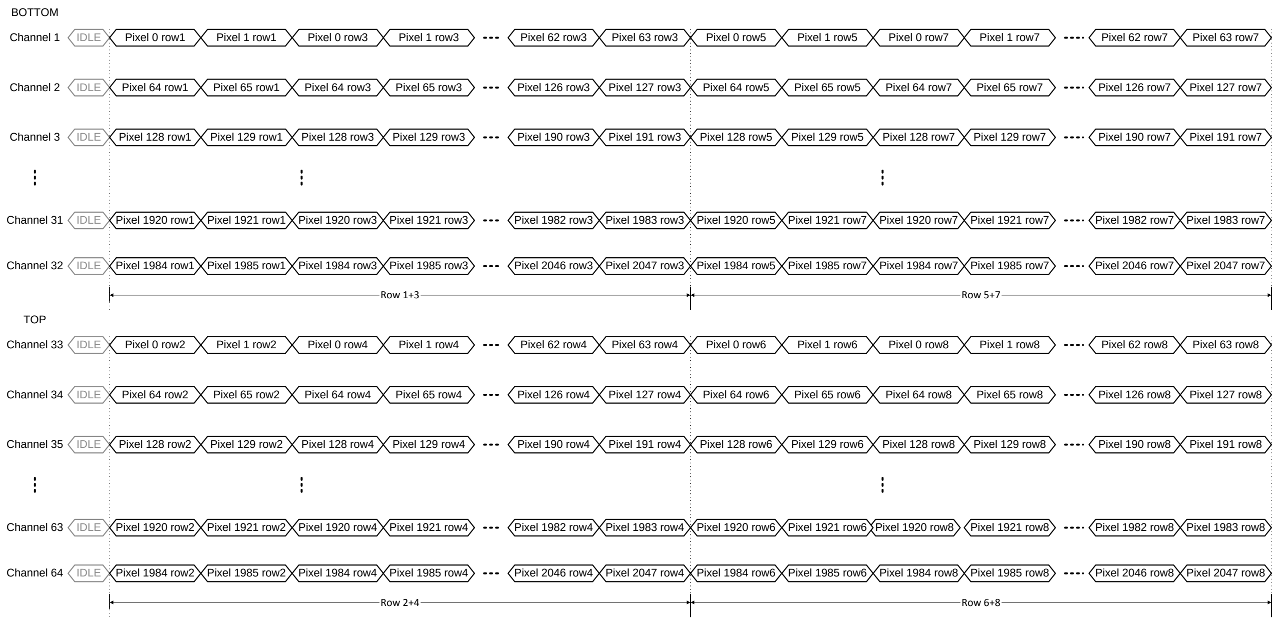


FIGURE 50: COLOR SUBSAMPLING IN X AND Y, PIXEL TO OUTPUT REMAPPING

64 bursts (2 x 32) of 128 (2 x 64) pixels happen in parallel on the data outputs. This means that four complete subsampled rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 1536 rows being read out (3072/2).

5.7 BINNING

This mode is only supported in two sided read-out. To maintain the same field of view but reduce the noise coming out of the sensor, a binning mode is implemented on the chip. This mode will sum 4 pixels (analog domain) to reduce the noise and data coming from the chip. The responsivity increases with x4. The PGA divide-by-3 can be used to counter this increase. Other PGA gains (x2, x3, x4) are not useable. Different binning schemes can be programmed by setting the appropriate registers. These binning schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. The registers involved in binning are detailed below. A distinction is made between a monochrome and color mode. Binning can be enabled in every windowing mode.

5.7.1 Monochrome binning

When monochrome binning is used, the CMV12000 will average 4 pixels and reads out this average pixel value. This will result in an image which is 4 times smaller than the original image (X-size/2 and Y-size/2, max 2048 x 1536).

To enable this monochrome binning, the following registers need to be changed. See section 0 for additional required register settings.

Image binning - mono			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines of the original image (min=1, max=3072)
Sub_offset	66	0	Value should be 0
Sub_step	67	1	Value should be 1
Bin_en	68[2]	0	Set to 1
Color	68[0]	1	Set to 1
Color_exp	68[3]	1	Set to 1

The figure below gives the monochrome binning example (skip 1x).

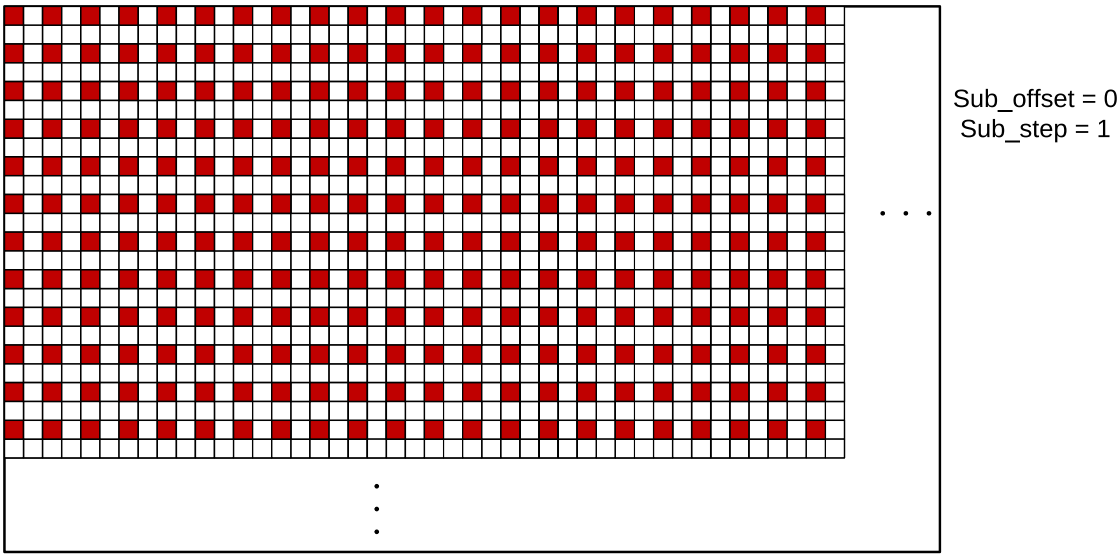


FIGURE 51: MONOCHROME BINNING (SKIP 1X)

When this monochrome binning mode is enabled, the pixel to output remapping is different from section 4.4. The correct remapping of the binned image is shown in the figure below.

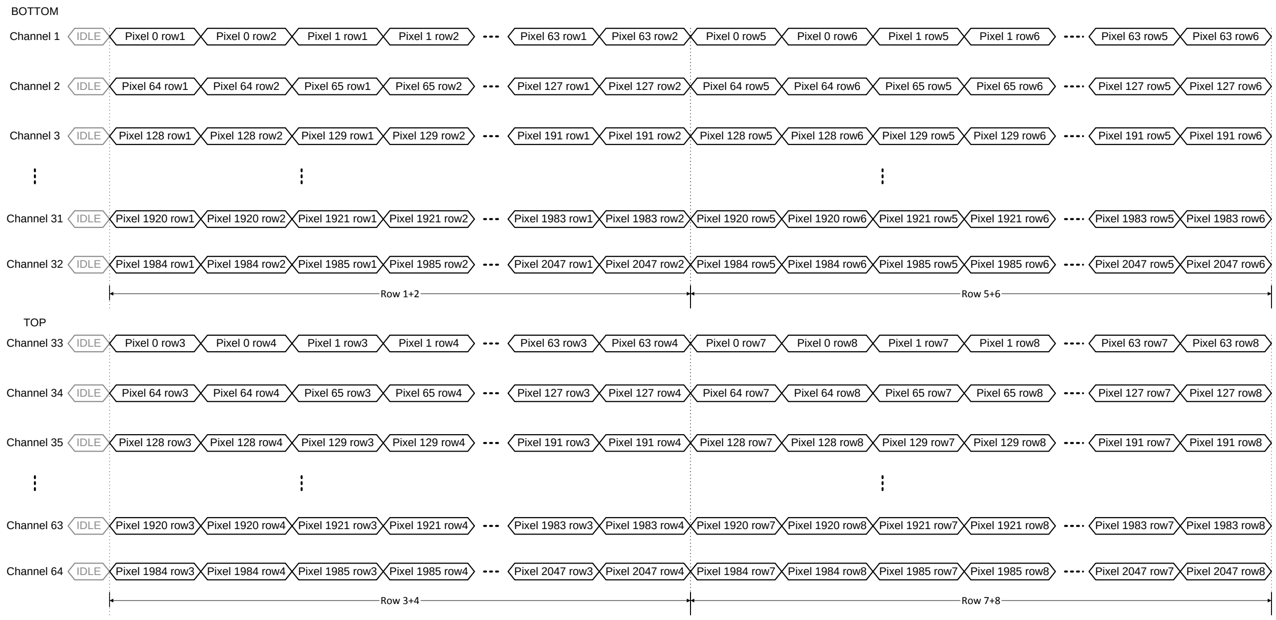


FIGURE 52: MONOCHROME BINNING, PIXEL TO OUTPUT REMAPPING

5.7.2 COLOR BINNING

When a color sensor is used, the binning scheme should take into account that a Bayer color filter is applied on the sensor. This Bayer pattern should be preserved when binning is enabled. This means that the number of rows and columns to be skipped should always be a multiple of two. A color binning scheme can be programmed to achieve these requirements. Of course, this color binning scheme can also be programmed in a monochrome sensor. See the table of registers below for more details. See section 0 for additional required register settings.

Image binning - color			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines_tot	1	3072	The value in this register defines the total number of lines of the original image (min=1, max=3072)
Sub_offset	66	0	Value should be 1
Sub_step	67	1	Value should be 1
Bin_en	68[2]	0	Set to 1
Color	68[0]	1	Set to 0
Color_exp	68[3]	1	Set to 0

The figure below gives the color binning example (skip 2x).

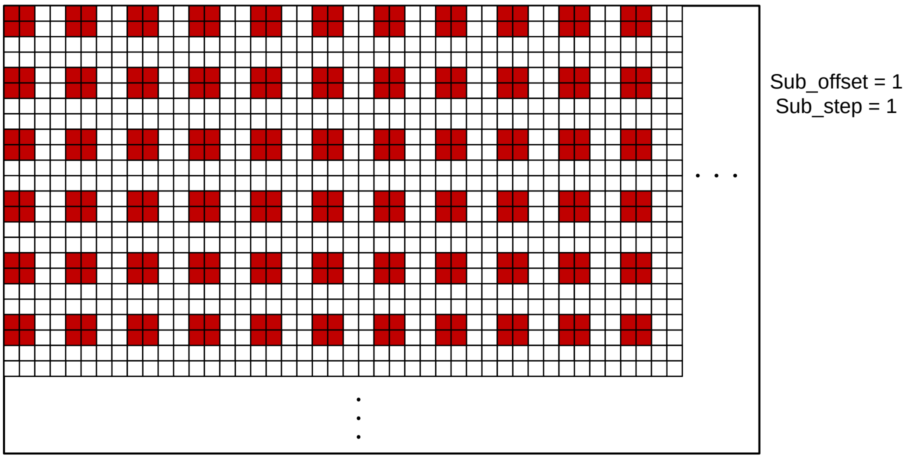


FIGURE 53: COLOR BINNING (SKIP 2X)

When this color binning mode is enabled, the pixel to output remapping is different from section 4.4. The correct remapping of the binned image is shown in the figure below.

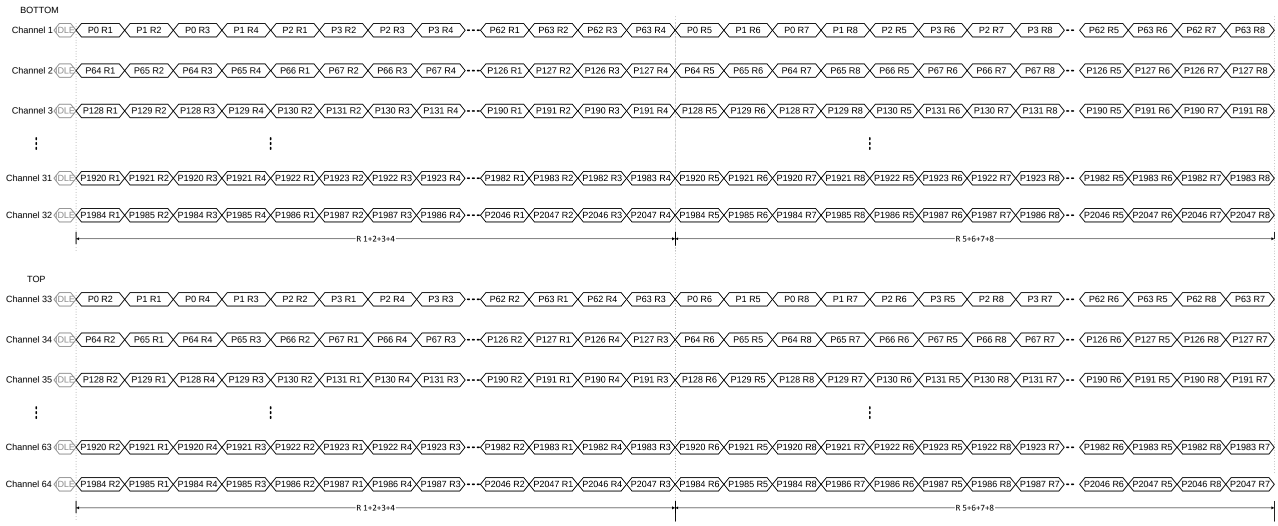


FIGURE 54: COLOR BINNING, PIXEL TO OUTPUT REMAPPING

5.8 Number of frames

When internal exposure mode is selected, the number of frames sent by the sensor after a frame request can be programmed in the corresponding sequencer register.

Number of frames			
Register name	**Register address**	**Default value**	**Description of the value**
Number_frames	80	1	The value in this register defines the number of frames grabbed and sent by the image sensor in internal exposure mode (min =1, max = 65535)

5.9 Output mode

The number of LVDS channels on each side can be selected by programming the appropriate sequencer register. The pixel remapping scheme and the read-out timing for each mode can be found in section 0 of this document. See section 5.15 for additional required register settings. The bottom channels use output pins OUT1_N/P to OUT32_N/P and the top channels use output pins OUT33_N/P to OUT64_N/P.

Output mode			
Register name	**Register address**	**Default value**	**Description of the value**
Output_mode	81[4:0]	0	0: 32 outputs used on each side 1: 16 outputs used on each side 3: 8 outputs used on each side 7: 4 outputs used on each side 15: 2 outputs used on each side 31: 1 output used on each side
Disable_top	81[5]	0	Set to 0 if using two sided read-out (top and bottom). Set to 1 to use only the bottom LVDS outputs (32 outputs or less)*.
Sub_offset	66	0	Set to 65535 when Disable_top = 1 and no subsampling in Y is used.

*Keep in mind that subsampling and binning is not supported when only reading out one side (Disable_top=1)!

5.10 Training pattern

As detailed in section 4.6, a training pattern is sent over the LVDS data channels whenever no valid image data is sent. The training pattern TP1 can be programmed using the sequencer register below.

Training pattern			
Register name	**Register address**	**Default value**	**Description of the value**
Training_pattern	89[11:0]	85	The 12 bits of this 12-bit word are sent in 12-bit mode. In 10-bit mode the 10 LSBs are sent. In 8-bit mode, the 8 LSBs are sent.

5.11 8-bit, 10-bit or 12-bit mode

The CMV12000 has the possibility to send 12 bits, 10 bits or 8 bits per pixel. The end user can select the desired resolution by programming the corresponding sequencer register. See section 3.8 for details on how the bit mode can be changed. See section 0 for additional required register settings.

8-bit, 10-bit or 12-bit mode			
Register name	**Register address**	**Default value**	**Description of the value**
Bit_mode	118[1:0]	1	0: 12 bits per pixel 1: 10 bits per pixel 2: 8 bits per pixel

5.12 Data rate

During start-up or after a sequencer reset, the data rate can be changed if a lower speed than 300 Mbps is desired. This can be done by applying a lower LVDS input clock (LVDS_CLK_P/N). See section 3.5 for more details on the input clock. See section 3.7 for details on the start-up sequence. No registers should be changed when a data rate different from 300 Mbps is used.

5.13 Power control

The power consumption of the CMV12000 can be decreased by disabling the LVDS data channels when they are not used (in 32, 16, 8, 4, 2 or 1 channel(s) mode). Disabling an output saves 15mW on the VDD18 supply per output.

Power control			
Register name	**Register address**	**Default value**	**Description of the value**
Channel_en_bot	90-91	All ‘1’	Bit 0-31 enable/disable the bottom data output channels 0: disabled 1: enabled

Power control			
Register name	**Register address**	**Default value**	**Description of the value**
Channel_en_top	92-93	All '1'	Bit 0-31 enable/disable the top data output channels 0: disabled 1: enabled
Channel_en	94[2:0]	All '1'	Bit 0 enables/disables the output clock channel Bit 1 enables/disables the control channel Bit 2 enables/disables the input clock channel 0: disabled 1: enabled

5.14 Offset and gain

5.14.1 Offset

A digital offset can be applied to the output signal. This dark level offset can be programmed by setting the desired value in the sequencer registers. A bottom and top channel offset can be given to the dark level by programming the appropriate registers.

Offset			
Register name	**Register address**	**Default value**	**Description of the value**
Offset_bot	87[11:0]	780	The value in this register defines the dark level offset applied to the bottom output signal (min = 0, max = 4095) 1824: 12 bits per pixel 533: 10 bits per pixel 600: 8 bits per pixel The optimal setting can differ per device.
Offset_top	88[11:0]	780	The value in this register defines the dark level offset applied to the top output signal (min = 0, max = 4095) 1820: 12 bits per pixel 533: 10 bits per pixel 600: 8 bits per pixel The optimal setting can differ per device.

5.14.2 Gain

An analog gain and ADC gain can be applied to the output signal. The analog gain is applied by a PGA in every column. The digital gain is applied after the ADC.

Gain			
Register name	**Register address**	**Default value**	**Description of the value**
PGA_gain	115[2:0]	0	0: unity gain 1: x2 gain 3: x3 gain 7: x4 gain
PGA_div	115[3]	0	1: divide signal by 3
ADC_range	116[7:0]	127	Change the slope of the ramp used by the ADC 205: 8 bit 155: 10 bit 255: 12 bit
ADC_range_mult	116[9:8]	1	Change the slope of the ramp used by the ADC 1: 8 bit 3: 10bit 3: 12bit

Gain			
Register name	Register address	Default value	Description of the value
DIG_gain	117[4:0]	4	Sets a digital gain according to the table below. Odd values give unity gain. Recommend to use the x1 setting.

Value	1	2	3	4	6	8	10	12	14	16
12b	**1**	2	3	4	6	8	10	12	14	16
10b	1/4	2/4	3/4	**1**	6/4	2	10/4	3	14/4	16/4
8b	1/6	2/6	3/6	4/6	**1**	8/6	10/6	2	14/6	16/6

The ADC range is dependent of the input clock speed, the slower the clock the larger the ADC range has to be. Below you can see a plot showing which ADC range to use with a certain clock speed and bit mode. For 12bit, the ADC range cannot be extended anymore, meaning that when using a slower clock, the digital swing (in DN) will decrease.

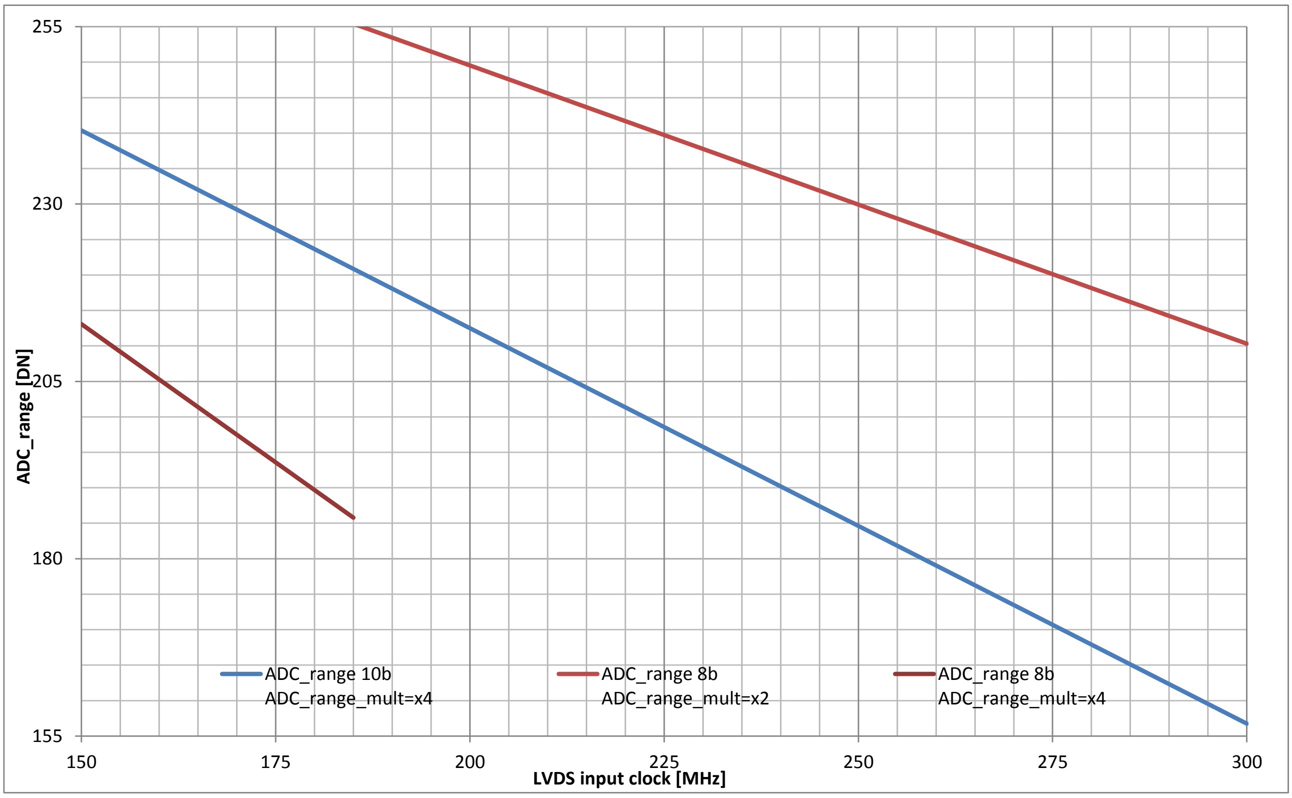


FIGURE 55: ADC RANGE VS. CLOCK SPEED

5.15 Black reference columns

When the appropriate SPI register is set, the 8 first and 8 last columns will be put to an electrical black reference. This electrical black reference can be used to correct row noise.

Black columns			
Register name	Register address	Default value	Description of the value
Black_col_en	89 bits[15]	0	0 : disable 1 : enable

5.16 Test Pattern

The CMV12000 has a built-in fixed test pattern. The pattern consists of increasing pixel values per column per channel. Per (top and bottom) channel the values of the column increase with 1. The value of the first column of a channel increases with 1 per channel. So channels 1/33 will contain 0, 1, 2 … 126, 127, channels 2/34 contain 1, 2, 3 … 127, 128, channels 32/64 contain 31, 32, 33 … 157, 158.

Test Pattern			
Register name	**Register address**	**Default value**	**Description of the value**
Test	122[1:0]	0	0 : disable 3 : enable

FIGURE 56: TEST PATTERN

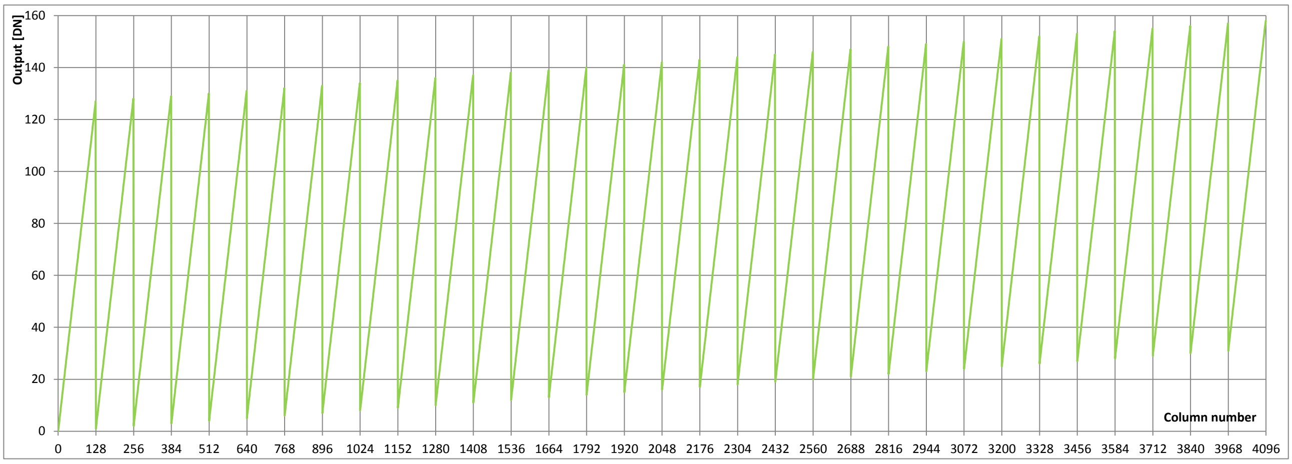


FIGURE 57: TEST PATTERN PROFILE

5.17 Additional required register settings

Depending on the output mode, bit mode and subsampling or binning mode additional register settings must be set. The tables below give an overview of the registers that need to be set for each mode.

5.17.1 8-bit mode

- Register with address 84: 143
- Register with address 113: 784
- Register with address 114: 101
- Register with address 109: 13416

Normal mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	3102	1822	1054	542	286	286
Register address 83	5894	5894	5894	5894	5894	5894
Register address 85	143	257	515	1031	2063	4127
Register address 86	143	257	515	1031	2063	4127
Register address 98	39705	39705	39705	39705	39705	39705

Subsampling mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	2334	1822	1054	542	286	286
Register address 83	5892	5892	5892	5892	5892	5892
Register address 85	191	257	515	1031	2063	4127
Register address 86	95	128	257	515	1031	2063
Register address 98	40217	40217	40217	40217	40217	40217

Binning mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	1310	1310	1054	542	286	286
Register address 83	5892	5892	5892	5892	5892	5892
Register address 85	383	383	515	1031	2063	4127
Register address 86	95	95	128	257	515	1031
Register address 98	40217	40217	40217	40217	40217	40217

5.17.2 10-BIT MODE

- Register with address 84: 128
- Register with address 113: 785
- Register with address 114: 80
- Register with address 109: 13287

Normal mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	3614	1822	1054	542	286	286
Register address 83	5893	5893	5893	5893	5893	5893
Register address 85	128	257	515	1031	2063	4127
Register address 86	128	257	515	1031	2063	4127
Register address 98	39705	39705	39705	39705	39705	39705

Subsampling mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	3102	1822	1054	542	286	286
Register address 83	5891	5891	5891	5891	5891	5891
Register address 85	143	257	515	1031	2063	4127
Register address 86	71	128	257	515	1031	2063
Register address 98	40217	40217	40217	40217	40217	40217

Binning mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	1566	1566	1054	542	286	286
Register address 83	5891	5891	5891	5891	5891	5891
Register address 85	287	287	515	1031	2063	4127
Register address 86	71	71	128	257	515	1031
Register address 98	40217	40217	40217	40217	40217	40217

5.17.3 12-BIT MODE

- Register with address 84: 216
- Register with address 113: 780
- Register with address 114: 179
- Register with address 109: 13931

Normal mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	2078	1822	1054	542	286	286
Register address 83	5897	5897	5897	5897	5897	5897
Register address 85	216	257	515	1031	2063	4127
Register address 86	216	257	515	1031	2063	4127
Register address 98	39705	39705	39705	39705	39705	39705

Subsampling mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	2078	1822	1054	542	286	286
Register address 83	5892	5892	5892	5892	5892	5892
Register address 85	217	257	515	1031	2063	4127
Register address 86	108	128	257	515	1031	2063
Register address 98	40217	40217	40217	40217	40217	40217

Binning mode						
Outputs used on each side	**32**	**16**	**8**	**4**	**2**	**1**
	Register values					
Register address 82	1310	1310	1054	542	286	286
Register address 83	5892	5892	5892	5892	5892	5892
Register address 85	383	383	515	1031	2063	4127
Register address 86	95	95	128	257	515	1031
Register address 98	40217	40217	40217	40217	40217	40217

6 REGISTER OVERVIEW

The table below gives an overview of all the sensor registers. The registers with the remark "Do not change" should not be changed.

Register overview			
address	default	value	remark
0	0		DNC
1	3072	Number_lines_tot[15:0]	
2	0	Y_start_1[15:0]	
3	0	Y_start_2[15:0]	
4	0	Y_start_3[15:0]	
5	0	Y_start_4[15:0]	
6	0	Y_start_5[15:0]	
7	0	Y_start_6[15:0]	
8	0	Y_start_7[15:0]	
9	0	Y_start_8[15:0]	
10	0	Y_start_9[15:0]	
11	0	Y_start_10[15:0]	
12	0	Y_start_11[15:0]	
13	0	Y_start_12[15:0]	
14	0	Y_start_13[15:0]	
15	0	Y_start_14[15:0]	
16	0	Y_start_15[15:0]	
17	0	Y_start_16[15:0]	
18	0	Y_start_17[15:0]	
19	0	Y_start_18[15:0]	
20	0	Y_start_19[15:0]	
21	0	Y_start_20[15:0]	
22	0	Y_start_21[15:0]	
23	0	Y_start_22[15:0]	
24	0	Y_start_23[15:0]	
25	0	Y_start_24[15:0]	
26	0	Y_start_25[15:0]	
27	0	Y_start_26[15:0]	
28	0	Y_start_27[15:0]	
29	0	Y_start_28[15:0]	
30	0	Y_start_29[15:0]	
31	0	Y_start_30[15:0]	
32	0	Y_start_31[15:0]	
33	0	Y_start_32[15:0]	
34	0	Y_size_1[15:0]	
35	0	Y_size_2[15:0]	
36	0	Y_size_3[15:0]	
37	0	Y_size_4[15:0]	
38	0	Y_size_5[15:0]	
39	0	Y_size_6[15:0]	
40	0	Y_size_7[15:0]	
41	0	Y_size_8[15:0]	
42	0	Y_size_9[15:0]	
43	0	Y_size_10[15:0]	
44	0	Y_size_11[15:0]	
45	0	Y_size_12[15:0]	
46	0	Y_size_13[15:0]	
47	0	Y_size_14[15:0]	
48	0	Y_size_15[15:0]	
49	0	Y_size_16[15:0]	
50	0	Y_size_17[15:0]	
51	0	Y_size_18[15:0]	
52	0	Y_size_19[15:0]	

Register overview			
address	default	value	remark
53	0	Y_size_20[15:0]	
54	0	Y_size_21[15:0]	
55	0	Y_size_22[15:0]	
56	0	Y_size_23[15:0]	
57	0	Y_size_24[15:0]	
58	0	Y_size_25[15:0]	
59	0	Y_size_26[15:0]	
60	0	Y_size_27[15:0]	
61	0	Y_size_28[15:0]	
62	0	Y_size_29[15:0]	
63	0	Y_size_30[15:0]	
64	0	Y_size_31[15:0]	
65	0	Y_size_32[15:0]	
66	0	Sub_offset[15:0]	
67	1	Sub_step[15:0]	
68	9	Color_exp[3] Bin_en[2] Sub_en[1] Color[0]	
69	0	Image_flipping[1:0]	Set to 2
70	0	Exp_dual[1] Exp_ext[0]	
71	1536	Exp_time[15:0]	
72	0	Exp_time[23:16]	
73	1536	Exp_time2[15:0]	
74	0	Exp_time2[23:16]	
75	0	Exp_kp1[15:0]	
76	0	Exp_kp1[23:16]	
77	0	Exp_kp2[15:0]	
78	0	Exp_kp2[23:16]	
79	1	Number_slopes[1:0]	
80	1	Number_frames[15:0]	
81	0	Disable_top[5] Output_mode[4:0]	
82	5682	Setting_1[15:0]	*
83	5893	Setting_2[15:0]	*
84	130	Setting_3[15:0]	*
85	130	Setting_4[15:0]	*
86	130	Setting_5[15:0]	*
87	780	Offset_bot[11:0]	**
88	780	Offset_top[11:0]	**
89	85	Black_col_en[15] Training_pattern[11:0]	
90	65535	Channel_en_bot[15:0]	
91	65535	Channel_en_bot[31:16]	
92	65535	Channel_en_top[15:0]	
93	65535	Channel_en_top[31:16]	
94	7	Channel_en[2:0]	
95	65535	ADC_clk_en_bot[15:0]	
96	65535	ADC_clk_en_top[15:0]	
97	0		FV
98	34952		*
99	34952		FV
100	0		DNC
101	0		DNC
102	8256		Set to 8312
103	4032		FV
104	64		FV
105	8256		FV
106	8256	Vtfl3[13:7] Vtfl2[6:0]	
107	12384		Set to 10326
108	12384		Set to 12381
109	12384		*

Register overview					
address	default	value			remark
110	12384				FV
111	34952				FV
112	0				Set to 5
113	778	Setting_6[15:0]			*
114	95	Setting_7[15:0]			*
115	0		PGA_div[3]	PGA_gain[2:0]	
116	383	ADC_range_mult[9:8]	ADC_range[7:0]		**
117	4			DIG_gain[4:0]	**
118	1			Bit_mode[1:0]	**
119	0				DNC
120	9				DNC
121	1				FV
122	32			Test_pattern[1:0]	DNC
123	0				DNC
124	5				Set to 15
125	2				FV
126	770				DNC
127	0	Temp_sensor[15:0]			

Notes:

* see section 0 for the value of these registers.

** See chapter 5.14 for the values of these registers

DNC = Do not change, these registers should never be written. They are fixed and should remain unchanged.

FV = Fixed value. These registers have a fixed value which might be updated in future revisions of this datasheet.

7 Mechanical specifications

7.1 Package drawing

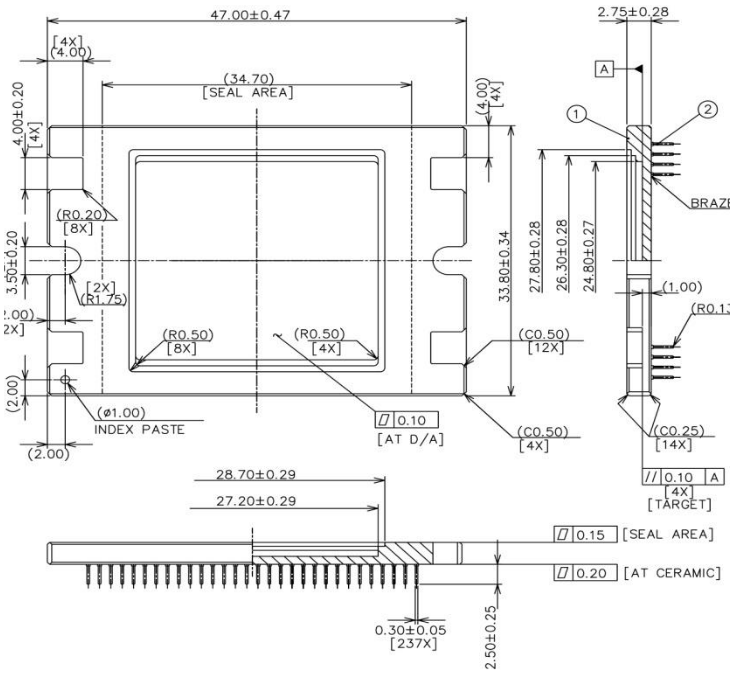


FIGURE 58: PACKAGE DRAWING OF THE CMV12000, ALL DISTANCES IN MM

7.2 Assembly drawing

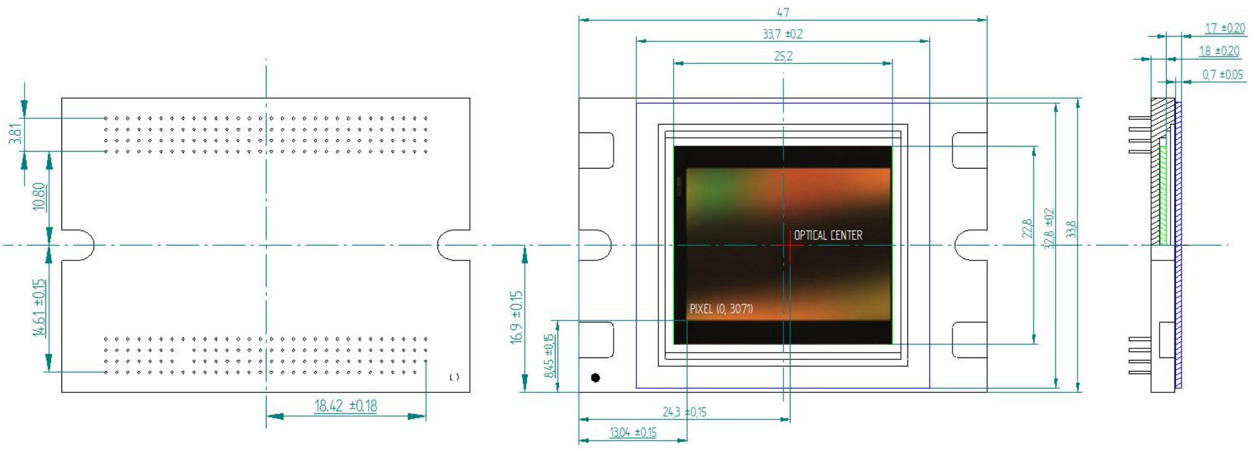


FIGURE 59: ASSEMBLY DRAWING OF CMV12000 WITH COVER GLASS AND SENSOR DIE, ALL DISTANCES IN MM

Rotation of die referenced to the outside of package: +/-0.5 degrees.

Tilt of die referenced to the die attach area (bottom cavity): +/-0.15 degrees.

7.3 Cover glass

The cover glass of the CMV12000 will be plain D263 glass with AR coatings. When a color sensor is used an IR-cutoff filter should be placed in the optical path of the sensor.

7.4 Color Filters

When a color version of the CMV12000 is used, the color filters are applied in a Bayer pattern. When flipping in Y is not enabled (register 69 =0), the first pixel read-out, pixel (0, 0), is the top left one and has a red filter. If register 69 is '2' (recommended), the bottom left pixel (0, 3071) is read-out first and it has a green filter.

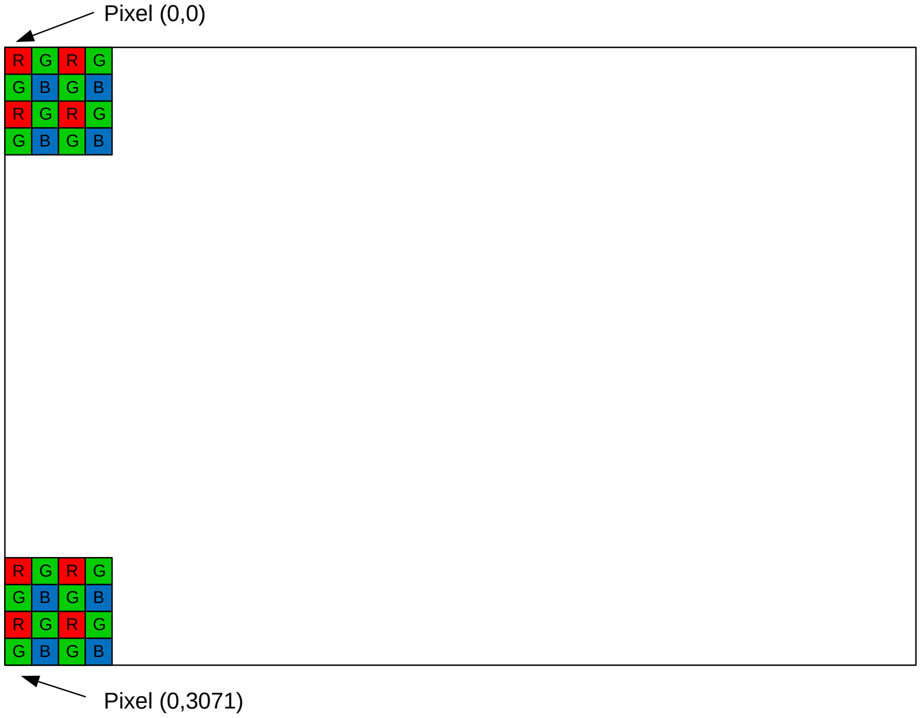
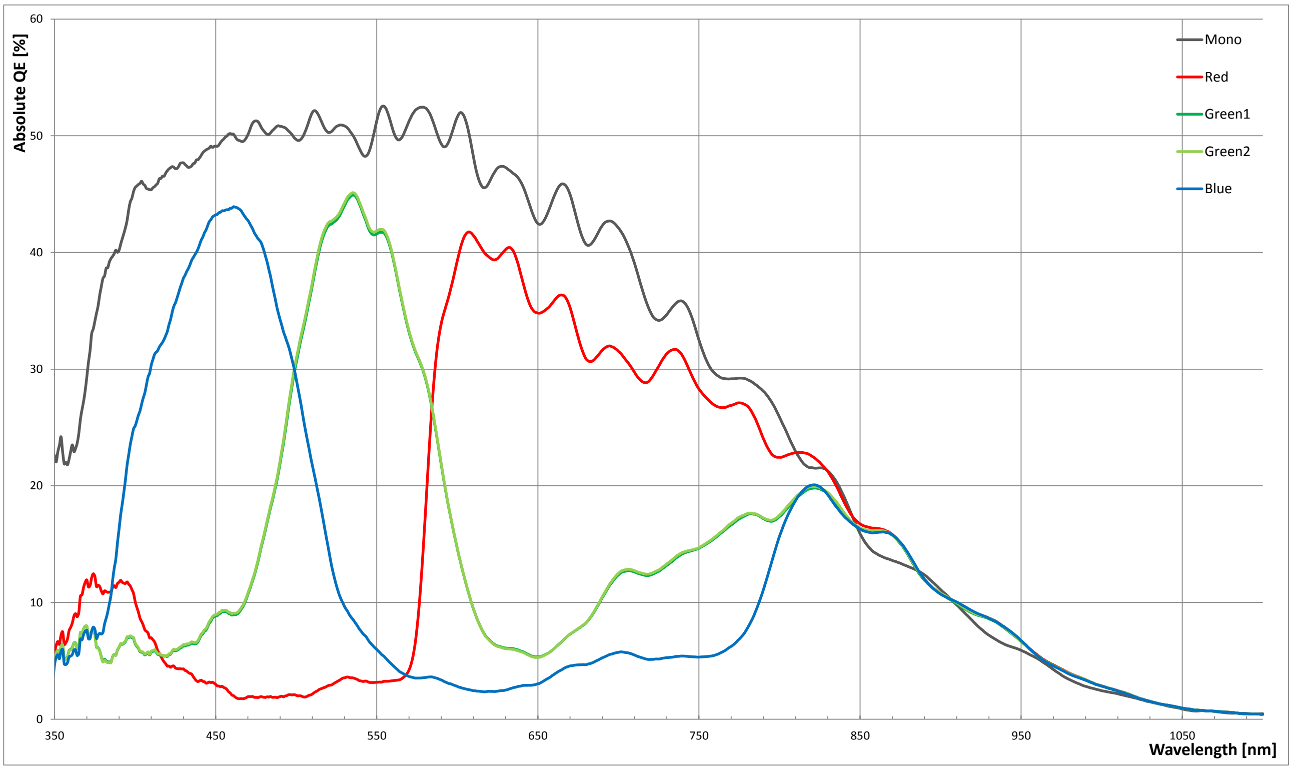


FIGURE 60: COLOR FILTER BAYER PATTERN

8 SPECTRAL RESPONSE

Below you can find the typical quantum efficiency of a monochrome and color device.



9 PIN LIST

The pin list of the CMV12000 can be found below.

Pin number	Pin name	Description	Type
A2	TANA	Test pin for analog pixel signals (do not connect)	Analog output
A3	VREF	Reference for column amps (decouple with 100nF to GND)	Bias
A4	VPCH_L	Precharge low voltage (decouple with 100nF to GND)	Bias
A5	OUTCTR_N	LVDS negative control channel output	LVDS output
A6	OUTCTR_P	LVDS positive control channel output	LVDS output
A7	OUT2_N	LVDS negative output channel 2	LVDS output
A8	OUT2_P	LVDS positive output channel 2	LVDS output
A9	GND	Ground pin	Ground
A10	VDD18	1.8V supply	Supply
A11	OUT9_N	LVDS negative output channel 9	LVDS output
A12	OUT9_P	LVDS positive output channel 9	LVDS output
A13	OUT13_N	LVDS negative output channel 13	LVDS output
A14	OUT13_P	LVDS positive output channel 13	LVDS output
A15	VDD18	1.8V supply	Supply
A16	VDD18	1.8V supply	Supply
A17	OUT19_N	LVDS negative output channel 19	LVDS output
A18	OUT19_P	LVDS positive output channel 19	LVDS output
A19	OUT23_N	LVDS negative output channel 23	LVDS output
A20	OUT23_P	LVDS positive output channel 23	LVDS output
A21	GND	Ground pin	Ground
A22	VDD18	1.8V supply	Supply
A23	OUT29_N	LVDS negative output channel 29	LVDS output
A24	OUT29_P	LVDS positive output channel 29	LVDS output
A25	GND	Ground pin	Ground
A26	VDD18	1.8V supply	Supply
A27	VDD18	1.8V supply	Supply
A28	GND	Ground pin	Ground
A29	GND	Ground pin	Ground
A30	VDD_PIX	3.0V supply	Supply
B1	CMD_COL_LOAD	Decouple with 100nF to VDD33	Bias
B2	VTREF	Test pin (decouple with 100nF to GND)	Analog input
B3	VREF_ADC	Reference for ADC (decouple with 100nF to GND)	Bias
B4	VDD18	1.8V supply	Supply
B5	GND	Ground pin	Ground
B6	OUT1_N	LVDS negative output channel 1	LVDS output
B7	OUT1_P	LVDS positive output channel 1	LVDS output
B8	OUT5_N	LVDS negative output channel 5	LVDS output
B9	OUT5_P	LVDS positive output channel 5	LVDS output
B10	OUT8_N	LVDS negative output channel 8	LVDS output
B11	OUT8_P	LVDS positive output channel 8	LVDS output
B12	OUT12_N	LVDS negative output channel 12	LVDS output
B13	OUT12_P	LVDS positive output channel 12	LVDS output
B14	OUT16_N	LVDS negative output channel 16	LVDS output
B15	OUT16_P	LVDS positive output channel 16	LVDS output
B16	OUT18_N	LVDS negative output channel 18	LVDS output
B17	OUT18_P	LVDS positive output channel 18	LVDS output
B18	OUT22_N	LVDS negative output channel 22	LVDS output
B19	OUT22_P	LVDS positive output channel 22	LVDS output
B20	OUT26_N	LVDS negative output channel 26	LVDS output
B21	OUT26_P	LVDS positive output channel 26	LVDS output

Pin number	Pin name	Description	Type
B22	GND	Ground pin	Ground
B24	OUT31_N	LVDS negative output channel 31	LVDS output
B25	OUT31_P	LVDS positive output channel 31	LVDS output
B26	GND	Ground pin	Ground
B27	GND	Ground pin	Ground
B28	GND	Ground pin	Ground
B29	CMD_RAMP	Decouple with 100nF to VDD33	Bias
B30	VTF_LOW2	Transfer low voltage 2 (decouple with 100nF to GND)	Bias
C1	CMD_LVDS	Decouple with 100nF to GND	Bias
C2	VTSIG	Test pin (decouple with 100nF to GND)	Analog input
C3	NC	Not connected	
C4	VPCH_H	Precharge high voltage (decouple with 100nF to GND)	Bias
C5	VTF_LOW0	Transfer low voltage 0 (decouple with 100nF to GND)	Bias
C6	CMD_COLAMP	Decouple with 100nF to VDD33	Bias
C7	OUT4_N	LVDS negative output channel 4	LVDS output
C8	OUT4_P	LVDS positive output channel 4	LVDS output
C9	OUT7_N	LVDS negative output channel 7	LVDS output
C10	OUT7_P	LVDS positive output channel 7	LVDS output
C11	OUT11_N	LVDS negative output channel 11	LVDS output
C12	OUT11_P	LVDS positive output channel 11	LVDS output
C13	OUT14_N	LVDS negative output channel 14	LVDS output
C14	OUT14_P	LVDS positive output channel 14	LVDS output
C15	GND	Ground pin	Ground
C16	GND	Ground pin	Ground
C17	OUT21_N	LVDS negative output channel 21	LVDS output
C18	OUT21_P	LVDS positive output channel 21	LVDS output
C19	OUT25_N	LVDS negative output channel 25	LVDS output
C20	OUT25_P	LVDS positive output channel 25	LVDS output
C21	OUT28_N	LVDS negative output channel 28	LVDS output
C22	OUT28_P	LVDS positive output channel 28	LVDS output
C24	OUT32_N	LVDS negative output channel 32	LVDS output
C25	OUT32_P	LVDS positive output channel 32	LVDS output
C26	VDD33	3.3V supply	Supply
C27	VDD33	3.3V supply	Supply
C28	GND	Ground pin	Ground
C29	VBGAP	Decouple with 100nF to GND	Bias
C30	VTF_LOW3	Transfer low voltage 3 (decouple with 100nF to GND)	Bias
D1	CMD_COL_PC	Decouple with 100nF to VDD33	Bias
D2	GND	Ground pin	Ground
D3	VDD33	3.3V supply	Supply
D4	VCLAMP	Decouple with 100nF to GND	Bias
D5	VRES_L	Reset low voltage (decouple with 100nF to GND)	Bias
D6	VTF_LOW1	Transfer low voltage 1 (decouple with 100nF to GND)	Bias
D7	OUT3_N	LVDS negative output channel 3	LVDS output
D8	OUT3_P	LVDS positive output channel 3	LVDS output
D9	OUT6_N	LVDS negative output channel 6	LVDS output
D10	OUT6_P	LVDS positive output channel 6	LVDS output
D11	OUT10_N	LVDS negative output channel 10	LVDS output
D12	OUT10_P	LVDS positive output channel 10	LVDS output
D13	OUT15_N	LVDS negative output channel 15	LVDS output
D14	OUT15_P	LVDS positive output channel 15	LVDS output
D15	OUT17_N	LVDS negative output channel 17	LVDS output
D16	OUT17_P	LVDS positive output channel 17	LVDS output
D17	OUT20_N	LVDS negative output channel 20	LVDS output

Pin number	Pin name	Description	Type
D18	OUT20_P	LVDS positive output channel 20	LVDS output
D19	OUT24_N	LVDS negative output channel 24	LVDS output
D20	OUT24_P	LVDS positive output channel 24	LVDS output
D21	OUT27_N	LVDS negative output channel 27	LVDS output
D22	OUT27_P	LVDS positive output channel 27	LVDS output
D23	OUT30_N	LVDS negative output channel 30	LVDS output
D24	OUT30_P	LVDS positive output channel 30	LVDS output
D25	GND	Ground pin	Ground
D26	VDD33	3.3V supply	Supply
D27	GND	Ground pin	Ground
D28	VDD_PIX	3.0V supply	Supply
D29	GND	Ground pin	Ground
D30	VDD_PIX	3.0V supply	Supply
E1	VDD18_PLL	1.8V supply	Supply
E2	VDD_RES	3.3V supply	Supply
E3	GND	Ground pin	Ground
E4	DIO2	Test pin (do not connect)	Analog output
E5	LVDS_CLK_N	LVDS input clock N	LVDS input
E6	LVDS_CLK_P	LVDS input clock P	LVDS input
E7	OUT35_N	LVDS negative output channel 35	LVDS output
E8	OUT35_P	LVDS positive output channel 35	LVDS output
E9	OUT38_N	LVDS negative output channel 38	LVDS output
E10	OUT38_P	LVDS positive output channel 38	LVDS output
E11	OUT42_N	LVDS negative output channel 42	LVDS output
E12	OUT42_P	LVDS positive output channel 42	LVDS output
E13	OUT46_N	LVDS negative output channel 46	LVDS output
E14	OUT46_P	LVDS positive output channel 46	LVDS output
E15	GND	Ground pin	Ground
E16	GND	Ground pin	Ground
E17	OUT51_N	LVDS negative output channel 51	LVDS output
E18	OUT51_P	LVDS positive output channel 51	LVDS output
E19	OUT55_N	LVDS negative output channel 55	LVDS output
E20	OUT55_P	LVDS positive output channel 55	LVDS output
E21	OUT59_N	LVDS negative output channel 59	LVDS output
E22	OUT59_P	LVDS positive output channel 59	LVDS output
E23	OUT62_N	LVDS negative output channel 62	LVDS output
E24	OUT62_P	LVDS positive output channel 62	LVDS output
E25	GND	Ground pin	Ground
E26	VDD33	3.3V supply	Supply
E27	GND	Ground pin	Ground
E28	SPI_IN	SPI data input pin	Digital input
E29	T_EXP2	Input pin for external exposure	Digital input
E30	CLK_IN	Master input clock	Digital input
F1	CMDN	Decouple with 100nF to GND	Bias
F2	CMDP	Decouple with 100nF to VDD33	Bias
F3	CMDP_COMP_INV	Decouple with 100nF to VDD33	Bias
F4	DIO1	Test pin (do not connect)	Analog output
F5	VDD33	3.3V supply	Supply
F6	OUT33_N	LVDS negative output channel 33	LVDS output
F7	OUT33_P	LVDS positive output channel 33	LVDS output
F8	OUT37_N	LVDS negative output channel 37	LVDS output
F9	OUT37_P	LVDS positive output channel 37	LVDS output
F10	OUT40_N	LVDS negative output channel 40	LVDS output
F11	OUT40_P	LVDS positive output channel 40	LVDS output

Pin number	Pin name	Description	Type
F12	OUT44_N	LVDS negative output channel 44	LVDS output
F13	OUT44_P	LVDS positive output channel 44	LVDS output
F14	OUT48_N	LVDS negative output channel 48	LVDS output
F15	OUT48_P	LVDS positive output channel 48	LVDS output
F16	OUT49_N	LVDS negative output channel 49	LVDS output
F17	OUT49_P	LVDS positive output channel 49	LVDS output
F18	OUT53_N	LVDS negative output channel 53	LVDS output
F19	OUT53_P	LVDS positive output channel 53	LVDS output
F20	OUT57_N	LVDS negative output channel 57	LVDS output
F21	OUT57_P	LVDS positive output channel 57	LVDS output
F22	OUT60_N	LVDS negative output channel 60	LVDS output
F23	OUT60_P	LVDS positive output channel 60	LVDS output
F24	NC	Not connected	
F25	NC	Not connected	
F26	VDD33	3.3V supply	Supply
F27	GND	Ground pin	Ground
F28	SPI_EN	SPI enable input pin	Digital input
F29	VRAMP2	Start voltage second ramp (decouple with 100nF to GND)	Bias
F30	SYS_RES_N	Input pin for sequencer reset	Digital input
G1	VDD_PIX	3.0V supply	Supply
G2	VCLAMP_ADC	Decouple with 100nF to GND	Bias
G3	DIO4	Test pin (do not connect)	Analog output
G4	VDD_RES	3.3V supply	Supply
G5	GND	Ground pin	Ground
G6	OUTCLK_N	LVDS negative clock output signal	LVDS output
G7	OUTCLK_P	LVDS positive clock output signal	LVDS output
G8	OUT36_N	LVDS negative output channel 36	LVDS output
G9	OUT36_P	LVDS positive output channel 36	LVDS output
G10	OUT39_N	LVDS negative output channel 39	LVDS output
G11	OUT39_P	LVDS positive output channel 39	LVDS output
G12	OUT43_N	LVDS negative output channel 43	LVDS output
G13	OUT43_P	LVDS positive output channel 43	LVDS output
G14	OUT47_N	LVDS negative output channel 47	LVDS output
G15	OUT47_P	LVDS positive output channel 47	LVDS output
G16	OUT50_N	LVDS negative output channel 50	LVDS output
G17	OUT50_P	LVDS positive output channel 50	LVDS output
G18	OUT54_N	LVDS negative output channel 54	LVDS output
G19	OUT54_P	LVDS positive output channel 54	LVDS output
G20	OUT58_N	LVDS negative output channel 58	LVDS output
G21	OUT58_P	LVDS positive output channel 58	LVDS output
G22	OUT61_N	LVDS negative output channel 61	LVDS output
G23	OUT61_P	LVDS positive output channel 61	LVDS output
G24	OUT64_N	LVDS negative output channel 64	LVDS output
G25	OUT64_P	LVDS positive output channel 64	LVDS output
G26	TDIG2	Test pin for digital sequencer signals (do not connect)	Digital output
G27	TDIG1	Test pin for digital sequencer signals (do not connect)	Digital output
G28	SPI_OUT	SPI data output pin	Digital output
G29	VRAMP1	Start voltage first ramp (decouple with 100nF to GND)	Bias
G30	FRAME_REQ	Frame request pin	Digital input
H1	GND	Ground pin	Ground
H2	NC	Not connected	
H3	CMDP_COMP	Decouple with 100nF to VDD33	Bias
H4	DIO3	Test pin (do not connect)	Analog output
H5	VDD18	1.8V supply	Supply

Pin number	Pin name	Description	Type
H6	GND	Ground pin	Ground
H7	OUT34_N	LVDS negative output channel 34	LVDS output
H8	OUT34_P	LVDS positive output channel 34	LVDS output
H9	GND	Ground pin	Ground
H10	VDD18	1.8V supply	Supply
H11	OUT41_N	LVDS negative output channel 41	LVDS output
H12	OUT41_P	LVDS positive output channel 41	LVDS output
H13	OUT45_N	LVDS negative output channel 45	LVDS output
H14	OUT45_P	LVDS positive output channel 45	LVDS output
H15	VDD18	1.8V supply	Supply
H16	VDD18	1.8V supply	Supply
H17	OUT52_N	LVDS negative output channel 52	LVDS output
H18	OUT52_P	LVDS positive output channel 52	LVDS output
H19	OUT56_N	LVDS negative output channel 56	LVDS output
H20	OUT56_P	LVDS positive output channel 56	LVDS output
H21	GND	Ground pin	Ground
H22	VDD18	1.8V supply	Supply
H23	OUT63_N	LVDS negative output channel 63	LVDS output
H24	OUT63_P	LVDS positive output channel 63	LVDS output
H25	GND	Ground pin	Ground
H26	VDD18	1.8V supply	Supply
H27	GND	Ground pin	Ground
H28	VDD_PIX	3.0V supply	Supply
H29	SPI_CLK	SPI clock input pin	Digital input
H30	T_EXP1	Input pin for external exposure	Digital input

10 SPECIFICATION OVERVIEW

Specification	Value	Comment
Effective pixels	4096 x 3072	
Pixel pitch	5.5 x 5.5 μm^2	
Optical format	22.5 x 16.9	mm
Full well charge	13.5 Ke-	Pinned photodiode pixel
Conversion gain	0.075 LSB/e-	10-bit mode
Sensitivity	4.64 V/lux.s 0.22 A/W	With micro lenses
Temporal noise (analog domain)	13 e-	Pipelined global shutter (GS) with correlated double sampling (CDS)
Dynamic range	60 dB	
Pixel type	Global shutter pixel	Allows fixed pattern noise correction and reset (kTC) noise canceling through correlated double sampling
Shutter type	Pipelined global shutter	Exposure of next image during read-out of the previous image
Parasitic light sensitivity - Shutter efficiency	1/50 000	
Color filters	Optional	RGB Bayer pattern
Micro lenses	Yes	
QE * FF	50%	@ 550 nm
Dark current signal	22 LSB/s	@ room temperature, 10-bit mode
DSNU	2 LSB/s	10-bit mode
Fixed pattern noise	<1 LSB	<0.1% of full swing in 10-bit mode
PRNU	<1.27%	RMS
LVDS output channels	64	Each data output running @ 300 Mbit/s. 32, 16, 8, 4, 2 and 1 output(s) selectable at reduced frame rate.
Frame rate	150 frames/s	Using a 10bit/pixel and 300 Mbit/s LVDS. Higher frame rate possible in row windowing mode or subsampling mode.
Timing generation	On-chip	Possibility to control exposure time through external pin
PGA	Yes	4 analog gain settings
Programmable Registers	Sensor parameters	Window coordinates, timing parameters, gain & offset, exposure time, flipped read-out in x and y direction …
Supported HDR modes	Interleaved integration times Multi slope	Interleaved exposure times for different columns: odd columns (double columns for color) have a different exposure compared to even columns (double columns for color). Final image is a combination of the two (through interpolation). Multiple slopes with partial reset of the pixel.
ADC	8bit/10bit/12bit	Column ADC
Interface	LVDS	Serial output data + synchronization signals
I/O logic levels	LVDS = 1.8V Logic levels = 3.3V	
Supply voltages	1.8V & 3.3V	3.3V for the pixel array and analog circuits 1.8V for digital circuits and the LVDS drivers

Specification	Value	Comment
Clock inputs	300 MHz	DDR input clock
Power	3000 mW	
Package	Ceramic package	Custom ceramic uPGA (237 pins)
Operating range	-30°C to +70°C	Dark current and noise performance will degrade at higher temperature
Cover glass	D263	Plain glass

11 ORDERING INFO

Part Number	**Epi Thickness**	**Chroma**	**Microlens**	**Package**	**Glass**
CMV12000-1E5M1PA	5 µm	mono	yes	ceramic 237p µPGA	AR coated
CMV12000-1E5C1PA	5 µm	RGB Bayer	yes	ceramic 237p µPGA	AR coated

On request the package and cover glass can be customized. For options, pricing and delivery time please contact info@cmosis.com.

12 HANDLING AND SOLDERING PROCEDURE

12.1 SOLDERING

12.1.1 MANUAL SOLDERING

Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350°C with 270°C maximum pin temperature, 2 seconds maximum duration per pin. Avoid global heating of the ceramic package during soldering. Failure to do so may alter device performance and reliability.

12.1.2 WAVE SOLDERING

Wave soldering is possible but not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. See the figure below for the wave soldering profile.

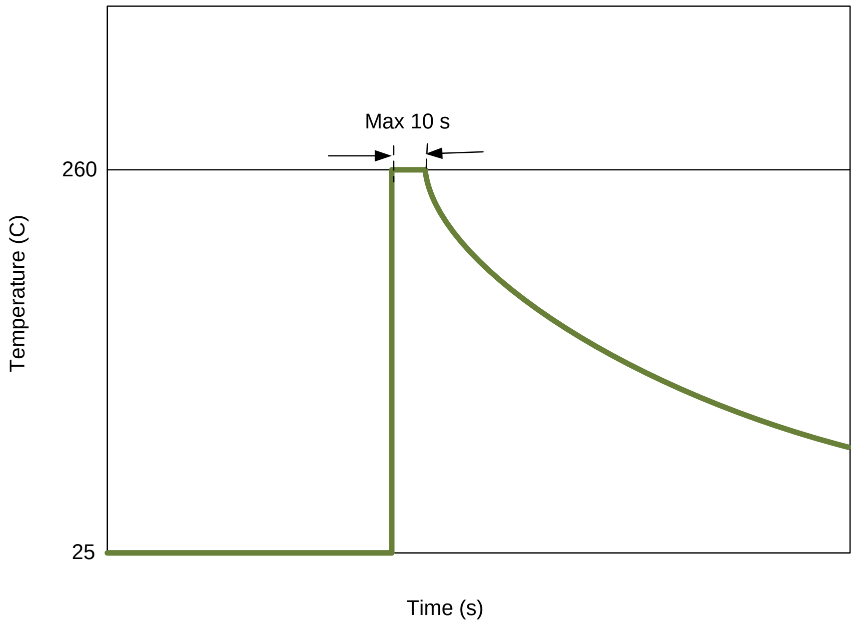


FIGURE 61: WAVE SOLDERING PROFILE

12.1.3 REFLOW SOLDERING

The figure below shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.

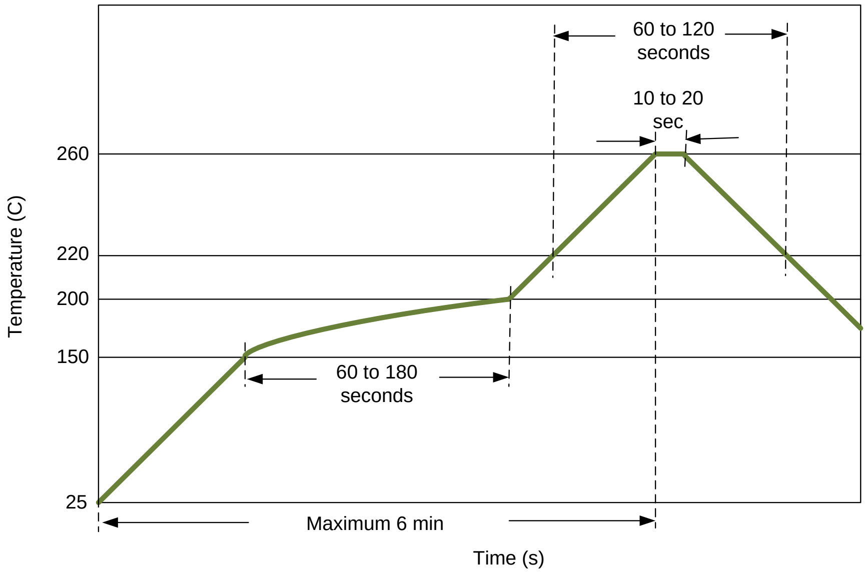


FIGURE 62: REFLOW SOLDERING

12.1.4 Soldering recommendations

Image sensors with color filter arrays (CFA) and micro lenses are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. Best solution will be flow soldering or manual soldering of a socket (through hole or BGA) and plug in the sensor at latest stage of the assembly/test process. The BGA solution allows more flexibility for the routing of the camera PCB.

12.2 Handling image sensors

12.2.1 ESD

The following are the recommended minimum ESD requirements when handling image sensors:

1. Ground workspace (tables, floors…)
2. Ground handling personnel (wrist straps, special footwear…)
3. Minimize static charging (control humidity, use ionized air, wear gloves…)

12.2.2 Glass cleaning

When cleaning of the cover glass is needed we recommend the following two methods:

1. Blowing off the particles with ionized nitrogen
2. Wipe clean using IPA (isopropyl alcohol) and ESD protective wipes

12.2.3 Image sensor storing

Image sensors should be stored under the following conditions:

1. Dust free
2. Temperature 20°C to 40°C
3. Humidity between 30% and 60%.
4. Avoid radiation, electromagnetic fields, ESD, mechanical stress

13 ADDITIONAL INFORMATION

For any additional questions related to the operation and specification of the CMV12000 imagers or feedback with respect to the present datasheet please contact techsupport@cmosis.com.