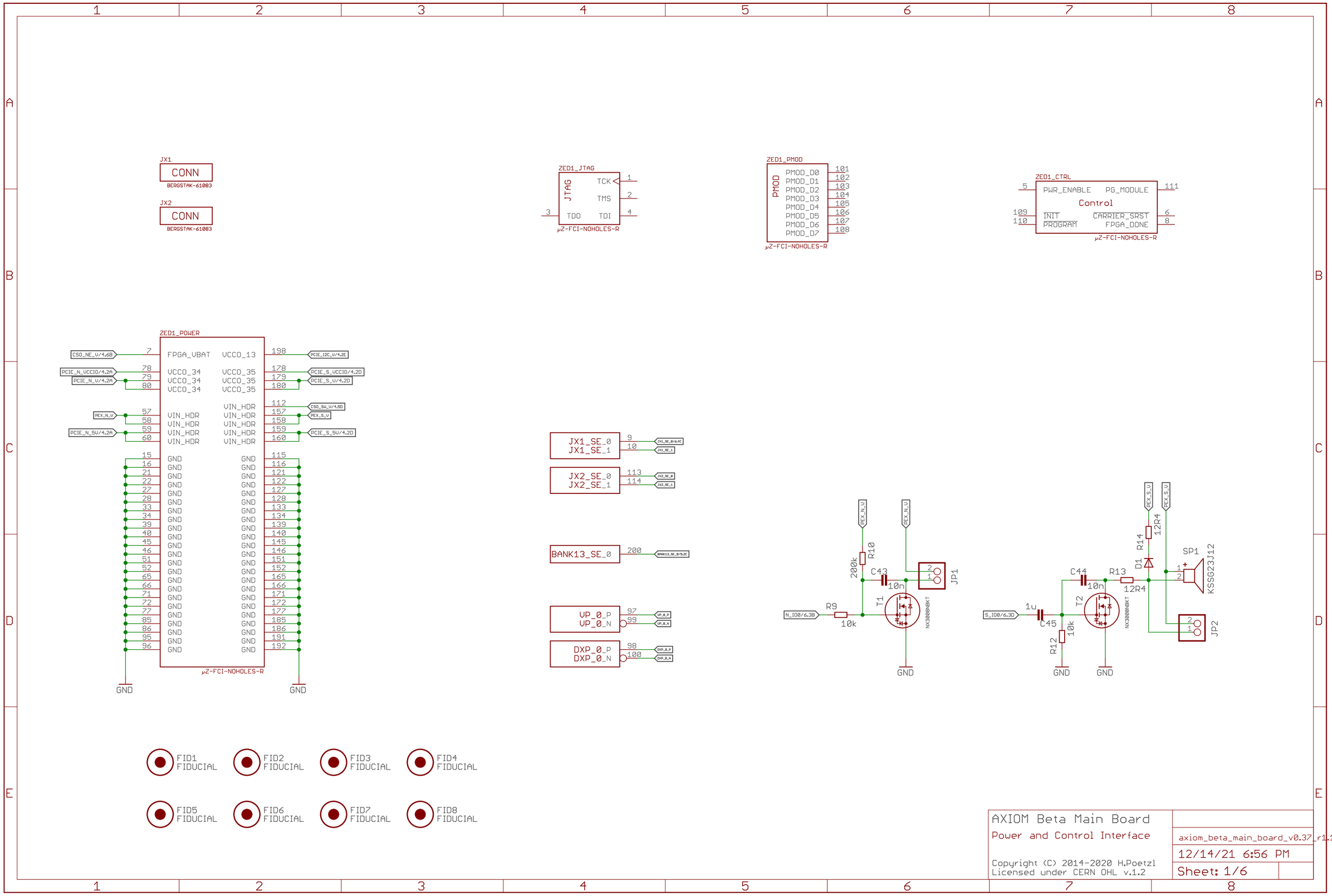


AXIOM Beta Main Board

Power and Control Interface

axiom_beta_main_board_v0.37_r1.1

12/14/21 6:56 PM

Sheet: 1/6

Copyright (C) 2014-2020 H.Poetzl
Licensed under CERN OHL v.1.2

AXIOM Beta Main Board

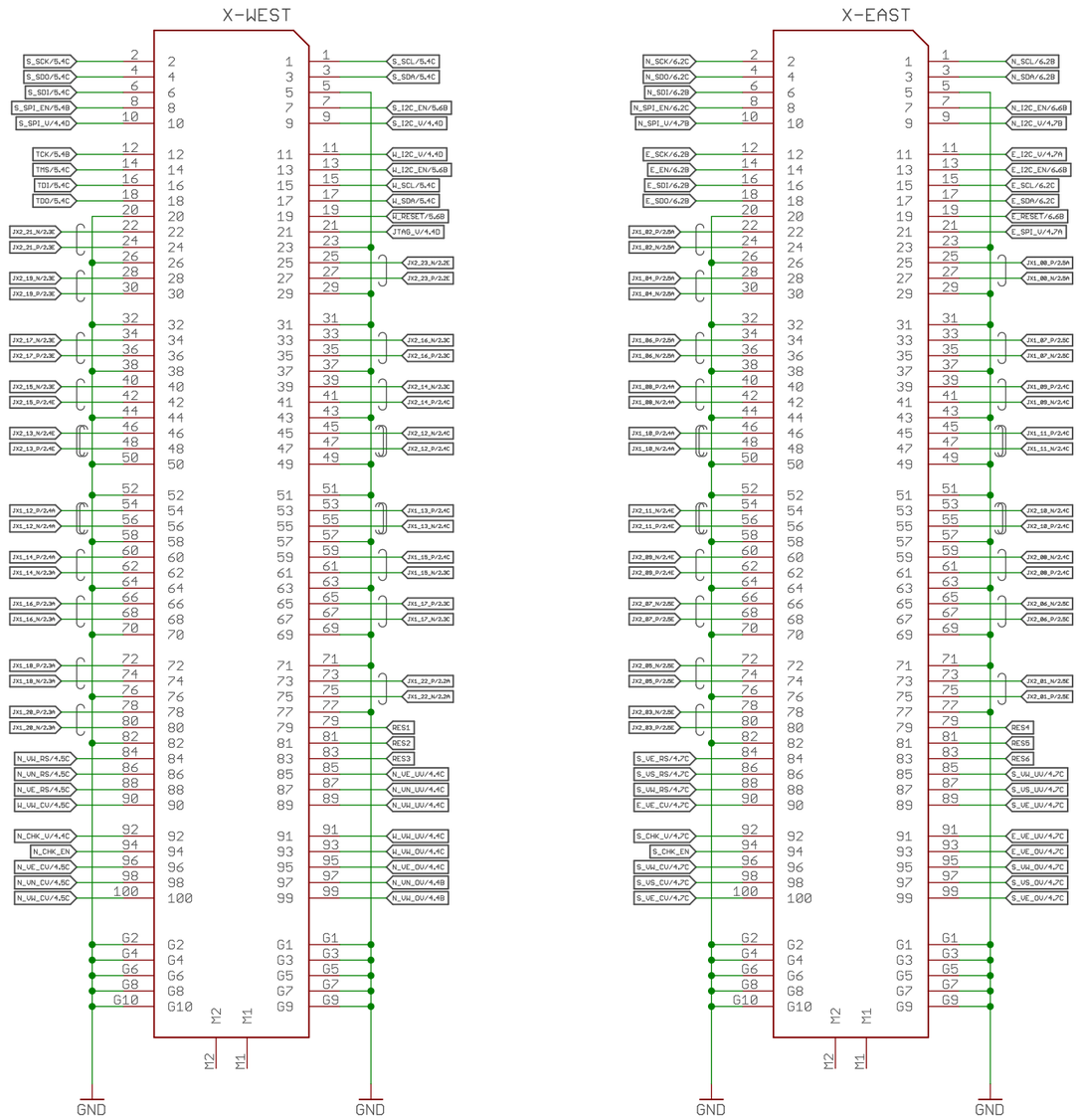
ZYNQ LVDS Interface

axiom_beta_main_board_v0.37_r1.1

12/14/21 6:56 PM

Sheet: 2/6

Copyright (C) 2014-2020 H.Poetzl
Licensed under CERN OHL v.1.2



AXIOM Beta Main Board

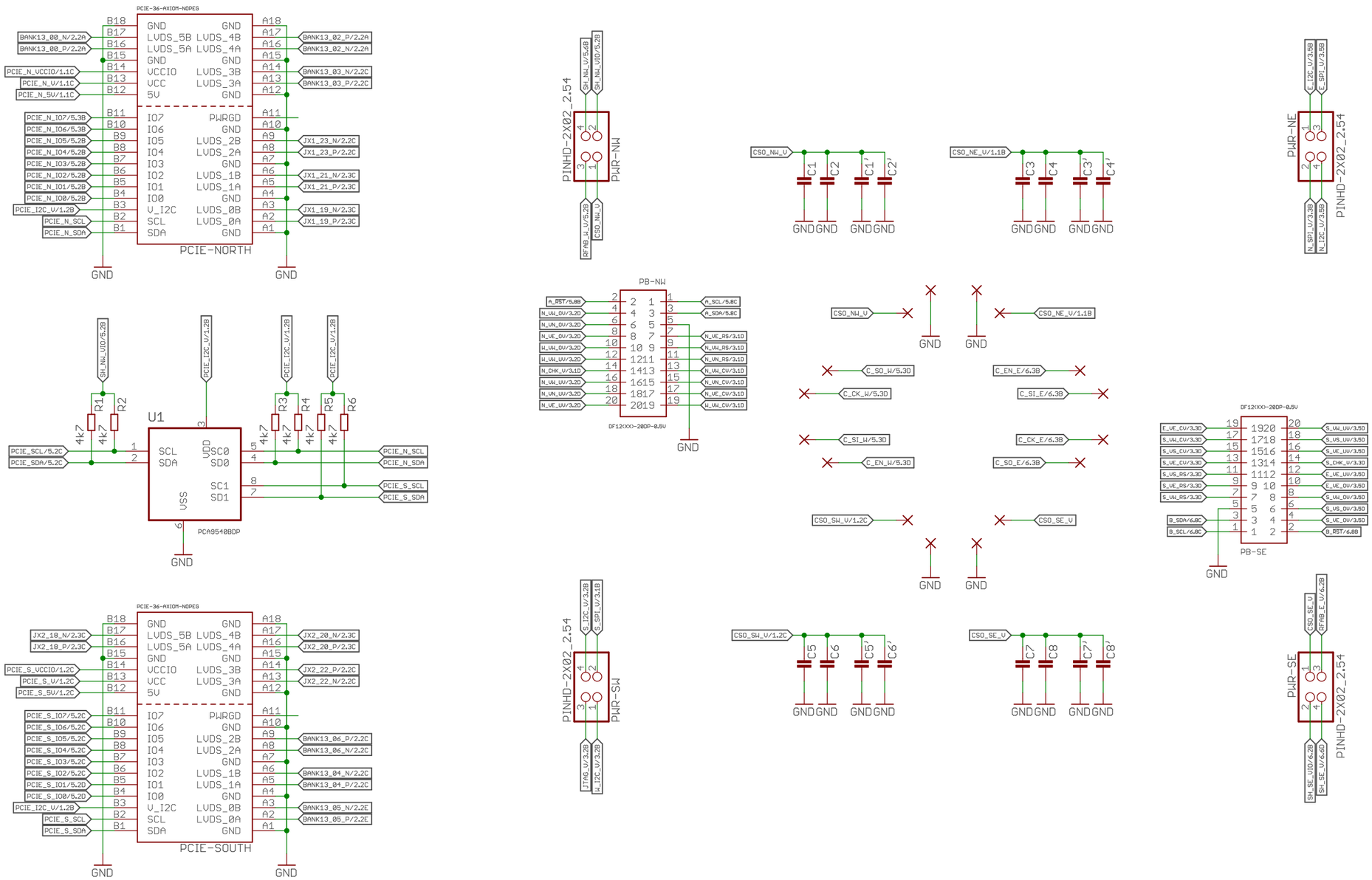
Interface Board Connection

axiom_beta_main_board_v0.37_r1.1

12/14/21 6:56 PM

Copyright (C) 2014-2020 H.Poetzl
Licensed under CERN OHL v.1.2

Sheet: 3/6



AXIOM Beta Main Board

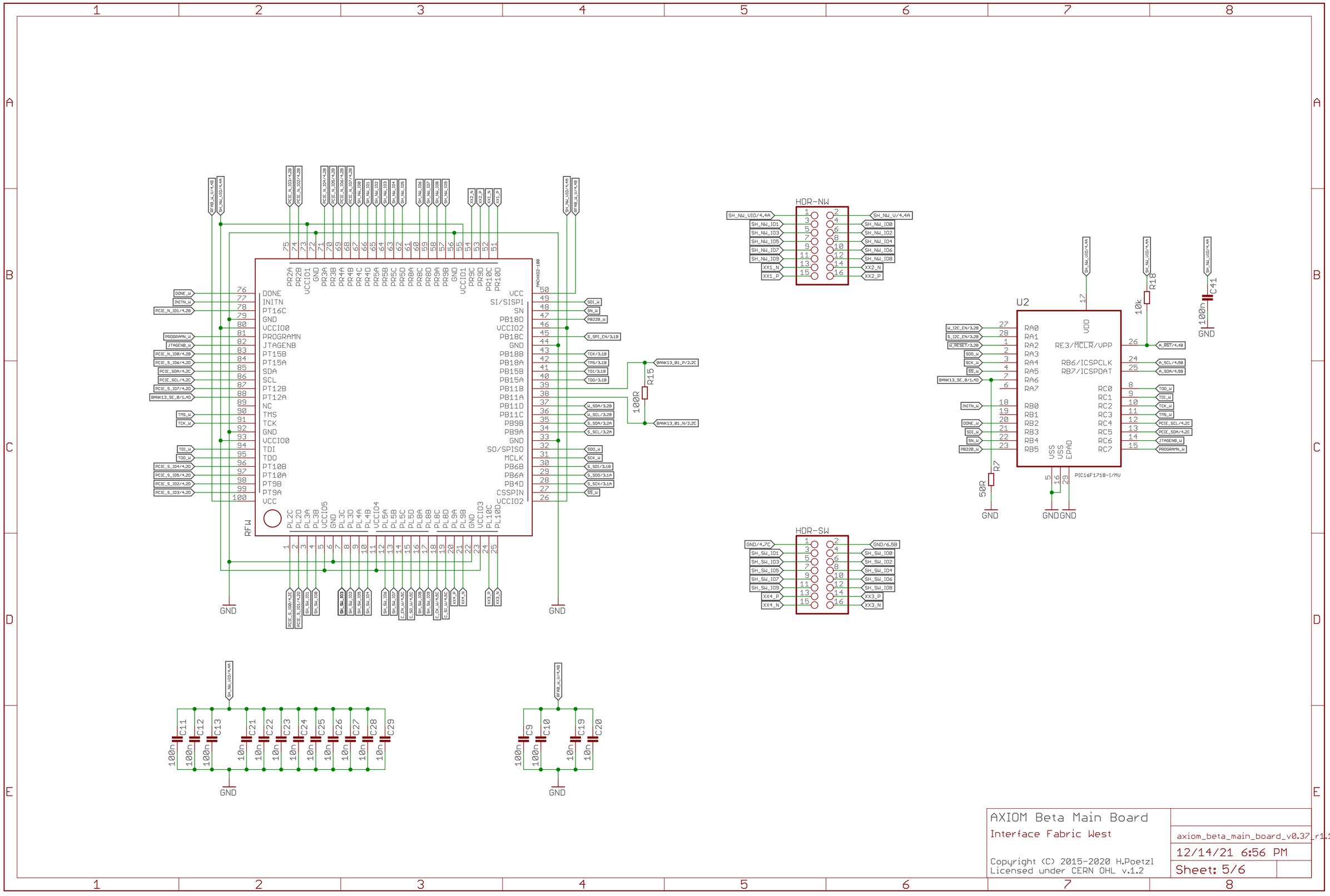
PCIE, Power, Center Area

Copyright (C) 2015-2020 H.Poetzl
Licensed under CERN OHL v.1.2

axiom_beta_main_board_v0.37_r1.1

12/14/21 6:56 PM

Sheet: 4/6



AXIOM Beta Main Board

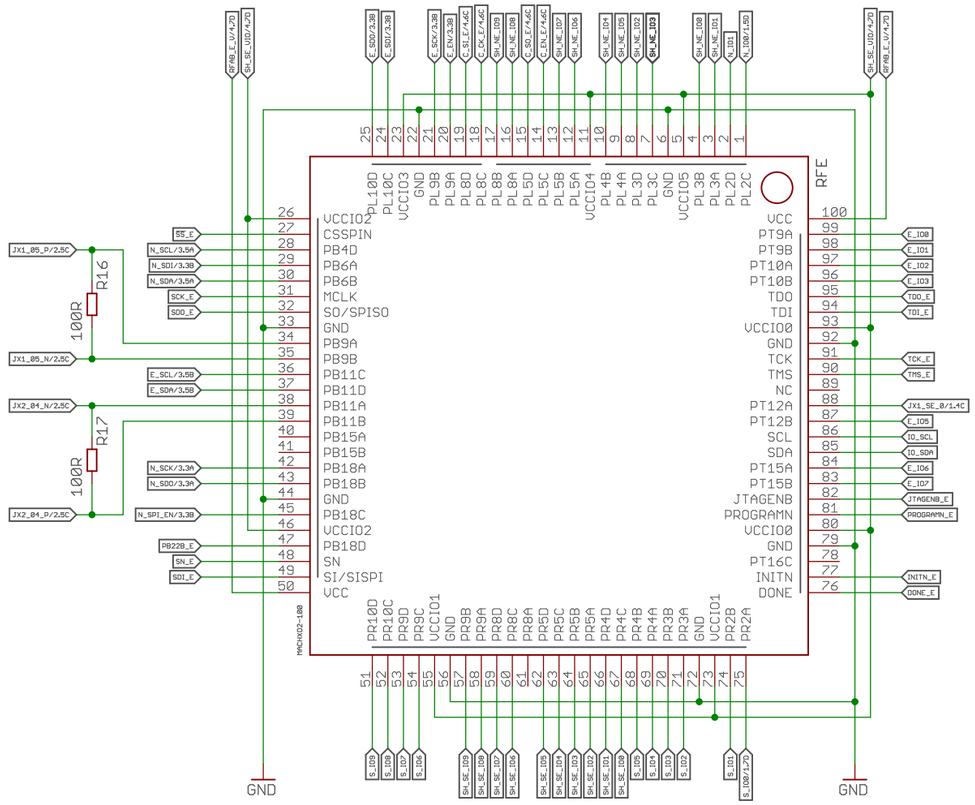
Interface Fabric West

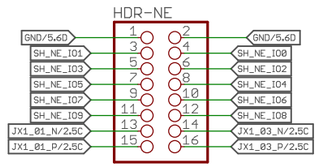
axiom_beta_main_board_v0.37_r1.1

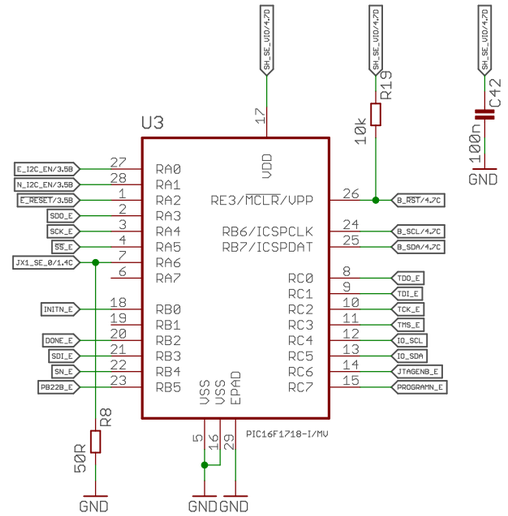
12/14/21 6:56 PM

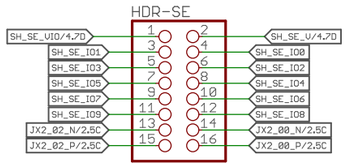
Sheet: 5/6

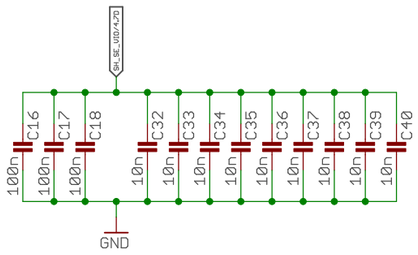
Copyright (C) 2015-2020 H.Poetzl
Licensed under CERN OHL v.1.2

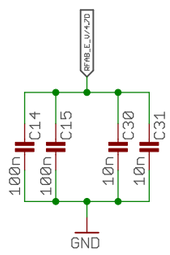












AXIOM Beta Main Board

Interface Fabric East

axiom_beta_main_board_v0.37_r1.1

12/14/21 6:56 PM

Sheet: 6/6

Copyright (C) 2015-2020 H.Poetzl
Licensed under CERN OHL v.1.2