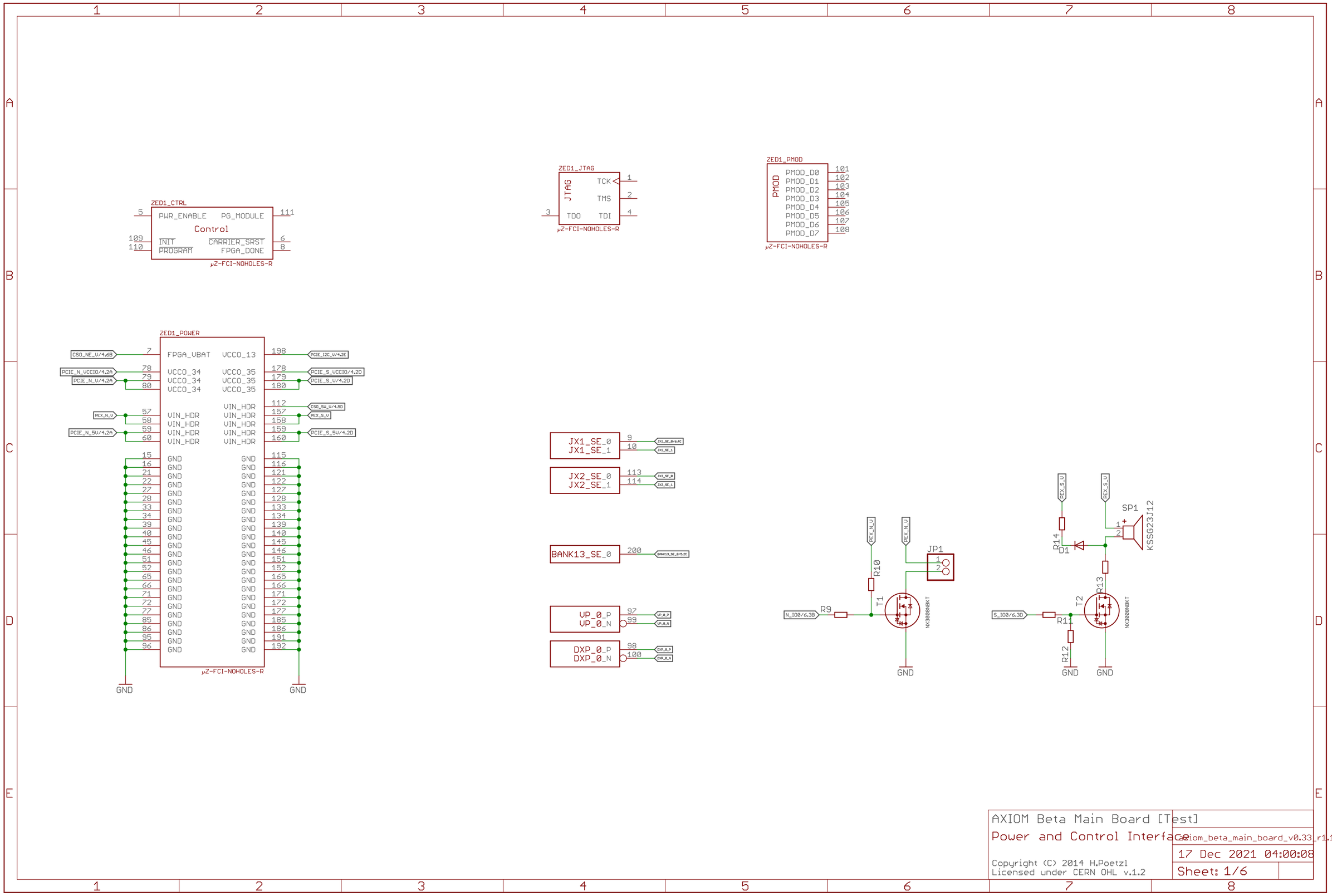
ZED1_CTRL
PWR_ENABLE
PG_MODULE
Control
INIT
CARRIER_SRST
PROGRAM
FPGA_DONE
μZ-FCI-NOHOLES-R
ZED1_JTAG
JTAG
TCK
TMS
TDO
TDI
μZ-FCI-NOHOLES-R
ZED1_PMOD
PMOD
PMOD_D0
PMOD_D1
PMOD_D2
PMOD_D3
PMOD_D4
PMOD_D5
PMOD_D6
PMOD_D7
μZ-FCI-NOHOLES-R
ZED1_POWER
FPGA_VBAT
VCCO_13
VCCO_34
VCCO_35
VIN_HDR
GND
μZ-FCI-NOHOLES-R
CS0_NE_U/4.6B
PCIE_N_VCCIO/4.2A
PCIE_N_U/4.2A
PEX_N_U
PCIE_N_5U/4.2A
PCIE_I2C_U/4.2E
PCIE_S_VCCIO/4.2D
PCIE_S_U/4.2D
CS0_SH_U/4.5D
PEX_S_U
PCIE_S_5U/4.2D
JX1_SE_0
JX1_SE_1
JX2_SE_0
JX2_SE_1
BANK13_SE_0
VP_0_P
VP_0_N
DXP_0_P
DXP_0_N
PEX_N_U
JP1
R10
R9
T1
NX3008NBKT
N_IO0/6.3B
PEX_S_U
SP1
KSSG23J12
R14
D1
R13
T2
R11
R12
S_IO0/6.3D
GND
AXIOM Beta Main Board [Test]
Power and Control Interface
axiom_beta_main_board_v0.33_r1.1
17 Dec 2021 04:00:08
Sheet: 1/6
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AXIOM Beta Main Board [Test]

ZYNQ LVDS Interface

axiom_beta_main_board_v0.33_r1.1

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Sheet: 2/6

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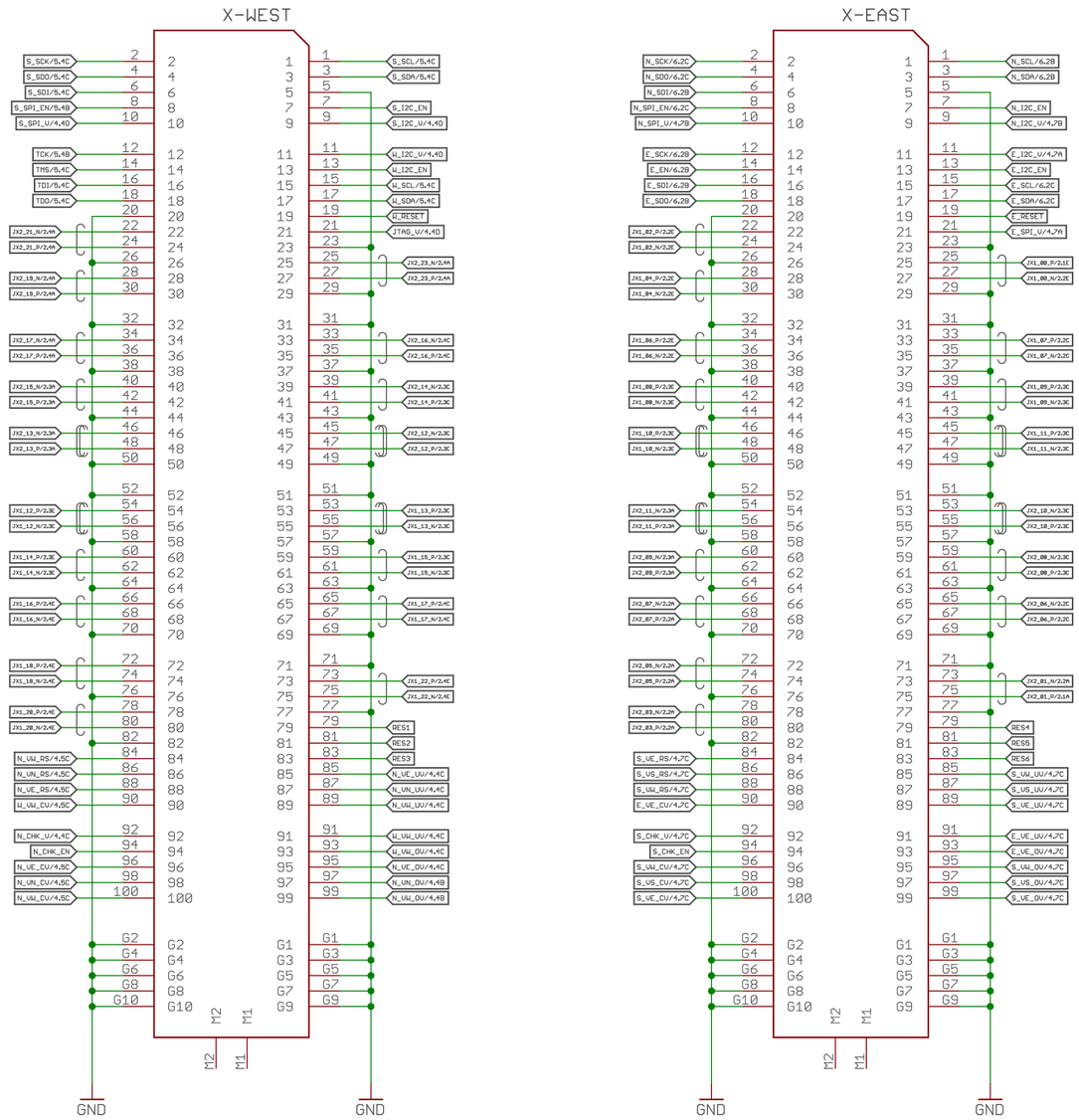

AXIOM Beta Main Board [Test]

Interface Board Connection

axiom_beta_main_board_v0.33_r1.1

17 Dec 2021 04:00:08

Sheet: 3/6

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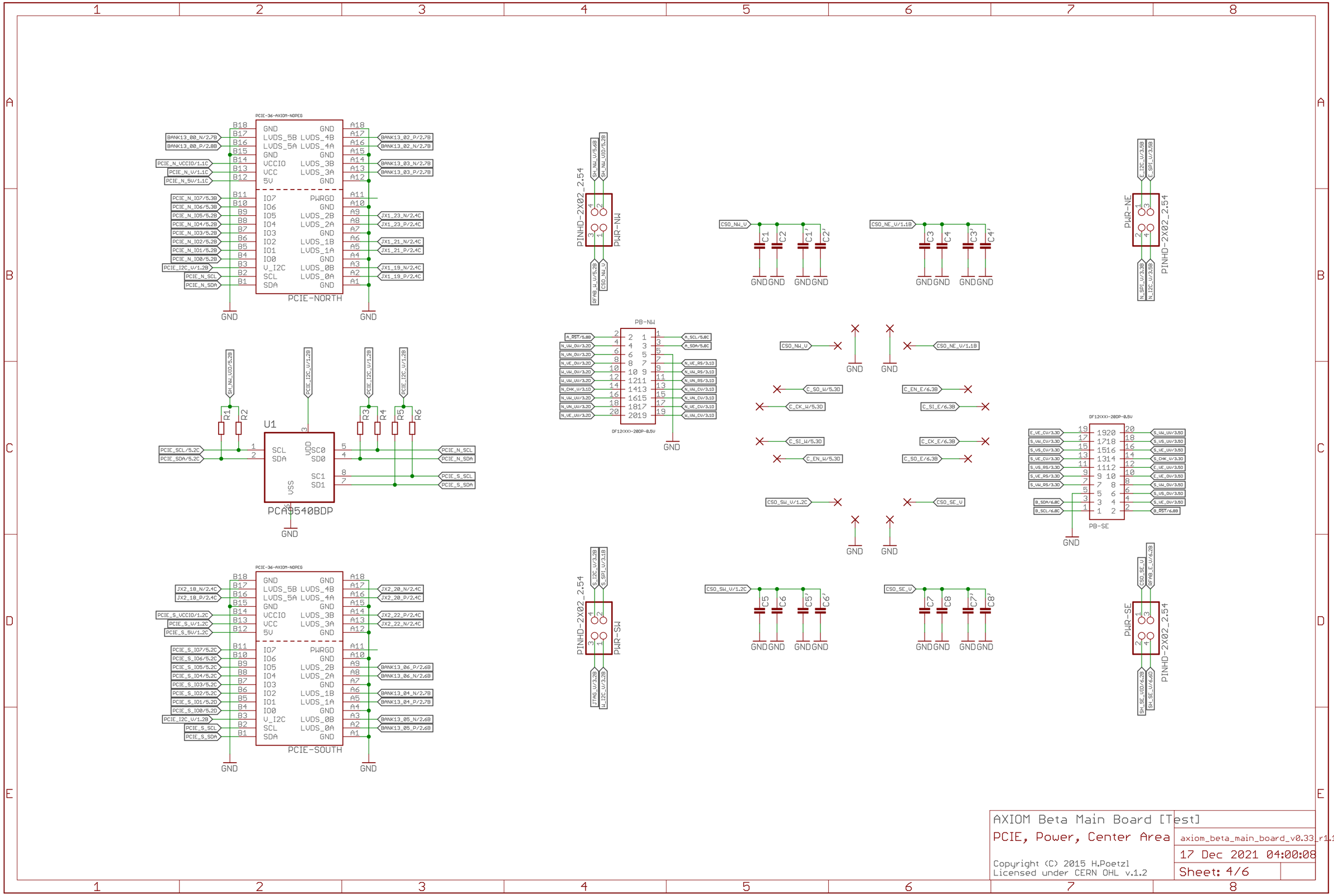

AXIOM Beta Main Board [Test]

PCIE, Power, Center Area

axiom_beta_main_board_v0.33_r1.1

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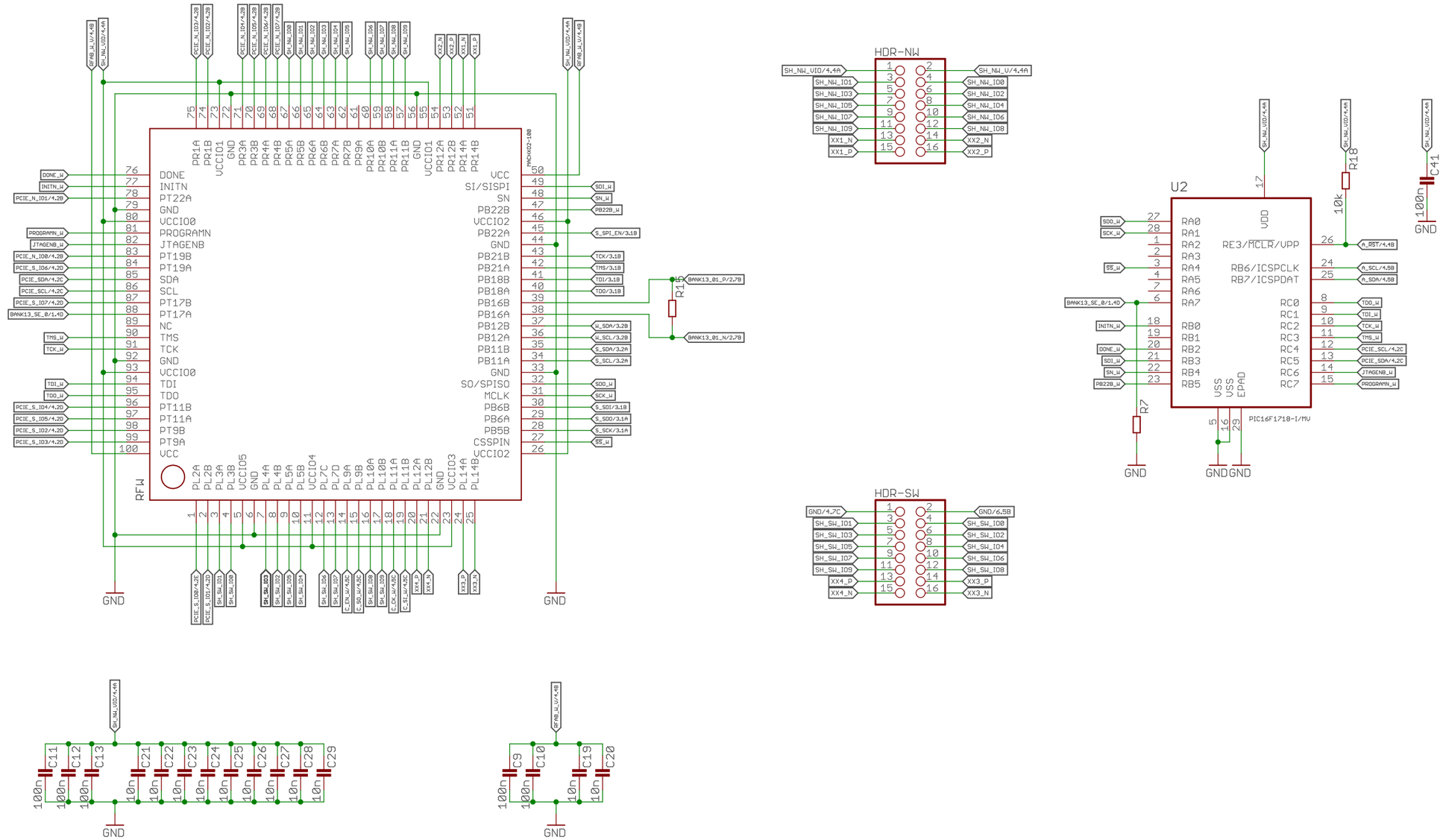

AXIOM Beta Main Board [Test]

Interface Fabric West

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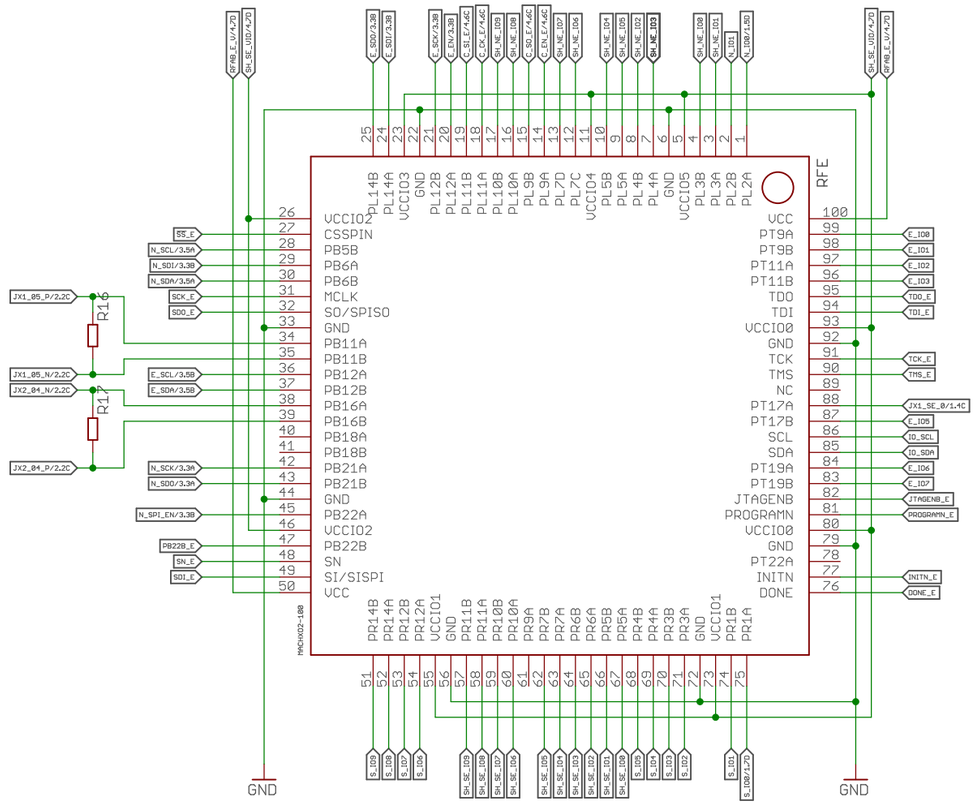
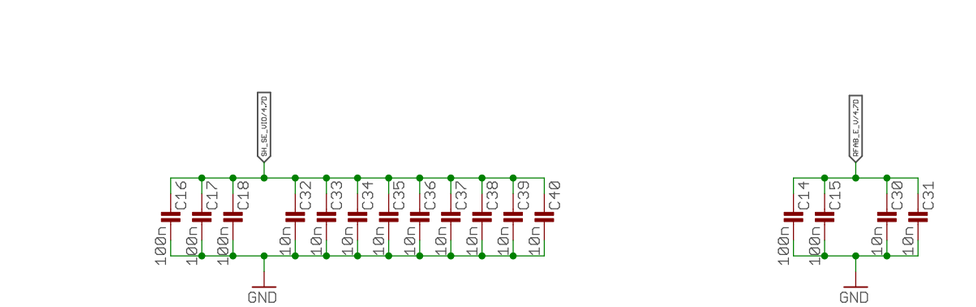
Sheet:





AXIOM Beta Main Board [Test]

Interface Fabric East

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