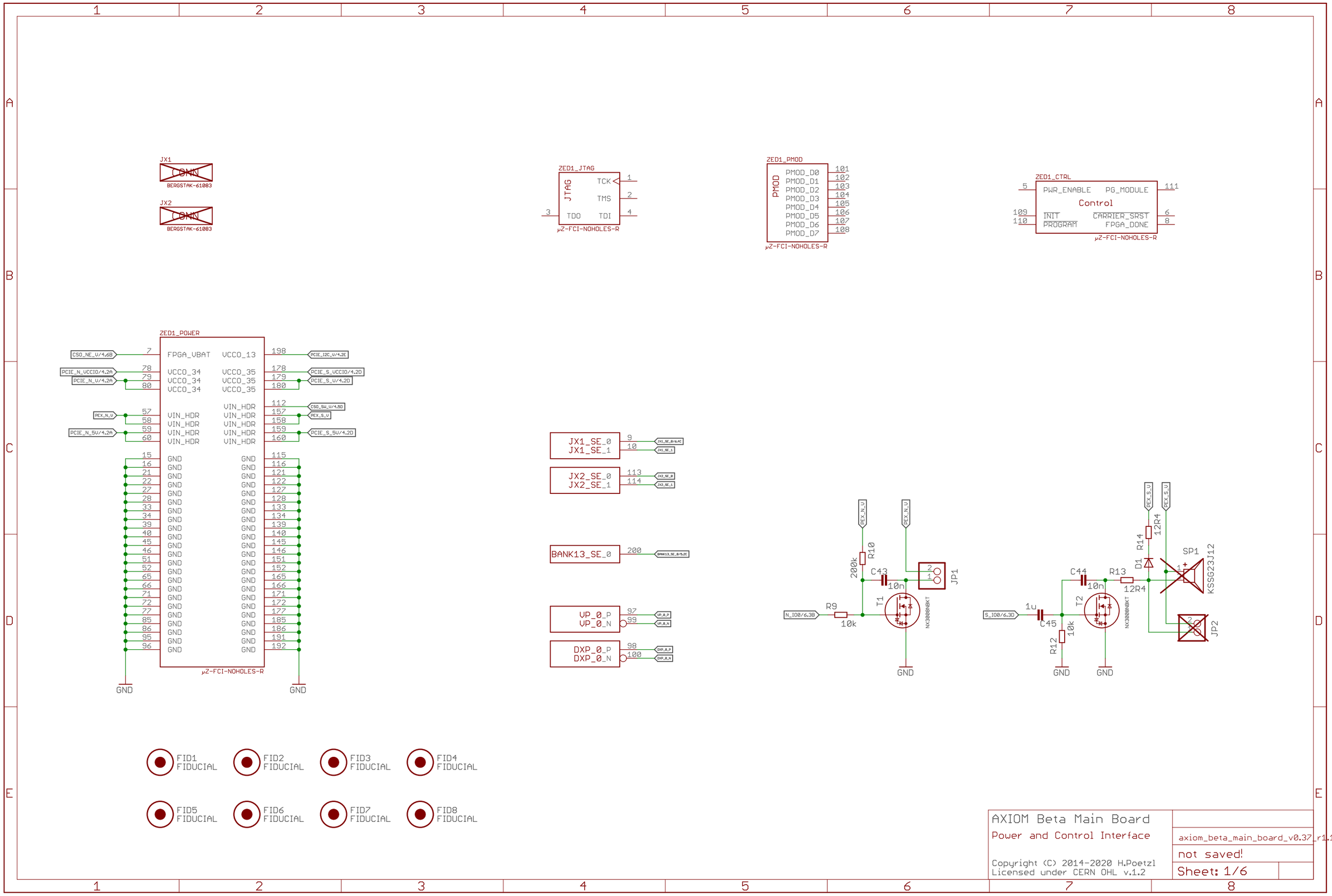

AXIOM Beta Main Board

Power and Control Interface

axiom_beta_main_board_v0.37_r1.1

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AXIOM Beta Main Board

ZYNQ LVDS Interface

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not saved!

Sheet: 2/6

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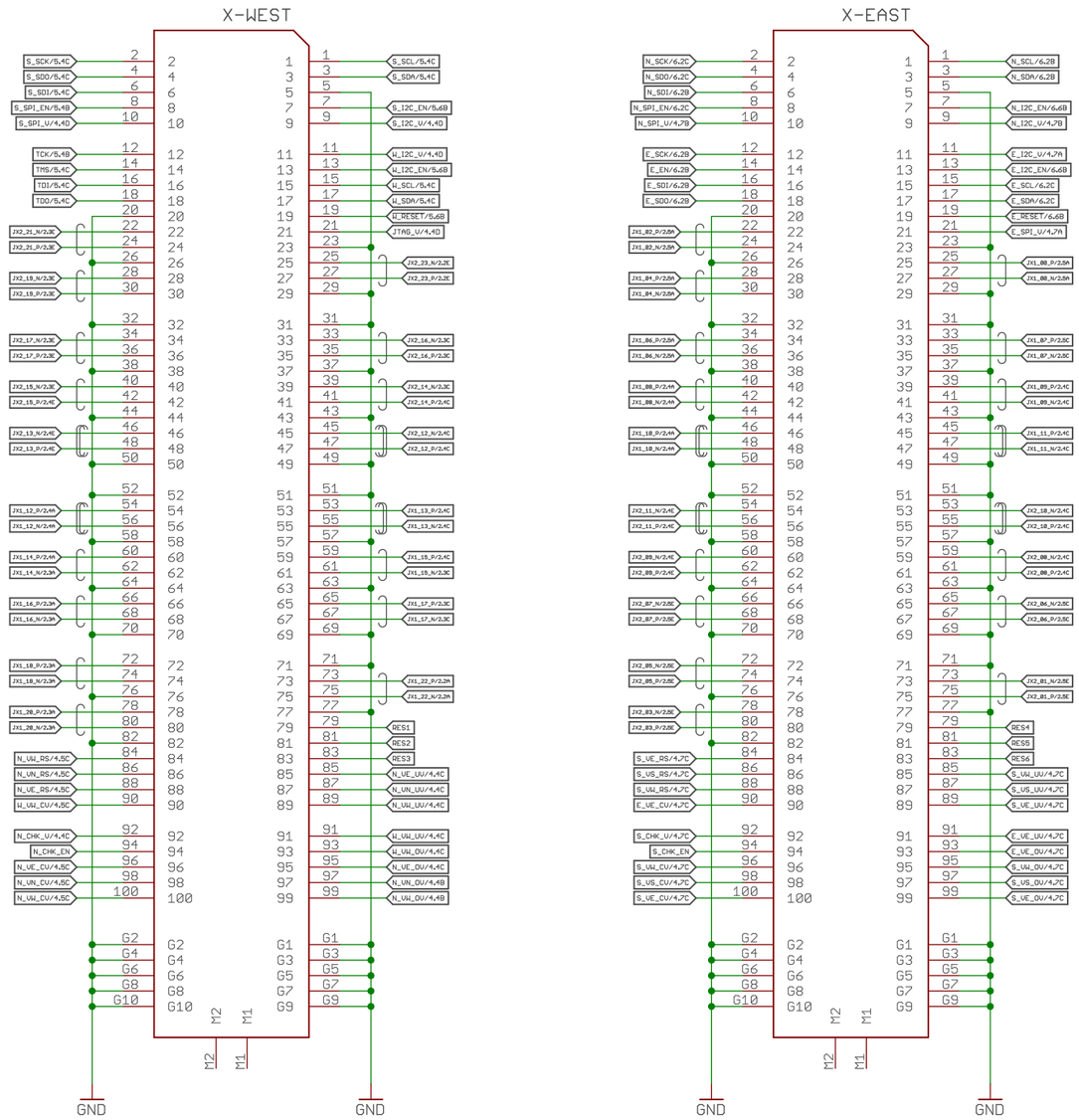

AXIOM Beta Main Board

Interface Board Connection

axiom_beta_main_board_v0.37_r1.1

not saved!

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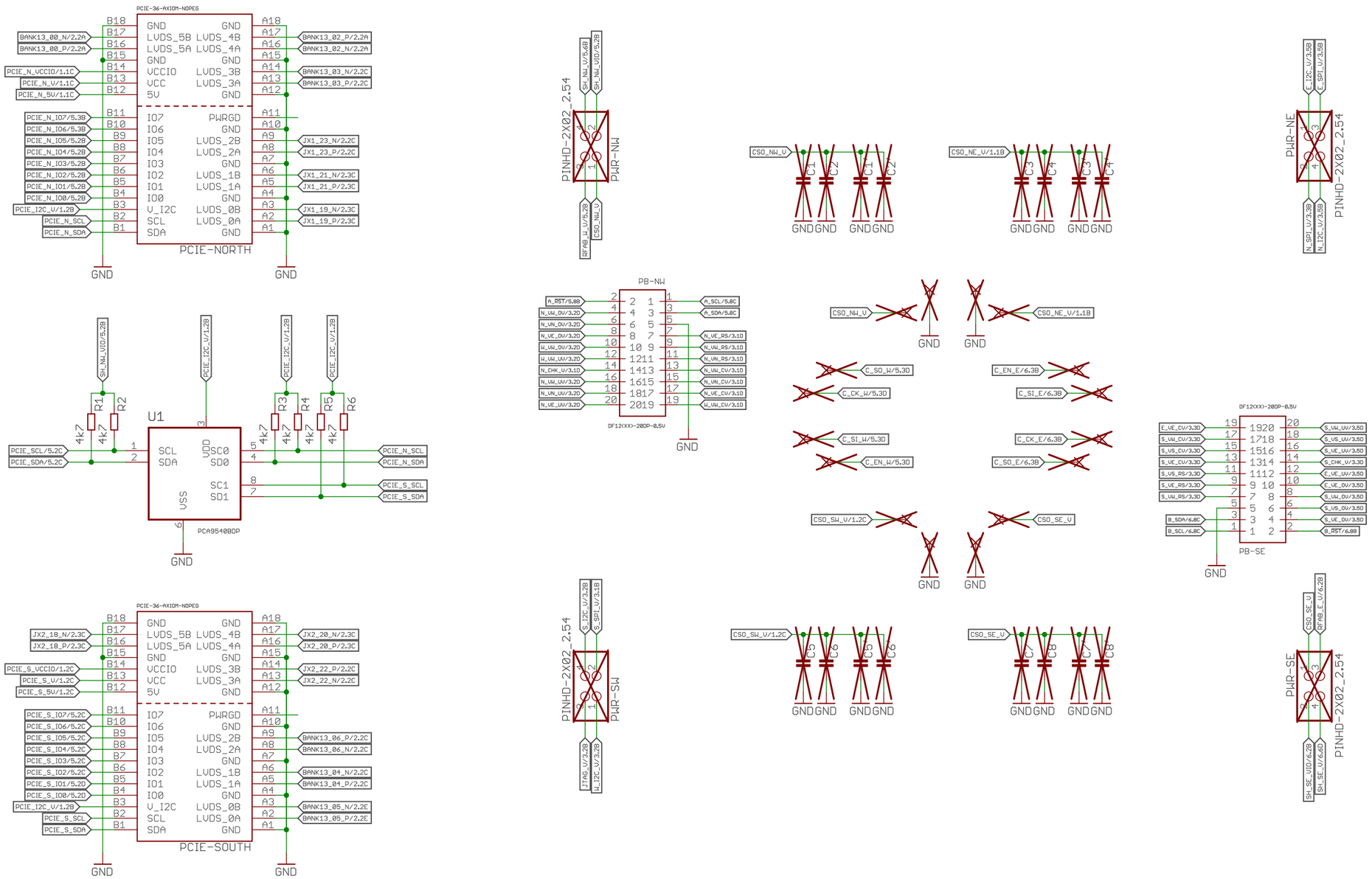
Sheet: 3/6



AXIOM Beta Main Board

PCIE, Power, Center Area

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not saved!

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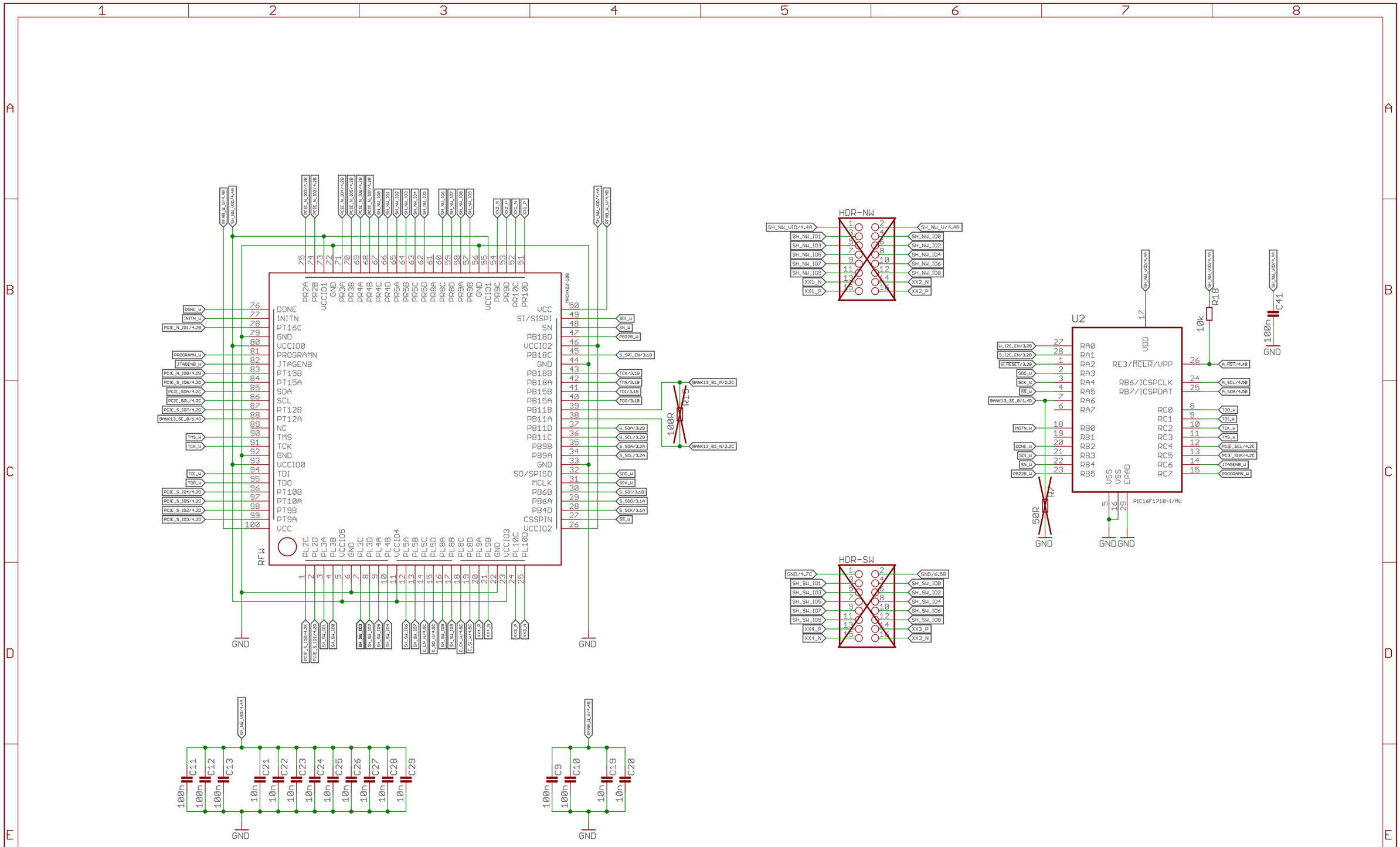

AXIOM Beta Main Board

Interface Fabric West

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axiom_beta_main_board_v0.37_r1.1

not saved!

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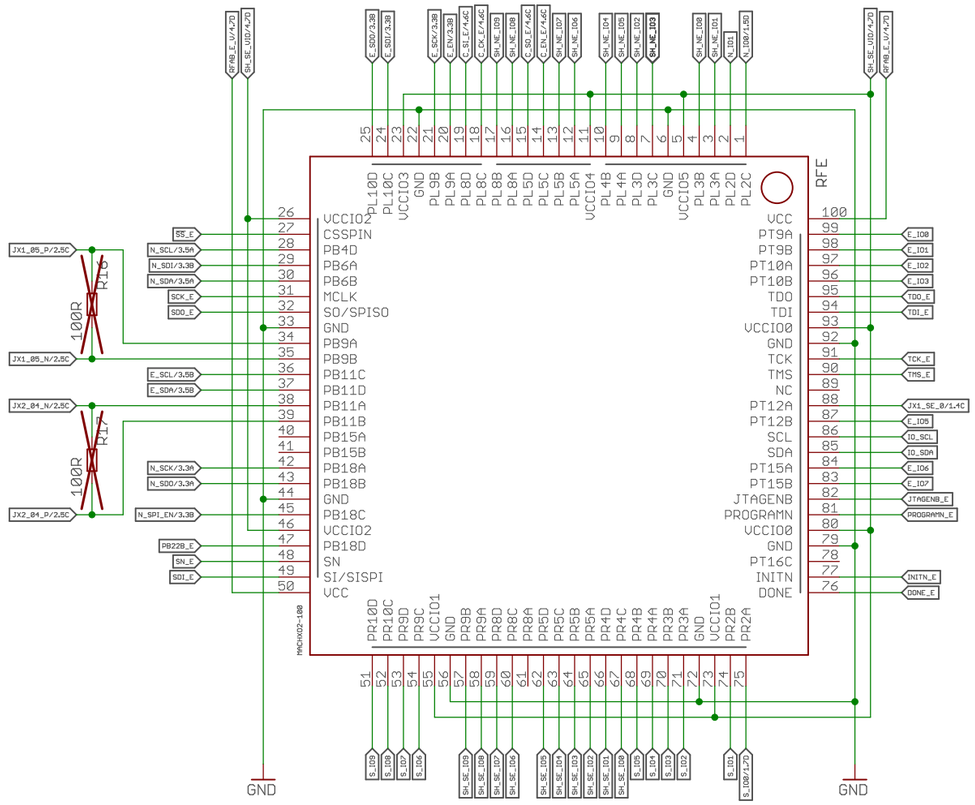

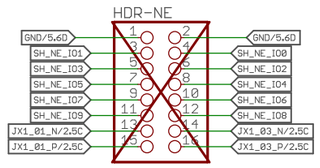

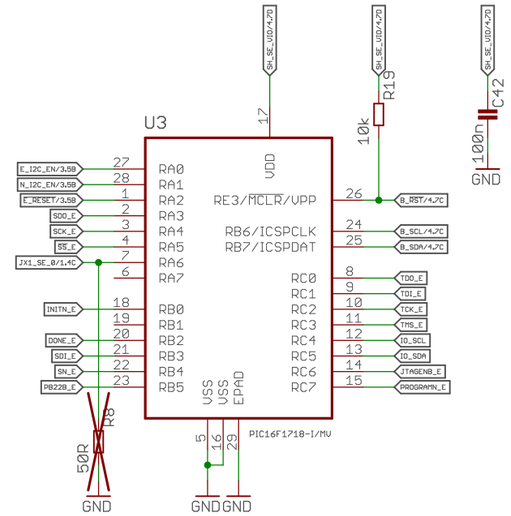

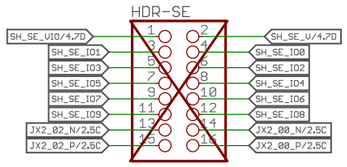

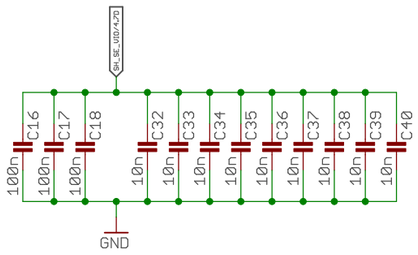

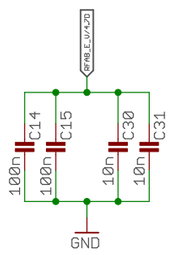

AXIOM Beta Main Board

Interface Fabric East

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not saved!

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