Project 1 – RISC-Toy Design

EE361 – Digital Circuit Design and Language

Kyung Hee University
Electrical Engineering

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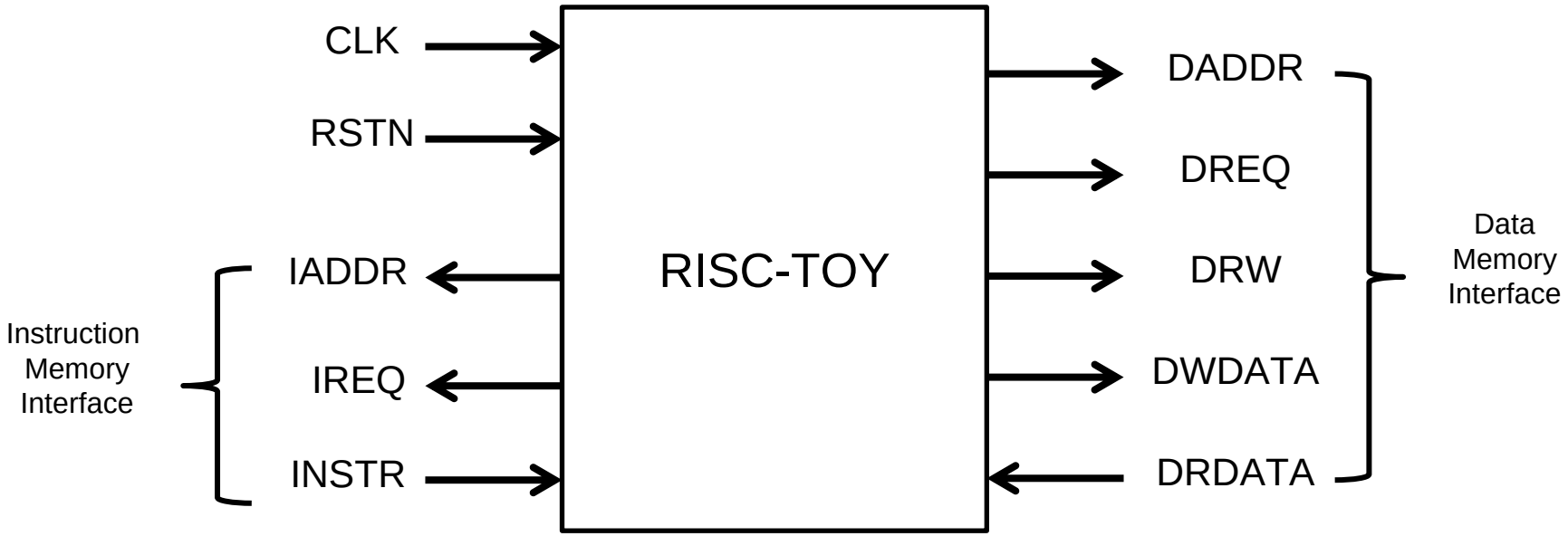
Interface

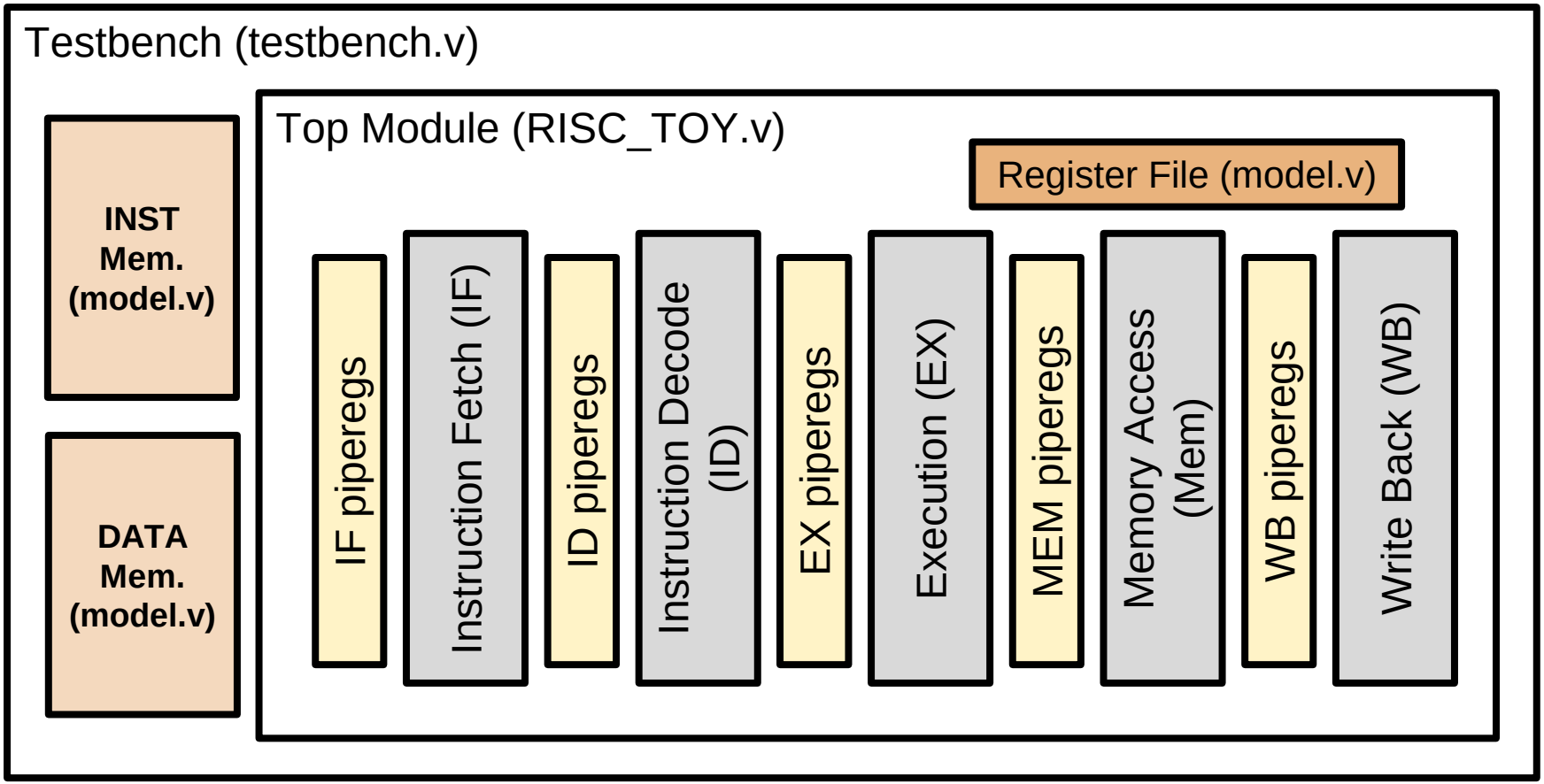
- RISC-Toy Interface

In CLK	Clock	**Out [31:2] DADDR**	Data mem. address
In RSTN	Reset / active low	**Out DREQ**	Data mem. request enable
Out [31:2] IADDR	Instruction address	**Out DRW**	Data mem. read(0)/write(1)
IREQ	Inst. request enable	**Out [31:0] DWDATA**	Data written into the mem.
In [31:0] INSTR	Instruction	**In [31:0] DRDATA**	Data read from the mem.



Modules

- Design of the 5-stage pipelined RISC-Toy



Memory Description

- Two memories: INST_MEM, DATA_MEM
  - ✓ CSN: Activate the memory when 'low'
    WEN: Read/Write enable
  - ✓ For INST_MEM Instantiation:
    - Write your own instruction test code in 'inst.hex' to test the processor.
    - Ex: For ADDI r1, r1, #10: 00_42_00_0A
- Register File (inside): 32-entry general purpose registers
  - ✓ 2-read 1-write interface
  - ✓ Write operation is synchronized to the posedge CLK.
  - ✓ Read operation is not related to the clock signal.

Guideline

- Follow the manual of the instruction set architecture.
- DO NOT use ‘initial’ and ‘delay’ statement except for testbench.v and model.v
- DO NOT modify template files.
- Implement stalls or other techniques to prevent pipeline hazards.
- Note that read from the register file is asynchronous, and write to the register file is synchronous.

Submission Rule (Due:6/2 11:59 PM)

- Submission file: Zip File - Verilog codes and report

File Name: prj1_xx.zip (xx: team number 01~24)

- **Verilog Codes**: **All the Verilog codes you used (including RISC_TOY.v, model.v, testbench.v)**
- Please do not modify model.v.
- Interface of the top module should be the same as page 2. Top module of the processor should be RISC_TOY.
- **Report format**: MS Word or Hancom (**.doc(x)** or **.hwp(x)**)
- The report should contain:
  - ✓ Sufficient explanation on the design procedure
  - ✓ Overall block diagram of the data path + control showing the pipeline stages
  - ✓ Explanation on methods to resolve pipeline hazards
  - ✓ Verifications using custom instruction test codes
  - ✓ Less than 10 pages (Korean available)