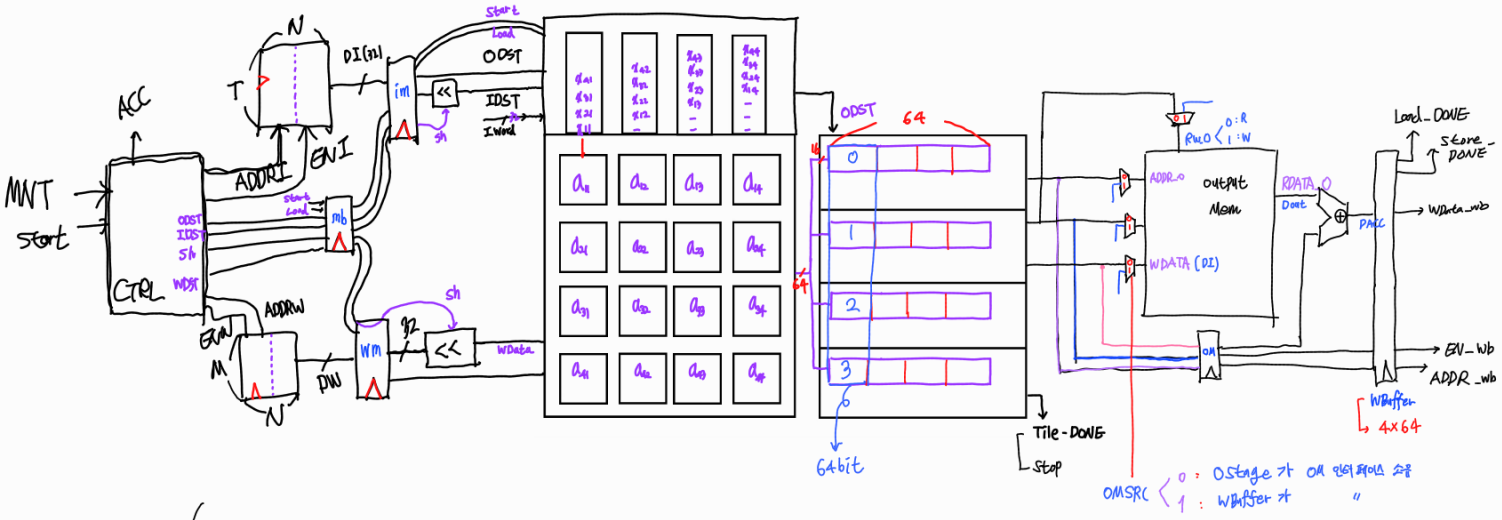
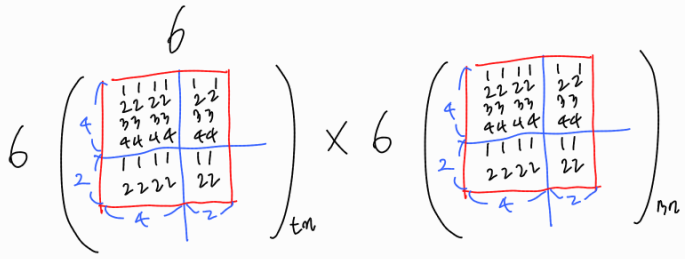




$$\Rightarrow \begin{pmatrix} 4 & 8 & 12 & 16 \\ 8 & 16 & 24 & 32 \\ 12 & 24 & 36 & 48 \\ 16 & 32 & 48 & 64 \end{pmatrix} \begin{pmatrix} 4 & 8 \\ 8 & 16 \\ 12 & 24 \\ 16 & 32 \end{pmatrix} + \begin{pmatrix} 2 & 4 & 6 & 8 \\ 4 & 8 & 12 & 16 \\ 6 & 12 & 18 & 24 \\ 8 & 16 & 24 & 32 \end{pmatrix} \begin{pmatrix} 2 & 4 \\ 4 & 8 \\ 6 & 12 \\ 8 & 16 \end{pmatrix} =$$

$$\begin{pmatrix} 4 & 8 & 12 & 16 \\ 8 & 16 & 24 & 32 \end{pmatrix} \begin{pmatrix} 4 & 8 \\ 8 & 16 \end{pmatrix} \quad \begin{pmatrix} 2 & 4 & 6 & 8 \\ 4 & 8 & 12 & 16 \end{pmatrix} \begin{pmatrix} 2 & 4 \\ 4 & 8 \end{pmatrix}$$

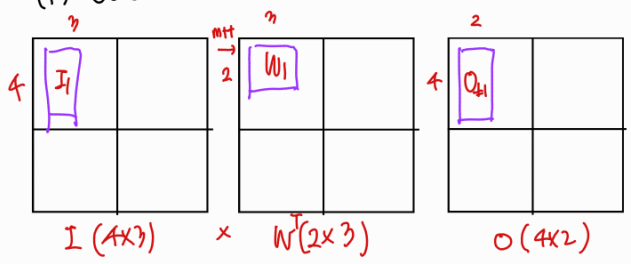
아래 표는 **두 개의 6 × 6 행렬을 더한 결과**를 16진수로 표현한 것입니다.

	0	1	2	3	4	5	
0	0x6	0xC	0x12	0x18	0x6	0xC	8
1	0xC	0x18	0x24	0x30	0xC	0x18	9
2	0x12	0x24	0x36	0x48	0x12	0x24	10
3	0x18	0x30	0x48	0x60	0x18	0x30	11
4	0x6	0xC	0x12	0x18	0x6	0xC	12
5	0xC	0x18	0x24	0x30	0xC	0x18	13

```
sim:/testbench/OUT_MEM/ram @ 2279 ps ~ 228 cycle ( 한 1개당 약 30cycle )
 0 : 0006000c00120018 000c001800240030 0012002400360048 0018003000480060
 4 : 0006000c00120018 000c001800240030 00000000xxxxxxxx 00000000xxxxxxxx
 8 : 0006000c00000000 000c001800000000 0012002400000000 0018003000000000
12 : 0006000c00000000 000c001800000000 00000000xxxxxxxx 00000000xxxxxxxx
```

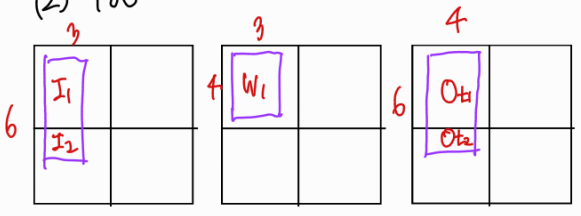
※ total_pt, min 개 - 1 case 생김

(1) 000



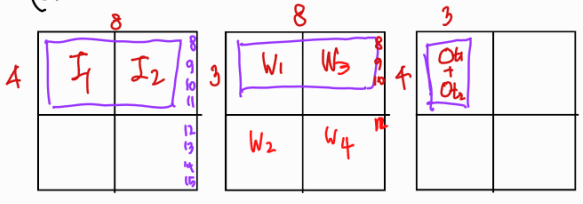
Mac (I1, W1) = Ot1 (4X2)

(2) 100

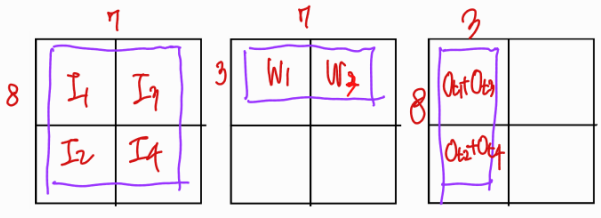


Mac (I1, W1) = Ot1 (4X4)
Mac (I2, W1) = Ot2 (2X4)
→ O (6X4)

(3) 001

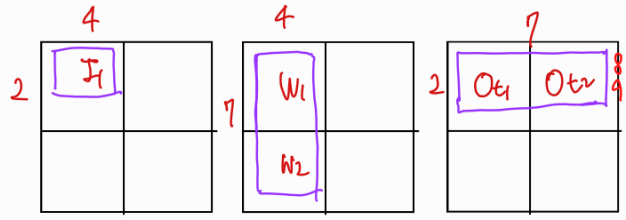


(4) 011



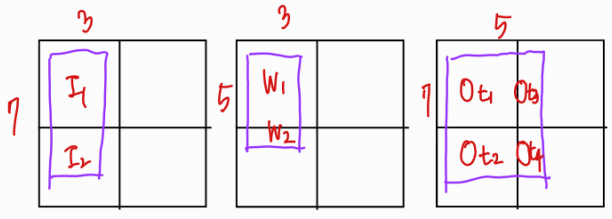
Mac (I1, W1) = Ot1 (4X3)
Mac (I2, W1) = Ot2 (4X3)
Mac (I3, W2) = Ot3 (4X3)
Mac (I4, W2) = Ot4 (4X3)

(5) 100



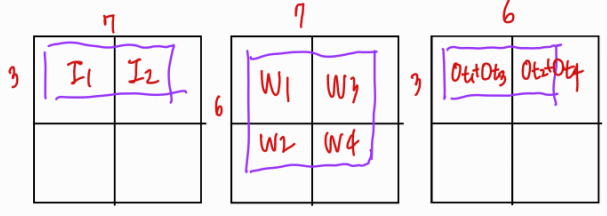
$Mac(I_1, W_1) = O_{t1}$ (2×4)
$Mac(I_1, W_2) = O_{t2}$ (2×3)

(6) 101



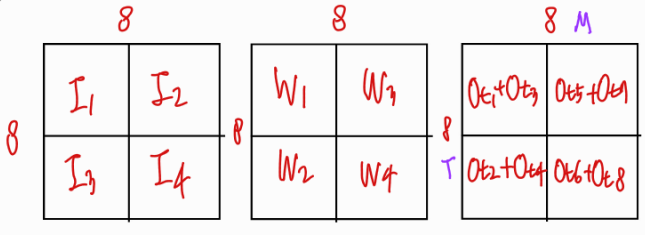
$Mac(I_1, W_1) = O_{t1}$ (4×4)
$Mac(I_2, W_1) = O_{t2}$ (3×4)
$Mac(I_1, W_2) = O_{t3}$ (4×1)
$Mac(I_2, W_2) = O_{t4}$ (3×1)

(7) 110



$Mac(I_1, W_1) = O_{t1}$]①
$Mac(I_2, W_3) = O_{t3}$]①
$Mac(I_1, W_2) = O_{t2}$]②
$Mac(I_2, W_4) = O_{t4}$]②

(8) 111



$Mac(I_1, W_1) = O_{t1}$]
$Mac(I_3, W_1) = O_{t2}$]
$Mac(I_2, W_3) = O_{t3}$]
$Mac(I_4, W_3) = O_{t4}$]
$Mac(I_1, W_2) = O_{t5}$]
$Mac(I_3, W_2) = O_{t6}$]
$Mac(I_2, W_4) = O_{t7}$]
$Mac(I_4, W_4) = O_{t8}$]

(8) SR[0:3][0:3]

SR {(0,0), (1,0), (2,0), (3,0)} (H … T)

SR {(0,1), (1,1), (2,1), (3,1)}

↙ IAdf[0]

SR[0][0] SR[1][0] SR[2][0] SR[3][0]

↙ j=0

falling.

LoadDone

① 32×4 ⇒ Load의 하강에지 감지 ⇒ ~rLoad & Load

② SReg에 입력 ⇒ " → 입력끝?

③ Run

assign LoadDone =

L: 0110

I-Cal.