



STM32 CubeMX

1. Description

1.1. Project

| | |
|-----------------|--------------------|
| Project Name | CDHboarde |
| Board Name | custom |
| Generated with: | STM32CubeMX 6.16.0 |
| Date | 11/20/2025 |

1.2. MCU

| | |
|----------------|---------------|
| MCU Series | STM32H7 |
| MCU Line | STM32H745/755 |
| MCU name | STM32H745BITx |
| MCU Package | LQFP208 |
| MCU Pin number | 208 |

1.3. Core(s) information

| | |
|---------|--------------------------------|
| Core(s) | ARM Cortex-M7 ARM Cortex-M4 |
|---------|--------------------------------|

2. Pinout Configuration



3. Pins Configuration

| Pin Number LQFP208 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|---------------|
| 6 | VSS | Power | | |
| 7 | VDD | Power | | |
| 8 | VBAT | Power | | |
| 13 | PI9 | I/O | FDCAN1_RX | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | VSSMPS | Power | | |
| 19 | VLXSMPS | Power | | |
| 20 | VDDSMPS | Power | | |
| 21 | VFBSPS | Power | | |
| 22 | PF0 | I/O | I2C2_SDA | |
| 23 | PF1 | I/O | I2C2_SCL | |
| 28 | VSS | Power | | |
| 29 | VDD | Power | | |
| 34 | PF10 * | I/O | GPIO_Input | User Button 1 |
| 37 | NRST | Reset | | |
| 39 | PC1 | I/O | SPI2_MOSI | |
| 40 | PC2_C | I/O | SPI2_MISO | |
| 42 | VSSA | Power | | |
| 44 | VDDA | Power | | |
| 46 | PA1 * | I/O | GPIO_Output | User Button 2 |
| 49 | VDD | Power | | |
| 50 | VSS | Power | | |
| 55 | VSS | Power | | |
| 56 | VDD | Power | | |
| 58 | PA5 | I/O | SPI1_SCK | |
| 59 | PA6 | I/O | SPI1_MISO | |
| 60 | PA7 | I/O | SPI1_MOSI | |
| 73 | VSS | Power | | |
| 74 | VDD | Power | | |
| 79 | VSS | Power | | |
| 80 | VDD | Power | | |
| 87 | PB10 | I/O | SPI2_SCK | |
| 89 | VCAP | Power | | |
| 90 | VSS | Power | | |
| 91 | VDDLDO | Power | | |

CDHboarde Project
Configuration Report

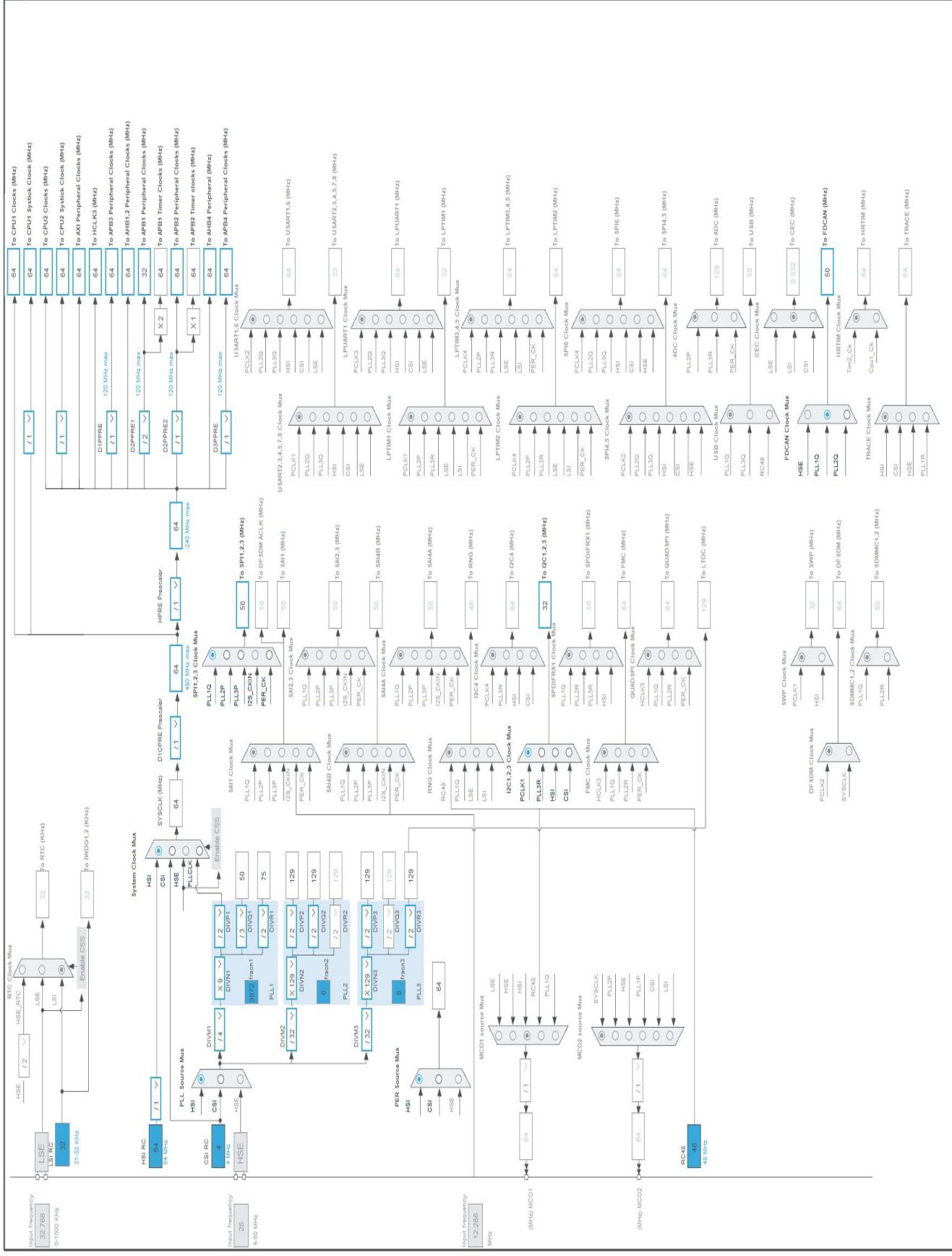
| Pin Number LQFP208 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|-------|
| 99 | VSS | Power | | |
| 100 | VDD | Power | | |
| 101 | PB12 | I/O | FDCAN2_RX | |
| 102 | PB13 | I/O | FDCAN2_TX | |
| 108 | VDD | Power | | |
| 109 | VSS | Power | | |
| 113 | VSS | Power | | |
| 114 | VDD | Power | | |
| 119 | VDD | Power | | |
| 120 | VSS | Power | | |
| 125 | VDD | Power | | |
| 126 | VSS | Power | | |
| 130 | PG2 * | I/O | GPIO_Output | PAY1 |
| 131 | PG3 * | I/O | GPIO_Output | PAY2 |
| 132 | VSS | Power | | |
| 133 | VDD | Power | | |
| 134 | PG4 * | I/O | GPIO_Output | PAY3 |
| 135 | PG5 * | I/O | GPIO_Output | PAY5 |
| 139 | VSS | Power | | |
| 140 | VDD50_USB | Power | | |
| 141 | VDD33_USB | Power | | |
| 151 | PA13 (JTMS/SWDIO) | I/O | DEBUG_JTMS-SWDIO | |
| 152 | VCAP | Power | | |
| 153 | VSS | Power | | |
| 154 | VDDLDO | Power | | |
| 155 | VDD | Power | | |
| 160 | VSS | Power | | |
| 161 | VDD | Power | | |
| 165 | PA14 (JTCK/SWCLK) | I/O | DEBUG_JTCK-SWCLK | |
| 166 | PA15 (JTDI) | I/O | DEBUG_JTDI | |
| 171 | PD1 | I/O | FDCAN1_TX | |
| 178 | VSS | Power | | |
| 179 | VDD | Power | | |
| 186 | VSS | Power | | |
| 187 | VDD | Power | | |
| 189 | PB3 (JTDO/TRACESWO) | I/O | DEBUG_JTDO-SWO | |
| 192 | PB6 | I/O | I2C1_SCL | |
| 193 | PB7 | I/O | I2C1_SDA | |
| 194 | BOOT0 | Boot | | |

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| Pin Number LQFP208 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|-------|
| 199 | VCAP | Power | | |
| 200 | VSS | Power | | |
| 201 | PDR_ON | Power | | |
| 202 | VDDLDO | Power | | |
| 207 | VSS | Power | | |
| 208 | VDD | Power | | |

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

| | |
|-----------|---------------|
| Series | STM32H7 |
| Line | STM32H745/755 |
| MCU | STM32H745BITx |
| Datasheet | DS12923_Rev1 |

1.2. Parameter Selection

| | |
|-------------|-----|
| Temperature | 25 |
| Vdd | 3.0 |

1.3. Battery Selection

| | |
|-------------------|-------------------|
| Battery | Li-SOCL2(DD36000) |
| Capacity | 36000.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 450.0 mA |
| Max Pulse Current | 1000.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

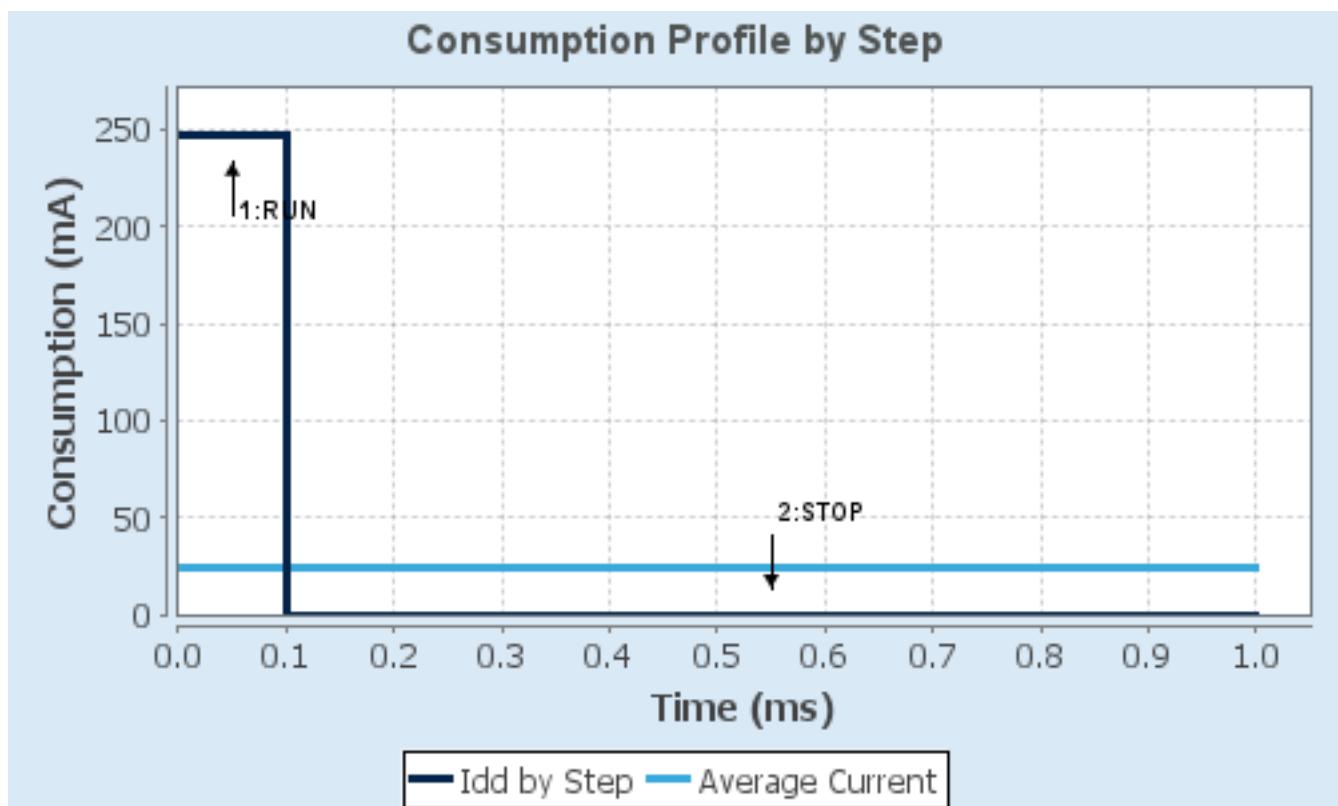
1.4. Sequence

| | | |
|-------------------------------|---------------------------------------|----------------------|
| Step | Step1 | Step2 |
| Mode | RUN | STOP |
| Vdd | 3.0 | 3.0 |
| Voltage Source | Battery | Battery |
| Range | VOS0: Scale0 | SVOS5: System-Scale5 |
| D1 Mode | DRUN/CRUN | DSTANDBY |
| D2 Mode | DRUN/CRUN | DSTANDBY |
| D3 Mode | DRUN | DSTOP |
| Fetch Type | CM7: ITCM/Cache / CM4: FLASH B/ART | CM7: NA / CM4: NA |
| CM7 Frequency | 480 MHz | 0 Hz |
| Clock Configuration | HSE BYP PLL ALL IPs ON | LSE Flash-ON |
| CM4 Frequency | 240 MHz | 0 Hz |
| Clock Source Frequency | 25 MHz | 0 Hz |
| Peripherals | | |
| Additional Cons. | 0 mA | 0 mA |
| Average Current | 247 mA | 145 µA |
| Duration | 0.1 ms | 0.9 ms |
| DMIPS | 1027.0 | 0.0 |
| Category | In DS Table | In DS Table |

1.5. Results

| | | | |
|---------------|-------------------------------|-----------------|--------------------|
| Sequence Time | 1 ms | Average Current | 24.83 mA |
| Battery Life | 1 month, 29 days, 21 hours | Average DMIPS | 1027.2001 DMIPS |

1.6. Chart



2. Software Project

2.1. Project Settings

| Name | Value |
|-----------------------------------|--|
| Project Name | CDHboarde |
| Project Folder | C:\Users\peyto\OneDrive - purdue.edu\Documents\CubeSat\CDHboarde |
| Toolchain / IDE | EWARM V8.50 |
| Firmware Package Name and Version | STM32Cube FW_H7 V1.12.1 |
| Application Structure | Advanced |
| Generate Under Root | No |
| Do not generate the main() | No |
| Minimum Heap Size | 0x200 |
| Minimum Stack Size | 0x400 |

2.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c./h' files | No |
| Backup previously generated files when re-generating | No |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | No |

2.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

| Rank | Function Name | Peripheral Instance Name |
|------|--------------------|--------------------------|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_FDCAN1_Init | FDCAN1 |
| 4 | MX_I2C1_Init | I2C1 |
| 5 | MX_SPI1_Init | SPI1 |

2.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

| Rank | Function Name | Peripheral Instance Name |
|------|---------------|--------------------------|
| 1 | MX_GPIO_Init | GPIO |

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| Rank | Function Name | Peripheral Instance Name |
|------|----------------|--------------------------|
| 2 | MX_FDCAN2_Init | FDCAN2 |
| 3 | MX_I2C2_Init | I2C2 |
| 4 | MX_SPI2_Init | SPI2 |

3. Peripherals and Middlewares Configuration

3.1. CORTEX_M7

3.1.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M7

Initialized Context: Cortex-M7

Power Domain: D1

Speculation default mode Settings:

Speculation default mode Enabled

Cortex Interface Settings:

CPU ICache Disabled

CPU DCache Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault,
NMI and FAULTMASK handlers

Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address **0x0 ***

MPU Region Size 4GB

MPU SubRegion Disable **0x87 ***

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

3.2. DEBUG

Debug: JTAG (4 pins)

3.2.1. Core(s) Settings:

Context(s): Cortex-M7

Initialized Context: Cortex-M7

Power Domain:

3.3. FDCAN1

mode: Activated

3.3.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M7

Initialized Context: Cortex-M7

Power Domain: D2

Clock Calibration Unit:

Clock Calibration Disable

Bit Timings Parameters:

Nominal Prescaler 16

Nominal Time Quantum **320.0 ***

Nominal Time Seg1 1

Nominal Time Seg2 1

Nominal Time for one Bit **960 ***

Nominal Baud Rate **1041666 ***

3.4. FDCAN2

mode: Activated

3.4.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain: D2

Clock Calibration Unit:

Clock Calibration Disable

Bit Timings Parameters:

Nominal Prescaler 16

Nominal Time Quantum **320.0 ***

Nominal Time Seg1 1

Nominal Time Seg2 1

Nominal Time for one Bit **960 ***

Nominal Baud Rate **1041666 ***

3.5. I2C1

I2C: I2C

3.5.1. Parameter Settings:

Core(s) Settings:

Context(s):

Cortex-M7

Initialized Context:

Cortex-M7

Power Domain:

D2

Timing configuration:

| | |
|-------------------------------|---------------------|
| Custom Timing | Disabled |
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x00707CBB * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

3.6. I2C2

I2C: I2C

3.6.1. Parameter Settings:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M4 |
| Initialized Context: | Cortex-M4 |
| Power Domain: | D2 |

Timing configuration:

| | |
|-------------------------------|---------------------|
| Custom Timing | Disabled |
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x00707CBB * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

3.7. RCC

3.7.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M7

Cortex-M4

Initialized Context: Cortex-M7

Power Domain: D3

Power Parameters:

SupplySource PWR_DIRECT_SMPS_SUPPLY

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

RCC Parameters:

TIM Prescaler Selection Disabled

HSE Startup Timeout Value (ms) 100

LSE Startup Timeout Value (ms) 5000

CSI Calibration Value 32

HSI Calibration Value 64

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 1 WS (2 CPU cycle)

Product revision rev.V

PLL range Parameters:

PLL1 clock Input range Between 8 and 16 MHz

PLL1 clock Output range MEDIUM VCO range

3.8. SPI1

Mode: Full-Duplex Master

3.8.1. Parameter Settings:

Core(s) Settings:

Context(s): **Cortex-M7**

Initialized Context: **Cortex-M7**

Power Domain: **D2**

Basic Parameters:

Frame Format **Motorola**

Data Size **4 Bits**

First Bit **MSB First**

Clock Parameters:

Prescaler (for Baud Rate) **2**

Baud Rate **25.0 MBits/s ***

Clock Polarity (CPOL) **Low**

Clock Phase (CPHA) **1 Edge**

Advanced Parameters:

CRC Calculation **Disabled**

NSSP Mode **Enabled**

NSS Signal Type **Software**

Fifo Threshold **Fifo Threshold 01 Data**

Tx Crc Initialization Pattern **All Zero Pattern**

Rx Crc Initialization Pattern **All Zero Pattern**

Nss Polarity **Nss Polarity Low**

Master Ss Idleness **00 Cycle**

Master Inter Data Idleness **00 Cycle**

Master Receiver Auto Susp **Disable**

Master Keep Io State **Master Keep Io State Disable**

IO Swap **Disabled**

3.9. SPI2

Mode: Full-Duplex Master

3.9.1. Parameter Settings:

Core(s) Settings:

Context(s): **Cortex-M4**

Initialized Context: **Cortex-M4**

Power Domain: **D2**

Basic Parameters:

Frame Format **Motorola**

Data Size **4 Bits**

First Bit MSB First

Clock Parameters:

| | |
|---------------------------|-----------------------|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | 25.0 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-------------------------------|------------------------------|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |
| Fifo Threshold | Fifo Threshold 01 Data |
| Tx Crc Initialization Pattern | All Zero Pattern |
| Rx Crc Initialization Pattern | All Zero Pattern |
| Nss Polarity | Nss Polarity Low |
| Master Ss Idleness | 00 Cycle |
| Master Inter Data Idleness | 00 Cycle |
| Master Receiver Auto Susp | Disable |
| Master Keep Io State | Master Keep Io State Disable |
| IO Swap | Disabled |

3.10. SYS_M4

Timebase Source: SysTick

3.10.1. Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M4 |
| Initialized Context: | Cortex-M4 |
| Power Domain: | |

3.11. SYS

Timebase Source: SysTick

3.11.1. Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | |

* User modified value

4. System Configuration

4.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label | Context | Power Domain |
|--------|---------------------|-------------------|-------------------------------|-----------------------------|-----------|---------------|-------------------------|-------------------------|
| DEBUG | PA13 (JTMS/SWDIO) | DEBUG_JTMS-SWDIO | n/a | n/a | n/a | | Cortex-M7 | Cortex-M7 |
| | PA14 (JTCK/SWCLK) | DEBUG_JTC K-SWCLK | n/a | n/a | n/a | | Cortex-M7 | Cortex-M7 |
| | PA15 (JTDI) | DEBUG_JTD I | n/a | n/a | n/a | | Cortex-M7 | Cortex-M7 |
| | PB3 (JTD0/TRACESWO) | DEBUG_JTD O-SWO | n/a | n/a | n/a | | Cortex-M7 | Cortex-M7 |
| FDCAN1 | PI9 | FDCAN1_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| | PD1 | FDCAN1_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| FDCAN2 | PB12 | FDCAN2_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| | PB13 | FDCAN2_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| I2C1 | PB6 | I2C1_SCL | Alternate Function Open Drain | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| | PB7 | I2C1_SDA | Alternate Function Open Drain | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| I2C2 | PF0 | I2C2_SDA | Alternate Function Open Drain | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| | PF1 | I2C2_SCL | Alternate Function Open Drain | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| SPI1 | PA5 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| | PA6 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| | PA7 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M7 | D2 |
| SPI2 | PC1 | SPI2_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| | PC2_C | SPI2_MISO | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| | PB10 | SPI2_SCK | Alternate Function Push Pull | No pull-up and no pull-down | Low | | Cortex-M4 | D2 |
| GPIO | PF10 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | User Button 1 | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label | Context | Power Domain |
|-----|-------------|------------------|-----------------------------|-----------------------------|---------------|------------|------------|-------------------------|
| PA1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | User Button 2 | Cortex-M7* | Cortex-M4 | Cortex-M7* Cortex-M4 |
| | PG2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PAY1 | Cortex-M7* | Cortex-M7* Cortex-M4 |
| | PG3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PAY2 | Cortex-M7* | Cortex-M7* Cortex-M4 |
| | PG4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PAY3 | Cortex-M7* | Cortex-M7* Cortex-M4 |
| | PG5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PAY5 | Cortex-M7* | Cortex-M7* Cortex-M4 |

* Initialized context

4.2. DMA configuration

nothing configured in DMA service

4.3. BDMA configuration

nothing configured in DMA service

4.4. MDMA configuration

nothing configured in DMA service

4.5. NVIC configuration

4.5.1. NVIC1

| Interrupt Table | Enable | Preenemption Priority | SubPriority |
|---|--------|-----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 15 | 0 |
| PVD and AVD interrupts through EXTI line 16 | | unused | |
| Flash global interrupt | | unused | |
| RCC global interrupt | | unused | |
| FDCAN1 interrupt 0 | | unused | |
| FDCAN1 interrupt 1 | | unused | |
| I2C1 event interrupt | | unused | |
| I2C1 error interrupt | | unused | |
| SPI1 global interrupt | | unused | |
| FDCAN calibration unit interrupt | | unused | |
| CM4 send event interrupt for CM7 | | unused | |
| FPU global interrupt | | unused | |
| HSEM1 global interrupt | | unused | |
| Hold core interrupt | | unused | |

4.5.2. NVIC1 Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|-----------------------------------|----------------------|------------------|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |

4.5.3. NVIC2

| Interrupt Table | Enable | Preenemption Priority | SubPriority |
|---|--------|-----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 15 | 0 |
| PVD and AVD interrupts through EXTI line 16 | | unused | |
| Flash global interrupt | | unused | |
| FDCAN2 interrupt 0 | | unused | |
| FDCAN2 interrupt 1 | | unused | |
| I2C2 event interrupt | | unused | |
| I2C2 error interrupt | | unused | |
| SPI2 global interrupt | | unused | |
| FDCAN calibration unit interrupt | | unused | |
| CM7 send event interrupt for CM4 | | unused | |
| FPU global interrupt | | unused | |
| HSEM2 global interrupt | | unused | |
| Hold core interrupt | | unused | |

4.5.4. NVIC2 Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|-----------------------------------|----------------------|------------------|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

The screenshot shows the 'Category view' section of the configuration tool. At the top, there are four tabs: 'Category view' (which is selected and underlined in blue), 'Context Execution view', 'Context Initialization view', and 'Power Domain view'. Below the tabs are three filter panels: 'Choose filters ...', '... by Context Execution' (with checkboxes for 'Cortex-M7' and 'Cortex-M4'), and '... by Power Domain' (with checkboxes for 'D1', 'D2', 'D3', and 'None'). A large empty box labeled 'Middleware' is positioned below these filters. The main content area contains a grid of system components, each represented by a blue button with a white icon and a checkmark. The components are organized into categories: System Core, Analog, Timers, Connectivity, Multimedia, Security, Computing, Trace and Debug, Power and Thermal, Utilities, and Other. The 'System Core' category has 12 items: BDMA, CORTEX_M4, CORTEX_M7 (selected), DMA, GPIO, MDMA, I2C1, I2C2, SPI1, SPI2, RCC, and SYS_M4. The 'Connectivity' category has 2 items: FDCAN1 and FDCAN2. The 'Trace and Debug' category has 1 item: DEBUG (selected). The other categories are currently empty.

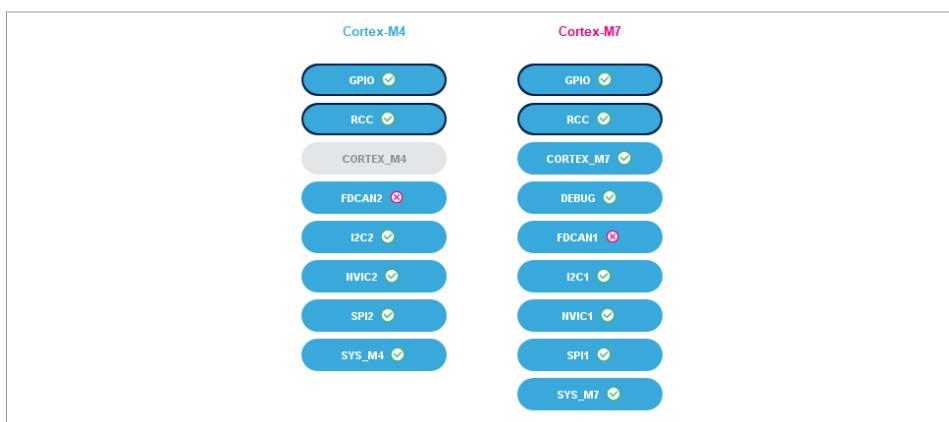
5.1.2. Without filters

The screenshot shows the configuration interface for the CDHboard Project. At the top, there are four tabs: "Category view" (selected), "Context Execution view", "Context Initialization view", and "Power Domain view". Below these tabs are three filter sections: "Choose filters ...", "... by Context Execution" (with checkboxes for Cortex-M7 and Cortex-M4), "... by Context Initialization" (with checkboxes for Cortex-M7, Cortex-M4, and None), and "... by Power Domain" (with checkboxes for D1, D2, D3, and None). A large empty box labeled "Middleware" is present below the filters. The main content area contains a grid of components under various categories:

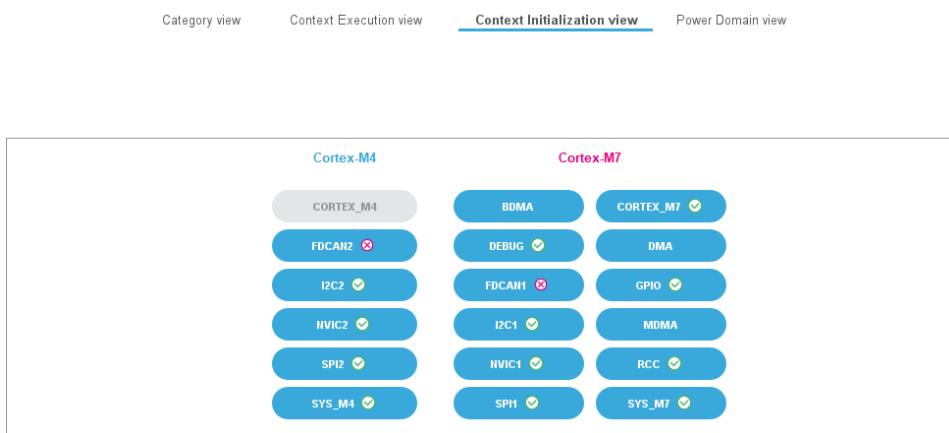
| System Core | Analog | Timers | Connectivity | Multimedia | Security | Computing | Trace and Debug | Power and Thermal | Utilities | Other |
|---|--------|--------|--|------------|----------|-----------|---|-------------------|-----------|-------|
| BDMA | | | FDCAN1 <input checked="" type="checkbox"/> | | | | DEBUG <input checked="" type="checkbox"/> | | | |
| CORTEX_M4 | | | FDCAN2 <input checked="" type="checkbox"/> | | | | | | | |
| CORTEX_M7 <input checked="" type="checkbox"/> | | | I2C1 <input checked="" type="checkbox"/> | | | | | | | |
| DMA | | | I2C2 <input checked="" type="checkbox"/> | | | | | | | |
| GPIO <input checked="" type="checkbox"/> | | | SPI1 <input checked="" type="checkbox"/> | | | | | | | |
| MDMA | | | SPI2 <input checked="" type="checkbox"/> | | | | | | | |
| HVIC1 <input checked="" type="checkbox"/> | | | | | | | | | | |
| HVIC2 <input checked="" type="checkbox"/> | | | | | | | | | | |
| RCC <input checked="" type="checkbox"/> | | | | | | | | | | |
| SYS_M4 <input checked="" type="checkbox"/> | | | | | | | | | | |
| SYS_M7 <input checked="" type="checkbox"/> | | | | | | | | | | |

5.2. Context Execution view

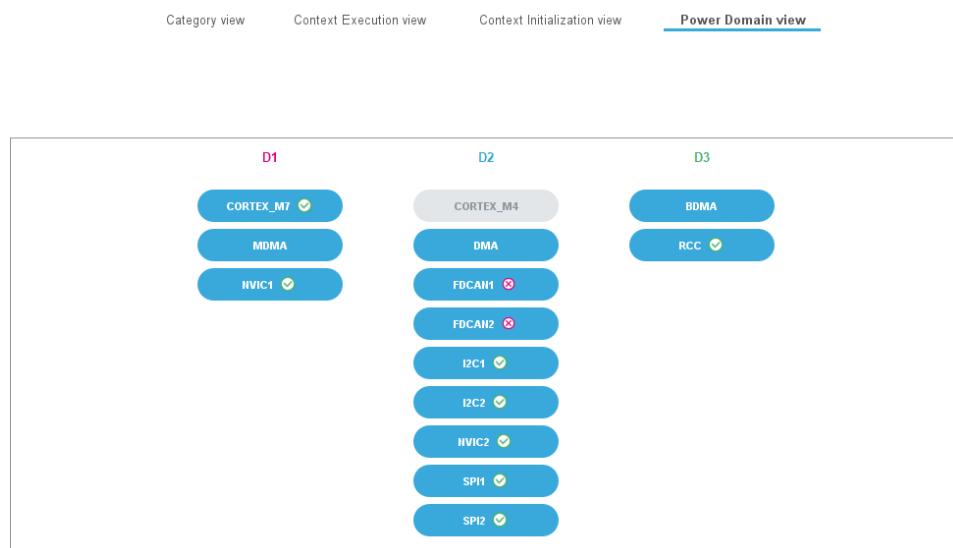
Category view Context Execution view Context Initialization view Power Domain view



5.3. Context Initialization view



5.4. Power Domain view



6. Docs & Resources

| Type | Link |
|-------------------|---|
| BSDL files | https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip |
| IBIS models | https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip |
| System View | https://www.st.com/resource/en/svd/stm32h7-svd.zip |
| Description | |
| Presentations | https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf |
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guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

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- Application Notes https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5286-stm32h7x5x7-dualcore-microcontroller-debugging-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
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& Software stm32cubeide-stmicroelectronics.pdf

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