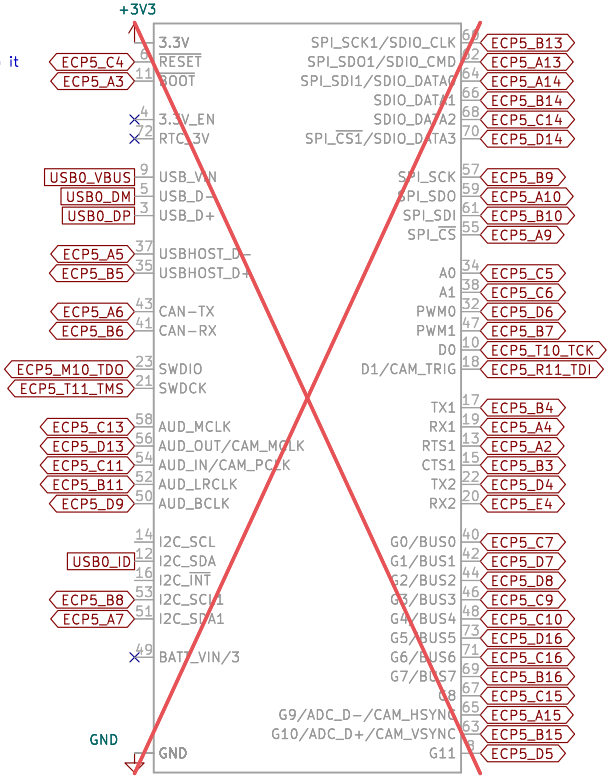
M.2 CARD EDGE

GPIOs here are all 3V3 from banks 0–3



NOPOP, this part just represents the card edge

internal pullup for ^boot so it
-used for other functions

LFE5U FPGA

bank2_3

FPGA_SELF_PROGRAM

3V3: GPIO / 2x LEDs

File: bank2_3.kicad_sch

bank8_configuration

FPGA_SELF_PROGRAM

3V3: SPI FLASH / startup config

File: bank8_configuration.kicad_sch

bank6_7

USB0{ULPI}

RAM{HyperRAM}

3V3/1V8: ULPI / PSRAM

File: bank6_7.kicad_sch

bank0_1

CLOCK_48MHZ

3V3: GPIO

File: bank0_1.kicad_sch

VCCRAM

usb

VDDIO

USB0{ULPI}

USB_DP — USB0_DP

USB_DM — USB0_DM

USB_VBUS_CONN — USB0_VBUS

USB_ID — USB0_ID

File: usb.kicad_sch

ram

RAM{HyperRAM}

File: ram.kicad_sch

330

R108

+3V3

Osc48MHz

OUT

VDD

EN

GND

Y1

C10

0.1uF

GND

power_supplies

File: power_supplies.kicad_sch

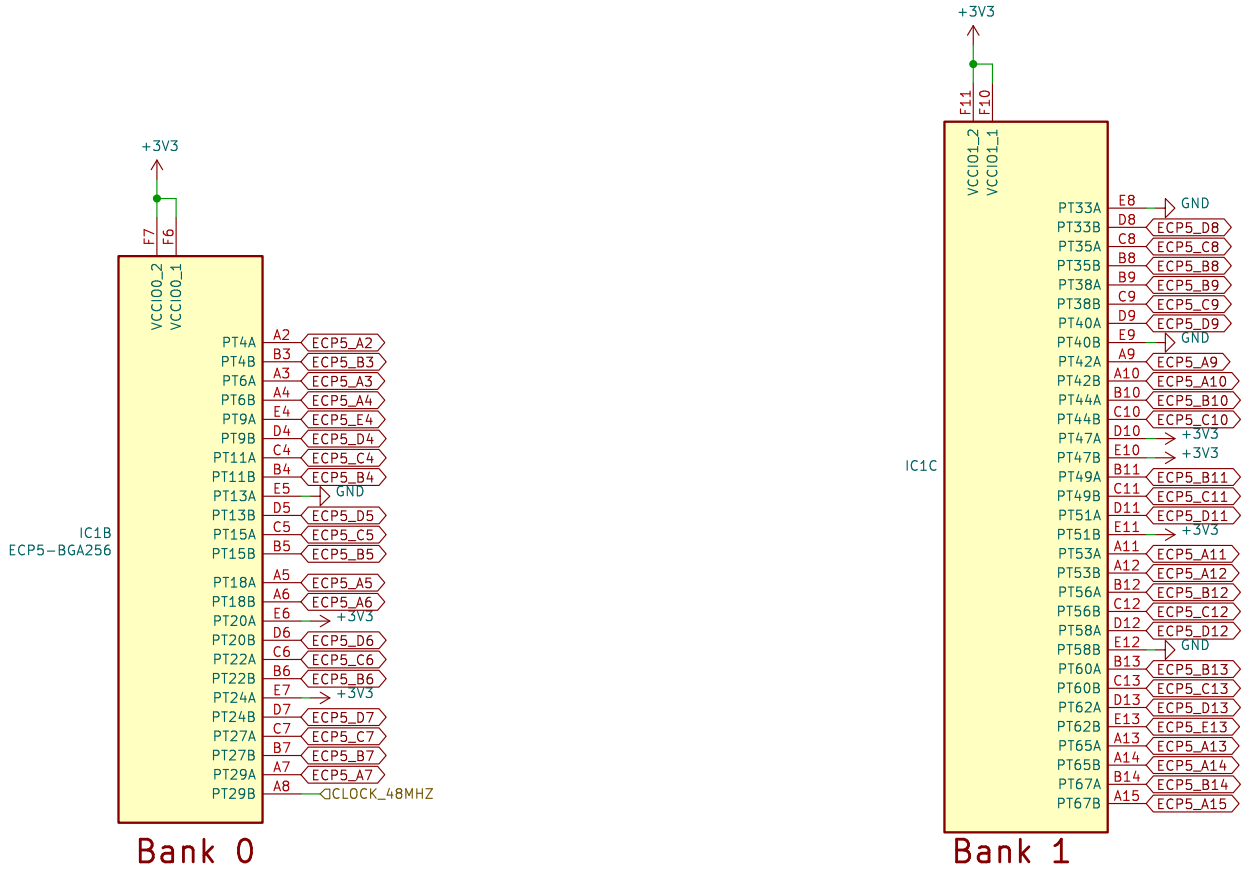
S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

Sheet: /

File: soldiercrab.kicad_sch

Title: SoldierCrab

Size: A4	Date: 2024–06–04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 1/8

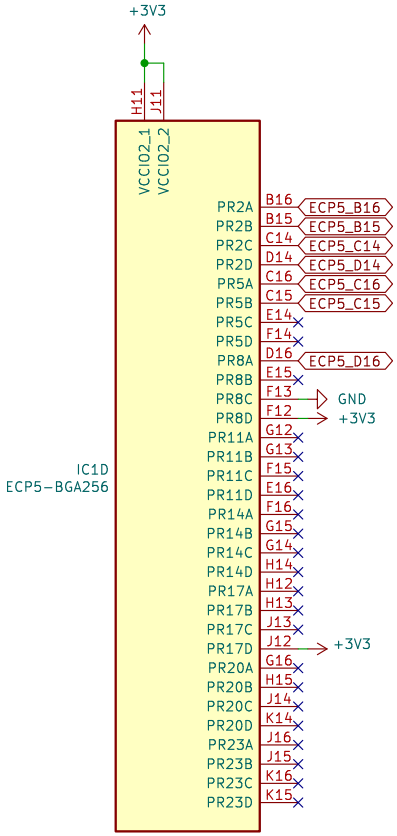


S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

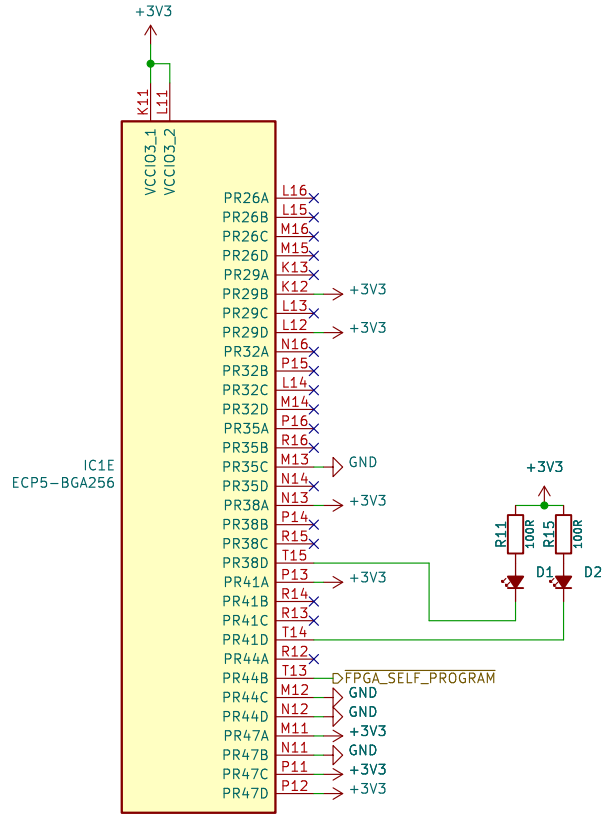
Sheet: /bank0_1/
File: bank0_1.kicad_sch

Title: SoldierCrab

Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 2/8



Bank 2



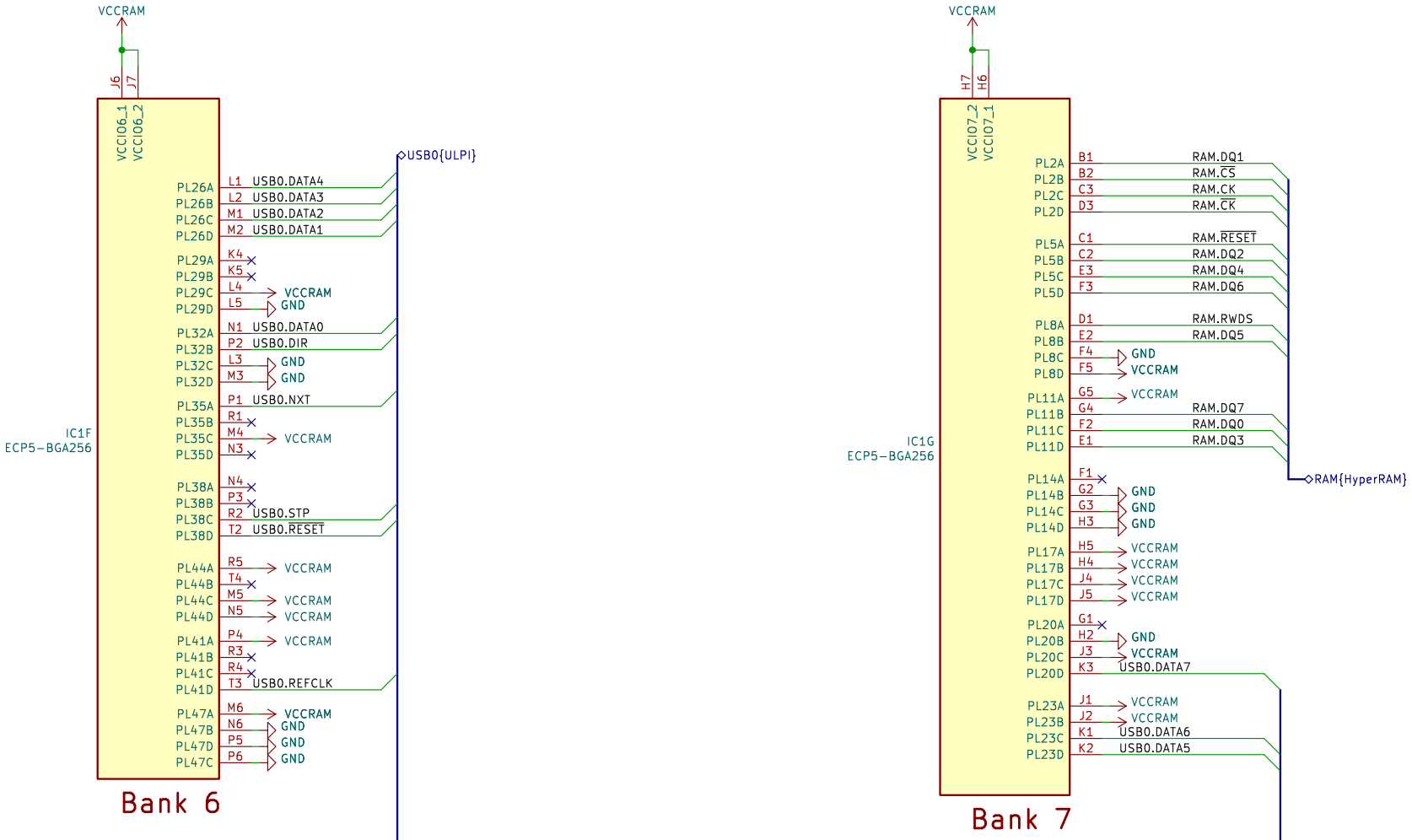
Bank 3

S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

Sheet: /bank2_3/
File: bank2_3.kicad_sch

Title: SoldierCrab

Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 3/8

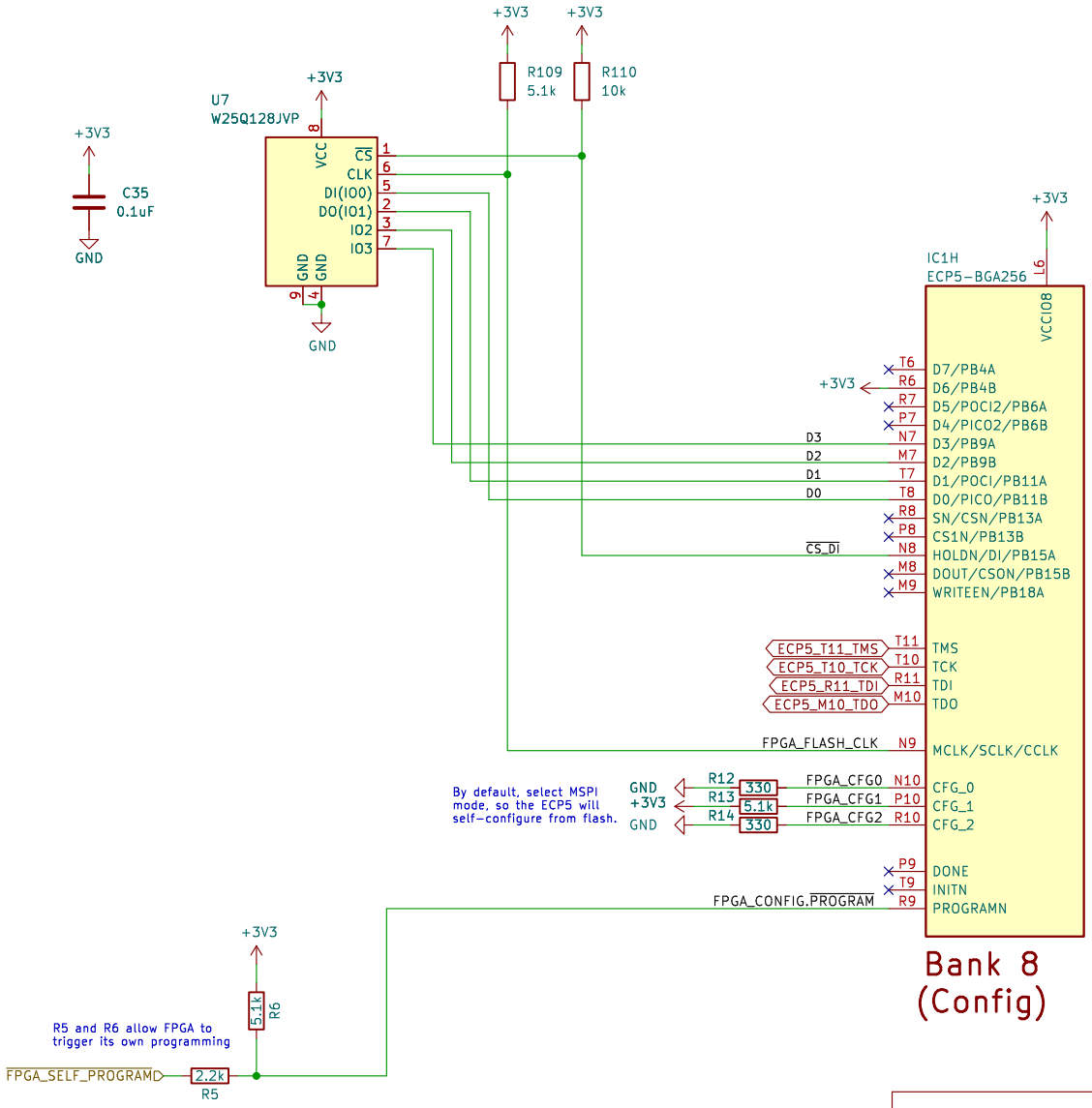


S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

Sheet: /bank6_7/
File: bank6_7.kicad_sch

Title: SoldierCrab

Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 4/8

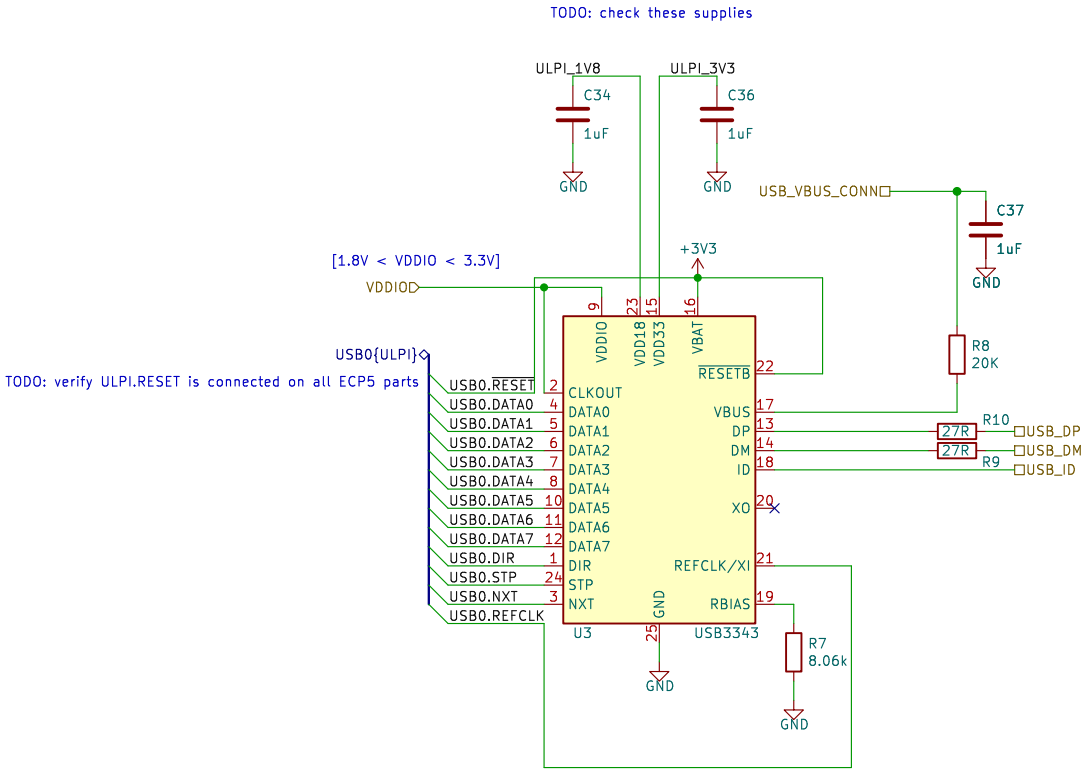


S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

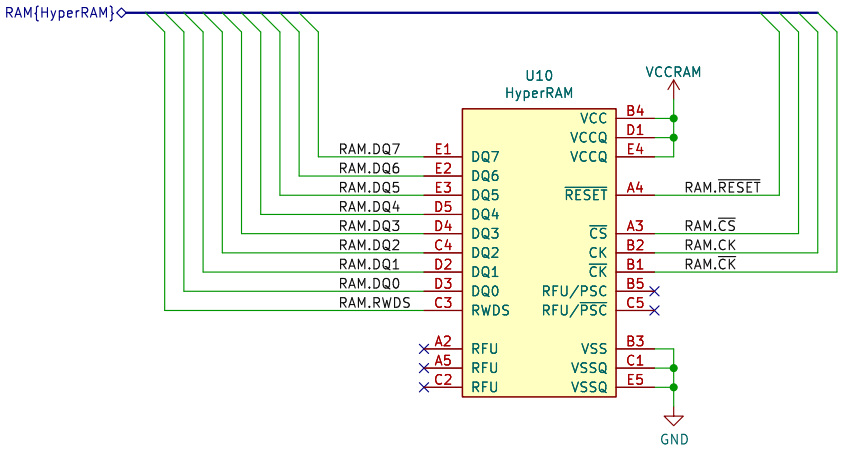
Sheet: /bank8_configuration/
File: bank8_configuration.kicad_sch

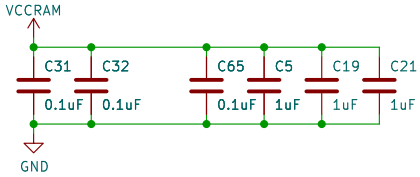
Title: SoldierCrab

Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 5/8



Sheet: /usb/		
File: usb.kicad_sch		
Title: SoldierCrab		
Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 6/8





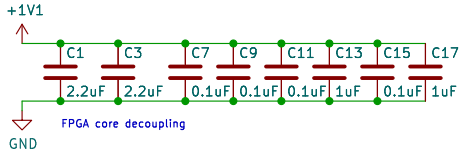
S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

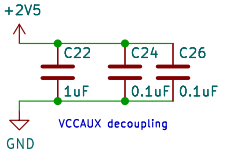
Sheet: /ram/
File: ram.kicad_sch

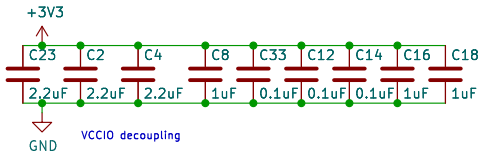
Title: SoldierCrab

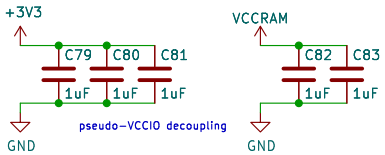
Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 7/8

decoupling under ECP5

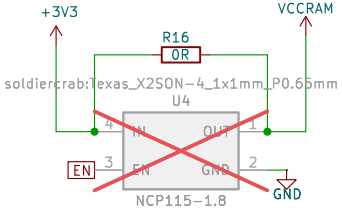






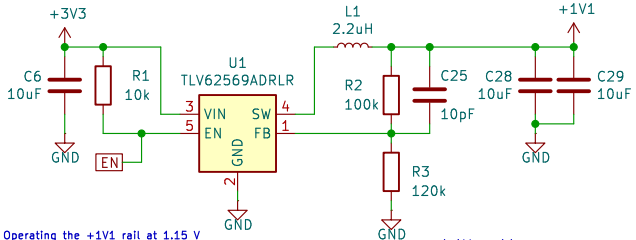


RAM VCC / ULPI VCCIO



USB3343: fine with VCCIO at 1V8 or 3V3.
PSRAM: depends on the RAM chip chosen
Both ULPI VCCIO and RAM VCC are fed by this net,
as the associated ECP5 pins are on the same bank.

1V1 / VCORE

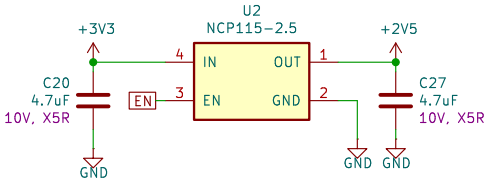


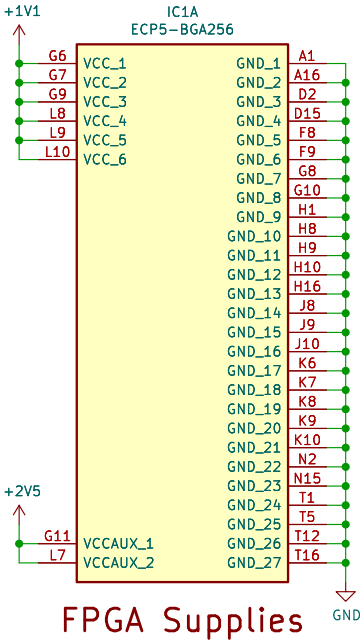
Operating the +1V1 rail at 1.15 V
is a compromise between performance
and power consumption. ECP5 core
supply voltage is specified as 1.1 V
while the higher performing ECP5-5G
(confirmed to be the same die) core
supply voltage is specified as 1.2 V.

1.1V @ 1A
- ECP5 VCC

R? = 120K for 1.2V output

2V5 / VCCAUX





FPGA Supplies

S.Holzapfel, apfelaudio UG (haftungsbeschränkt)

Sheet: /power_supplies/
File: power_supplies.kicad_sch

Title: SoldierCrab

Size: A4	Date: 2024-06-04	**Rev: 2.0.0**
KiCad E.D.A. 8.0.3		Id: 8/8