ELEC 240
Lab 7 - Digital Logic

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1 Objective

The objective of this lab was to learn the underlying logical operations behind an adder and to then apply these principles to implement a one-bit full adder on a breadboard.

2 Materials

- Test Board
- 1x 74HC00 Quad 2-input NAND gate
- 1x 7486 Quad 2-input XOR gate
- 2x LEDs
- 1x Quad DIP switch
- 5x 330Ω resistors
- Yellow, Red, and Black wire (signal, power, gnd)
- Wire strippers and cutters

3 Test Description

In the first section of the lab, we learned about the logic underlying the fundamental NAND and XOR gates and their truth tables for all combinations of inputs. We then formulated an expression for the correct output of the adder for the three input bits. We then applied DeMorgan's law to simplify the circuit so that it only uses NAND and XOR gates, and we then constructed the one-bit full adder.

3.1 Pre-Lab Calculations and Schematics

To begin, we had to understand the underlying logic behind a NAND and a XOR gate, which the adder was composed of. Below in Figure 1 is the truth table for a NAND gate, and in Figure 2 is the truth table for a XOR gate.

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Figure 1: NAND Truth Table

A	B	A NAND B
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2: XOR Truth Table

We then derived the following expression for the Sum S and Carry C output bits of the adder based on the three one-bit inputs x, y, z.

$$S = (x \bigoplus y) \bigoplus z$$

$$C = (x \bullet y) \vee (x \bigoplus y) \bullet z$$

We then created the following truth table for the sum and carry bits based on these outputs as follows in Fig 3:

x	y	z	$x \bullet y$	$x \bigoplus y$	$(x \bigoplus y) \bigoplus z$	$(x \bullet y) \vee (x \bigoplus y)$	C	S
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	1
0	1	0	0	1	1	1	0	1
0	1	1	0	1	0	1	1	0
1	0	0	0	1	1	1	0	1
1	0	1	0	1	0	1	1	0
1	1	0	0	0	1	0	0	1
1	1	1	1	0	1	1	1	1

Figure 3: Naive Truth Table for the Sum and Carry bits

However, the direct implementation of the above truth table into logic requires the use of 2 XOR gates for the sum bit 2 NAND gates, and 1 OR gate for the carry bit. Since we want to reduce the complexity of our adder, we can use DeMorgan's laws to simplify the requirements for the carry bits:

$$x \bullet y = \neg(x \vee y)$$

$$x \vee y = \neg(x \bullet y)$$

We then obtain the following equation for the carry bit expression by applying the above DeMorgan's laws:

$$C = \neg \left(\neg(x \bullet y) \bullet \neg \left(\left(x \bigoplus y \right) \bullet z \right) \right)$$

The truth table is depicted below in Fig 4;

x	y	z	$x \bullet y$	$x \bigoplus y$	$\neg((x \bigoplus y) \bullet z)$	$\neg(x \bullet y) \bullet \neg((x \bigoplus y) \bullet z)$	C
0	0	0	0	0	1	1	0
0	0	1	0	0	1	1	0
0	1	0	0	1	1	1	0
0	1	1	0	1	0	0	1
1	0	0	0	1	1	1	0
1	0	1	0	1	0	0	1
1	1	0	0	0	1	1	0
1	1	1	1	0	1	0	1

Figure 4: Modified Truth Table for the Sum and Carry bits

The circuit that implements this truth table's equation is depicted below in Fig 5 :

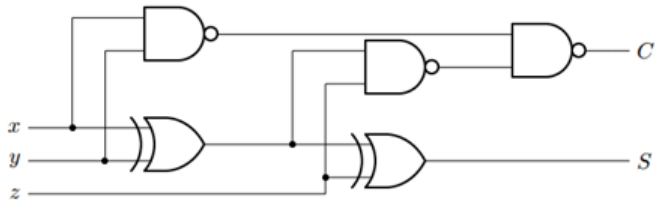

Figure 5: One-Bit Full Adder Circuit Diagram

4 Results and Discussion

Your text here

Note (To be deleted): The heart of your report is the presentation of your results and a discussion of those results. In your discussion, you should not only analyze your results, but also discuss the implications of those results.

5 References

Your text here

Note (To be deleted): List any datasheets, websites, lab procedure, etc. used during the lab.

6 Conclusion

Your text here

Note (To be deleted): While the "Results and Discussion" section focused on the test results individually, the "Conclusion" discusses the results in the context of the entire experiment. Usually, the objectives given in the "Introduction" are reviewed to determine whether the experiment succeeded. If the objectives were not met, you should analyze why the results were not as predicted.

7 Errors

Your text here

Note (To be deleted): Briefly list sources of error and discuss how to eliminate or deal with them