Worcester Polytechnic Institute

Electrical and Computer Engineering Department

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**Test and Testable Design**
**Online Offering – Spring 2024**
**Homework 3: Test generation with Verilog testbenches**
**Due Date: February 25**

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In this homework, you are provided with Netlist of the c5315 benchmark and other required files (See attached file) to use Adjustable Expected Coverage Per Test method mentioned in your textbook and generate test vectors for this module. Decide on the value of parameters of the Adjustable Expected Coverage method and its adjustment scheme to improve the resulted test.

## Caution:

Do not use Verilog codes directly from the book, as those codes are for demo purposes only and may contain inaccuracies. Please start with sample codes available on course site (Tools and Extra Materials) and make necessary corrections and modifications.

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## Attention:

This homework covers “Chapter 5 – Test Pattern Generation Methods and Algorithms” module on Canvas.

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## Deliverables:

All Verilog codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of "*ECE5724 - Comprehensive Format Syllabus.pdf*" file. The file has been posted on Canvas.

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