Worcester Polytechnic Institute

Electrical and Computer Engineering Department

Test and Testable Design
Online Offering – Spring 2024
Homework 2: Fault Simulation
Due Date: February 18

Background Information:

Atalanta:

Atalanta is an Automatic Test Pattern Generator and fault simulator for stuck-at faults in combinational circuits. Find the related files and manual on the uploaded folder.

HOPE:

HOPE is a parallel fault simulator for combinational and synchronous sequential circuits. Please find the related files and manuals on the uploaded folder.

Benchmark:

Benchmarks are groups of designed circuits which are used for evaluating methods and tools of circuit testing. There are different types of benchmarks. For example, ISCAS-85 series contain combinational benchmarks, ISCAS-89 series contain sequential benchmarks and ITC-99 series are behavioral benchmarks.

Description:

The c5315 benchmark circuit is one of ISCAS-85 benchmarks. The description is synthesized into a netlist of primitive components in the Component Library (c5315_net.v). In addition, the equivalent netlist in .bench format is created (c5315.bench).

You are to:

A. Apply *Atalanta* to c5315.bench file to generate a test set for the circuit. Store the resulting test vectors in a file named “c5315.pat”. Write down the reported number of collapsed faults, number of detected faults, and fault coverage for future comparisons.
B. Apply *HOPE* to the c5315.bench file and use “c5315.pat” as the input test set. Write down the reported number of collapsed faults, number of detected faults, and fault coverage for future comparisons. Please consider that the input test file of *HOPE* has a different format than that generated by *Atalanta*. Section “TEST PATTERN FILE” in “hope_readme.txt” describes the file format of the input test file for *HOPE*.
C. Write a Verilog testbench that performs serial fault simulation for the module c5315_net using c5315.pat as the circuit test set. Your testbench must at least report the number of collapsed faults, number of detected faults, and fault coverage.
D. Write a Verilog code generating fault dictionary for c5315_net, use c5315.pat as the test set.

Attention:

This homework covers “Chapter 3 – Fault and Defect Modeling” and “Chapter 4 – Fault Simulation Applications and Methods” module on Canvas.

Deliverables:

All Verilog codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of "*ECE5724 - Comprehensive Format Syllabus.pdf*" file. The file has been posted on Canvas.
