Worcester Polytechnic Institute

Electrical and Computer Engineering Department

Test and Testable Design
Online Offering – Spring 2024
Homework 5: BIST design and implementation
Due Date: April 14

Description:

You are already familiar with the *SSC* circuit of Homework 1. In this homework, you are provided with the netlist of this circuit (netlist_SSC_V1). You are to:

1- Insert scan into the *SSC_net* module.
2- Design and implement a parameterized RTS BIST architecture for the *SSC_net* module.
3- Configure parameters of the BIST architecture and report a reasonable fault coverage.
4- Compare your results (i.e., test time and coverage) with Homework 4.

Attention:

This homework covers “Chapter 9 – Logic Built-in Self-test” module on Canvas.

Deliverables:

All Verilog codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of "*ECE5724 - Comprehensive Format Syllabus.pdf*" file. The file has been posted on Canvas.