Worcester Polytechnic Institute

Electrical and Computer Engineering Department

Test and Testable Design
Online Offering – Spring 2024
Homework 4: Scan insertion and scan testing by Verilog virtual tester
Due Date: March 17

Description:

In this homework, you are provided with the netlist of the SSC circuit (netlist_SSC_V1) that you got familiar with in homework 1. In addition, the equivalent netlist in the .bench format is created (SSC.bench). You are to:

1- Unfold "SSC.bench" file and separate the combinational part as discussed in the course lectures.
2- Apply *Atalanta* to the unfolded file to generate a good test for the combinational part of the circuit
3- Insert full-scan into the *SSC_net* module in the "netlist_SSC_V1.v" file.
4- Develop a virtual tester to verify the generated test. Write down the reported number of collapsed faults, number of detected faults, and fault coverage.

Caution:

Do not use Verilog codes directly from the book, as those codes are for demo purposes only and may contain inaccuracies. Please start with sample codes available on course site (Tools and Extra Materials) and make necessary corrections and modifications.

Attention:

This homework covers “Chapter 7 – Design for Test by Means of Scan” module on Canvas.

Deliverables:

A complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of "*ECE5724 - Comprehensive Format Syllabus.pdf*" file. The file has been posted on Canvas.